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Minimization of Output Voltage Ripple of Two-Phase Interleaved Buck Converter with Active Clamp

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Abstract: A control technique combining pulse width modulation (PWM) and pulse amplitude modulation (PAM) is presented herein to reduce the output voltage ripple of the converter as little as possible. Such a converter requires a two-stage cascaded structure. The first stage is the buck-boost converter, which is used to adjust the output voltage of the second power stage, whereas the second stage is the two-phase interleaved buck converter, which is used to reduce the output voltage ripple. In theory, the two phases of the second stage operate under the condition of individual duty cycles of 50% with a phase difference of 180° between the two, and hence, the currents in the two phases are cancelled for any period of time, thereby making the output voltage of the converter almost voltage-free. Moreover, in order to improve the overall efficiency further, the proposed soft-switching technique based on an active clamp is presented and applied to these two stages to render the main and auxiliary switches turned on with zero-voltage switching (ZVS). Finally, the operating principles and control strategies of the proposed converter are described, and then, their effectiveness is verified by experimental results.

Keywords: active clamp; buck converter; current sharing; FPGA; fully-digitalized; output voltage ripple; PAM; PWM

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1. Introduction

As far as the switching DC-DC power supply is concerned, due to the switching of the power switch, the inductor current is a time-varying current, and when the AC component of this current flows through the output capacitor, output voltage ripples will be generated. Due to excessive output voltage ripple, the reliability of the switching DC-DC power supply will be decreased.

Conventionally, reducing the output voltage ripple is nothing more than increasing the switching frequency or increasing the value of the output capacitor, but increasing the switching frequency will increase the switching loss of the power switch, whereas increasing the output capacitor will not only increase the cost but also reduce the stability of the system. Therefore, the literature [1,2] proposed the use of multiphase interleaved control, which reduces the current flowing into the output capacitor by increasing the switching frequency and using the interleaved control, thereby reducing the output voltage ripple. However, this structure will affect the output voltage ripple when the input voltage fluctuates or the load fluctuates, and hence, the effect of reducing the output voltage ripple is insignificant. The literature [3,4] uses external passive components, such as transformers,

capacitors, and inductors, to generate an AC current that is opposite to the main inductor current to reduce the output voltage ripple, but if this method is applied to the N-phase structure, the added auxiliary components will cause the circuit to be bulky, which will increase the difficulty of circuit analysis.

The literature [5] uses the concept of current injection to inject a current opposite to the inductor current through an external operational amplifier circuit. However, when this method is applied to a continuous conduction mode (CCM) converter, it will not be able to use the current transformer (CT) to detect the inductor current, and due to the bandwidth limitation, the hall sensor cannot be used. Therefore, only the current detection resistor can be used, which will increase the conduction loss. Hence, this structure is not suitable for high current output. In order to overcome the above-mentioned problems, this paper proposes a two-stage step-down structure. The first power stage adopts a buck-boost converter and the second power stage adopts a two-phase interleaved buck converter; the proposed structure has the following characteristics: (i) the output voltage ripple will not change due to input voltage changes; (ii) load changes have little effect on the output voltage ripple; (iii) the second power stage adopts an interleaved structure, so it is suitable for large current output applications; (iv) the circuit design and control method are simple. Since the second power stage uses a two-phase interleaved structure, when the line impedance of each phase is different and the components of each phase are slightly different, the two-phase currents will be unbalanced. As the converter operating time increases, it is more likely to cause the inductor to saturate or the components to age due to overheating. As a result, the performance of the converter will be reduced. Therefore, current-sharing control must be added to fine-tune the duty cycles of the second power stage to achieve the purpose of current sharing. The literature [6–8] proposes current-sharing techniques, but these methods must stabilize the output voltage as well as balance the current of each phase, so the effect of reducing the output current ripple is limited.

In the early days of the soft-switching technology, a full-resonance or semi-resonance structure was used [9,10], which mainly used auxiliary inductors in series with power switches in the circuit and auxiliary capacitors in parallel with power switches to form a resonance circuit so as to achieve zero-voltage or zero-current switching. When the voltage resonance reaches zero, the power switch is turned on to achieve zero-voltage switching (ZVS); when the current resonance reaches zero, the power switch is turned off to achieve zero-current switching (ZCS). Although the switching loss can be reduced by using this method, the power switch must withstand high voltage/current stress during resonance, and it must use high rated voltage/current specifications and high turn-on resistance, which increases circuit cost and conduction loss. In addition, the turn-on and turn-off time of the power switch are determined by the resonance frequency, so variable frequency control must be utilized, which makes the design of the filter difficult.

Later, active clamp [11–13], zero-voltage transition [14–16], and zero-current transition [17,18] technologies were developed. The active clamping technology is a resonant circuit formed by external inductors, capacitors, and power switches. Before the main power switch is turned on, the energy of the main power switch is pumped away to achieve zero-voltage switching and clamp the peak voltage on the switch. In addition, the switching frequency does not change with changes in load and input voltage.

As far as the zero-voltage transition and zero-current transition technology is concerned, it is through the additional auxiliary circuit that the auxiliary switch is turned on before the main power switch is turned on, and the transient resonance technique is used to make the main power switch reach zero voltage or current switching. In the multiphase structure, the literature [19,20] proposes the use of additional auxiliary circuits to achieve soft switching, but due to the addition of too many auxiliary components, not only circuit cost but also conduction loss is increased. The literature [21] proposed a zero-voltage transition technology for a multiphase converter. In a two-phase power stage, the same resonance circuit is used to achieve zero-voltage transition. However, this structure uses variable frequency control, which makes the design of the filter difficult.

Based on the aforementioned, in order to get quite small output ripple and stabilize the output voltage, the two-stage cascaded circuit adopted herein is that the first stage regulates the system output voltage under negative feedback control by sensing the system output voltage, and the second stage regulates the phase currents under a constant duty of about 0.5 with current-sharing control. However, in general, the efficiency of the two-stage structure is lower than that of the single-stage structure. Consequently, the proposed soft-switching technology based on active clamp is applied to these two stages to improve the overall efficiency.

2. Proposed Circuit System

Figure 1 shows the proposed two-stage circuit system. The first stage is constructed by a buck-boost converter with active clamp, and the second stage is built up by a two-phase interleaved buck converter with an active clamp. The first stage is used to control the system output voltage, and the second stage is used to control the system output voltage ripple as little as possible. As for voltage feedback control, the sensed analog system output voltage is sent to the analog-to-digital converter (ADC) after the voltage follower so as to get the corresponding digital signal. Afterwards, this digital signal is transferred to the FPGA via the serial peripheral interface (SPI) to obtain the desired control force after the voltage proportional–integral (PI) controller. On the other hand, as for the current-sharing control to be considered, the sensed analog currents in the switches S_{m2} and S_{m3} are sent to the ADC after the current-sensing transformers CT_1 and CT_2 and then to the FPGA via the SPI to obtain the desired control force after the current-sharing PI controller. Based on these two control forces and the PWM generator, the associated gate driving signals for all the switches are created. It is noted that in order to achieve the minimal system output voltage ripple, the two gate driving signals for the switches S_{m2} and S_{m3} should be shifted by 180 degrees in relation to each other, and the corresponding duty cycles are regulated in the vicinity of 0.5.

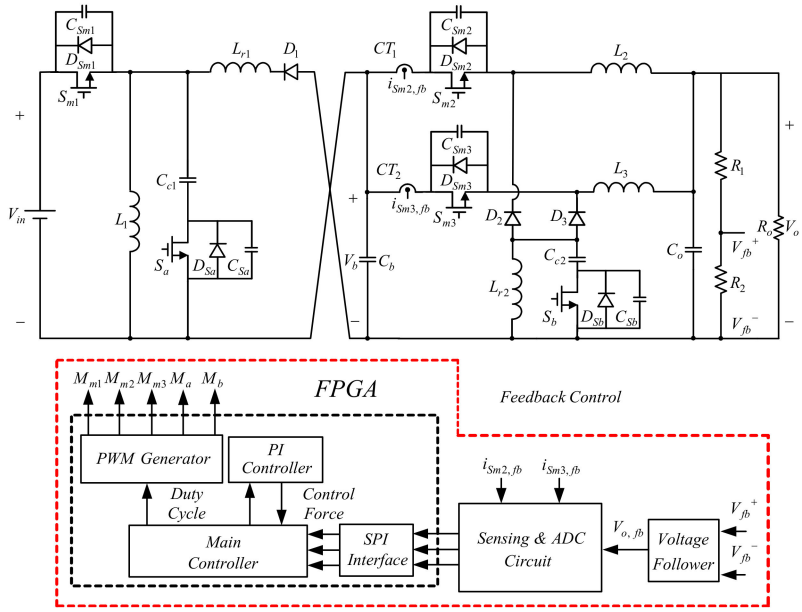

Figure 1. System configuration.

3. Basic Operating Principles

The proposed converter is a combination of the buck-boost converter with an active clamp and the two-phase interleaved boost converter with an active clamp.

Before analyzing the circuit operation principle, the following assumptions are made: (1) all the power switches and diodes are considered ideal; (2) the inductance and capacitance have no internal resistance; (3) the input inductance is extremely large and can

be regarded as an ideal constant current source; (4) the output capacitance is very large and can be regarded as an ideal constant voltage source; (5) the circuit operates in the continuous conduction mode (CCM) in the steady state; (6) the capacitance of the clamp capacitor is much larger than the capacitance of the resonant capacitor, which is equal to the parasitic capacitance of the switch; and (7) the capacitance of the clamp capacitor is large enough such that the voltage on this capacitor can be regarded as a fixed value.

3.1. First-Stage Operating Principles

First, define the symbols of the components, voltages, and currents as shown in Figures 2 and 3: (i) the voltage V_{in} is the input voltage, namely, system input voltage; (ii) the voltage V_b is the first-stage output voltage; (iii) the current I_{L1} is the DC current flowing through the main inductor L_1; (iv) the diodes D_{Sm1} and D_{Sm2} are the parasitic diodes of the main switch S_{m1} and the auxiliary switch S_a, respectively; (v) the capacitors C_{Sm1} and C_{Sa} are the parasitic capacitors of S_{m1} and S_a, respectively; (vi) the currents i_{Sm1} and i_{Sa} are the currents flowing through S_{m1} and S_a, respectively; (vii) the voltages v_{Sm1} and v_{Sa} are the voltages on S_{m1} and S_a, respectively; (viii) the capacitor C_{c1} is the clamping capacitor; (ix) the inductor L_{r1} is the resonance inductor; (x) the diode D_1 is the output diode; (xi) the capacitor C_b is the output capacitor; (xii) the resistor R_b is the output load resistor; (xiii) the voltage v_{Sa} is the voltage on S_a; (xiv) the voltage V_{Cc1} is the voltage on C_{c1}; and (xv) the current i_{Lr1} is the current flowing through L_{r1}.

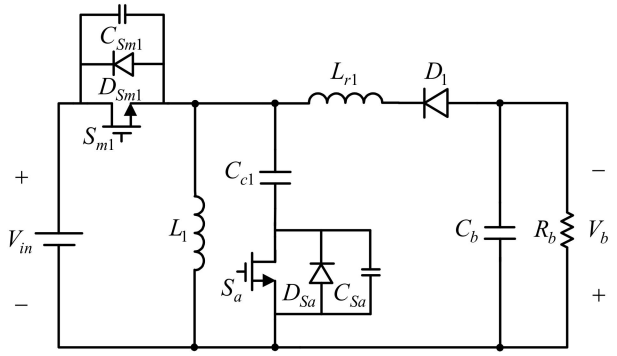

Figure 2. Buck-boost converter with active clamp.

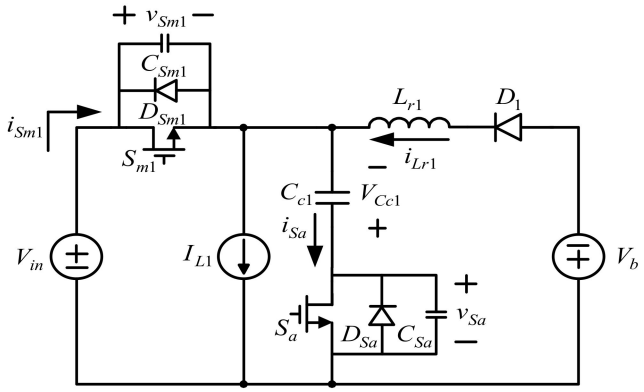

Figure 3. Equivalent circuit for the circuit shown in Figure 2.

Based on the above definitions, Figure 2 can be simplified to the equivalent circuit shown in Figure 3. There are nine operating states over one PWM cycle, as shown in Figure 4. In addition, in Figures 5–13, the current flow is indicated by the real line, and no current flow is denoted by the dotted line; Table 1 shows the corresponding soft-switching states and types.

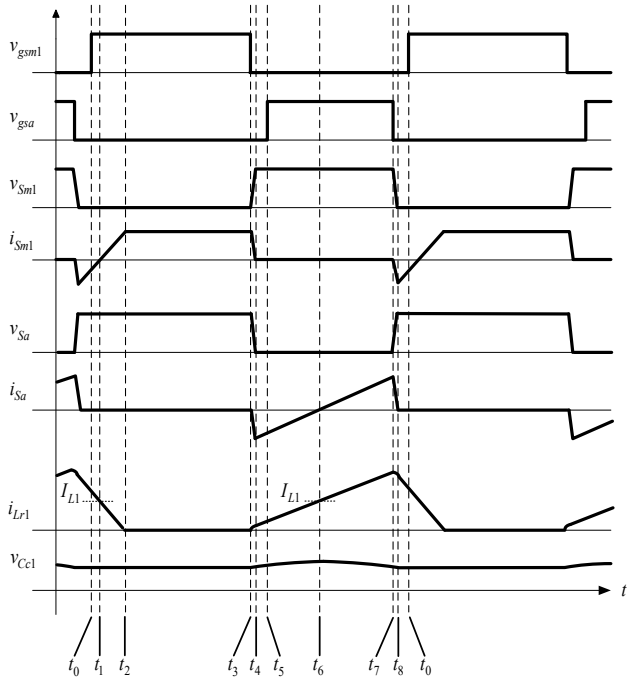

Figure 4. Illustrated waveforms for the buck-boost converter with active clamp.

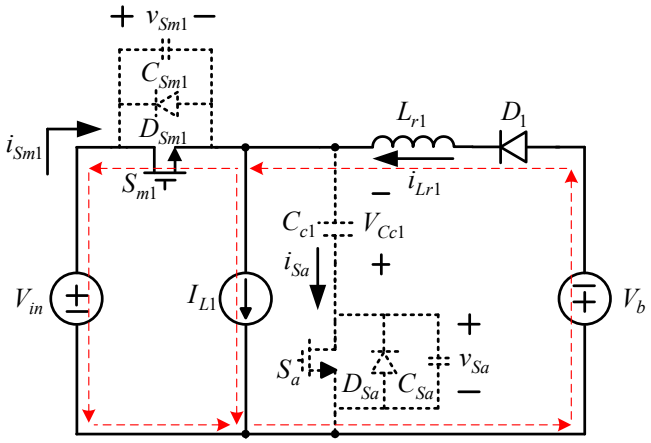

Figure 5. First-stage current flow in state 1.

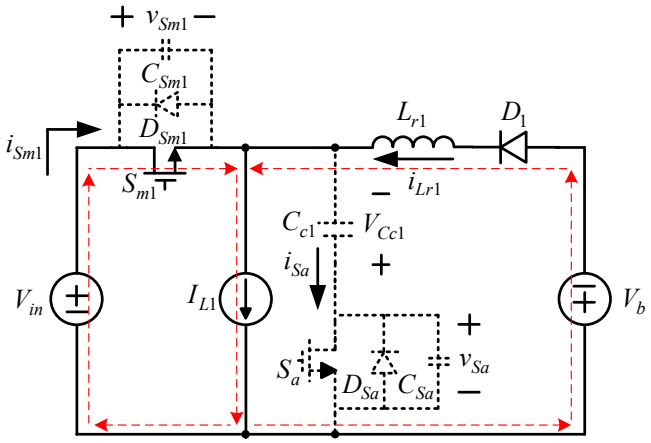

Figure 6. First-stage current flow in state 2.

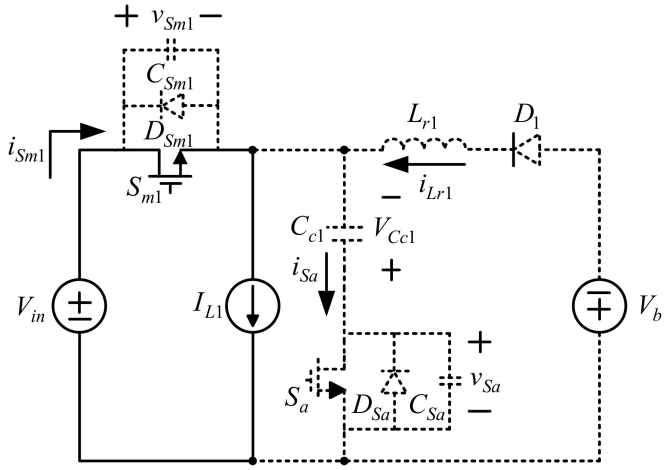

Figure 7. First-stage current flow in state 3.

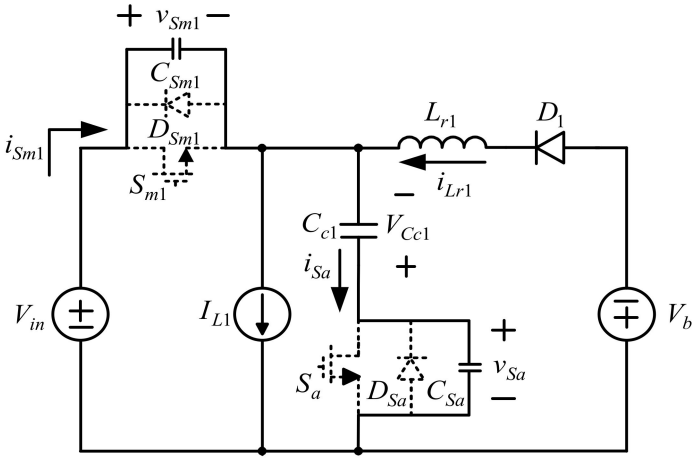

Figure 8. First-stage current flow in state 4.

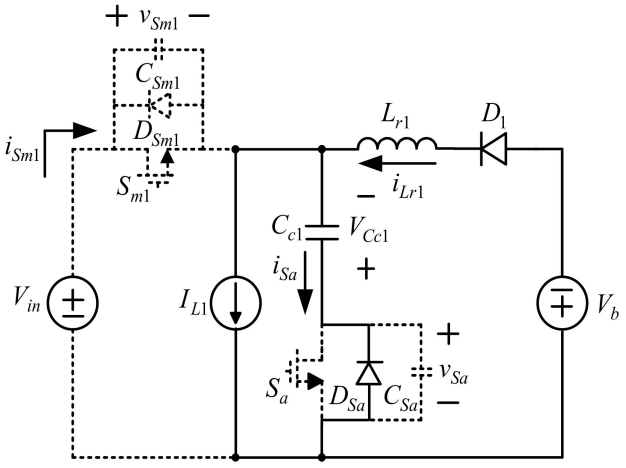

Figure 9. First-stage current flow in state 5.

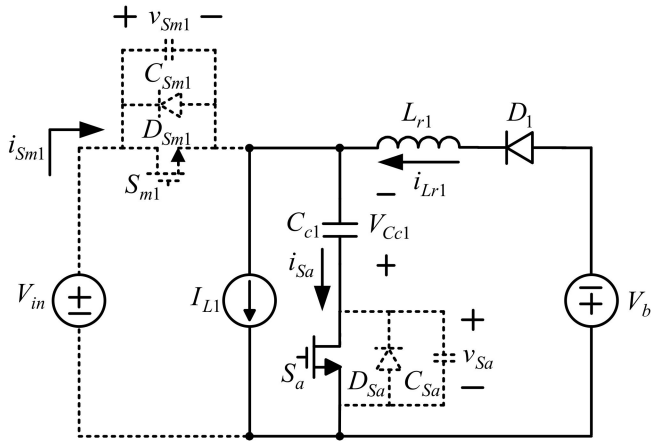

Figure 10. First-stage current flow in state 6.

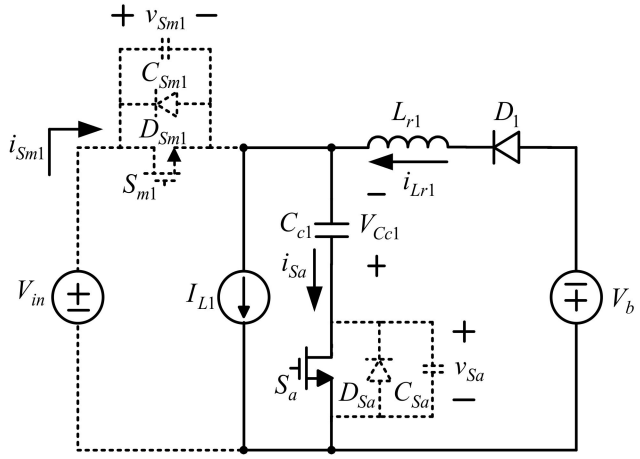

Figure 11. First-stage current flow in state 7.

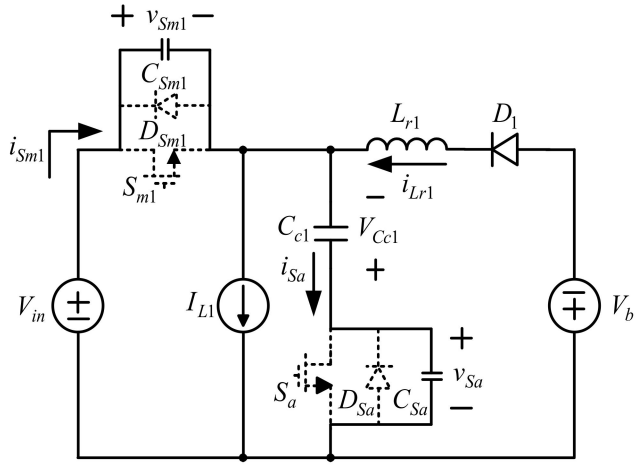

Figure 12. First-stage current flow in state 8.

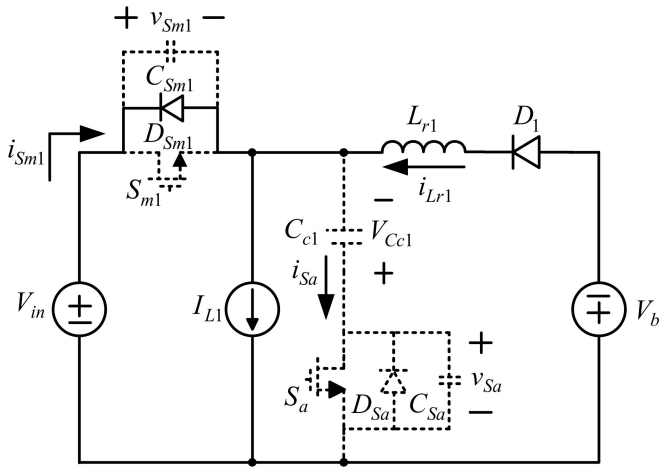

Figure 13. First-stage current flow in state 9.

Table 1. Soft-switching states and types for the first stage.

Interval	State	Soft-Switching Type
$t_0 \leq t \leq t_1$	State 1	S_{m1} with ZVS turn-on
$t_5 \leq t \leq t_6$	State 6	S_a with ZVS turn-on

3.1.1. State 1: $[t_0 \leq t \leq t_1]$

As shown in Figure 5, before the time instant t_0, the resonant inductor current i_{Lr1} is larger than main inductor current I_{L1}, making the body diode D_{sm1} of the main switch S_{m1} conducted. In this time, the auxiliary switch S_a is cut off. When the time reaches t_0, S_{m1} is turned on with ZVS, and afterwards the current i_{Sm1} rises from negative to zero. Once the resonant inductor current i_{Lr} is equal to the main inductor current I_{L1}, this state comes to an end. The initial condition in this state is

$$i_{Lr1}(t_0) = I_{L1} - i_{Sm1}(t_0). \tag{1}$$

The corresponding state equation is

$$i_{Lr1}(t) = -\frac{(V_b + V_{in})}{L_{r1}}(t - t_0) + i_{Lr1}(t_0). \tag{2}$$

As $t = t_1$, $i_{Lr1}(t_1) = I_{L1}$, the elapsed time is Δt_1, which can be expressed as

$$\Delta t_1 = t_1 - t_0 = \frac{[i_{Lr1}(t_0) - I_{L1}]\, L_{r1}}{V_b + V_{in}}. \tag{3}$$

3.1.2. State 2: $[t_1 \leq t \leq t_2]$

As shown in Figure 6, when the time reaches t_1, the resonant inductor current i_{Lr1} is smaller than the main inductor current I_{L1}, making the current i_{Sm1} begin to rise from zero to positive. The moment i_{Lr1} falls to zero, the diode D_1 is turned off, and this state comes to an end. The initial condition in this state is

$$i_{Lr1}(t_1) = I_{L1}. \tag{4}$$

The corresponding state equation is

$$i_{Lr1}(t) = -\frac{(V_b + V_{in})}{L_{r1}}(t - t_1) + i_{Lr1}(t_1). \tag{5}$$

As $t = t_2$, $i_{Lr1}(t_2) = 0$. The elapsed time is Δt_2, which can be expressed as

$$\Delta t_2 = t_2 - t_1 = \frac{I_{L1} L_{r1}}{V_b + V_{in}}. \tag{6}$$

3.1.3. State 3: $[t_2 \leq t \leq t_3]$

As shown in Figure 7, when the diode D_1 is cut off, the operation goes into state 3. At this instant, the main switch S_{m1} is turned on. This state is the same as the traditional boost converter working in state 1. The elapsed time Δt_3 can be expressed to

$$\Delta t_3 = DT_s - \Delta t_1 - \Delta t_2 \tag{7}$$

where D and T_s are the duty cycle and switching period of the gate driving single for the main switch S_{m1}, respectively.

3.1.4. State 4: $[t_3 \leq t \leq t_4]$

As shown in Figure 8, when the main switch S_{m1} is cut off, this state begins. The main inductor current I_{L1} charges the parasitic capacitor C_{Sm1}, making the voltage across S_{m1}, called v_{Sm1}, begin to rise. According to KVL, it can be known that $V_{in} + V_{Cc1} = V_{Sm1} + V_{Sa}$. Therefore, the voltage across the auxiliary switch S_a, called v_{Sa}, begins to fall. As the voltage v_{Sa} drops to zero, this state comes to the end. The initial condition in this state is

$$i_{Lr1}(t_3) = 0,\ v_{Sa}(t_3) = V_{Cc1} + V_{in} \text{ and } v_{Sm1}(t_3) = 0. \tag{8}$$

Via Figure 8, the corresponding state equation can be obtained to be

$$\begin{cases} i_{Lr1}(t) = I_{L1}\left[1 - \cos\omega_1(t - t_3)\right] - \frac{V_{in}+V_b}{Z_1}\sin\omega_1(t - t_3) \\ v_{Sa}(t) = V_{Cc1} + V_{in} - I_{L1}Z_1\sin\omega_1(t - t_3) - (V_{in} + V_b)\left[1 - \cos\omega_1(t - t_3)\right] \\ v_{Sm1}(t) = I_{L1}Z_1\sin\omega_1(t - t_3) + (V_{in} + V_b)\left[1 - \cos\omega_1(t - t_3)\right] \end{cases} \tag{9}$$

where

$$C_{Sm1} = C_{Sa} = C_{S1},\ \omega_1 = \sqrt{\frac{1}{2C_{S1}L_{r1}}},\ \text{and } Z_1 = \sqrt{\frac{L_{r1}}{2C_{S1}}}. \tag{10}$$

In addition, $\cos\omega_1(t_4 - t_3) \approx 1$ and $\sin\omega_1(t_4 \sim t_3) \approx \omega_1(t_4 - t_3)$ under the condition that $\omega_1(t_4 - t_3) \approx 0$. Based on this, the $v_{Sm1}(t_4)$ equation can be rewritten to

$$v_{Sm1}(t_4) = I_{L1}Z_1\omega_1(t_4 - t_3). \tag{11}$$

As $t = t_4$, $V_{Sm1}(t_4) = V_{Cc1} + V_{in}$. The corresponding elapsed time is Δt_4, which can be expressed as

$$\Delta t_4 = t_4 - t_3 = \frac{V_{Cc1} + V_{in}}{\omega_1 I_{L1} Z_1}. \tag{12}$$

3.1.5. State 5: $[t_4 \leq t \leq t_5]$

As shown in Figure 9, when the voltage across the auxiliary switch S_a, called v_{Sa}, falls to zero, its body diode D_{Sa} is conducted, and this state begins. During this state, the main switch S_{m1} is cut off and the resonant inductor is linearly magnetized. As soon as the auxiliary switch S_a is turned on, this state comes to an end. The corresponding state equation is

$$i_{Lr1}(t) = \frac{(V_{Cc1} - V_b)}{L_{r1}}(t - t_4) + i_{Lr1}(t_4). \tag{13}$$

As $t = t_5$, elapsed time Δt_5 can be obtained to be

$$\Delta t_5 = t_5 - t_4 = \frac{L_{r1}[i_{Lr1}(t_5) - i_{Lr1}(t_4)]}{V_{Cc1} - V_b}. \tag{14}$$

3.1.6. State 6: $[t_5 \leq t \leq t_6]$

As shown in Figure 10, the auxiliary switch S_a is turned on with ZVS. At this moment, the resonant inductor L_{r1} is still linearly magnetized. Once the resonant inductor current rises to the main inductor current I_{L1}, this state comes to the end. The corresponding state equation is

$$i_{Lr1}(t) = \frac{(V_{Cc1} - V_b)}{L_{r1}}(t - t_5) + i_{Lr1}(t_5). \tag{15}$$

As $t = t_6$, $i_{Lr1}(t_6) = I_{L1}$, the time elapsed time Δt_6 can be obtained to be

$$\Delta t_6 = t_6 - t_5 = \frac{L_{r1}[I_{L1} - i_{Lr1}(t_5)]}{V_{Cc1} - V_b}. \tag{16}$$

3.1.7. State 7: $[t_6 \leq t \leq t_7]$

As shown in Figure 11, when the time reaches t_6, the resonant inductor L_{r1} is still linearly demagnetized. Since the resonant inductor current i_{L1} is larger than the main switch current I_{L1}, according to KCL, i_{Lr1} is equal to I_{L1} plus i_{Sa}, making the current in the auxiliary switch S_a, i_{Sa}, begin to linearly rise from zero. As soon as the resonant inductor current i_{Lr1} increases to the maximum value $I_{Lr,max}$, this state comes to an end. The initial condition in this state is

$$i_{Lr1}(t_6) = I_{L1}. \tag{17}$$

The corresponding state equation is

$$i_{Lr1}(t) = \frac{(V_{Cc1} - V_b)}{L_{r1}}(t - t_6) + i_{Lr1}(t_6). \tag{18}$$

As $t = t_7$, $i_{Lr}(t_7) = I_{Lr1,max}$. The corresponding elapsed time Δt_7 can be obtained to be

$$\Delta t_7 = t_7 - t_6 = \frac{L_{r1}(I_{Lr1,max} - I_{L1})}{V_{Cc1} - V_b}. \tag{19}$$

3.1.8. State 8: $[t_7 \leq t \leq t_8]$

As shown in Figure 12, when the time reaches t_7, the auxiliary switch S_a is cut off, this state begins. Since the resonant inductor L_{r1} resonates with the parasitic capacitance C_{Sm1} of S_{m1} and the parasitic capacitance C_{Sa} of S_a, the voltage across S_{m1}, v_{Sm1}, begins to fall. According to KVL, V_{in} plus V_{Cc1} is equal to v_{Sm1} plus v_{Sa}, making v_{Sa} begin to rise. As v_{Sm1} drops to zero, this state comes to an end. The initial condition in this state is

$$v_{Sa}(t_7) = 0 \text{ and } v_{Sm1}(t_7) = V_{Cc1} + V_{in}\ . \tag{20}$$

The corresponding state equation is

$$\begin{cases} i_{Lr1}(t) = I_{L1}\left[1 - \cos\omega_1(t - t_7)\right] + i_{Lr1}(t_7)\cos\omega_1(t - t_7) + \frac{V_{Cc1} - V_b}{Z_1}\sin\omega_1(t - t_7) \\ v_{Sa}(t) = V_{Cc1} - \left[I_{L1} - i_{Lr1}(t_7)\right] Z_1 \sin\omega_1(t - t_7) - (V_{Cc1} - V_b)\cos\omega_1(t - t_7) - V_b \\ v_{Sm1}(t) = \left[I_{L1} - i_{Lr1}(t_7)\right] Z_1 \sin\omega_1(t - t_7) + (V_{Cc1} - V_b)\cos\omega_1(t - t_7) + V_b + V_{in} \end{cases}. \tag{21}$$

$\cos\omega_1(t_8 - t_7) \approx 1$ and $\sin\omega_1(t_8 - t_7) \approx \omega_1(t_8 - t_7)$ on the condition that $\omega_1(t_8 - t_7) \approx 0$. Based on this, the $v_{Sm1}(t_8)$ equation can be rewritten to

$$v_{Sm1}(t_8) = \left[I_{L1} - i_{Lr1}(t_7)\right] Z_1\omega_1(t_8 - t_7) + V_{Cc1} + V_{in}. \tag{22}$$

As $t = t_8$, $v_{Sm1}(t_8) = 0$, the corresponding elapsed time is Δt_8, which can be express to be

$$\Delta t_8 = t_8 - t_7 = \frac{V_{Cc1} + V_{in}}{\omega_1(I_{Lr1,max} - I_{L1})\ Z_1}. \tag{23}$$

3.1.9. State 9: $[t_8 \leq t \leq t_0]$

As shown in Figure 13, when the voltage across the main switch S_{m1}, v_{Sm1}, falls to zero, the parasitic diode D_{Sm1} is turned on, and this state begins. At this moment, the auxiliary switch S_a is not conducted, and the resonant inductor L_{r1} is linearly magnetized. The moment S_{m1} is turned on, this state comes to an end, and the next cycle will be repeated.

The corresponding equation can be obtained to be

$$L_{r1}\frac{di_{Lr1}(t)}{dt} = -(V_{in} + V_b). \tag{24}$$

According to (24), the resonant inductor current i_{Lr1} can be obtained to be

$$i_{Lr1}(t) = \frac{-(V_{in} + V_b)}{L_{r1}}(t - t_8) + i_{Lr1}(t_8). \tag{25}$$

As $t = t_0$, the elapsed time to Δt_9, which can be expressed as

$$\Delta t_9 = t_0 - t_8 = \frac{L_{r1}[i_{Lr1}(t_8) - i_{Lr1}(t_0)]}{V_{in} + V_b}. \tag{26}$$

Since the converter operates in the steady state, the voltage-second balance for the main inductor over a PWM cycle T_{s1} should hold. Accordingly, the following equation can be obtained to be

$$V_{in}(D + \alpha)T_s - V_{Cc1}(1 - D - \alpha)T_s = 0 \tag{27}$$

where

$$\alpha = \frac{\Delta t_8 + \Delta t_9}{T_s}. \tag{28}$$

Therefore, the ratio of the clamp capacitor voltage V_{Cc1} to the input voltage V_{in} is

$$\frac{V_{Cc1}}{V_{in}} = \frac{D + \alpha}{1 - D - \alpha}. \tag{29}$$

On the other hand, the voltage-second balance applied to the resonant inductor L_{r1} is

$$(V_{Cc1} - V_b)(1 - D - \alpha)T_s - (V_{in} + V_b)(\alpha + \beta)T_s = 0 \tag{30}$$

where

$$\beta = \frac{\Delta t_1 + \Delta t_2}{T_s}. \tag{31}$$

Substituting (29) into (30) yields the ratio of the output voltage V_b to the input voltage V_{in} is

$$\frac{V_b}{V_{in}} = \frac{D - \beta}{1 - D + \beta}. \tag{32}$$

3.2. Second Stage

First, define the symbols of the components, voltages, and currents, as shown in Figures 14 and 15: (i) the voltage V_b is the second-stage input voltage; (ii) the voltage V_o is the output voltage, namely, system output voltage; (iii) the currents I_{L2} and I_{L3} are the currents flowing through the main inductors L_2 and L_3, respectively; (iv) the diodes D_{Sm2}, D_{Sm3}, and D_{Sb} are the parasitic diodes of the main switches S_{m2} and S_{m3} and auxiliary switch S_b, respectively; (v) the capacitors C_{Sm2}, C_{Sm3}, and C_{Sb} are the parasitic capacitors of S_{m2}, S_{m3}, and S_b, respectively; (vi) the currents i_{Sm2}, i_{Sm2}, and i_{Sb} are the currents flowing through S_{m2}, S_{m3}, and S_b, respectively; (vii) the capacitor C_{c2} is the clamping capacitor; (viii) the inductor L_{r2} is the resonance inductor; (ix) the diodes D_2 and D_3 are the output diodes; (x) the capacitor C_o is the output capacitor; (xi) the resistor R_o is the output load resistor; (xii) the voltage v_{Sm2}, v_{Sm3}, and v_{Sb} are the voltages on S_{m2}, S_{m3}, and

S_b, respectively; (xiii) the voltage V_{Cc2} is the voltage on C_{c2}; (xiv) the currents i_{D2} and i_{D3} are the currents flowing through the output diodes D_2 and D_3, respectively; and (xv) the current i_{Lr2} is the current flowing through L_{r2}.

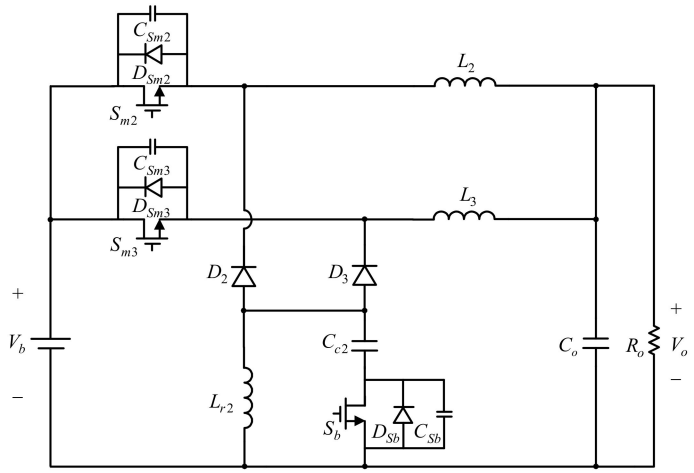

Figure 14. Two-phase interleaved buck converter with active clamp.

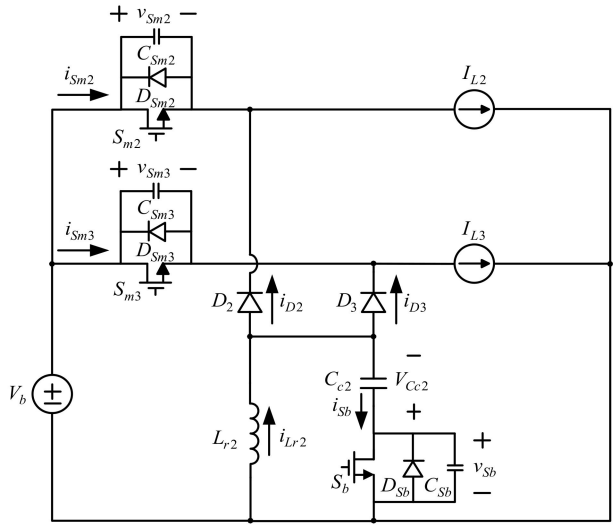

Figure 15. Equivalent circuit for the circuit shown in Figure 14.

Based on the above definitions, Figure 14 can be simplified to the equivalent circuit shown in Figure 15. There are fourteen operating states over one PWM cycle, as shown in Figure 16. However, the two-phase interleaved structure is of symmetricity. Consequently, only the states 1 to 7 will be taken to analyze the behavior of this converter. In addition, in Figures 17–23, the current flow is indicated by the real line, and no current flow is denoted by the dotted line; Table 2 shows the corresponding soft-switching states and types.

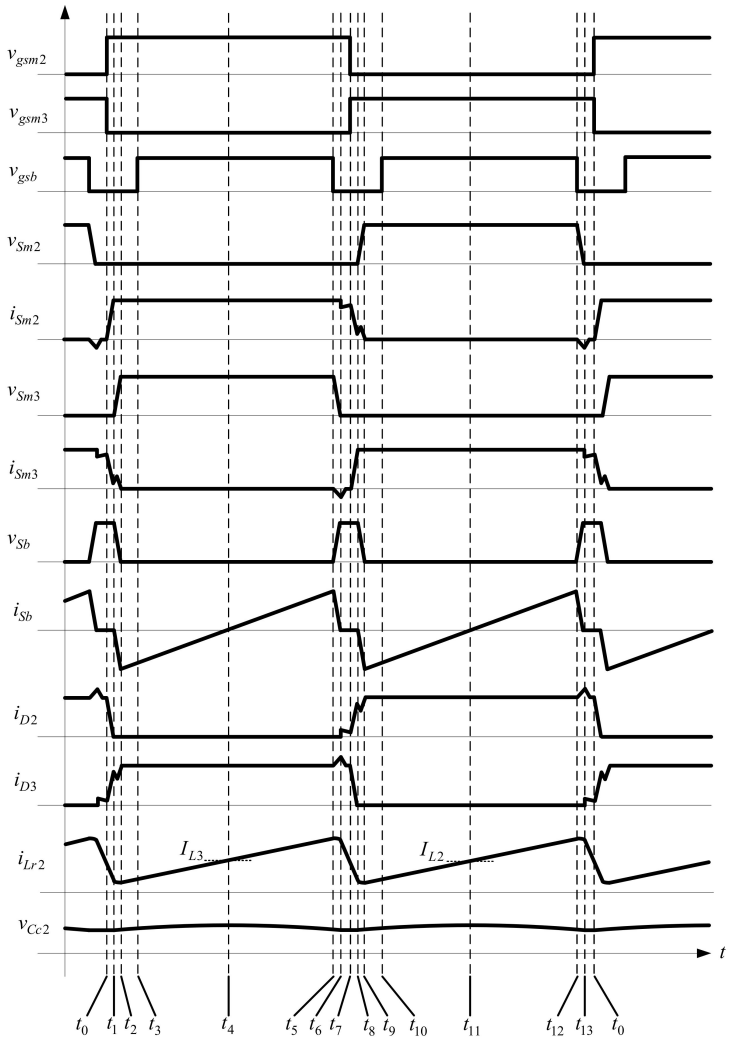

Figure 16. Illustrated waveforms for the two-phase interleaved buck converter with active clamp.

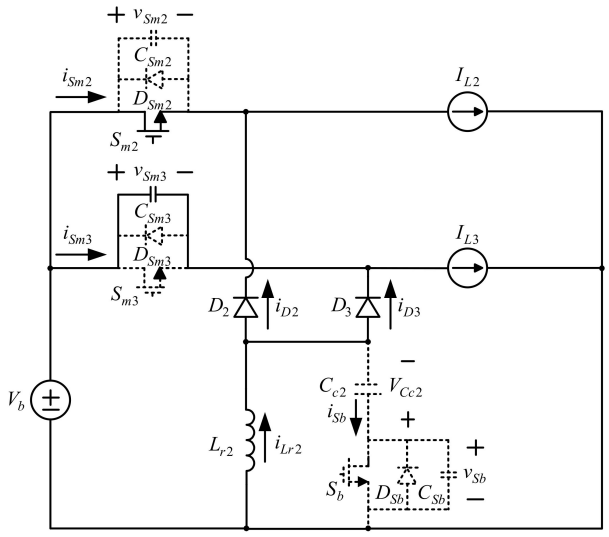

Figure 17. Second-stage current flow in state 1.

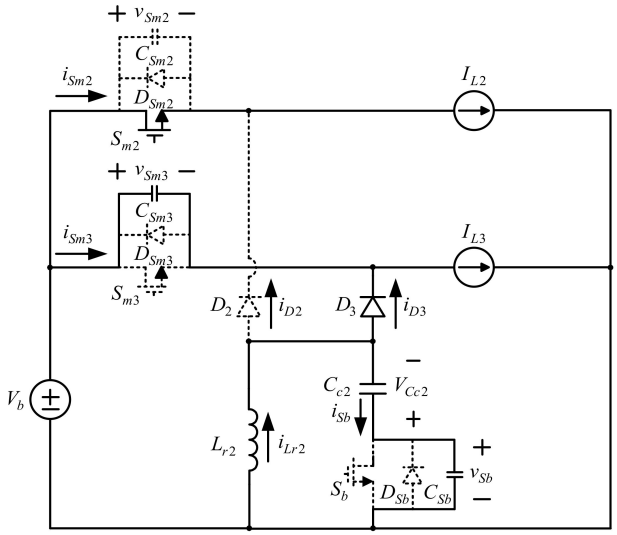

Figure 18. Second-stage current flow in state 2.

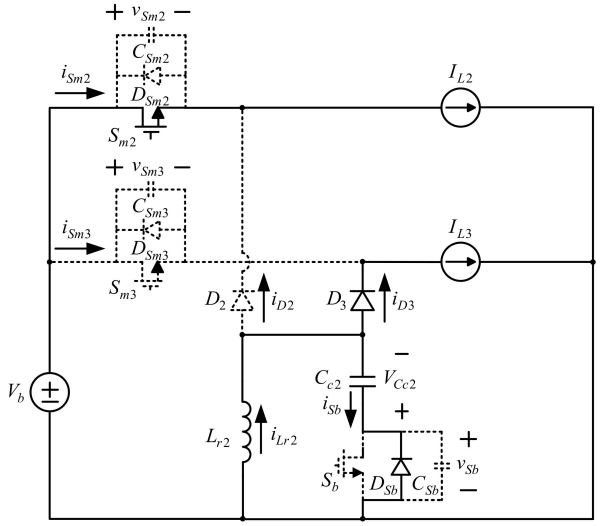

Figure 19. Second-stage current flow in state 3.

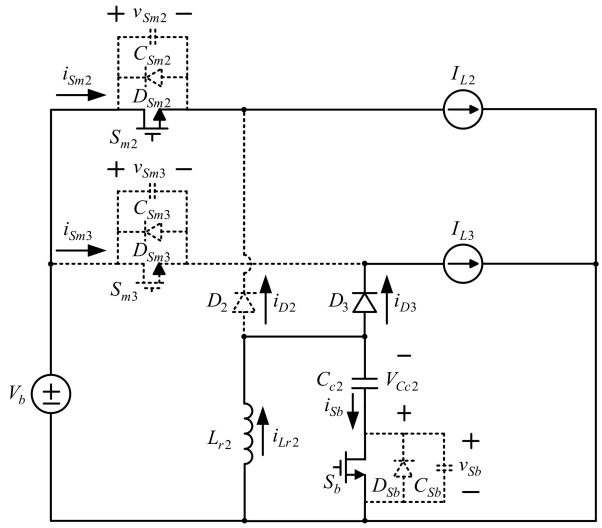

Figure 20. Second-stage current flow in state 4.

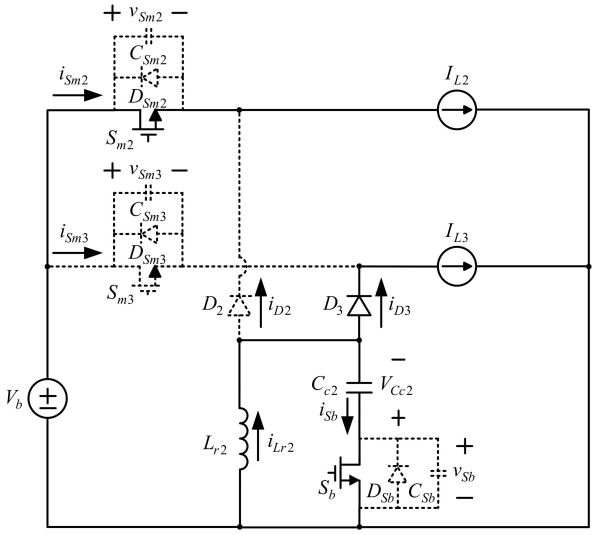

Figure 21. Second-stage current flow in state 5.

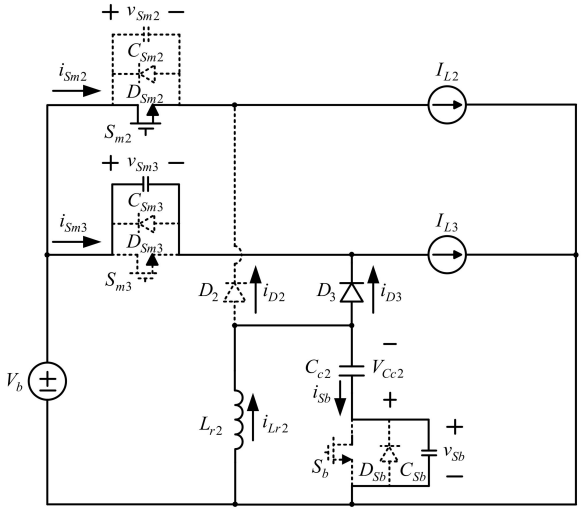

Figure 22. Second-stage current flow in state 6.

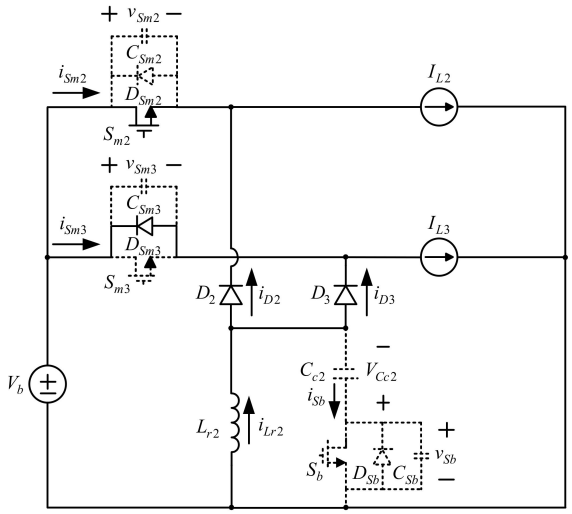

Figure 23. Second-stage current flow in state 7.

Table 2. Soft-switching states and types for the second stage.

Interval	State	Soft-Switching Types
$t_0 \le t \le t_1$	State 1	S_{m2} with ZVS turn-on
$t_3 \le t \le t_4$	State 4	S_b with ZVS turn-on
$t_7 \le t \le t_8$	State 8	S_{m3} with ZVS turn-on
$t_{10} \le t \le t_{11}$	State 11	S_b with ZVS turn-on

3.2.1. State 1: $[t_0 \le t \le t_1]$

As shown in Figure 17, before the time instant t_0, the main switch S_{m2} is conducted, but the main switch S_{m3} is cut off. Since the resonant inductor L_{r1} is demagnetized, the body diode D_{Sm2} of the main switch S_{m2} is conducted. At this instant, the auxiliary switch S_b is cut off. As shown in Figure 17, when $t = t_0$, the main switch S_{m2} is turned on with ZVS. Since the output diode D_2 is still conducted, the voltage across S_{m3} is clamped at zero. As soon as the current in D_2 is zero, this state comes to an end. The initial condition in this state is

$$i_{Lr2}(t_0) = I_L - i_{Sm3}(t_0). \tag{33}$$

The corresponding state equation is

$$i_{Lr2}(t) = -\frac{V_b}{L_{r2}}(t - t_0) + i_{Lr2}(t_0). \tag{34}$$

As $t = t_1$, the elapsed time T_1 can be obtained to be

$$T_1 = t_1 - t_0 = \frac{[i_{Lr2}(t_0) - i_{Lr2}(t_1)]\ L_{r2}}{V_b}. \tag{35}$$

3.2.2. State 2: $[t_1 \le t \le t_2]$

As shown in Figure 18, when the time reaches t_1, since the output diode D_2 is cut off, the voltage across the main switch S_{m3}, called v_{Sm3}, goes up. According to KVL, $V_b + V_{Cc2} = V_{Sm3} + V_{Sb}$, making the voltage across the auxiliary switch S_b, called v_{Sb}, begin to fall. The moment the voltage v_{Sb} drops to zero, this state comes to an end. The initial condition in this state is

$$v_{Sb}(t_1) = V_b + V_{Cc2} \text{ and } v_{Sm3}(t_1) = 0. \tag{36}$$

The corresponding state equation is

$$\begin{cases} i_{Lr2}(t) = I_{L3}\,[1 - \cos\omega_2(t - t_1)\,] + i_{Lr2}(t_1)\cos\omega_2(t - t_1) - \frac{V_b}{Z_1}\sin\omega_2(t - t_1) \\ v_{Sb}(t) = V_{Cc2} - [I_{L3} - i_{Lr2}(t_1)]\ Z_2 \sin\omega_2(t - t_1) + V_b\cos\omega_2(t - t_1) \\ v_{Sm3}(t) = [I_{L3} - i_{Lr2}(t_1)]\ Z_2 \sin\omega_2(t - t_1) + V_b\,[1 - \cos\omega_2(t - t_1)\,] \end{cases} \tag{37}$$

where

$$C_{Sm2} = C_{Sm3} = C_{Sb} = C_{S2},\ \omega_2 = \sqrt{\frac{1}{2C_{S2}L_{r2}}},\ \text{and}\ Z_2 = \sqrt{\frac{L_{r2}}{2C_{S2}}}. \tag{38}$$

In addition, $\cos\omega_2(t_2 - t_1) \approx 1$ and $\sin\omega_2(t_2 \sim t_1) \approx \omega_2(t_2 - t_1)$ under the condition that $\omega_1(t_2 - t_1) \approx 0$. Based on this, the $v_{Sm3}(t_2)$ equation can be rewritten to

$$v_{Sm3}(t_2) = [I_{L3} - i_{Lr2}(t_1)]\ Z_2\omega_2(t_2 - t_1). \tag{39}$$

As $t = t_2$, $v_{Sm3}(t_2) = V_b + V_{Cc2}$. Therefore, the elapsed time T_2, which can be expressed as

$$T_2 = t_2 - t_1 = \frac{V_b + V_{Cc2}}{\omega_2[I_{L3} - i_{Lr2}(t_1)]\ Z_2}. \tag{40}$$

3.2.3. State 3: $[t_2 \leq t \leq t_3]$

As shown in Figure 19, when the voltage across the auxiliary switch S_b drops to zero, the body diode D_{Sb} of S_b conducts, and hence, this state begins. During this state, the main switch S_{m3} is cut off, whereas the resonant inductor is linearly magnetized. As S_b is turned on, this state comes to the end. The corresponding state equation is

$$i_{Lr2}(t) = \frac{V_{Cc2}}{L_{r2}}(t - t_2) + i_{Lr2}(t_2). \tag{41}$$

As $t = t_3$, the elapsed time is T_3, which can be expressed as

$$T_3 = t_3 - t_2 = \frac{L_{r2}[i_{Lr2}(t_3) - i_{Lr2}(t_2)]}{V_{Cc2}}. \tag{42}$$

3.2.4. State 4: $[t_3 \leq t \leq t_4]$

As shown in Figure 20, when the time reaches t_3, the auxiliary switch S_b is turned on with ZVS. During this state, the resonant inductor L_{r2} is still linearly magnetized. Once the resonant inductor current i_{Lr2} is equal to the main inductor I_{L3}, this state comes to the end. The corresponding state equation is

$$i_{Lr2}(t) = \frac{V_{Cc2}}{L_{r2}}(t - t_3) + i_{Lr2}(t_3). \tag{43}$$

As $t = t_4$, $i_{Lr2}(t_4) = I_{L3}$, the elapsed time is T_4, which can be expressed as

$$T_4 = t_4 - t_3 = \frac{L_{r2}[I_{L3} - i_{Lr2}(t_3)]}{V_{Cc2}}. \tag{44}$$

3.2.5. State 5: $[t_4 \leq t \leq t_5]$

As shown in Figure 21, when the time reaches t_4, the resonant inductor L_{r2} is still linearly magnetized. Since the resonant inductor current i_{Lr2} is larger than I_{L3}, according to KVL, it can be noted that $i_{Lr2} = I_{L3} + i_{Sb}$, making the current in the auxiliary switch S_b, i_{Sb}, begin to linearly rise from zero. As i_{Lr2} rises to the maximum value, this state comes to the end.

The corresponding initial condition is

$$i_{Lr2}(t_4) = I_{L3}. \tag{45}$$

The corresponding state equation is

$$i_{Lr2}(t) = \frac{V_{Cc2}}{L_{r2}}(t - t_4) + i_{Lr2}(t_4). \tag{46}$$

As $t = t_5$, $i_{Lr2}(t_5) = I_{Lr2,max}$, the elapsed time is T_5, which can be expressed as

$$T_5 = t_5 - t_4 = \frac{L_{r2}(I_{Lr2,max} - I_{L3})}{V_{Cc2}}. \tag{47}$$

3.2.6. State 6: $[t_5 \leq t \leq t_6]$

As shown in Figure 22, when the time reaches t_5, the auxiliary switch S_b is turned off, and hence, this state begins. Since the resonant inductor L_{r2} resonates with the parasitic capacitor C_{Sm3} of the main switch S_{m3} and the parasitic capacitor C_{Sb} of the auxiliary switch S_b, the voltage across S_{m3}, called v_{Sm3}, begins to fall. According to KVL, $V_b + V_{Cc2} = v_{Sm3} + v_{Sb}$, making the voltage across S_b, called v_{Sb}, begin to rise. The moment the voltage v_{Sm3} drops to zero, this state comes to the end. The initial condition in this state is

$$v_{Sb}(t_5) = 0 \text{ and } v_{Sm3}(t_5) = V_b + V_{Cc2}. \tag{48}$$

The corresponding state equation is

$$\begin{cases} i_{Lr2}(t) = I_{L3}\left[1-\cos\omega_2(t-t_5)\right] + i_{Lr2}(t_5)\cos\omega_2(t-t_5) + \frac{V_{Cc2}}{Z_2}\sin\omega_2(t-t_5) \\ v_{Sb}(t) = V_{Cc2} - \left[I_{L3} - i_{Lr2}(t_5)\right] Z_2 \sin\omega_2(t-t_5) + V_{Cc2}\cos\omega_2(t-t_5) \\ v_{Sm3}(t) = \left[I_{L3} - i_{Lr2}(t_5)\right] Z_2 \sin\omega_2(t-t_5) + V_{Cc2}\cos\omega_2(t-t_5) + V_b \end{cases}. \quad (49)$$

$\cos\omega_2(t_6-t_5) \approx 1$ and $\sin\omega_2(t_6 \sim t_5) \approx \omega_2(t_6-t_5)$ on the condition that $\omega_2(t_6-t_5) \approx 0$. Based on this, the $v_{Sm3}(t_6)$ equation can be rewritten to

$$v_{Sm3}(t_6) = \left[I_{L3} - i_{Lr2}(t_5)\right] Z_2\omega_2(t_6-t_5) + V_{Cc2} + V_b. \quad (50)$$

As $t = t_6$, $v_{Sm3}(t_6) = 0$. Therefore, the elapsed time is T_6, which can be expressed by

$$T_6 = t_6 - t_5 = \frac{V_{Cc2} + V_b}{\omega_2(I_{Lr2,max} - I_{L3})\, Z_2}. \quad (51)$$

3.2.7. State 7: $[t_6 \le t \le t_7]$

As shown in Figure 23, when the voltage v_{Sm3} of the main switch S_{m3} falls to zero, its parasitic diode D_{Sm3} and the output diode D_2 are turned on, and this state begins. During this state, the auxiliary switch S_b is cut off, and the resonant inductor L_{r2} is linearly demagnetized. As soon as the main switch S_{m3} conducts, this state comes to the end, and the next cycle will be repeated. The corresponding equation is

$$i_{Lr2}(t) = -\frac{V_b}{L_{r2}}(t-t_6) + i_{Lr2}(t_6). \quad (52)$$

As $t = t_7$, the elapsed time is T_7, which can be expressed as

$$T_7 = t_7 - t_6 = \frac{\left[i_{Lr2}(t_6) - i_{Lr2}(t_7)\right] L_{r2}}{V_b}. \quad (53)$$

Since the converter operates in the steady state, the voltage-second balance for the main inductor L_2 over a PWM cycle T_{s2} should hold. Accordingly, the following equation can be obtained to be

$$(V_b - V_o)(D+\alpha+\beta)T_s - (V_{Cc2} + V_o)(1-D-\alpha-\beta)T_s = 0 \quad (54)$$

where

$$\alpha = \frac{T_6 + T_7}{T_s} \quad (55)$$

$$\beta = \frac{T_1 + T_2}{T_s}. \quad (56)$$

On the other hand, the voltage-second balance applied to the resonant inductor L_{r2} is

$$V_{Cc2}(1-D-\alpha-\beta)T_s - V_b(\alpha+\beta)T_s = 0. \quad (57)$$

Rearranging (57) yields the ratio of the clamp capacitor voltage V_{Cc2} to the output voltage V_o as following:

$$\frac{V_{Cc2}}{V_b} = \frac{\alpha+\beta}{1-D-\alpha-\beta}. \quad (58)$$

Substituting (58) into (54) yields the output voltage V_o to the input voltage V_d as follows:

$$\frac{V_o}{V_b} = D. \quad (59)$$

4. Control Strategy

4.1. Output Voltage Ripple Minimization

For the traditional buck converter operating in CCM to be considered, the circuit is shown in Figure 24. Figure 25 shows its equivalent circuit, where the voltage v_p is a pulse voltage that is determined by the input voltage V_{in} and the duty cycle D, and the inductor current $i_{L1}(t)$ is the DC component plus AC component, namely, $i_{L1}(t) = I_{L1} + \Delta i_{L1}(t)$.

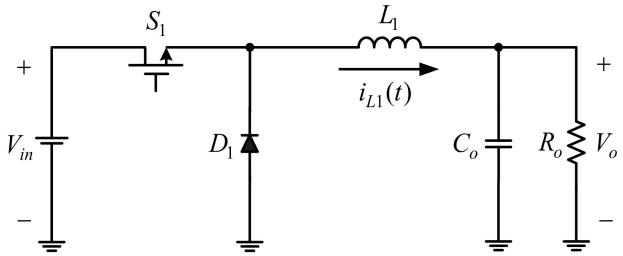

Figure 24. Traditional buck converter.

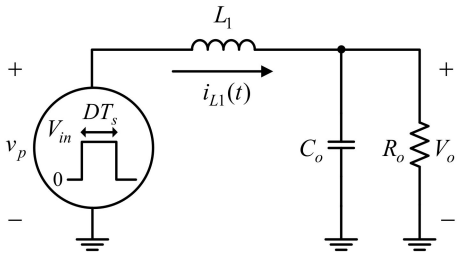

Figure 25. Simplified circuit for Figure 24.

The output voltage ripple comes from the AC part of the inductor current, which is the inductor current ripple, also called output current ripple, namely, $\Delta i_{L1}(t)$, as shown in Figure 26. In addition, the equivalent circuit for the output voltage ripple can be shown in Figure 27. The magnetizing slope m_1 and the demagnetizing slope m_2 as shown in Figure 26 are

$$m_1 = \frac{V_{in} - V_o}{L_1} \tag{60}$$

$$m_2 = -\frac{V_o}{L_1}. \tag{61}$$

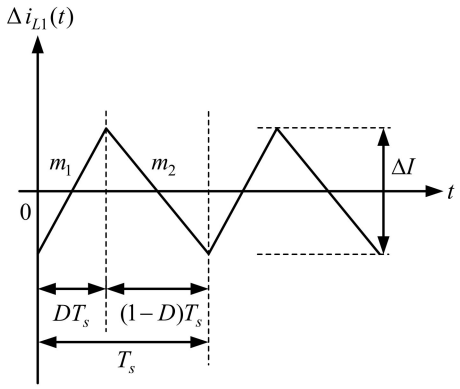

Figure 26. AC part of the inductor current.

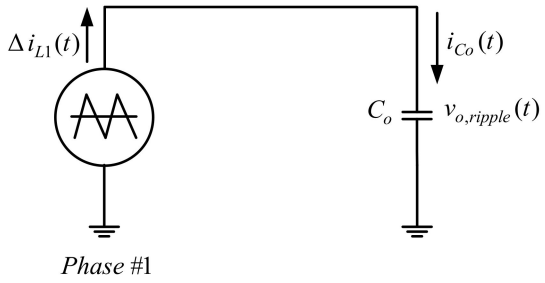

Figure 27. Equivalent circuit for the output voltage ripple.

The peak-to-peak value of the inductor current ripple ΔI can be denoted by

$$\Delta I = m_1 D T_s = |m_2|(1-D)T_s \, . \tag{62}$$

From (60), (61), and (62), it can be seen that the inductor current ripple $\Delta i_{L1}(t)$ can be expressed as

$$\Delta i_{L1}(t) = \begin{cases} m_1 t - \frac{\Delta I}{2} & (0 < t \le D T_s) \\ \frac{\Delta I}{2} + m_2 t & (D T_s \le t < T_s) \end{cases} \tag{63}$$

Therefore, for the N-phase interleaved buck converter, the kth phase inductor current ripple $\Delta i_{Lk}(t)$ can be represented by

$$\Delta i_{Lk}(t) = \Delta i_{L1}\left[t - (k-1)\frac{T_s}{N}\right]. \tag{64}$$

In addition, the current flowing into the output capacitor C_o is equal to the sum of AC components of the inductor currents of individual phases, as shown in Figure 28.

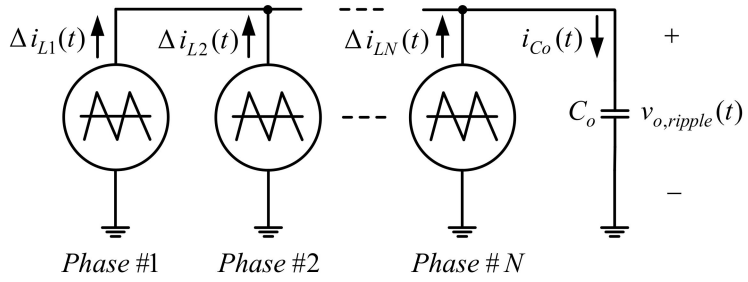

Figure 28. Equivalent circuit for the output voltage ripple of the N-phase interleaved buck converter.

Therefore, the current ripple $i_{Co}(t)$ of the output capacitor C_o can be represented by

$$i_{Co}(t) = \sum_{k=1}^{N} \Delta i_{L1}(t). \tag{65}$$

Meanwhile, the peak-to-peak value of Δi_{Co} can be expressed by

$$\Delta i_{Co} = Max(i_{Co}(t)) - Min(i_{Co}(t)) \tag{66}$$

where $Max(i_{Co}(t))$ and $Min(i_{Co}(t))$ represent the maximum and minimum values over one period, respectively.

If a two-phase interleaved buck converter is taken into account, then the relationship between the output current ripple Δi_{Co} and the duty cycle D can be shown as follows:

$$\Delta i_{Co} = \begin{cases} \frac{V_o T_s}{L_1}(1-2D) & if\ D \le 0.5 \\ \frac{V_o T_s}{L_1}(1-D)\left(\frac{2D-1}{D}\right) & if\ D > 0.5 \end{cases} . \tag{67}$$

In the same way, based on [22], the peak-to-peak output current ripple can be obtained to be

$$\Delta i_{Co} = \Delta I \times KI \tag{68}$$

where ΔI is the peak-to-peak value of the AC component of each phase, and KI is the output current ripple elimination factor, which is defined as

$$KI = \frac{N(D - \frac{m}{N})(\frac{m+1}{N} - D)}{D(1 - D)} \tag{69}$$

where m = floor($N \times D$); that is, the maximum integer of the product of N and D.

Based on (68) and (69), for the N-phase interleaved buck converter, the curve of the output current ripple versus duty cycle can be drawn in Figure 29. From Figure 29, it can be seen that as the number of phases N multiplied by the duty cycle D belongs to integers, the output current ripple can be zero in theory. Accordingly, if the two-phase interleaved buck converter has a duty cycle of 0.5, then the smallest output voltage ripple can be obtained under the smallest output current ripple.

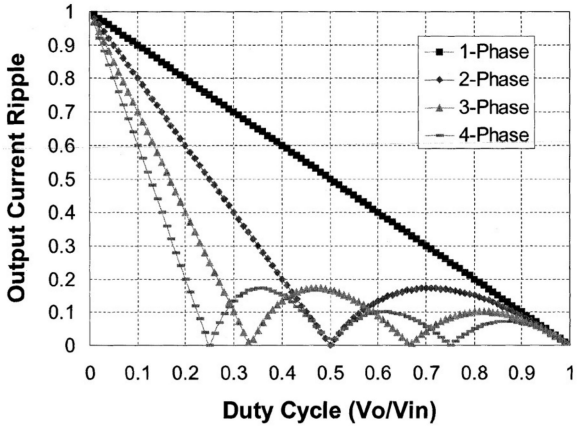

Figure 29. Curves for relationship between phase number, duty cycle, and output current ripple.

4.2. Output Voltage Regulation

However, based on the information mentioned in Section 4.1, another problem will happen. Since the input voltage V_{in} of a single-stage converter cannot be automatically tuned in general, the output voltage V_o cannot be regulated to a desired value from light load to rated load under a fixed duty cycle. Consequently, to conquer this problem, a buck-boost converter is added in the front of the two-phase interleaved buck converter. As shown in Figure 30, the output voltage V_o can be regulated to a desired value based on the feedback control and the pulse width modulation (PWM) control by sensing the output voltage V_o, and this is applied to the first stage so as to make the second-stage input voltage V_b varied. As for the pulse amplitude modulation (PAM) control, it is applied to the second stage under a fixed duty cycle of 0.5 with the input voltage V_b varied. By doing so, the output voltage ripple can be minimized and the output voltage V_o can be regulated.

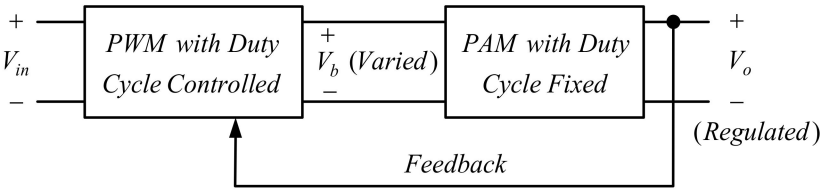

Figure 30. Schematic diagram for the control strategy based on PAM cooperated with PWM.

4.3. Current-Sharing Control

However, there exists a difference in impedance between two phases, since the second stage takes the two-phase interleaved buck converter. Consequently, the current-sharing control is needed to make the output current evenly distributed between the two phases. In general, the current is sampled at half of the duty cycle to reduce noise interference. However, this does not work herein, since the switching frequency of the first stage is double that of the second stage. Accordingly, as shown in Figure 31, the current is sampled at 90% of the duty cycle and two-cycle delay control with the first cycle sampling currents of two phases simultaneously: the second cycle calculating out the control force and the third cycle sending out the desired PWM control signals to the switches, so as to realize current-sharing control.

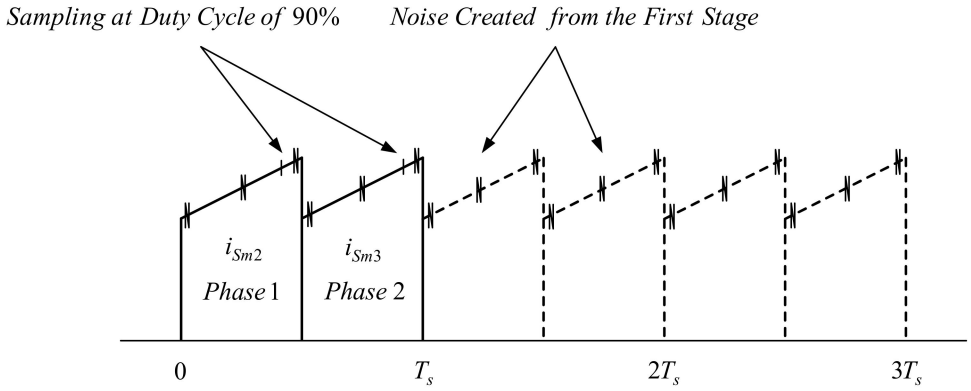

Figure 31. Proposed sampling method for current sharing.

As for the current-sharing operation shown in Figure 32, the two-phase switch currents i'_{Sm2} and i'_{Sm3}, after two analog-to-digital converters ADC1 and ADC2, respectively, are subtracted from each other, and then, this value is sent to the current-sharing proportional–integral (PI) controller to generate the required control force. This control force with a minus sign is superimposed on the duty cycle of 50% for the first phase, whereas this control force with a plus sign is superimposed on the duty cycle of 0.5 for the second phase. For example, if the control force is positive, the duty cycle of the first phase is decreased but the duty cycle of the second phase is increased; otherwise, the duty cycle of the first phase is increased but the duty cycle of the second phase is decreased. Hence, the duty cycle is controlled in the vicinity of the duty cycle of 0.5 so as to make the output current evenly distributed between the two phases.

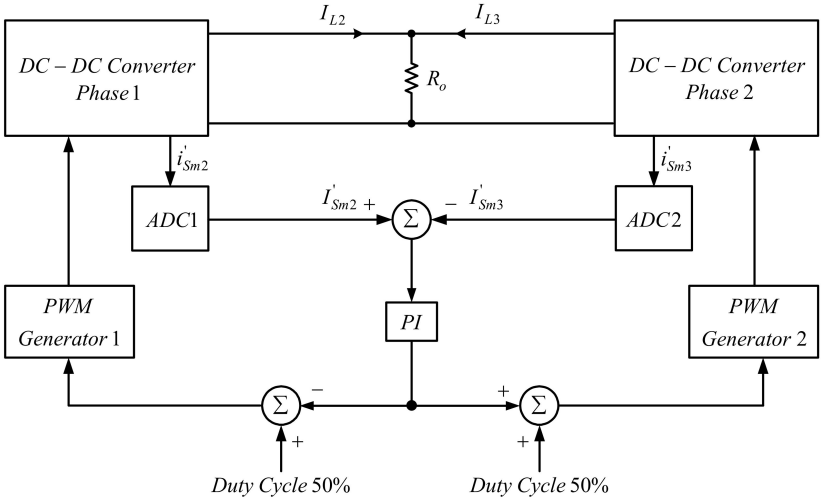

Figure 32. Current-sharing control strategy.

5. Design of Resonant Inductor and Clamp Capacitor

Prior to this section, the parameters for the system and components are shown in Table 3.

Table 3. System and component specifications.

Parameters for System and Components	Specifications
Operating mode	CCM
Input voltage (V_{in})	36–60 V
Output voltage (V_o)	24 V
Rated output power ($P_{o,rated}$)/current ($I_{o,rated}$)	192 W/8 A
Minimum output power ($P_{o,min}$)	38.4 W
Switching frequency (f_s)/period (T_s)	First stage: f_{s1} = 100 kHz/T_{s1} = 10 µs
	Second stage: f_{s2} = 50 kHz/T_{s2} = 20 µs
Inductors	First stage: L_1 = 120 µH
	Second stage: L_2 = L_3 = 180 µH
Output capacitors	First stage: C_{o1} = 330 µF
	Second stage: C_{o2} = 100 µF
Resonant inductors	First stage: L_{r1} = 10 µH
	Second stage: L_{r2} = 10 µH
Clamp capacitors	First stage: C_{c1} = 2 µF
	Second stage: C_{c2} = 4.4 µF

5.1. Design of First-Stage Resonant Inductor L_{r1}

Based on state 4 of the first stage and from (10) and (12), the voltage across C_{c1} and V_{Cc1} can be expressed as

$$V_{Cc1} = \frac{I_{L1}}{2C_{S1}}\Delta t_4 - V_{in,\min}. \tag{70}$$

From (29), we can know the ratio of clamp capacitor voltage V_{Cc1} to input voltage V_{in}. Since the value of α is positive, V_{Cc1} is larger than 48 V. In addition, from the switch datasheet [23], the curve of rising time t_r and falling time t_f versus switch current I_{ds} can be obtained, and hence, the time interval Δt_4 is about 20 ns. Therefore, substituting associated values into (71) yields the value of C_{S1}, which is finally chosen to be 1 nF:

$$C_{S1} \le \frac{I_{L1}}{2(V_{Cc1} + V_{in,min})}\Delta t_4. \tag{71}$$

In general, the resonant frequency is ten times the switching frequency or more, namely, $\omega_1 > 20\pi f_{s1}$, in order to avoid the resonant time being too long and hence affecting the normal operation of the converter. Therefore, from (10), substituting the associated values into (72) yields the value of L_{r1}, which is finally chosen to be 10 µH:

$$L_{r1} \le \frac{1}{2C_{S1}(20\pi f_s)^2}. \tag{72}$$

5.2. Design of First-Stage Voltage Clamp Capacitor C_{c1}

From Figure 4, it can be seen that the capacitor C_{c1} has slight charge and discharge behavior during states 4 to 8. Accordingly, from states 7 and 8, the voltage ripple on C_{c1} can be expressed as

$$\Delta v_{Cc1} = \frac{\Delta Q}{C_{c1}} = \frac{I_{Sa,max}(\Delta t_7 + \Delta t_8)}{2C_{c1}} \tag{73}$$

where $\Delta t_7 + \Delta t_8$ is the time interval from t_6 to t_8.

Since Δt_8 is quite small, Equation (19) can be rewritten as

$$\Delta t_7 + \Delta t_8 \cong \Delta t_7 = \frac{L_{r1}(I_{Lr1,max} - I_{L1})}{V_{Cc1} - V_b}. \tag{74}$$

In order to make the value of V_{Cc1} constant, the clamp capacitor voltage ripple Δv_{Cc1} is 5% of V_{Cc1}. Therefore, substituting the associated values into (73) and (74) yields the value of C_{c1}, which is finally chosen to be 2 μF.

5.3. Design of Second-Stage Resonant Inductor L_{r2}

From (38) and (51), the voltage across C_{c2}, V_{Cc2}, can be expressed as

$$V_{Cc2} = \frac{I_{L3}}{2C_{s2}} T_6 - V_b. \tag{75}$$

Via the switch datasheet [24], the curve of rising time t_r and falling time t_f versus switch current I_{ds} can be obtained, and hence, the time interval T_6 is about 100 ns.

From (58), we can know the ratio of the clamp capacitor voltage V_{Cc2} to the input voltage V_b. Since $(\alpha + \beta)T_{s2}$ is larger than T_6 = 100 ns, the inequality of V_{Cc2} can be expressed as

$$V_{Cc2} > V_b \left(\frac{\alpha + \beta}{1 - D - \alpha - \beta} \right). \tag{76}$$

Based on (75) and (76), the inequality of C_{S2} can be signified by

$$C_{S2} \leq \frac{I_{L3}}{2(V_{Cc2} + V_b)} T_6. \tag{77}$$

Therefore, substituting the associated values into (77) yields the value of $C_{S2,}$ which is finally chosen to be 4 nF.

In general, the resonant frequency is ten times the switching frequency or more, namely, $\omega_2 > 20\pi f_{s2}$, in order to avoid the resonant time being too long and hence affecting the normal operation of the converter. Therefore, based on (38), substituting the associated values into (78) yields the value of L_{r2}, which is finally chosen to be 10 μH:

$$L_{r2} \leq \frac{1}{2C_{S2}(20\pi f_s)^2}. \tag{78}$$

5.4. Design of Second-Stage Voltage Clamp Capacitor C_{c2}

From Figure 16, it can be seen that the capacitor C_{c2} has a slight charge and discharge behavior during states 2 to 6. Accordingly, from states 5 and 6, the voltage ripple on C_{c1} can be expressed as

$$\Delta v_{Cc2} = \frac{\Delta Q}{C_{c2}} = \frac{I_{Sb,max}(T_5 + T_6)}{2C_{c2}} \tag{79}$$

where $T_5 + T_6$ is the time interval from t_4 to t_6.

In order to make the voltage on C_{c2}, called V_{Cc2}, stable at a constant, it is assumed that the voltage ripple is 5% of V_{Cc2}. From (47), since T_6 is quite small, the following equation can be obtained to be

$$T_5 + T_6 \cong T_5 = \frac{L_{r2}(I_{Lr2,max} - I_{L3})}{V_{Cc2}}. \tag{80}$$

Substituting the associated values into (79) and (80) yields the value of C_{C2}, which is finally chosen to be 4.4 μF.

6. Experimental Results

Figures 33–40 show results measured under an input voltage of 48 V. From Figures 33–37, it can be seen that the main and auxiliary switches of the first and second stages all have ZVS turned on. From Figure 38, it can be seen that the current is evenly distributed between the two phases. From Figure 39, it can be seen that the output voltage ripple without switching noise considered is about 8 mV, below 0.017% of 48 V. From Figure 40, it can be seen that the proposal with soft switching has higher efficiency than hard switching. The maximum difference in efficiency between the two is about 5.8%. The proposed has the maximum efficiency of 89.4% and the rated-load efficiency of 85.5%.

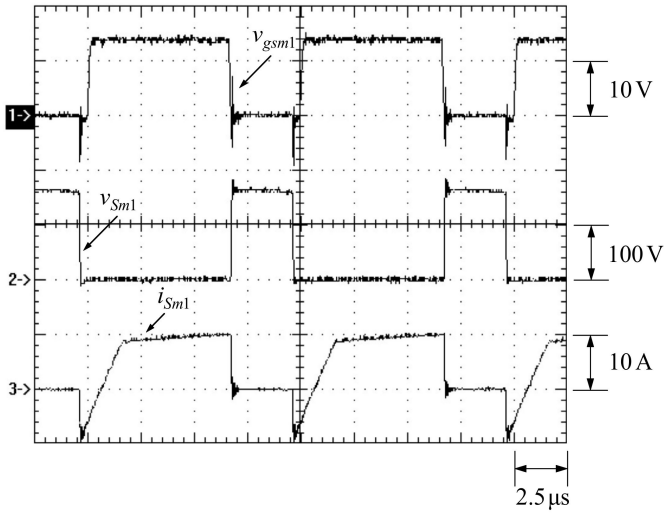

Figure 33. ZVS turn-on of S_{m1}.

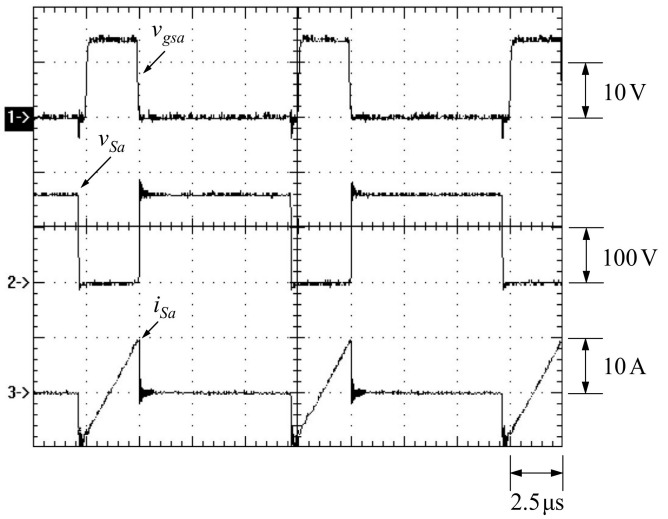

Figure 34. ZVS turn-on of S_a.

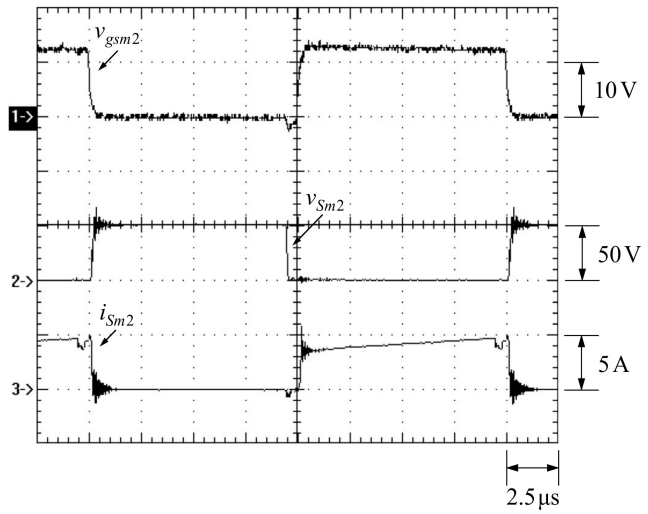

Figure 35. ZVS turn-on of S_{m2} of the first phase.

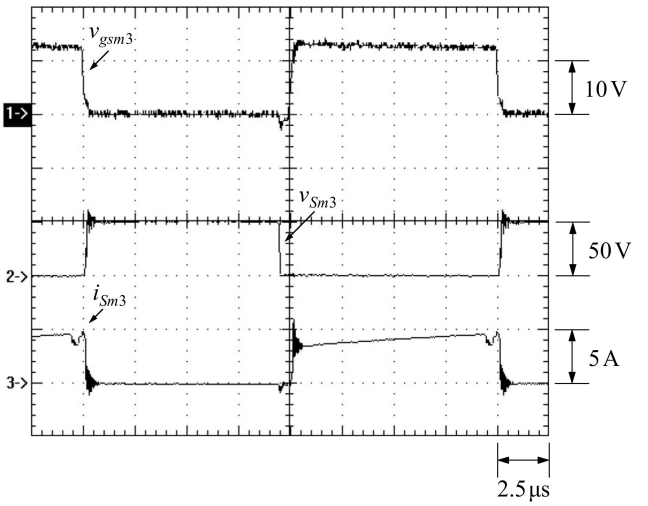

Figure 36. ZVS turn-on of S_{m3} of the first phase.

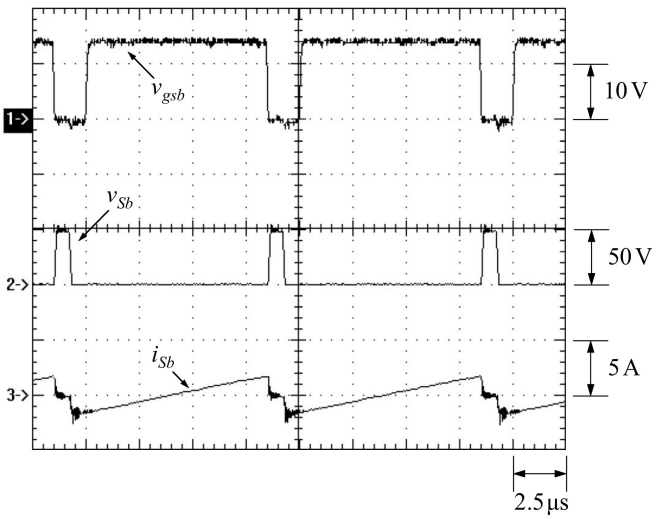

Figure 37. ZVS turn-on of S_b.

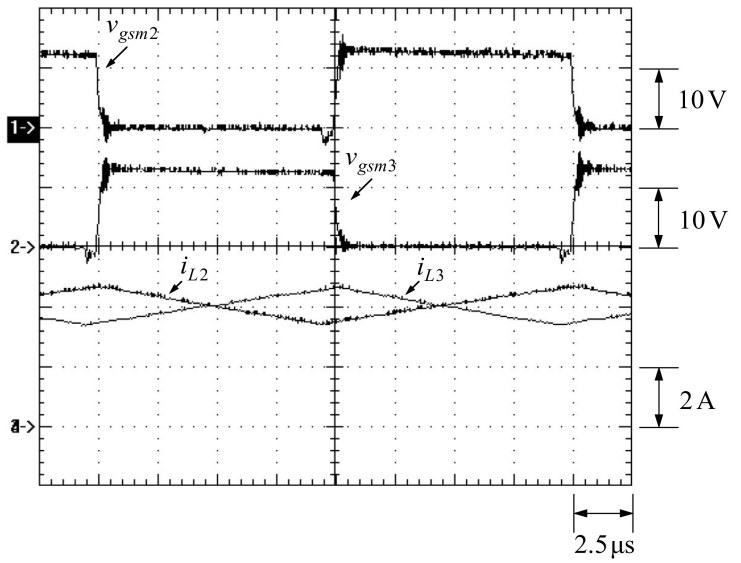

Figure 38. Gate driving signals v_{gsm2} and v_{gsm3} and inductor currents i_{L2} and i_{L3} of two phases.

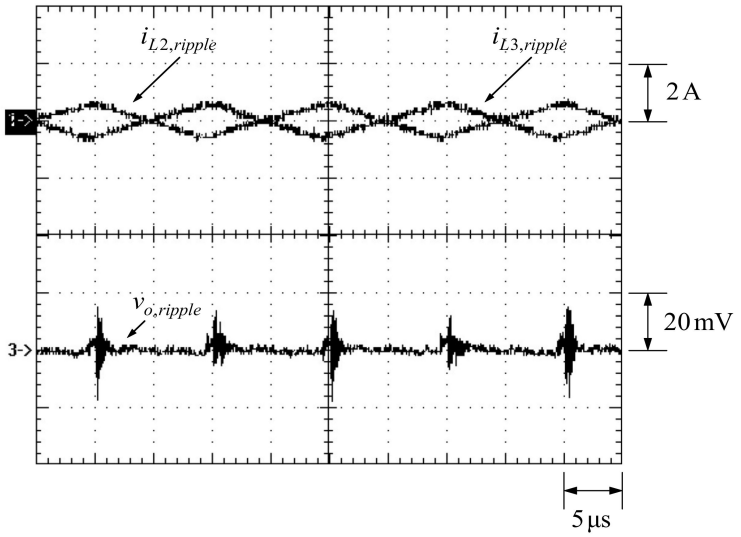

Figure 39. Current ripples of two phases, $i_{L2,ripple}$ and $i_{L3,ripple}$, and output voltage ripple $v_{o,ripple}$.

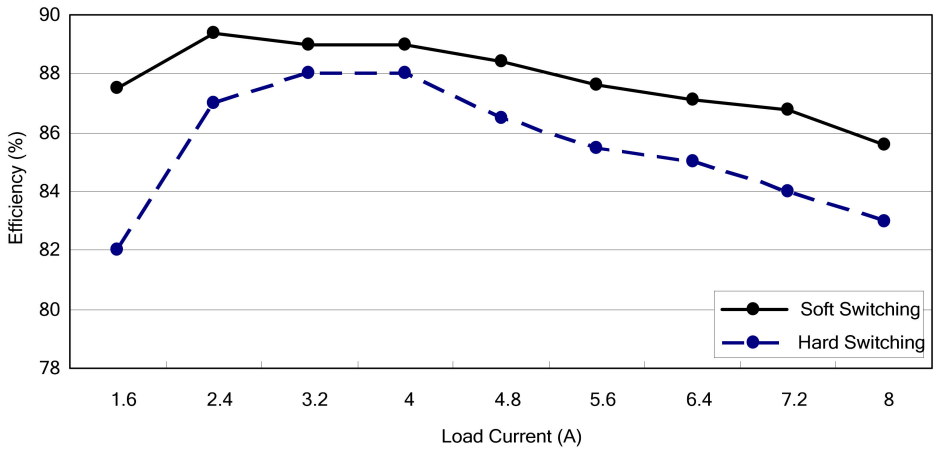

Figure 40. Curve of efficiency versus load current.

7. Output Voltage Ripple Comparison

Since this paper focuses on minimizing the output voltage ripple, the comparison of the output voltage ripple between the existing circuits and the proposed circuit is shown in Table 4, in terms of technical feature, power stage number, DC output voltage, output voltage ripple and ripple percentage. It is noted that the output voltage ripple is figured out without switching noise considered, and the ripple percentage is defined as output voltage ripple divided by DC output voltage multiplied by 100%. From Table 4, it can be seen that the proposed circuit has the smallest ripple percentage among them.

Table 4. Comparison of output voltage ripple.

Comparison Items	Compared Circuits					
	[2]	[4]	[5]	[7]	[8]	**Proposed**
Technical feature	Inductors coupled	Auto-transformer	Linear amplifier	Output series	Switched capacitors	PWM plus PFM control
Power stage number	1	1	1	2	1	2
DC output voltage	5 V	5 V	5 V	50 V	200 V	48 V
Output voltage ripple	90 mV	18 mV	82 mV	2.2 V	0.8 V	8 mV
Ripple percentage	1.8%	0.36%	1.64%	4.4%	0.4%	0.017%

8. Conclusions

The proposed circuit has several advantages described as follows:

(1) This two-stage converter has only a single feedback control loop under PWM control, which is applied to the first stage.
(2) The second stage is under PAM control with the fixed duty cycle of about 0.5.
(3) Due to PAM control with the fixed duty cycle of about 0.5 plus current-sharing control, the output voltage ripple of the second stage is quite small, about 8 mV, independent of the input voltage.
(4) Two phases of the second stage use only one resonant tank. Three phases or more with only one resonant tank will work also.
(5) Two stages have the proposed active clamp circuits to make the main and auxiliary switches all have ZVS turn-on, thus improving the overall conversion efficiency.

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