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Independent Upper- and Lower-Arm Switching Scheme Based on Reference Current Polarity for Three-Level NPC Inverters

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Abstract: This study presents a novel switching scheme for three-level neutral point clamped (NPC) inverters. The proposed switching method independently drives the upper- and lower-arm elements of the inverter based on the polarity information of the reference current. The proposed switching scheme does not require the inclusion of dead-time for each switching, except when the current polarity changes. Therefore, unlike the conventional inverter switching method, dead-time compensation is not needed, and the possibility of an arm-short accident is prevented. In this study, a switching procedure is detailed, and the operation mode analysis of the proposed switching scheme is presented. The effectiveness of the proposed switching method is verified experimentally by application to a grid-connected inverter that requires inverter current control.

Keywords: current control; inverters; pulse width modulation; photovoltaic system

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1. Introduction

Three-level inverters are widely used for medium- and large-capacity inverters. As three-level inverters have good performance and efficiency, they also have complex circuits and controls. In the case of a three-level inverter having a neutral point, the voltage applied to the switching element is halved compared to that of a two-level inverter. In addition, since the three-level inverter has a smaller current ripple than the two-level inverter, it is advantageous as a grid-connected inverter, where the problem of harmonics included in the output current is important. Therefore, studies on three-level inverters have been continuously investigated [1,2]. In the case of H-bridge-type power converters, which are driven by a conventional complementary switching method, when the switching elements of the upper- and lower-arm are turned on simultaneously, an arm-short of the DC link occurs. Therefore, in order to prevent an arm-short, dead-time must be inserted into all switching signals. For the perfect prevention of an arm-short, sufficient dead-time is required. However, when the dead-time is inserted, output waveform distortion is generated due to errors generated during the dead-time. Therefore, various studies have investigated dead-time compensation, such as extracting and compensating harmonics generated by dead-time or adjusting the effective application time according to the current direction [3,4]. The dead-time compensation in the three-level neutral point clamped (NPC) inverter is also compensated by analyzing the dead-time effect similar to the dead-time compensation used in the two-level inverter [5–10].

Furthermore, dead-time elimination methods have been proposed, which do not need to insert the dead-time according to the current polarity [11–13]. In these cases, there is a problem in accurately detecting the polarity of the actual current. An alternative switching method capable of operating without dead-time by driving a switching device according

to the polarity of the reference current in the two-level inverter has been proposed [14]. This method is useful for the current control system.

In the case of a three-level NPC inverter, a study that eliminates the dead-time by dividing the switching modes according to the polarity of the voltage reference and the polarity of the actual current has been proposed [15,16]. However, if the polarity of the actual current cannot be accurately detected, there is a possibility of an arm-short when the current polarity is switched.

A method using the voltage of the IGBTs has also been proposed to detect the actual current polarity accurately, but it has a disadvantage in that an additional circuit must be added in parallel to the IGBTs [17].

In the current study, a new switching method for a three-level NPC inverter is proposed. Since the proposed switching method independently switches the upper- and lower-arm elements based on information on the polarity of the reference current rather than the actual current, sensing of the actual current is not involved; therefore, the proposed method is easily applicable. Moreover, the possibility of an arm-short does not exist, and dead-time compensation is not required.

The detailed switching strategy and operation mode analysis of the proposed switching method are described, and the effectiveness of the proposed switching method is verified by applying it to a 1 MW grid-connected photovoltaic power generation system.

The authors state that this paper is based on a preliminary version [18] presented at the RTUCON conference in Riga, Latvia, in 2019.

2. 3 Phase Three-Level NPC Inverter

Figure 1 shows the circuit of a typical NPC three-level inverter; as shown in the figure, four switches and two clamping diodes constitute one arm. A clamping diode is connected to the neutral point *Z* between the DC link capacitors depending on the operating switching state and is used to clamp the output voltage to zero.

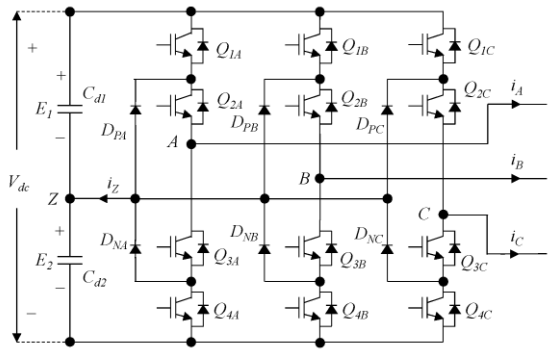

Figure 1. Circuit of a typical NPC three-level inverter.

Table 1 depicts the switching mode of the conventional switching method and the on/off state of the switch according to the inverter output voltage. In switching mode *P*, the two upper switches are turned on so that the voltage V_{AZ} between point *A* and neutral point *Z* becomes $+E_1$. In switching mode *N*, the two sub-switches are turned on so that V_{AZ} becomes E_2. In switching mode *O*, switches S_2 and S_3 are turned on, and the output voltage across the clamping diode is zero. Switch pairs S_1 and S_2 operate in a complementary manner with S_3 and S_4.

Table 1. Switching mode of the conventional switching method.

Switching Mode	Switching Signal				Expected Inverter Terminal Voltage V_{AZ}
	S_1	S_2	S_3	S_4	
P	On	On	Off	Off	E_1
O	Off	On	On	Off	0
N	Off	Off	On	On	$-E_2$

Figure 2 shows the waveform of the switching signal of the phase opposition disposition (POD) modulation scheme, which is a conventional carrier-based switching signal scheme. It can also be generated via other PWM methods, including space vector PWM. Whichever method is used, when S_1, S_2, and S_3 are operated simultaneously, an arm-short occurs as shown in Figure 3a. Alternatively, an arm-short occurs when S_2, S_3, and S_4 are turned on simultaneously (Figure 3b). In rare cases, an arm-short is possible when all the switching elements are turned on (Figure 3c).

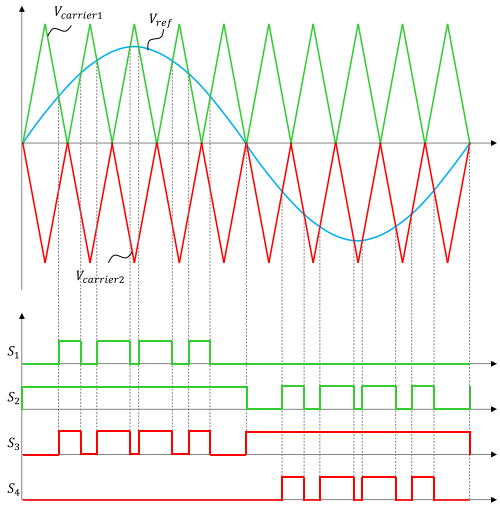

Figure 2. Switching signal waveforms of the conventional phase opposition disposition (POD) modulation scheme.

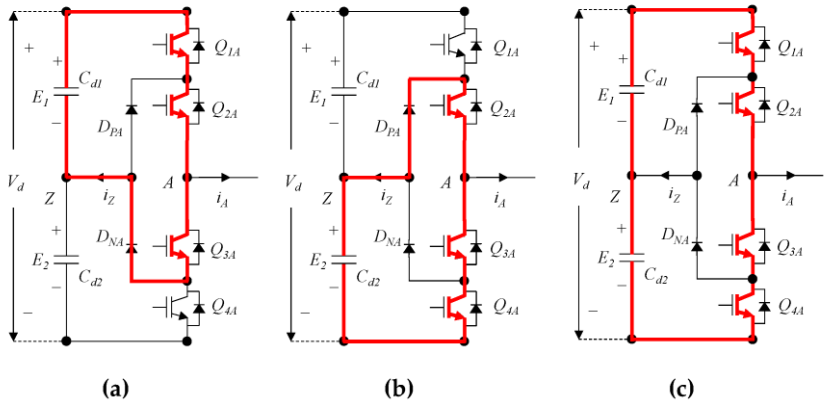

Figure 3. Current path of the short circuit for phase A: (**a**) transition of mode-P and mode-O; (**b**) transition of mode-N and mode-O; (**c**) transition of mode-P and mode-N.

As previously mentioned, when an H-bridge-type power converter is driven using the conventional PWM switching method in a complementary manner without dead-time, a short-circuit occurs in the DC link. Therefore, the dead-time needs to be included to prevent an arm-short, as depicted in Figure 4. In the figure, D_{ap} and D_{an} are reference

signals, t_p and t_n are the turn-on time of S_1 and S_4, respectively, and t_d is the dead-time. S_1~S_4 are switching signals, and G_1~G_4 are gate signals with the dead-time. As a result, it can be observed that the modulation error occurs in the output voltage during dead-time, compared to the ideal case, which necessitates compensation to reduce the voltage error and harmonics caused because of the dead-time.

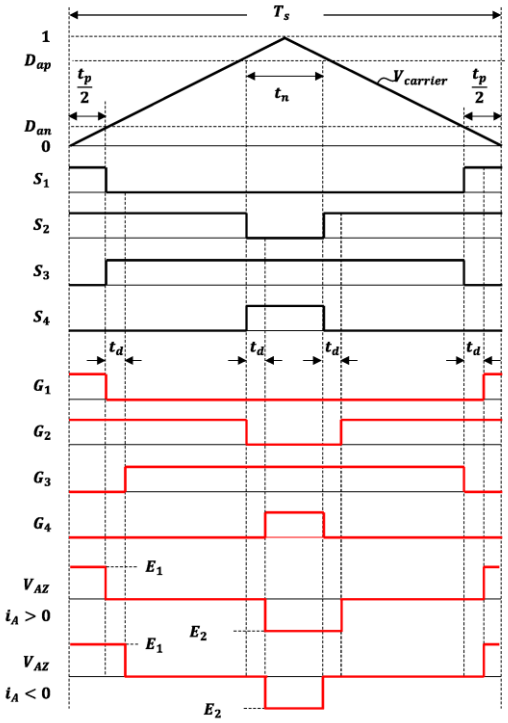

Figure 4. Waveforms of the conventional switching signal with dead-time and the output terminal voltage.

3. Proposed Switching Scheme

In this study, we present a novel switching method of three-phase NPC three-level inverters that selects a switching device using the polarity information of the reference current. The grid-connected PV system or motor driving system is controlled by the current control method.

Therefore, the selection of switching elements can be used for the information about the reference current polarity rather than the actual current.

Figure 5 shows the proposed switching signal generation scheme. The method of generating the primary switching signals S_1, S_2, S_3, and S_4 is the same as the conventional POD modulation method:

$$S_1 = \begin{cases} 1 & when\ V_{cmd} \geq V_{cp} \\ 0 & when\ V_{cmd} < V_{cp}, \end{cases} \quad (1)$$

$$S_4 = \begin{cases} 1 & when\ V_{cmd} \leq V_{cn} \\ 0 & when\ V_{cmd} > V_{cn}, \end{cases} \quad (2)$$

$$S_2 = \begin{cases} 1 & when\ V_{cmd} > V_{cn} \\ 0 & when\ V_{cmd} \leq V_{cn} \end{cases} = \overline{S_4}\ , \quad (3)$$

$$S_3 = \begin{cases} 1 & when\ V_{cmd} < V_{cp} \\ 0 & when\ V_{cmd} \geq V_{cp} \end{cases} = \overline{S_1}\ , \quad (4)$$

where V_{cmd} is the output voltage command, and V_{cp} and V_{cn} are carrier signals.

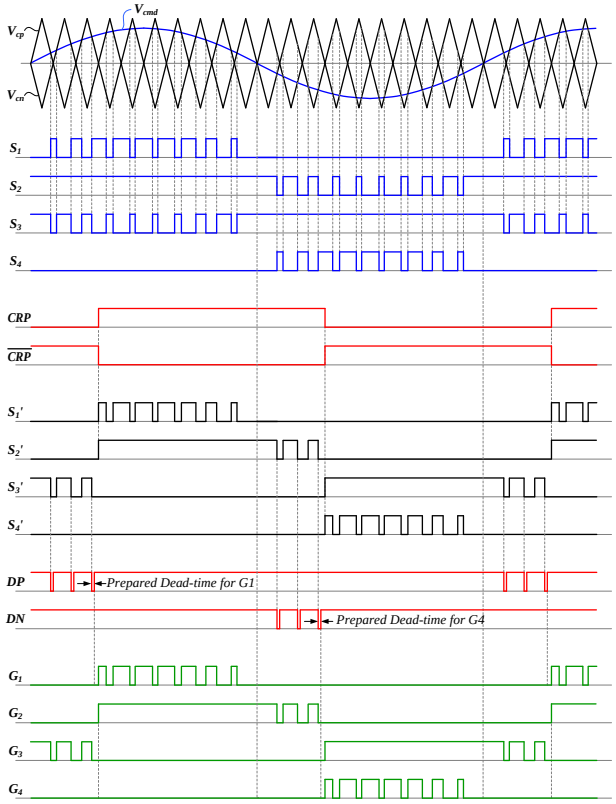

Figure 5. Proposed switching signal generation scheme.

The switching devices are determined for each operation mode according to the reference current polarity, as follows:

$$S_1{}' = CRP \,\&\, S_1, \tag{5}$$

$$S_2{}' = CRP \,\&\, S_2 = CRP \,\&\, \overline{S_4}, \tag{6}$$

$$S_3{}' = \overline{CRP} \,\&\, \overline{S_1}, \tag{7}$$

$$S_4{}' = \overline{CRP} \,\&\, S_4, \tag{8}$$

where

$$CRP = \begin{cases} 1 & when\ Current\ Reference \geq 0 \\ 0 & when\ Current\ Reference < 0. \end{cases} \tag{9}$$

Dead-time DP and DN are determined for gate signals G_1 and G_4, respectively. DP is the dead-time from the negative-going transition (NGT) of S_3, whereas DN is the dead-time from the NGT of $S_2{}'$. Although DP and DN are determined, they are not always adopted.

Therefore, the final gate signal can be obtained as follows:

$$G_1 = DP \,\&\, S_1{}' = DP\&CRP \,\&\, S_1, \tag{10}$$

$$G_2 = S_2{}' = CRP \,\&\, \overline{S_4}, \tag{11}$$

$$G_3 = S_3{}' = \overline{CRP} \,\&\, S_1, \tag{12}$$

$$G_4 = DN \,\&\, S_4{}' = DN \,\&\, \overline{CRP}\&S_4. \tag{13}$$

Figure 6 depicts the hardware implementation of the proposed switching scheme. In the conventional switching method, the hardware for inserting the dead-time includes four

one-shot and four AND-gates. In the hardware implementation of the proposed method, two one-shots are reduced, and two AND-gates and one NOT-gate are added, simplifying the circuit.

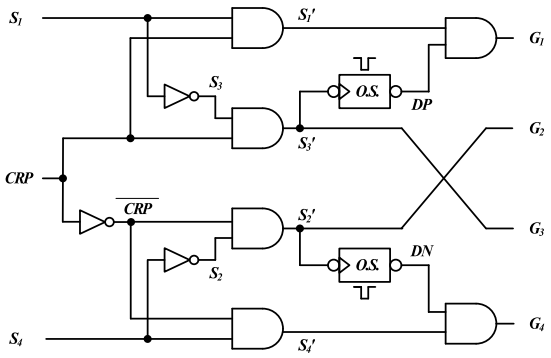

Figure 6. Logical diagram of the proposed switching scheme.

Table 2 shows the status of the switching elements in the conduction mode for the proposed switching method. Mode *O* in the conventional switching method (Table 1) is divided into modes *PO* and *NO* according to the polarity of the voltage and current. In addition, a new mode *OO* is presented in which all the switches are turned off.

Table 2. Conduction mode.

Conduction Mode	Switch Status				Terminal Voltage $V_{AZ}/V_{BZ}/V_{CZ}$
	Q_2	Q_2	Q_3	Q_4	
PP	On	On	Off	Off	E_1
PO	Off	On	Off	Off	0
OO	Off	Off	Off	Off	E_1 $(I < 0)/-E_2$ $(I > 0)$
NO	Off	Off	On	Off	0
NN	Off	Off	On	On	$-E_2$

The current path of each conduction mode for phase *A* is shown in Figure 7. From Figure 7, only Q_{1A} and Q_{2A} are turned on when the current is positive, and only Q_{3A} and Q_{4A} are turned on when the current is negative. Therefore, dead-time is no longer required, except when the polarity of the reference current is changed.

Table 3 depicts the operation mode according to the conduction mode, which is determined by the output voltage polarity and the reference current polarity. Table 4 shows the conduction mode from phase *X* to phase *Y*, i.e., when the *XY* line current is positive. Here, *X* and *Y* denote *A* and *C*, respectively. According to the conduction mode of each phase, a total of nine modes are possible.

Table 3. Operation mode.

Operation Mode	Current Reference Polarity	Voltage Polarity	Conduction Mode
Mode-I	Positive	Positive	*PP/PO*
Mode-II	Positive	Negative	*PO/OO*
Mode-III	Negative	Negative	*NN/NO*
Mode-IV	Negative	Positive	*NO/OO*

Table 4. Conduction mode from phase A to phase C.

A-C Conduction Mode	Conduction Mode of Phase *A*	Conduction Mode of Phase *C*	A-C Line to Line Voltage
Mode-1	*PP*	*NN*	$E_1 + E_2$
Mode-2	*PP*	*NO*	E_1
Mode-3	*PP*	*OO*	0
Mode-4	*PO*	*NN*	E_2
Mode-5	*PO*	*NO*	0
Mode-6	*PO*	*OO*	$-E_1$
Mode-7	*OO*	*NN*	0
Mode-8	*OO*	*NO*	$-E_2$
Mode-9	*OO*	*OO*	$-E_1 - E_2$

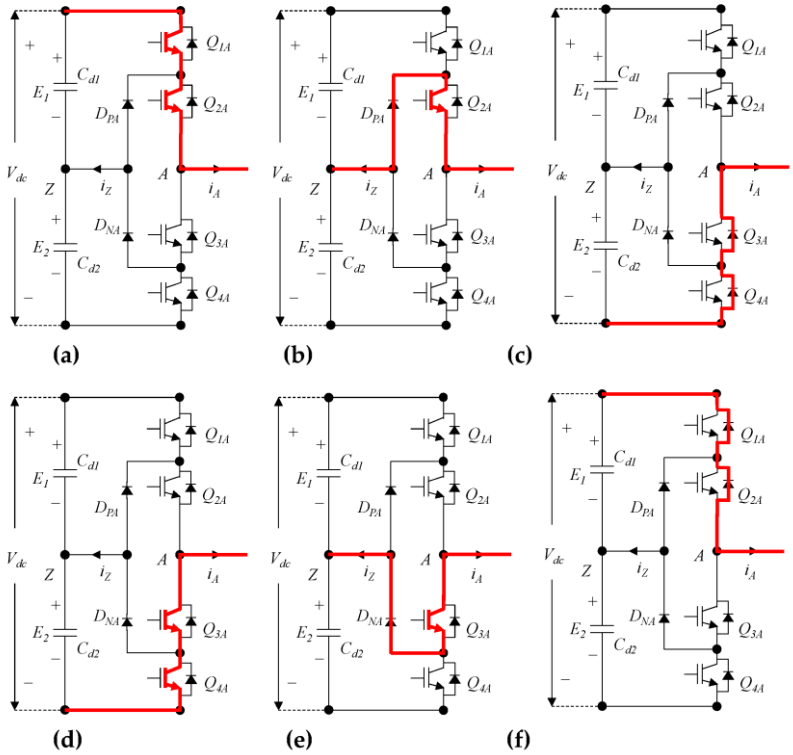

Figure 7. Current path of each conduction mode for phase *A*: (**a**) *PP* mode; (**b**) *PO* mode; (**c**) *OO* mode ($i_A > 0$); (**d**) *NN* mode; (**e**) *NO* mode; (**f**) *OO* mode ($i_A < 0$).

In Equations (10) and (13), the dead-time for switching Q_1 and Q_4 is determined when the polarity of the reference value is changed. The determined dead-time may or may not be applied depending on the switching conditions. Even if the dead-time is applied, it is shorter than the determined dead-time, and is applied just once when the polarity of the reference current is changed. Moreover, during this time, no dead-time compensation is required in the current control system as the actual current is near zero.

However, if the polarity of the reference current is changed before the polarity of the actual current, the current discontinuity may occur near-zero current in the proposed switching scheme, as depicted in Figure 8; hence, the proposed switching method is not recommended for systems where the output current is not significant compared to the ripple current caused by switching.

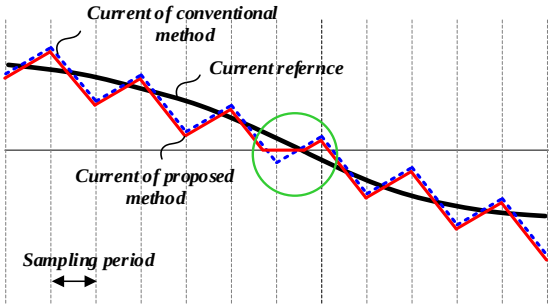

Figure 8. Occurrence of current discontinuity.

4. Experimental Results

An experiment was conducted to confirm the effectiveness of the proposed switching scheme by applying it to a 1 MW grid-connected photovoltaic (PV) system, as shown in Figure 9. The 1 MW PV inverter is a multi-central type, with two 500 kW inverter panels in parallel. Each inverter panel consists of four 125 kW power stacks connected in parallel, and the same switching signals drive each power stack. Figure 10 displays the image of the 1 MW PV inverter system used in the experiment. Table 5 shows the detailed specifications of the 1 MW grid-connected PV inverter proposed in this study.

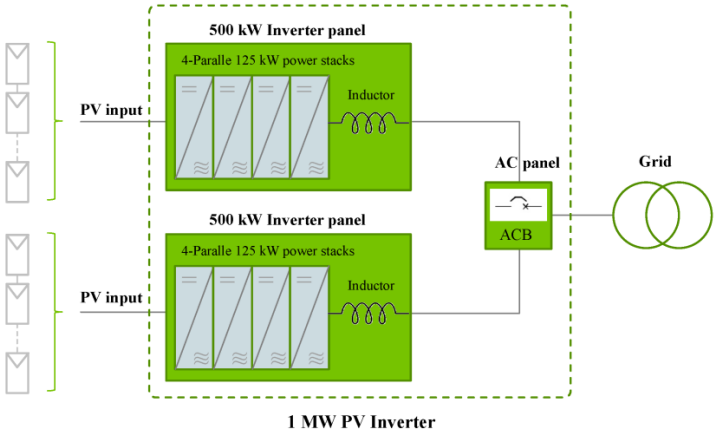

Figure 9. 1 MW PV system used in the experiment.

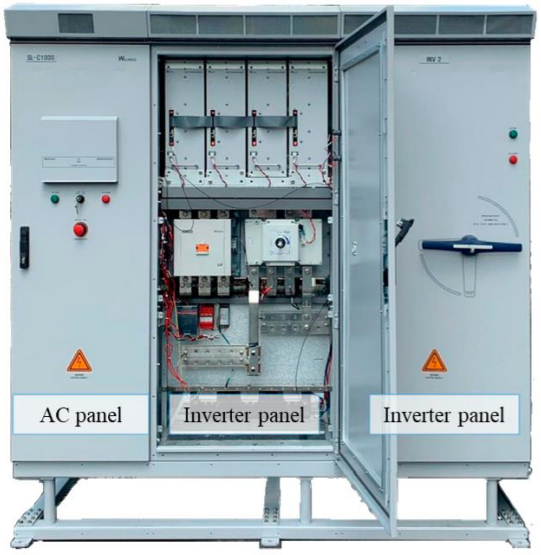

Figure 10. Image of the 1 MW PV inverter system.

Table 5. Specification of the 1 MW PV inverter system.

Item		Value
Input	PV voltage (max)	1000 V
	Operation voltage range	550–1000 V
	MPPT voltage range	550–1000 V
	PV current (max)	1652.8 A
Output	Power	1000 kW
	Frequency	60 Hz (59.3–60.5)
	Voltage	340 V (3Φ3W)
	Current (max)	1698 A
ETC	Operating temperature	−20–50 °C
	IP degree	IP44
	Cooling	Forced air

Figure 11 displays the image of the 125 kW power stack, and Figure 12 presents the circuit for one of the arms. The ratings of the main components of the 125 kW power stack and 500 kW inverter panel are shown in Tables 6 and 7, respectively.

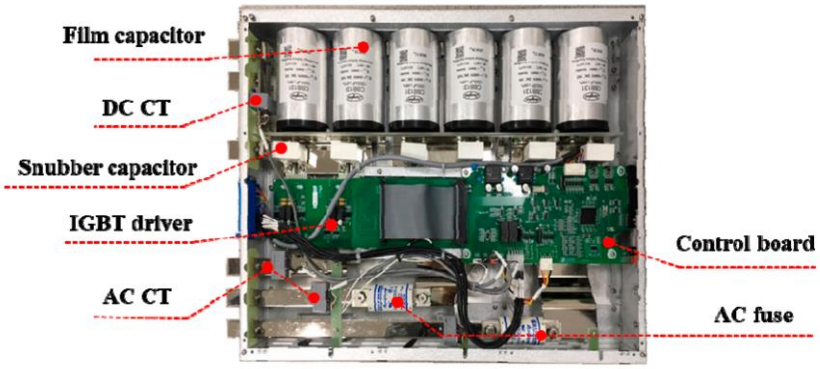

Figure 11. Image of the 125 kW power stack.

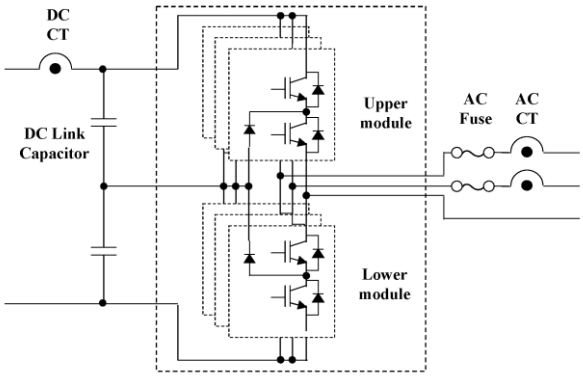

Figure 12. Schematic of one of the arms of the 125 kW power stack.

Table 6. Ratings of the major parts for the 125 kW Power stack.

Item	Value
DC CT	300 A
DC link capacitor	1000 μF/700 V ×3P2S
IGBT Module (upper)	650 V/400 A ×3 EA
IGBT Module (lower)	650 V/400 A ×3 EA
AC Fuse	700 V/300 A
AC CT	300 A

Table 7. Rating of the major parts for the 500 kW inverter panel.

Item	Value
Power stack	125 kW × 4P
DC Fuse	630 A, 1000 V × 2P
DC SPD	1000 V/40 kA
DC EMI Core	Nano crystal/200 mm
DC Switch	1000 A/1000 V
Filter inductor	0.1 mH/1000 A
Filter capacitor	40 μF/450 V × 4P
MC	1260 A/1000 V

The total harmonic distortion (THD) measurement results indicate that the proposed switching method has lesser THD than the conventional switching method with dead-time compensation. This may be because the adopted dead-time compensation method may be not perfect. If the dead-time compensation is perfect, there are no differences in the harmonic characteristics, but this is nearly impossible.

Figures 13 and 14 depict the experimental results obtained using the conventional switching method and the proposed switching scheme, respectively. Figures 13a and 14a show the waveforms of the grid voltage and the output current of the inverter system, whereas Figures 13b and 14b depict the gate signals. In this case, the grid voltage and inverter output current are in phase, so the power factor of the grid is in unity. However, the inverter output current is slightly lagged from the inverter output voltage due to the filter inductance between the inverter output stage and the grid; thus, mode of operation II (Table 3) exists in the vicinity of the change in polarity of the current from positive to negative. Comparison of the current waveforms shows that there is no difference between the proposed switching method and the conventional switching method with dead-time compensation.

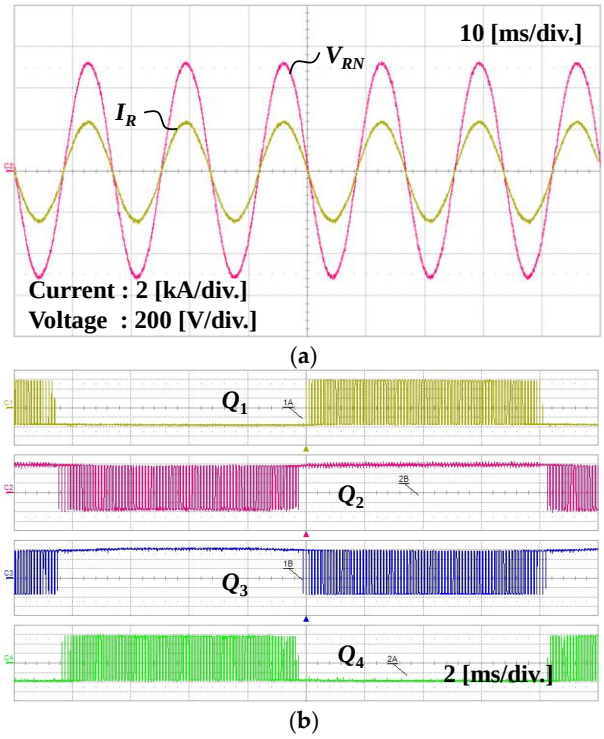

Figure 13. Experimental results in the case where the power factor is controlled at 1.0 using the conventional switching method: (**a**) waveforms of the output voltage and current; (**b**) waveforms of the gate signal.

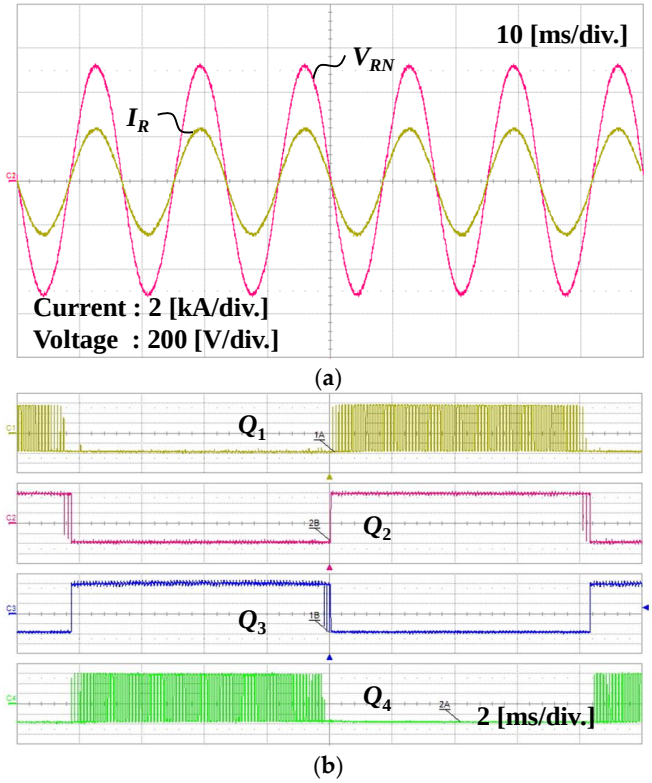

Figure 14. Experimental results in the case where the power factor is controlled at 1.0 using the proposed switching scheme: (**a**) waveforms of the output voltage and current; (**b**) waveforms of the gate signal.

Figures 15 and 16 show the experimental waveforms when the power factor of the system was controlled to 0.9, whereas Figures 17 and 18 show the experimental waveforms when the power factor was controlled to −0.9. The power factor was controlled through d-axis current control. This shows that the proposed switching method implements well, whether the current is lagging or leading. Therefore, when the proposed switching method is adopted, the possibility of an arm-short is eliminated, and dead-time compensation is not required.

Figure 19 is an enlarged waveform of the output current and gate signal when the power factor is 1.0. However, the inverter output current is slightly lagged from the output voltage due to the filter inductance between the grid and the inverter output stage. Therefore, it can be observed that operation mode II (Table 3) exists at the instant wherein the polarity of the current changes from positive to negative.

Figures 20 and 21 show the experimental results when the phase of the output current is controlled to be the same as the phase of the grid voltage when the PV output voltage is 750 V, the grid voltage is 340 V, and the inverter output power is 1 MW. In Figure 20, the conventional switching method with dead-time compensation is used, whereas in Figure 21, the proposed scheme is used. It can be observed that there are no differences in the experimental result of the conventional switching method that requires dead-time compensation and the proposed switching scheme. This proves that arm-short accidents can be prevented with the proposed switching scheme, and dead-time compensation is no longer required.

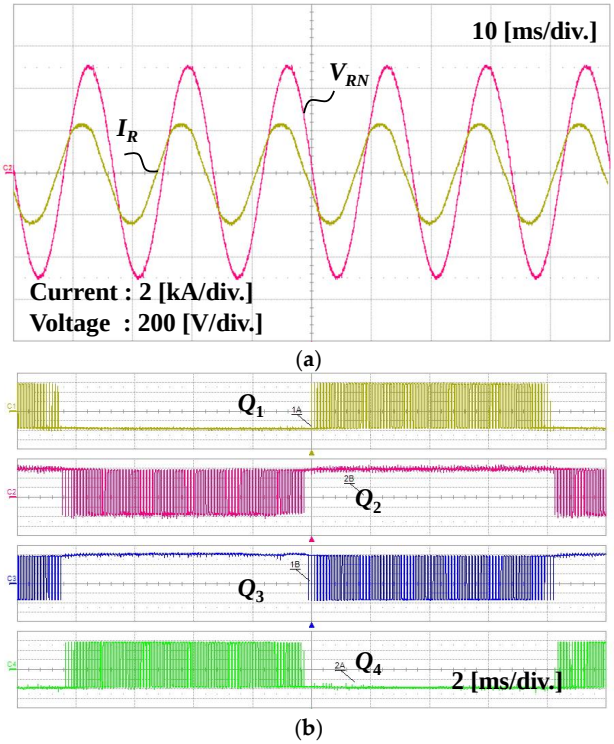

Figure 15. Experimental results in the case where the power factor is controlled at 0.9 (lag) using the conventional switching method: (**a**) waveforms of the output voltage and current; (**b**) waveforms of the gate signal.

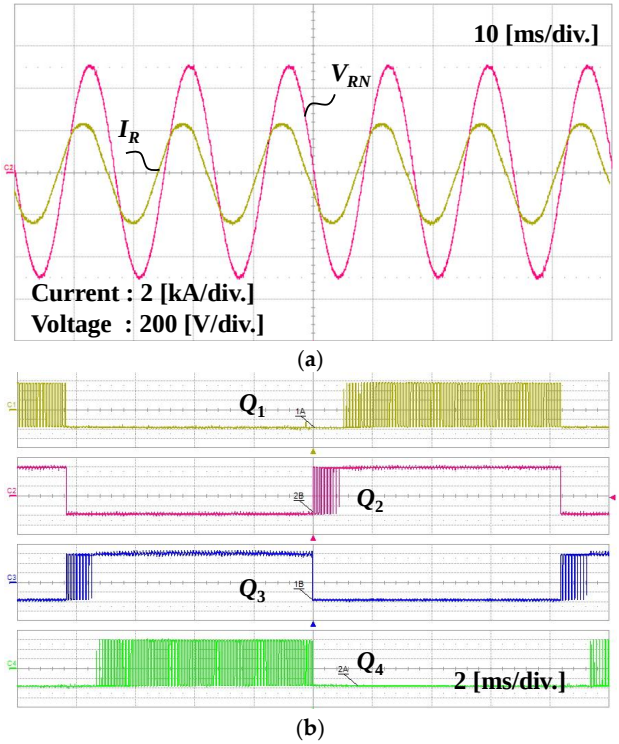

Figure 16. Experimental results in the case where the power factor is controlled at 0.9 (lag) using the proposed switching scheme: (**a**) waveforms of the output voltage and current; (**b**) waveforms of the gate signal.

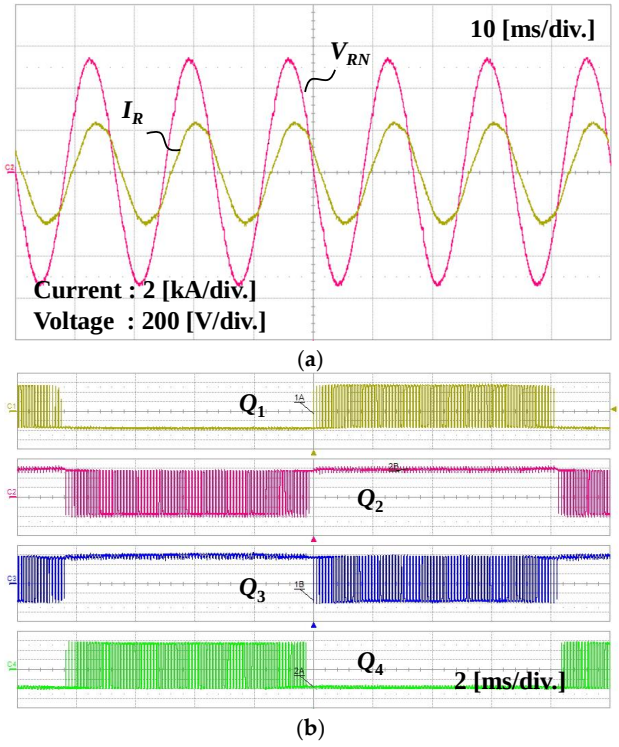

Figure 17. Experimental results in the case where the power factor is controlled at −0.9 (lead) using the conventional switching method: (**a**) waveforms of the output voltage and current; (**b**) waveforms of the gate signal.

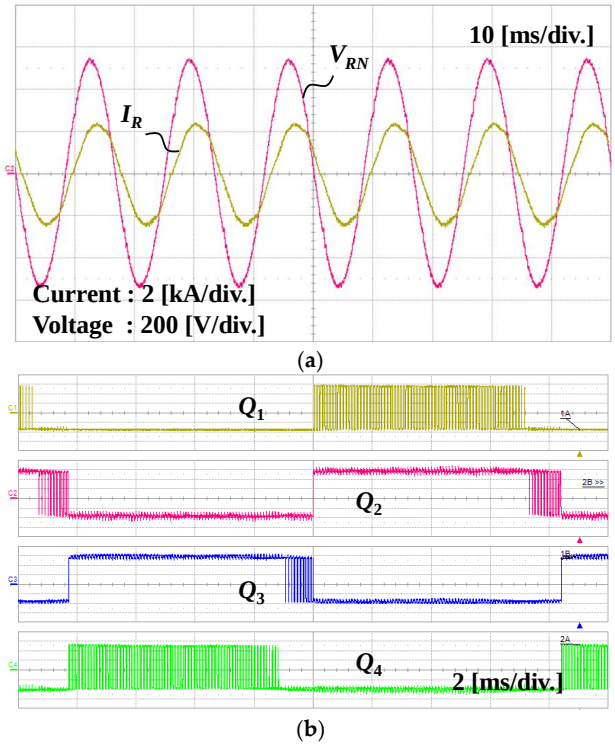

Figure 18. Experimental results in the case where the power factor is controlled at −0.9 (lead) using the proposed switching scheme: (**a**) waveforms of the output voltage and current; (**b**) waveforms of the gate signal.

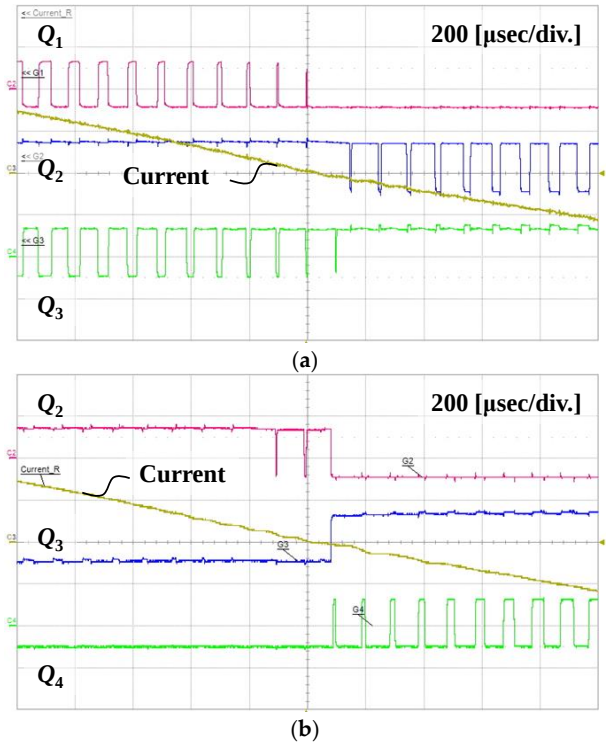

Figure 19. Magnified waveforms of the current and gate signals in the case of a unity power factor at the grid: (**a**) waveforms of the conventional switching method; (**b**) waveforms of the proposed switching scheme.

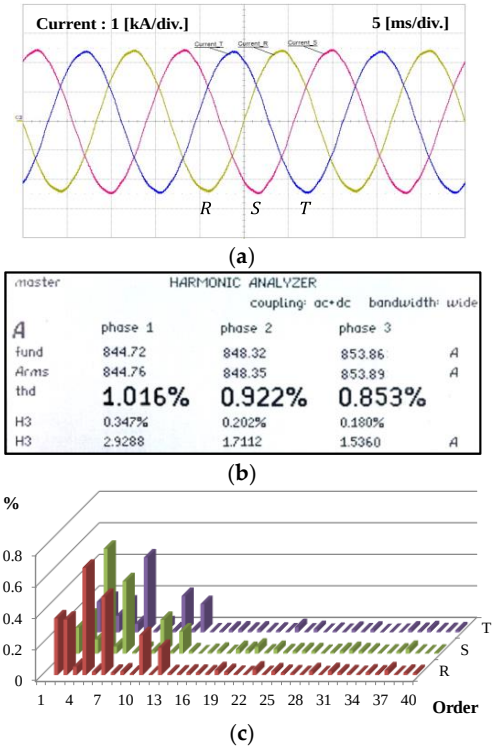

Figure 20. Experimental results of the conventional switching method: (**a**) current waveforms; (**b**) THD of the current; (**c**) harmonic analysis.

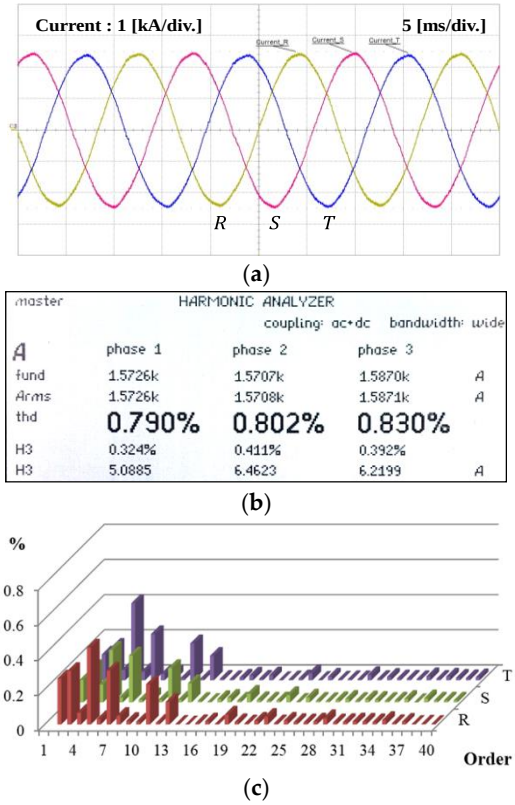

Figure 21. Experimental results of the proposed switching scheme: (**a**) current waveforms; (**b**) THD of the current; (**c**) harmonic analysis.

The THD measurement results indicate that the THD of the proposed switching method is lesser than that of the conventional switching method with dead-time compensation. This may be because the adopted dead-time compensation method is not perfect. If dead-time compensation is perfect, there are no differences in the harmonic characteristics, but this is nearly impossible.

Figure 22 shows the result of measuring the efficiency of the power, and it was measured to be 98% at the 1 MW rated output. Since the proposed method only reduces the gate drive power to half compared to the conventional method, the efficiency improvement is not significant.

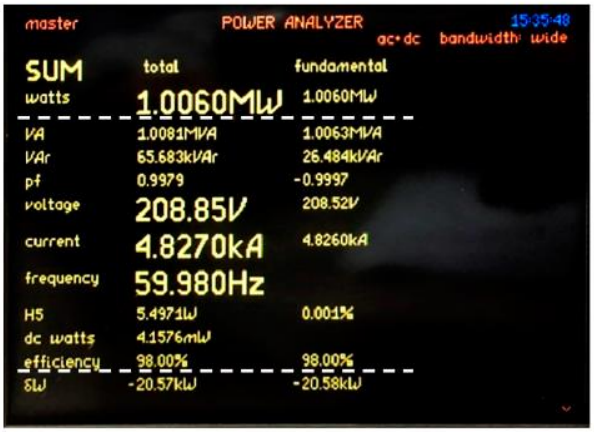

Figure 22. Efficiency measurement result at the 1 MW rated output.

5. Conclusions

A novel switching scheme that independently drives the upper- and lower-arm elements of an inverter using the polarity information of the reference current instead of the polarity information of the actual current was proposed in this study. The proposed switching scheme does not require the inclusion of dead-time for every switching signal, except at the instant at which the reference current polarity changes. Therefore, dead-time compensation is not required with the proposed switching scheme. In addition, it prevents arm-short circuit accidents and reduces the gate drive power to half. However, the proposed switching scheme can be applied only to a current control system because it requires the polarity information of the reference current. The switching procedure was detailed, and an operation mode analysis of the proposed switching scheme was presented. An experiment was performed to verify the effectiveness of the proposed switching scheme by applying it to a multi-central type 1 MW grid-connected inverter system. The obtained results established that with the proposed switching scheme, arm-short accidents can be prevented, and dead-time compensation is no longer required.

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