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All-SiC ANPC Submodule for an Advanced 1.5 kV EV Charging System under Various Modulation Methods

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Abstract: This work is focused on the design and experimental validation of the all-SiC active neutral-point clamped (ANPC) submodule for an advanced electric vehicle (EV) charging station. The topology of the station is based on a three-wire bipolar DC bus (±750 V) connecting an ac grid converter, isolated DC-DC converters, and a non-isolated DC-DC converter with a battery energy storage. Thus, in all types of power converters, the same three-level submodule may be applied. In this paper, a submodule rated at 1/3 of the nominal power of the grid converter (20 kVA) is discussed. In particular, four different modulation strategies for the 1.5 kV ANPC submodule, exclusively employing fast silicon carbide (SiC) MOSFETs, are considered, and their impact on the submodule performance is analyzed. Moreover, the simulation study is included. Finally, the laboratory prototype is described and experimentally verified at a switching frequency of 64 kHz. It is shown that the system can operate with all of the modulations, while techniques PWM2 and PWM3 emerge as the most efficient, and alternating between them, depending on the load, should be considered to maximize the efficiency. Furthermore, the results showcase that the impact of the different PWM techniques on switching oscillations, including overvoltages, can be nearly fully omitted for a parasitic inductance optimized circuit, and the choice of modulation should be based on power loss and/or other factors.

Keywords: ANPC converter; EV charging; multilevel converter; PWM methods; SiC MOSFETs

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1. Introduction

There is no doubt that easily available fast charging infrastructure is a necessary condition in the further expansion of electric vehicles (EVs) beyond current numbers, even in the most developed countries [1,2]. In comparison to traditional cars, the charging time of EVs is, and will be, longer than refueling a tank with gasoline. However, fast charging stations may offer a reduction in time from the range of hours to tens of minutes [3]. This is associated with an increase in charging power to hundreds of kWs, and, unfortunately, a rising number of such stations is challenging for the power system. Therefore, an answer to this problem may be a battery energy storage, reducing power peaks during fast charging periods [4,5]. Additionally, the storage may also act as local energy storage for a PV plant, and perform short-time grid support services. All in all, the EV charging station with energy storage becomes a high-power and complex power electronics system, as can be seen in Figure 1. Moreover, to decrease current levels and conduction losses in a common DC-link (750–800 V), a bipolar topology may also be taken into account [6]. All three types of power converters in such a system: grid-connected AC-DC, isolated DC-DC, and non-isolated DC-DC, should be based on one of the multilevel topologies. Furthermore, in the optimal scenario, all of them should be based on the same topology to reduce the complexity and cost of the whole system, and to introduce modularity into the system. While the isolation stage of the AC-side is omitted in this paper, as the focus is on the

presented ANPC submodule, it is worth noting that either conventional low-frequency transformers or solid-state transformers [7] are applicable in the EV charging system.

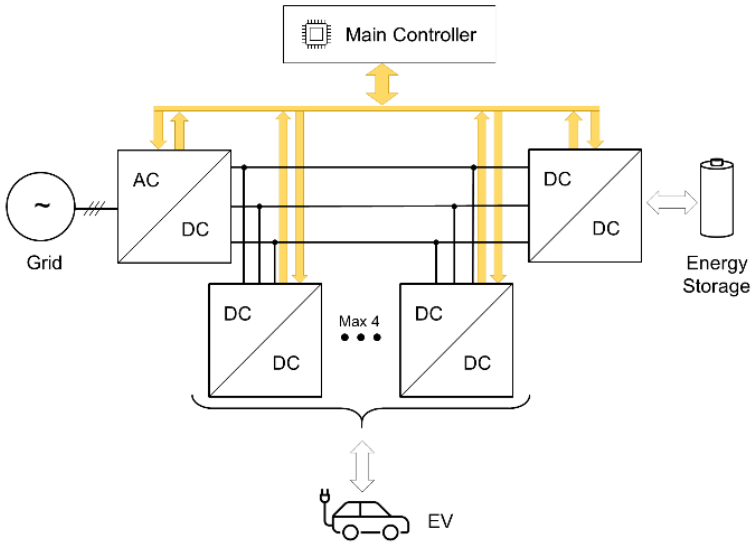


Figure 1. Bipolar DC grid-based EV charging station with energy storage.

Several multilevel converter topologies are applicable in EV charging systems [8]. Most notably, neutral point clamped (NPC), T-type, flying capacitor (FC), and modular multilevel converter (MMC) topologies can be named. In the discussed case, the active neutral point clamped (ANPC) topology of the submodule, introduced in [9], was selected as it is characterized by more flexible control and the possibility to reach a more balanced power loss distribution among the semiconductors compared to the conventional NPC topology, while keeping the power device stress on a similar level [10,11]. Moreover, when compared to other common multilevel structure, such as T-type and FC converter topologies, the former is less efficient for the systems in such voltage range (1500 V) than the NPC-derived topologies [12], whereas the latter cannot be employed in a system with a bipolar DC bus for obvious reasons. Finally, when a comparison with MMC-based systems [13] is considered, ANPC converters seem more appropriate, as MMC introduces a bulkier structure, and adds further complexity to the system [8]. Furthermore, ANPC systems were positively verified in terms of both three-wire [14] and EV charging systems [15].

Moreover, as the SiC technology is constantly developing and providing power semiconductor devices with superior performance compared to conventional Si counterparts [16–18], especially for this specific voltage range, applying SiC MOSFETs to the switches lead to, amongst many, increased efficiency and higher power density. However, briefly after the commercial introduction of SiC power devices, when the SiC technology was still relatively new, the cost of such power devices was significantly higher compared to conventional Si IGBTs. Thus, different hybrid Si/SiC ANPC topologies were introduced, in which SiC MOSFETs can be applied as the power devices for two or four out of six devices per leg depending on the preferred PWM technique, showcasing satisfactory results in terms of achieving a balance between cost and performance [18–22]. Nevertheless, even though the hybrid topologies should be considered when the cost is taken into account, the all-SiC system is still unmatched when strictly performance and maximization of efficiency are considered [19]. Moreover, such a converter structure is and will become even more compelling, as the wide-band-gap technology is currently becoming more and more advanced, and thus SiC power devices will develop to be affordable to a greater extent yearly.

Since the number of switches in the ANPC leg is high, so is the variety of PWM methods applicable in such a system. Moreover, depending on the focus of a specific appli-

cation, there are modulation techniques that can target various factors, such as efficiency or power density, ensuring equal loss distribution, or, finally lowering line filter requirements [10,23–25]. Furthermore, according to the literature, the impact of commutation path lengths is a crucial matter, determining the proper PWM method for a specific application as well. This is especially relevant when systems with SiC power devices are considered, as wide-band-gap semiconductors are capable of high-speed switching, and thus are more prone to ringing and overvoltages compared to its Si counterparts.

However, in this paper, except for validating the constructed low-volume prototype of the all-SiC ANPC single leg rated at 1500 V DC and 6.67 kVA power (1/3 of three-phase 20 kVA system), it is shown that when enough care and focus is put into the design process of the converter and thus the commutation path lengths are vastly minimized, the variances between different modulation techniques in this regard are not as apparent and the choice may be limited to other factors, namely in this case, efficiency. The conclusions are based on a parasitic inductance optimized ANPC leg that can be used as a submodule to construct full power electronic systems, e.g., three-phase bidirectional AC/DC converters as shown in Figure 1.

Furthermore, in this paper, the PWM techniques are compared based on efficiency and switching performance, strictly for an all-SiC system. In contrast, other researchers have focused on a comparison between different Si/SiC configurations with strictly bound modulation techniques, where each configuration was tested with its specific PWM method. Finally, the conclusion is drawn that while all modulation techniques are viable, two emerge as the most competent, one for lower power ratings and another for higher power ratings. Thus, the assumption is made that to operate optimally, the modulation technique should be changed according to the load. Moreover, while systems comprised of ANPC submodules have been shown in the past, they are connected with other power semiconductor device types, such as IGBTs [26,27] or IGCT [28]. There are no publications regarding SiC MOSFET-based systems rated at MV level, whereas for such an application, the impact of parasitic inductances due to high dv/dt rates and a high switching speed is much more severe, and thus also more critical during the design process [29].

The paper is organized as follows. After the introduction, in Section 2, the basic principles of the ANPC topology are explained together with the considered PWM methods and their operation principles. Then, the simulation study is shown in Section 3, and, in Section 4, the experimental model of the SiC-based submodule is presented along with the results showcasing the experimental validation and further the discussion. Finally, the paper is concluded with a summary in Section 5.

2. Modulation Strategies in Active Neutral Point Clamped (Anpc) Converter

The most popular inverter topology used in industrial power electronic is a basic three-phase two-level (2-L) inverter [30]. This is mainly due to its simple design and well-understood operation principles. However, the voltage stress of semiconductor power devices in such topology is greater than in the DC-link voltage bus. This prevents the use of 1.2 kV SiC power devices in 2-L inverters with greater DC voltage. A well-known alternative to 2-L inverters are three-level (3-L) inverters [31]. The use of such a topology provides a halved maximum voltage stress in semiconductor power devices. Furthermore, due to the three-level nature of the output filter inductor voltage in 3-L inverters, it is possible to reduce the harmonic distortion and output filter volume [32,33]. The low switching time of SiC power MOSFETs also allows a reduction in switching losses. On the other hand, the high value of stray inductance and di/dt of transistors during commutation lead to voltage overshoots, which have a negative impact on MOSFETs' lifetime, energy conversion efficiency, and EMI. In 3-L inverters' three different operation states (positive state P, zero state 0, and negative state N) can be recognized, differing in voltage applied to the inductor. A highly regarded 3-L inverter topology is the ANPC, used in the discussed submodule. The ANPC converter consists of six active switches, S_1–S_6, connected according to Figure 2.

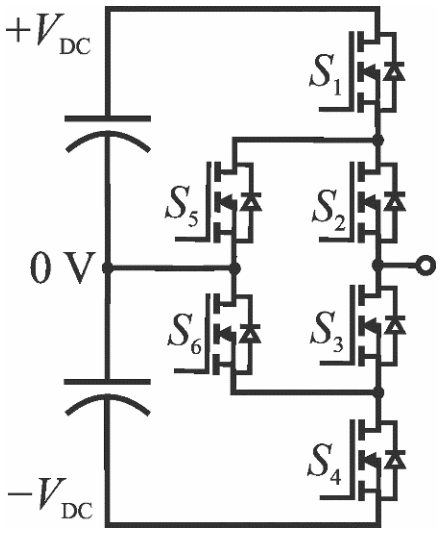


Figure 2. A single-phase leg of the ANPC converter with SiC MOSFETs.

In the ANPC converter, when the output voltage is positive, the inverter is switching between positive $+V_{DC}$ voltage and zero voltage; and when the output voltage is negative, the inverter is switching between negative $-V_{DC}$ and zero voltage. Control of the converter when the voltage is positive and negative is analogous. Therefore, in this article, the different control methods are only described when the voltage is positive. P and N states can be obtained only by turning on transistors S_1 and S_2 in P state, and S_3 and S_4 in N state. During P state, transistor S_6 can be turned on. Similarly, during N state, transistor S_5 can be on as well. This ensures constant v_{DS} voltages equal to V_{DC} on transistors S_3 and S_4 during P state, and on S_1 and S_2 during N state. Simultaneously, in the ANPC topology, there are different approaches to obtain zero state. Four modulation strategies of the ANPC and one of the NPC converters are depicted in Table 1 and Figure 3. In this paper, there are four different modulations described (PWM1–PWM4). These PWM techniques differ from each other in regard to the zero state, in which the current flows through different conduction paths marked in Figure 4 by 2 and 3.

Table 1. Switching states of the ANPC inverter.

State	S_1	S_2	S_3	S_4	S_5	S_6	Conduction Path(s)	PWM Method
P	1	1	0	0	0	1/0	1	1, 2, 3, 4
0U3	1	0	1	0	0	1	3	2
0U2	0	1	0	0	1	0	2	1
0U1	0	1	0	1	1	0	2	4
0F	0	1	1	0	1	1	2 and 3	3
0L1	1	0	1	0	0	1	3	4
0L2	0	0	1	0	0	1	3	1
0L3	0	1	0	1	1	0	2	2
N	0	0	1	1	1/0	0	4	1, 2, 3, 4

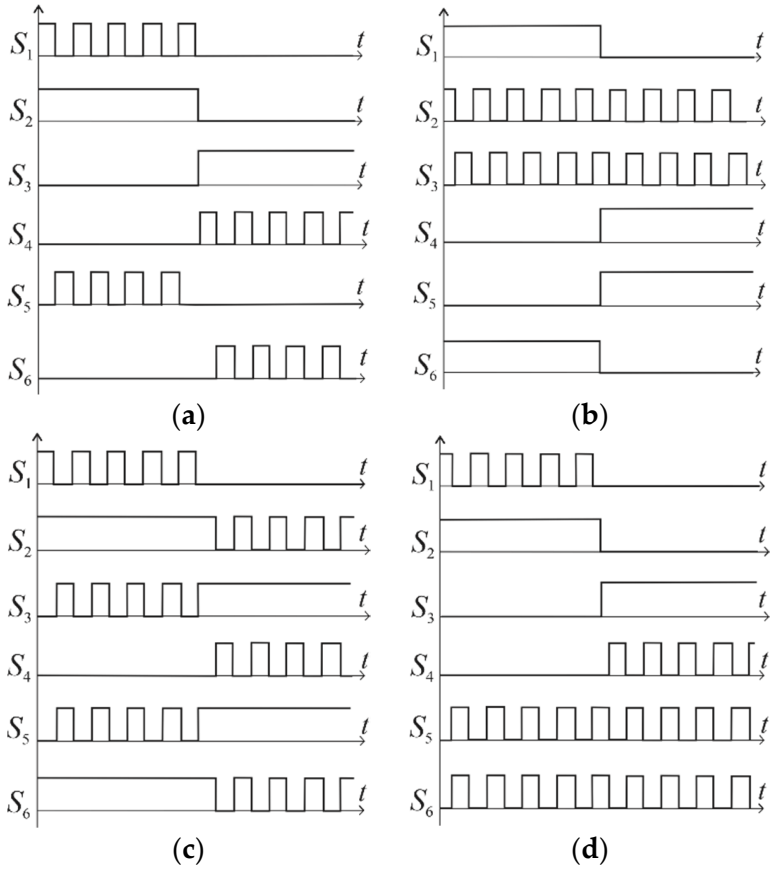


Figure 3. Different modulation strategies for the ANPC converters (**a**) PWM 1, (**b**) PWM 2, (**c**) PWM 3, (**d**) PWM 4.

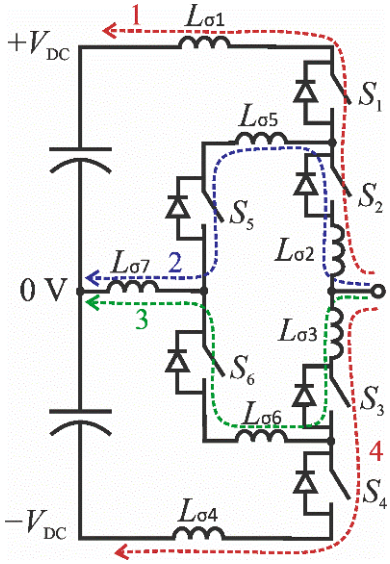


Figure 4. ANPC converter with depicted stray inductances and highlighted conduction paths.

In method PWM1 [34], during zero state transistors, S_2 and S_5 are on, and the current flows through conduction path two (marked in blue in Figure 4). In this control method, during transition P–0 a high value of di/dt in $L_{\sigma 1}$, $L_{\sigma 5}$, $L_{\sigma 7}$ causes voltage spikes on the switching transistors. In technique PWM2 [35], during zero state, the current flows via transistors S_3 and S_6, and in this case during the transition there is a high value of di/dt in stray inductances $L_{\sigma 1}$–$L_{\sigma 3}$, and $L_{\sigma 5}$–$L_{\sigma 7}$. When we compare the transition in PWM2 to

the one in PWM1, the equivalent stray inductance is higher, and thus, di/dt is higher as well, which leads to a higher value of voltage spikes. In method PWM3 [23,36], during zero state, transistors S_2, S_3, S_5, and S_6 are on, and current flows through conduction paths two and three; equivalent resistances of both conduction paths are lower, which leads to immensely lower conduction losses. PWM4 [22] is similar to PWM1. In both cases, after the transition from P to 0, the current flows through conduction path two. However, in PWM4 instead of transistor $S_{6,}$ transistor S_4 is turned on, and thus, even if the modulation pattern differs, the outcome is highly similar.

Generally, the described modulation strategies can be applied using SiC MOSFETs and/or IGBTs in one inverter leg. For hybrid topologies mentioned in Section 1, MOSFETs should be controlled with high frequency, while IGBTs should be switched with fundamental frequency to maximize the system performance. As mentioned before, SiC MOSFETs are more expensive than IGBTs, and thus using different transistors in one module leads to a reduced cost of the converter. However, as SiC MOSFETs become less and less expensive, and the system exhibits better performance with all-SiC configuration. A system with six SiC MOSFETs per leg is thus justified and interesting for further studies, especially including the impact of various modulation techniques.

3. Simulation Study

The system in which the ANPC leg submodule was tested with the different PWM techniques in this paper has been chosen as an open-loop single-phase inverter with a resistive load, as it can mimic the converter's behavior for a power factor near one quite satisfactorily while keeping the circuitry simple. Thus, both simulation and experimental tests were conducted in such a setup, according to system parameters shown in Table 2.

Table 2. System parameters.

Parameter	Description
DC voltage	1500 V
AC voltage	230 V RMS/50 Hz
Rated power	6.67 kVA (1/3 of 20 kVA)
Operating frequency	64 kHz
SiC MOSFETs	NTH4L040N120SC1
Filter inductor	220 µH
Filter capacitor	4.7 µF
DC capacitors	2 × 610 µF

At first, a simulation study in Plecs simulation software was performed to preliminarily showcase the differences in the modulation methods, and establish the power loss split between the converter components. The MOSFETs were modeled based on datasheet values, including the impact of increased junction temperature and different gate resistances. The other crucial source, namely the inductor, has also been included in the power loss analysis, estimating the power loss as a sum of conduction power loss, based on inductor resistance applied in the system based on a real model measurement. Furthermore, component resistances, such as ESR, were added to ensure the converter's loss model is as accurate as possible. However, as Plecs does not simulate the transistor switching processes fully, but rather operates on the basis of a lookup table with power switching loss, the impact of parasitic inductances and ringing could not be observed in the simulation study. Thus, the data from the simulation study were limited to power loss determination and its split between the converter components.

The simulation tests were performed at near-nominal parameters (see Table 2) for all five PWM methods described in Section 2. The impact of the different modulation techniques on the total power loss and its distribution among the converter components based on the simulation study can be observed in Figure 5. In general, for the system parameters, PWM4 is the optimal technique for maximizing efficiency, as the total power

loss reached just 114 W, while other PWM methods (PWM1, PWM2, and PWM4) settled close to each other at roughly 137 W.

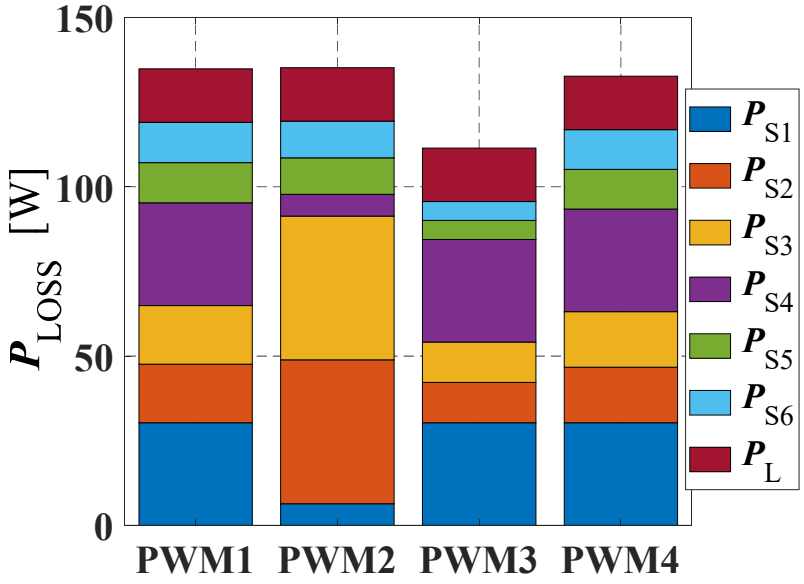


Figure 5. Power loss distribution among the converter components.

When we consider the power loss distribution among the converter components, the situation differs quite notably for the semiconductor power devices, as shown in Table 3, whereas the inductor exhibits nearly identical power loss for all the modulation techniques. At first, PWM1 shows medium total power losses, in which MOSFETs S_1 and S_4 are characterized by the highest value of roughly 30 W each, while pair S_2 and S_3 show 17.3 W, and the last pair S_5 and S_6 just 11.9 W per device. The second modulation method, PWM2, is similar in terms of total power loss. However, it is also characterized by a highly imbalanced distribution—transistors S_2 and S_3 are the sources of over a 70% semiconductor power loss with 42.5 W, while pairs S_1, S_4, and S_5, S_6 emit 6.4 and 10.8 W, respectively. PWM3 exhibits top performance in terms of power loss, with nearly the most imbalanced distribution, as over 60% of the power loss with 30.3 W is dissipated on pair S_1, S_4, while pairs S_2, S_3, and S_5, S_6 are the source of 11.8 and 5.6 W, respectively. However, it is worth noting that the source of this higher imbalance compared with PWM1 and PWM4 is lower power loss for the other MOSFET pairs, and not the increase in the S_1, S_4 pair. Finally, results for method PWM4 are very similar to PWM1 in terms of the loss distribution at 30.3, 16.4, and 11.7 W for transistor pairs S_1, S_4; S_2, S_3; and S_5, S_6, respectively. In terms of the conducting paths and thus power losses, these methods are akin to each other.

Table 3. Power loss distribution among the ANPC submodule transistors.

V_{DC} = 1500 V; P = 6.5 kW; v_{AC} = 230 V rms				
Parameter	**PWM1**	**PWM2**	**PWM3**	**PWM4**
$P_{(S1,S4)}$ [W]	30.3	6.4	30.3	30.3
$P_{(S2,S3)}$ [W]	17.3	42.5	11.8	16.4
$P_{(S5,S6)}$ [W]	11.9	10.8	5.6	11.7

4. Experimental Study

4.1. The ANPC Submodule Prototype

In order to validate the system experimentally, the next step was to design and construct the ANPC leg prototype. Since the system was to operate with a ±750 V DC bus, at least 1200 V rated transistors were needed in the multilevel structure. Based on preliminary calculations from the simulation study and analytical calculations, NTH4L040N120SC1 SiC

MOSFETs were chosen from a group of on the shelf, state-of-the-art power devices as all of the switches, since these are characterized by satisfactory on-state resistance of 40 mΩ and external Kelvin source connection. Therefore, they lead to minimized conduction and switching losses and provide the possibility to switch the transistor in a fast and a robust manner. Furthermore, as mentioned before, it was crucial to minimize the conduction loop lengths in order to lower the effect of parasitic inductances that could lead to excessive ringing, and cause overvoltages and increased power loss, which could result in working outside the safe operating area of the power device and potentially even breakage. This was achieved through the employment of a 4-layer power board structure along with a highly compacted layout of the SiC MOSFETs, as well as additional 82 nF fast bypass capacitors, put between $+/0$ and $0/-$ potentials as close to the power devices as possible. Since the plan was to test several PWM methods, none of the conduction paths were favored, and all were of similar length. However, such placement of the transistors leads to a situation where the whole semiconductor power loss has to be dissipated in the near vicinity of the center of the heatsink, thus leading to a less balanced heat distribution; in summary, more capable power loss dissipation measures had to be used. Therefore, as the submodule was to operate with a power of near 6.7 kW in a low-volume system, heatsink Fischer LAM 6 with a highly efficient 48 V fan was employed in the prototype shown in Figure 6.

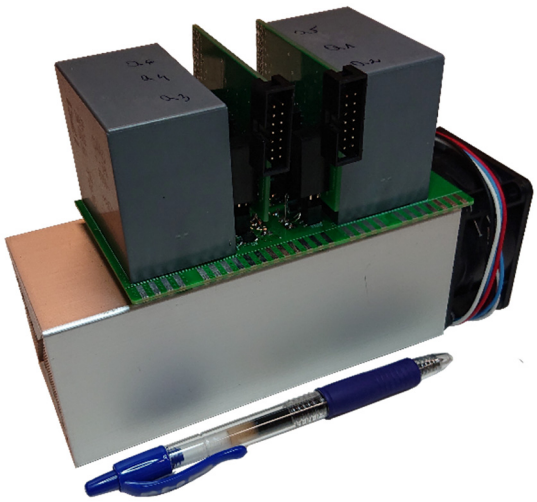
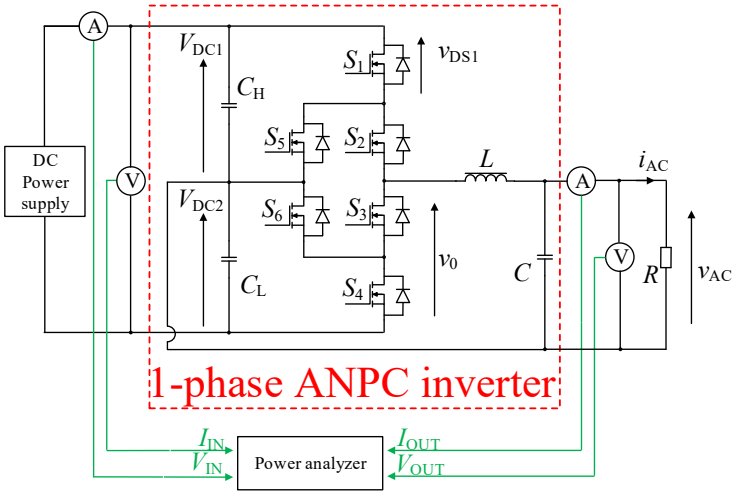


Figure 6. ANPC submodule—photo of the prototype.

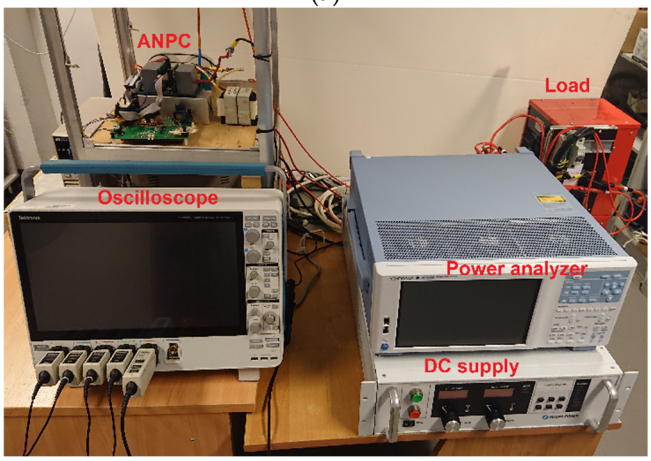
Moreover, the prototype consists of self-made gate drivers based on the UCC21750 chip from Texas Instruments, providing satisfactory switching performance as well as fault protection measures. Finally, the component count of the experimental model of the submodule concludes with two main DC capacitors rated at 800 V and 60 µF. The constructed ANPC leg prototype is shown in Figure 6.

4.2. Experimental Setup

Alongside the ANPC submodule prototype, the experimental setup consisted of an LC line filter, constructed from a 220 µH inductor and a 4.7 µF capacitor, as well as a reconfigurable resistive load. Furthermore, since single-phase systems require high DC capacitance, two additional 550 µF/900 V capacitors were added to support the built-in submodule capacitances. The converter was controlled at 64 kHz operating frequency via a DSP-based circuit, established on TMS320F28379D launchpad. The system was supplied through a 2 kV/5 A DC power supply from Magna Power, and a Yokogawa WT5000 power analyzer was used to measure the efficiency. Finally, the waveforms were obtained using Tektronix MSO56 oscilloscope with isolated voltage probes (Tektronix THDP0100 and P2505A) and a current probe (Tektronix TCP0030A). The scheme and the photo of the experimental setup are shown in Figure 7.



(**a**)



(**b**)

Figure 7. Experimental setup for the ANPC single-phase inverter system with a resistive load—(**a**) scheme, (**b**) photo.

4.3. Results from the Experimental Study

The core focus of the performed tests was to validate the constructed ANPC sub-module up to its nominal parameters, and establish the most proficient PWM technique. Since in the whole EV system and the 1500 V DC bipolar bus is required to be connected with the European grid (230 V RMS/50 Hz) at a rated power of 1/3 out of 20 kVA, the modulation index m applied was equal to 0.45, resulting in a voltage gain of roughly 0.153. Figure 8 presents an exemplary oscillogram with line frequency-focused view for PWM3 at 6.7 kW, showcasing ANPC leg output voltage v_0, DC-link voltages V_{DC1} and V_{DC2}, load AC voltage v_{AC}, and current i_{AC}. As the impact of the PWM method is minimal in a 50 Hz context, it is assumed that for other modulation techniques, the waveforms are identical and thus are not shown. As can be seen, there is still some imbalance between the $+/0$ and $0/-$ DC voltages, regardless of high 610 µF capacitance; however, its impact is limited regarding the load AC current and voltages as its THD settled below 5% for all the tests, and thus we can omit the mismatches throughout the further result analysis. For the nominal parameters, the AC load current settled at roughly 28 A, whereas the load voltage was established close to 230 V RMS resulting in a power of 6.5 kW. This operating point was further used as a nominal for further experimental comparison between the different PWM methods.

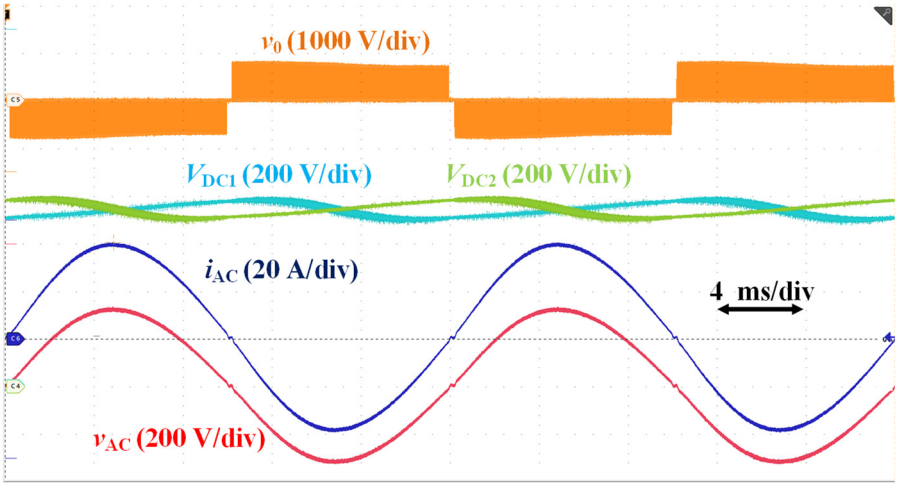
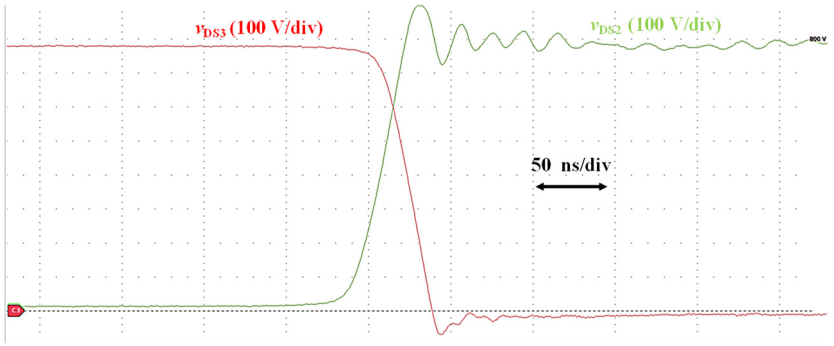


Figure 8. Experimental results from a test at 1500 V DC and 6.5 kW power (m = 0.45, v_{AC} = 230 V) with a line frequency-focused view. From the top: ANPC leg output voltage v_0, DC-link voltages V_{DC1} and V_{DC2}, load AC voltage v_{AC}, and current i_{AC}.

4.3.1. Transistor Overvoltage and Ringing

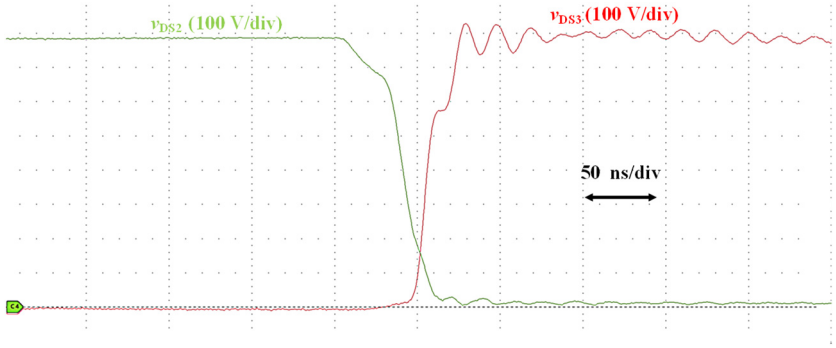
At first, a study on transistor overvoltage and ringing for different PWM methods was conducted. Since the switching behavior of MOSFETs within the transistor pairs S_1 and S_4, S_2 and S_3, as well as S_5 and S_6 were identical, only the switching voltages for the bottom switches (S_3, S_4, S_6) were measured. Unfortunately, due to the highly compacted design of the submodule, it was impossible to apply current probes and measure the transistor currents. Nevertheless, in terms of the safety of operation for the semiconductor power devices, the drain–source voltage is the crucial factor, while the impact of the current oscillations was indirectly included in the study through efficiency measurements. Furthermore, it is worth noting that transistor overvoltages were also affected by the DC-link voltage imbalances. Thus, peak overshoot voltages could have been even more limited with a higher capacitance, and would not occur if the submodule was used in a different system, e.g., three-phase inverter, where DC-link voltage balancing is assured.

Figures 9 and 10 depict the experimental switching waveforms near the peak line current for the system, operating at nominal values for the modulation technique with the highest voltage oscillations (PWM2). As shown, even though the oscillation is visible, it does not exceed 900 V, which is a safe value for the MOSFETs applied in the system. Furthermore, it is worth noting that due to DC-link voltage imbalance, the waveforms for the positive line current (Figure 9) are different from those obtained for the negative current (Figure 10). This variance between DC-link voltages V_{DC1} and V_{DC2} settled at roughly 60 V, corresponding to roughly 4% of nominal voltage.



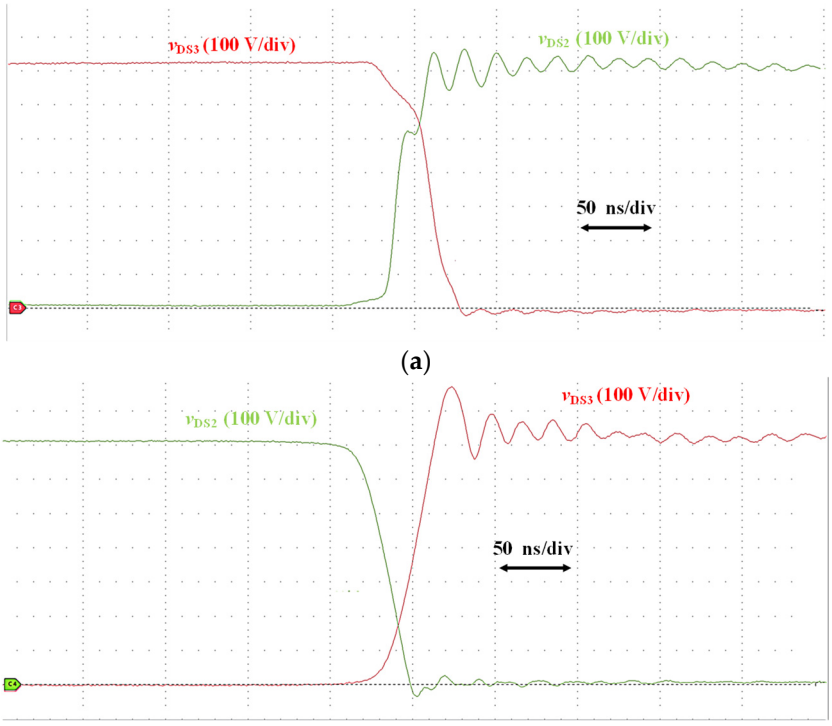
(**a**)

Figure 9. *Cont.*



(**b**)

Figure 9. Exemplary experimental waveforms showcasing drain–source transistors for positive load current ($i_{AC} > 0$) for the modulation technique with highest overvoltages (PWM2)—(**a**) turn-on, (**b**) turn-off.



(**a**)

(**b**)

Figure 10. Exemplary experimental waveforms showcasing drain–source transistors for negative load current ($i_{AC} < 0$) for the modulation technique with highest overvoltages (PWM2)—(**a**) turn-on, (**b**) turn-off.

Peak overvoltage values for all the studied modulation techniques are showcased in Table 4. In the previously shown figures, only switching near the peak value of the line current was considered, whereas the data shown in Table 4 consist of the highest value throughout the entire 50 Hz period. Thus, this data are the basis for considerations for all the switches. Based on this data, we can observe that the peak overvoltage value difference between the PWM methods reached maximally 8% of the nominal drain–source voltage of 750 V for PWM2, while the variances between PWM1, PWM3, and PWM4 were as low as 4% of the nominal voltage. The difference between PWM1 and PWM4 is the most visible when transistor voltages are compared. For PWM1, transistors S_1 and S_4 (depending on the line current sign) are not bound to any constant potential, but rather float depending on the current ANPC leg state. This is not an issue for PWM4, as transistors S_5 and S_6 connect the floating potential to the zero voltage, and thus peak transistor voltage overshoots are

lower. The significant difference between PWM2 and other techniques is caused by this method's relatively lengthy conduction loop, as mentioned in Section 2. Nevertheless, the variance is still on a minimal level. Therefore, when a similar power rating as in the presented system is considered, it is safe to assume that for a well-optimized system, in terms of conduction path length, the effect of chosen PWM technique on the transistor overvoltage is somewhat limited and should not be as important as other factors, such as power loss and its distribution or filter requirements, or even omitted at all. However, this effect is enlarged when the current is higher. Thus, such an approach should not be applicable in very high power systems.

Table 4. Results for the different modulation patterns at nominal ratings of the ANPC leg.

	V_{DC} = 1500 V; P = 6.5 kW; v_{AC} = 230 V rms			
Parameter	**PWM1**	**PWM2**	**PWM3**	**PWM4**
$v_{DS\_max(S3)}$ [V]	832	957	846	827
$v_{DS\_max(S4)}$ [V]	889	802	868	873
$v_{DS\_max(S6)}$ [V]	857	848	842	843
$P_{LOSS(exp.)}$ [W]	182	177	165	182
$P_{LOSS(sim.)}$ [W]	137	137	114	136

4.3.2. Power Losses

The other crucial factor in which the PWM methods were compared is the system efficiency. Since power loss could not be measured individually on every converter component without impacting the inverter performance, total power loss was measured as the difference between input and output converter power, according to Figure 7.

Figure 11a showcases the total inverter efficiency at nominal system voltages (1500 V DC and 230 V AC), with a constant modulation index at 0.45 and varying load resistance, so that the power could be measured in 20–100% range of its nominal value. As shown, modulation techniques PWM3 and PWM2, similarly as in the simulation study, exhibit the highest efficiency. For the nominal power, and thus with the highest transistor current, PWM4 shows the lowest power losses, implying that the conduction losses are the main source of power loss. This is since this modulation method employs all four middle switches (S_2, S_3, S_5, S_6), and thus, the lowest effective on resistance. PWM2, on the other hand, showcases top performance for lower power, below 60% of the nominal value. In this modulation type, when only the positive half of the line current is considered, transistors S_1 and S_5 do not switch at all as the switching occurs between S_2 and S_3. Therefore, switching loss is limited to this transistor pair, contrary to other PWM techniques where the switching occurs for more power devices. However, when higher power is regarded, the importance of switching loss is diminished, and the efficiency becomes very similar for all the methods except for PWM3, which is characterized by more available conduction paths. Thus, using PWM2 and PWM3 alternately, depending on the load conditions, should be considered to ensure the lowest power losses throughout the whole operating range. Furthermore, developing an algorithm that optimally chooses the modulation technique according to the operating point may be considered. When we study the two other methods more generally, in terms of efficiency, they are pretty similar with the slight advantage for PWM1 for lower power ratings.

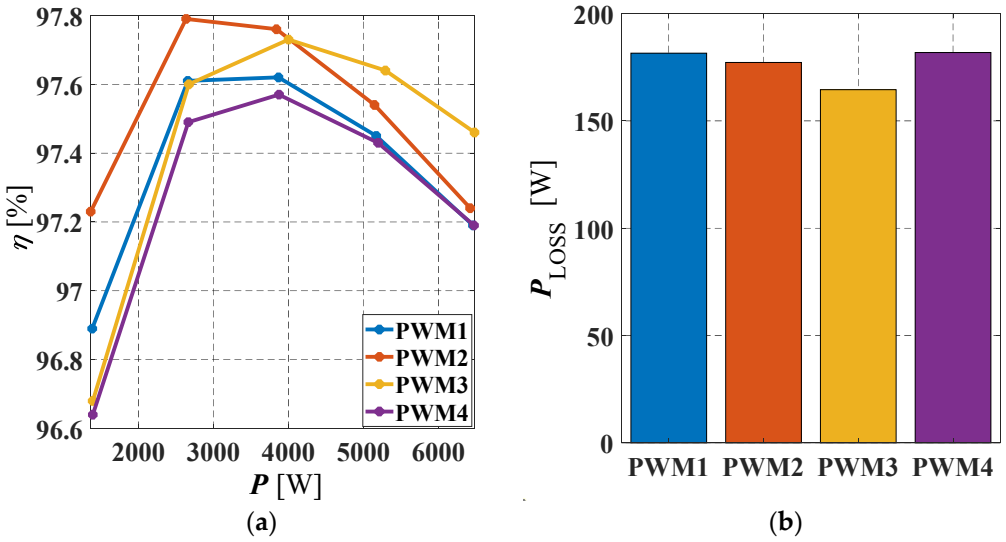


Figure 11. Experimental characteristics showcasing performance of the ANPC leg in function of converter power P—(**a**) efficiency at 1500 V DC, 230 V AC, and $m = 0.45$, (**b**) power loss at nominal operating point (1500 V DC, 6.5 kW, $m = 0.45$).

Furthermore, to exhibit the difference in actual loss values rather than efficiency, Figure 11b focuses on the power loss difference for different modulation techniques at the nominal operating point with the full power of 6.5 kW. When we compare the results from the experimental tests with the simulation study (see Table 4) we can observe that the presumptions noted in Section 3 are confirmed via the experiments on the prototype as well, with lowest power losses for PWM3 with 165 W. In contrast, techniques PWM1, PWM2, and PWM4 settled close to each other at 182, 177, and 182 W respectively.

5. Conclusions

This paper presents an MV ANPC submodule with state-of-the-art SiC MOSFETs for an advanced EV charging system. The constructed low-volume prototype of the all-SiC ANPC leg rated at 1500 V DC and 6.67 kW power has been experimentally validated to work with satisfactory switching performance and efficiency above 97.5% for the nominal operating point, which is a substantial value for such a low modulation index and voltage gain (1500 V DC to 230 V AC). Furthermore, as the design process's focus was to minimize the parasitic inductances in the converter, the transistor voltages and ringing were relatively low below 5% of the steady-state value, so that satisfactory switching performance could be achieved. Finally, several PWM techniques have been analyzed, tested, and compared for the specific application shown in this paper, focusing on the impact of all the presented modulation methods strictly for an all-SiC ANPC leg. This is in contrary to other publications in the area, in which the different PWM techniques were applied, but only in various SiC/Si hybrid ANPC leg configurations, usually limited to 1–2 modulations per configuration.

The obtained results show that for an MV all-SiC ANPC inverter submodule rated at 1.5 kV DC and applied in an advanced EV charging system, shown in Figure 1, PWM2 is the best for lower power, while PWM3 is the choice for a higher power (over 60% of nominal value). However, for other power electronics applications, depending on the required voltage levels (and thus the modulation index), as well as for other state-of-the-art SiC MOSFETs and/or Si IGBTs, the outcomes may vary, as so would the ratio between switching and conduction loss, power loss distribution among the components, as well as other factors. Thus, efficiency wise it is not easy to strictly determine which PWM technique is the optimal choice universally, as there are nuances for each application that can affect the power loss quite noticeably. Furthermore, changing the modulation technique during operation, depending on the load parameters should also be considered to achieve the

best performance, and thus, the highest efficiency. Nevertheless, based on the theoretical and experimental performed studies for a parasitic inductance optimized system with similar power ratings as in the presented ANPC leg, the impact of conduction loops on transistor overvoltages and ringing between the different PWM methods, even for a quite high voltage of 1.5 kV, is not crucial, and can be nearly fully omitted. Thus, the optimal choice for the modulation technique should be limited to other required parameters, such as efficiency.

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