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Discontinuous Current Mode Modeling and Zero Current Switching of Flyback Converter

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Abstract: The flyback converters are widely used in low power applications. The switch typically requires 600 V breakdown voltage in order to perform large step-down voltage. Thus, slight variation on the switch control can either permanently damage the switch or decrease the efficiency of the power conversion. In order to achieve higher power efficiency, the previous literature suggested operating the flyback converter in the discontinuous current mode (DCM). It is then required to understand the critical conditions of the DCM through analyzing the dynamic behavior and discontinuous current mechanism. This paper started from the current waveform analyses, proceeded to the derivation of zero current switching (ZCS) formulation, and finally reached the necessary conditions for the DCM. The entire DCM operation was divided into three phases that subsequently affect the result of the zero voltage switching (ZVS) and then to the ZCS. The experiment shows a power efficiency of over 96% when the output power is around 65 W. The switch used in this paper is a Gallium Nitride High-Electron-Mobility Transistor (GaN HEMT) that is advantageous at the high breakdown voltage up to 800 V. The important findings from the experiments include that the output power increases with the increasing input DC voltage and the duty cycle is rather linearly decreasing with the increasing switching frequency when both the zero voltage switching (ZVS) and ZCS conditions are satisfied simultaneously.

Keywords: flyback; discontinuous current mode; GaN HEMT

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Citation: Kumar, R.; Wu, C.-C.; Liu, C.-Y.; Hsiao, Y.-L.; Chieng, W.-H.; Chang, E.-Y. Discontinuous Current Mode Modeling and Zero Current Switching of Flyback Converter. *Energies* **2021**, *14*, 5996. https://doi.org/10.3390/en14185996

Academic Editor: Idir Nadir

Received: 11 July 2021
Accepted: 16 September 2021
Published: 21 September 2021

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1. Introduction

The rapid advancement of electric vehicles [1–3], military technology [4], grid technology [5,6] and factory automation [7] have led to an increased demand for the dc-dc converter. Isolated converters are required, where isolation is needed between the input and output side. Flyback converters are widely used topology for low power and large step-down voltage applications. During the transfer of energy from the input to the output side, an intermediate flyback transformer is used. The transformer is designed such that the primary windings turns of the transformer are higher compared to the secondary winding turns for large step-down voltage applications.

The converter usually operates in two modes based on the output load. In continuous conduction mode (CCM), the transformer is unable to transfer the complete energy since the part of energy always remains in the core. In this mode, the semiconductor switch is stressed at a higher voltage [8–10]. In addition, it leads to hard switching operation, which decreases the conversion efficiency. In [11–15], an active clamp-based flyback converter is discussed to reduce the voltage stress on the switch. However, using the additional switch requires an additional gate driver circuit. Apart from that, this topology increases

the current stress on the switch. That can considerably affect the switch lifetime especially if the Gallium Nitride High Electron Mobility Transistor (GaN HEMT) based power switch is used [16–20]. In terms of output voltage control of the converter, the bandwidth is limited by the right half-plane zero location. Considering these limitations in the CCM operation, the converter is preferred to operate in the discontinuous conduction mode (DCM). However, this mode of operation brings other challenges for the circuit designer, such as larger filter requirements at the input and output side [21–24], and increased electromagnetic interference [25,26]. The detailed comparison between both operations is discussed in [27,28]. In the DCM operation, the transformer is able to transfer the complete energy to the output side. In other words, the transformer secondary winding current becomes zero. However, due to the presence of leakage inductance and output capacitance of the switch, results in the voltage oscillation which is because of the resonance effect that is discussed in [29]. Few studies have presented some methods using divided resonant capacitor [30], the secondary-side resonant method [31], and dynamic resonant period control [32], for mitigating voltage spike and increasing power conversion efficiency to improve the traditional methods, such as RCD clamp circuit, or active clamp circuit. In [30], the design methodology for a flyback converter with divided resonant capacitor is analyzed by considering leakage and load variations, which is discussed to reduce the voltage spikes and improve the efficiency of the switch. This method further improves the overall conversion efficiency of the converter. In [31], a secondary-side resonant method is proposed using equivalent circuit analysis model to improve synchronous rectifier operation and reduce primary RMS current. In [32], a dynamic resonant period control for zero voltage switching is proposed, which can adjust the ON-time in auxiliary switch to reduce leakage energy loss and prevent large voltage stress on the component, while the efficiency of the converter is further improved by achieving the zero voltage during the switching ON of the switch. The designed methodology for the ZVS operation is discussed in [33,34]. According to these studies, taking equivalent circuit analysis model and design methodology as consideration for achieving ZVS and ZCS operation are important issue to reach the superior performance. The quasi-resonant flyback converter in [31–34] use multiple switches to activate the voltage oscillation on the secondary side. The quasi-resonant flyback converter in [30] is equipped with a resonance capacitance on the secondary side. The quasi-resonant flyback converter in [35] controls the duty calculated every switching period. Their methods are practical with additional sensors required. Our paper derives the originality of the DCM resonance due to the interaction between the output voltage and the output current with simple duty control and without additional transistor switch and sensor feedback. Our method is not quite in the domain of quasi-resonant flyback converters. We are looking for the low switching loss method which yields a high efficiency in the DCM operation for a conventional flyback converter in high switching frequency using GaN HEMT. Our method is simply achieved by having ZVS with ZCS occurred simultaneously in the instance of switching. The quasi-resonant flyback converter achieved only ZCS and not the ZVS.

To date, quite several flyback controllers are available in the market. In addition to the conventional single working-mode controller, some multiple working-mode controllers, such as UCC 28600 [36] and XDPS21071 [37] for Secondary-Side-Regulated (SSR), and LM 5180 for Primary-Side-Regulated (PSR) [38], have also been developed for improving the conversion efficiency of the flyback throughout the entire load [39,40]. It was commonly agreed that the flyback converter with low output current is suitable for discontinuous current mode (DCM) operation and continuous current mode (CCM) operation is suitable for large output current. In general, the DCM operation yields better power conversion efficiency. On the other hand, the DCM can cause larger voltage peak, which may damage the switch. The suitable operation modes depending on the application and the switch used. Take XDPS21071 [37] for example, it operates in a guaranteed DCM mode under all conditions. To maximize efficiency at light and medium loads, XDPS21071 also implemented frequency reduction mode and burst mode. For USB PD applications, CCM

operation under fixed-frequency control makes EMI and system design relatively simple. Moreover, several of the previous literature present more complete analysis with the parasitic components including transformer parasitic capacitance, leakage inductance or the diode parasitic capacitance [41–45] in flyback converter to show the good agreement between simulation and measurement results.

This paper aims to provide an insight of the DCM mechanism and zero current switching approach without basing on the trial and error method and intend to utilize the theories to reduce the number of experiments, which are organized as follows. In Section 2, the detailed operation of the flyback converter is discussed in the ZCS. During the discussion, a template of the key waveforms is used in the OFF period of the switch. The template waveform is divided into three intervals based on the (1) drain to source voltage rising period, (2) current conduction period in the secondary winding and (3) zero current conduction period in the secondary winding. In these intervals, governing equations of the converters are derived, and the key parameters are calculated. In Section 3, a SPICE simulation analysis method is carried out. Based on the SPICE analysis, the critical conditions for the DCM operation, including the conditions of large resistor load and small duty cycle, can be verified. Afterward, experimental results are presented, and the comparison with SPICE analysis is provided in Section 4. The conclusion of this work is discussed in Section 5.

2. Materials and Methods

The transistor used in this paper is cascode power module derived from D-mode GaN HEMT described in [46], shown in Figure 1. An N-type metal oxide semiconductor (NMOS) in series with the D-mode GaN HEMT is connected to achieve the module operation similar to the enhancement mode. The NMOS is always remained on during regular operation. The GaN HEMT is then switched on and off by using a charge pump-based circuit and a conventional gate driver. Since the GaN HEMT is driven independently, the highly negative gate to source voltage surge during turn off is avoided, and in addition, high switching frequency operation is made possible. The parameter of GaN device is analyzed using a Keysight B1500A. The turn-on voltage (v_{GS},on) for the D-mode GaN HEMT is −7 V, the drain-source parasitic capacitance (C_{DS}) is 30 pF. The breakdown voltage of the GaN HEMT is 800 V and the maximum current is 35 A.

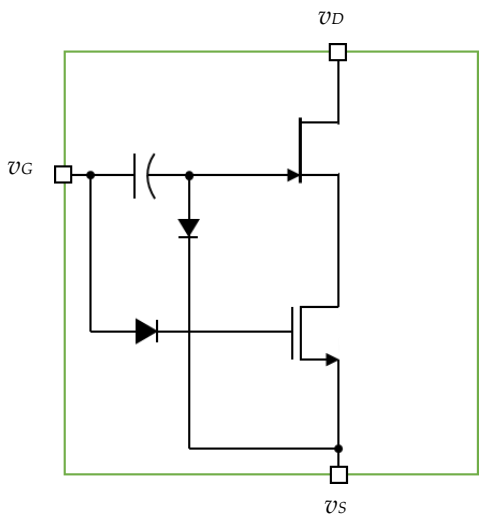

Figure 1. The cascode GaN HEMT power module.

2.1. Flyback Converter Circuit

Figure 2 depicts an equivalent circuit of the flyback converter. There are two diodes, the rectifier diode (D_S) and the snubber diode (D_B), used in the circuit. The rectifier diode is a fast recovery diode (FRD) and the snubber diode is a high breakdown voltage up to

1000 V diode which is not a fast recovery diode. The output capacitor (C_O) is large enough that allows the output voltage to be assumed constant during analyses.

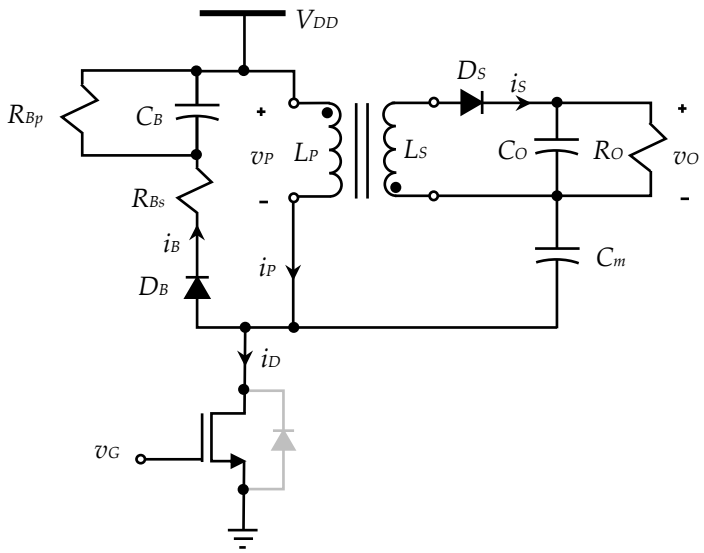

Figure 2. The equivalent circuit of flyback converter.

2.2. Transformer

The equivalent circuit of the transformer is modified from the Steinmetz equivalent circuit as shown in Figure 3. Assuming that R_P and R_S are very small and R_{core} is very large, the power loss due to them are ignored from the analysis. The overall inductance on the primary side is L_P which can be divided into two parts, namely the magnetization inductance L_{Pm} and the leakage inductance L_{Pl}, in terms of the coupling coefficient. The individual inductances are defined as follows.

$$L_{Pm} = kL_P \tag{1}$$

and

$$L_{Pl} = (1-k)L_P \tag{2}$$

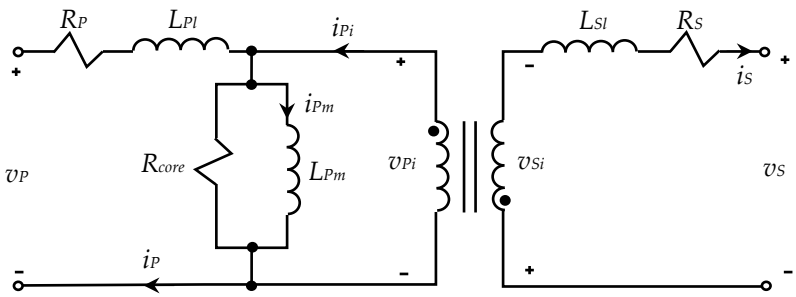

Figure 3. The equivalent circuit of the transformer.

Since the flyback converter uses windings in opposite dot-orientation as a convention, we thus define the current as follows.

$$i_P = i_{Pm} - i_{Pi} = i_{Pm} - i_S/a \tag{3}$$

In the flyback converter arrangement, i_{Pi} is a non-negative value, i.e., $i_{Pi} \geq 0$, since $i_S \geq 0$ for the secondary winding outputs to a diode D_S in series. The voltage on the primary winding is written as:

$$v_P = L_{Pl}\frac{di_P}{dt} + v_{Pi} \tag{4}$$

The voltage on the mutual inductance is exerted by the magnetization current.

$$v_{Pi} = L_{Pm}\frac{di_{Pm}}{dt} \tag{5}$$

Thus, Equation (4) is then simplified into:

$$v_P = L_P\frac{di_{Pm}}{dt} - aL_{Pl}\frac{di_S}{dt} \tag{6}$$

The turn ratio a is defined as follows.

$$a = \frac{N_1}{N_2} = \sqrt{\frac{L_P - L_{Pl}}{L_S - L_{Sl}}} \approx \sqrt{\frac{L_P}{L_S}} \tag{7}$$

The leakage inductances can be measured from the short circuit test in order to distinguish it from the overall inductance. The coupling coefficient is estimated as follows.

$$k = \sqrt{1 - \frac{L_{Pl}}{L_P}} \tag{8}$$

The parameters of the transformer in this paper, measured from the open and short circuit test [47] using the RLC meter GWINSTEK LCR819, are listed in Table 1.

Table 1. Parameters of the transformer.

Symbol	Original	Value	Unit
L_P	RLC meter open circuit test	400	µH
R_P	RLC meter open circuit test	0.9	Ohm
Q_{oc}	RLC meter open circuit test	277.4	-
C_m	RLC meter short circuit test	333.7	nF
L_{Pl}	RLC meter short circuit test	9.97	µH
L_S	RLC meter open circuit test	10.27	µH
L_{Sl}	RLC meter short circuit test	0.27	µH
a	Equation (7)	6.24	-
k	Equation (8)	98.7%	-

2.3. Wave Form Assumptions

The wave forms for the v_{DS}, i_S and i_P are as shown in Figure 4. The wave forms are obtained empirically from the experiments, which yield good efficiencies from the input and output power relations.

During the switch turn-on time, the inductor current rises in a ramp-up function which correlates with the inductance L_P and input voltage V_{DD} as follows.

$$I_{P,\max} = \frac{\delta T V_{DD}}{L_P} \tag{9}$$

During the switch turn-off time, the output current i_S is in a sinusoidal alike ramp-down function. The peak of the ramp function is denoted by $i_{S,max}$. The current flows to the capacitor C_O within a time period called the continuous current mode time t_{CCM}.

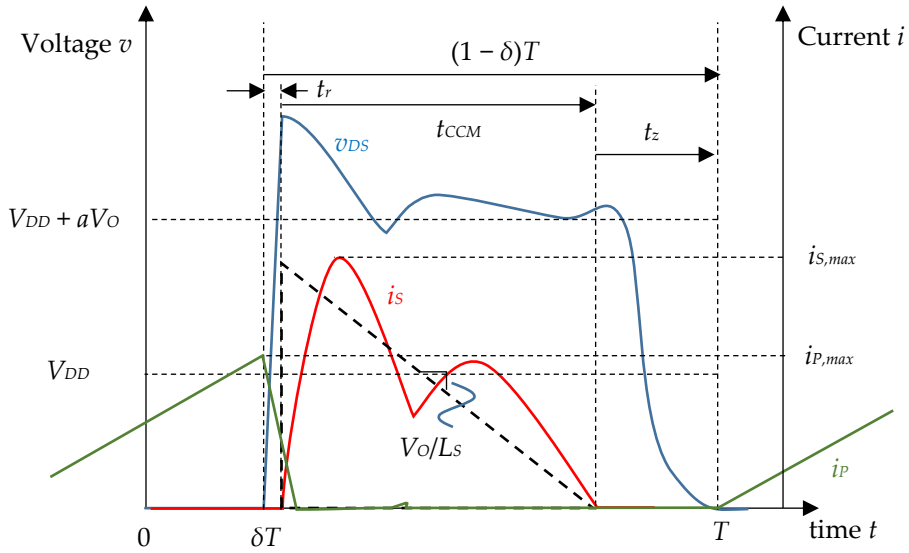

Figure 4. Template of the flyback converter responses.

There are three phases during the turn-off process of the switch, which are

(1) the drain-source voltage rising phase,
(2) the current flowing on the secondary winding phase, and,
(3) the zero current in the secondary winding phase.

2.4. Steady State Assumptions

We had applied two assumptions in the steady state of the flyback converter as follows.

(1) The ratio of the peak value of currents is:

$$i_{S,\max} = \zeta a i_{P,\max} \tag{10}$$

where ζ denotes the transformer peak current attenuation. It shall be noted that the attenuation does not imply the energy loss; however, it has the effect to the current flowing time on the secondary winding.

(2) Current flows in the secondary winding only during the diode conduction time which is referred to as the continuous current time t_{CC}. This assumption can be written into two equations separately as follows.

$$t_{CC} = \lambda(1-\delta)T,\ 0 \le \lambda \le 1 \tag{11}$$

$$\frac{i_{S,\max}}{2}\frac{t_{CC}}{T} = \frac{V_O}{R_O} \tag{12}$$

Substituting Equation (12) into (10), we obtain:

$$\frac{i_{S,\max}}{a}\frac{V_O t_{CC}}{aL_S} = \zeta i_{P,\max} = \zeta\frac{V_{DD}\delta T}{L_P} \tag{13}$$

Equation (13) subsequently yields:

$$t_{CC} = \zeta\frac{V_{DD}\delta T}{aV_O} \tag{14}$$

Substituting Equation (14) into (11), we obtain:

$$\lambda = \zeta\frac{\delta}{a(1-\delta)}\frac{V_{DD}}{V_O} \tag{15}$$

From Equations (12)–(14), we calculate the output voltage V_O as follows.

$$\frac{V_{DD}\delta T}{L_P}\zeta\frac{V_{DD}\delta}{a} = \frac{V_O^2}{R_O} \tag{16}$$

The voltage gain is then written as follows.

$$\frac{V_O}{V_{DD}} = \delta\sqrt{\frac{\zeta R_O T}{2L_P}} = \delta\sqrt{\frac{\zeta R_O}{2L_P f_S}} \tag{17}$$

The transformer peak current attenuation ζ, which may also be deemed as the power efficiency, may be evaluated from the experiment as follows.

$$\zeta = V_O^2\frac{a f_S L_P}{\delta V_{DD}^2 R_O} \tag{18}$$

The experimental examples are as shown in Table 2. The necessary condition for the ZVS is $aV_O/V_{DD} \geq 1$. Referring to Figure 4, the drain-source voltage v_{DS} will have a steady state value at V_{DD} when the current on both the primary i_P and the secondary winding i_S are zero, the only current flowing to the switch is the current from the snubber. The drain-source voltage v_{DS} will drop from $V_{DD} + aV_O$ to V_{DD}. Assuming the damping of the voltage oscillation is small, the minimum voltage of v_{DS} is $V_{DD} - aV_O$ which must be a non-positive voltage. At the time when $v_{DS} = 0$, the switch turns on again that is known as the ZVS.

Table 2. Parameters used to estimate output voltage.

Symbol	Original	Value	Unit
a	Measurement (LCR819)	6.24	-
R_O	Measurement (Element)	50	Ohm
L_P	Measurement (LCR819)	400	µH
V_{DD}	Input parameter	300	V
δ	Input parameter	48%	-
f_S	Input parameter	280	kHz
$T = 1/f_S$	Input parameter	3.57	µs
V_O	Measurement (on Flyback)	56.3	V
ζ	Equation (18)	1	-
t_{CC}	Equation (14)	1.5	µs

2.5. Drain-Source Voltage Rising Phase

In the drain-source voltage rising phase we have assumed that the current on the secondary winding is zero. The equivalent circuit is as shown in Figure 5. During this phase, the diode transits from its reverse bias state to the forward bias state. The junction capacitor C_{j0} must be refilled with the reverse recovery charge Q_{rr}. The drain-source capacitor C_{DS} needs also also need the reverse recovery charge on the way to turn the switch off.

The KVL equation yields that:

$$V_{DD} = v_P + v_{DS} = L_P\frac{di_P}{dt} + v_{DS} \tag{19}$$

where:

$$i_D = C_{oss}\frac{dv_{DS}}{dt} = (C_{DS} + C_{GD})\frac{dv_{DS}}{dt} \tag{20}$$

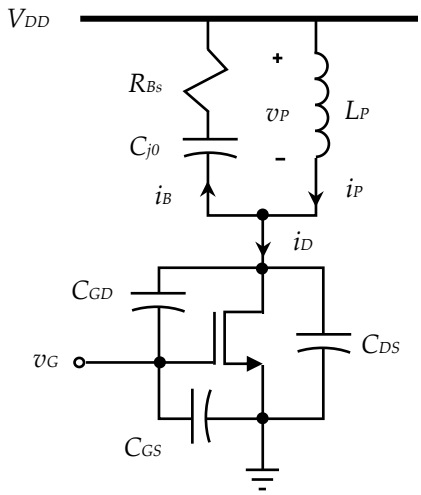

Figure 5. Equivalent circuit for the drain-source voltage rising phase.

The current flowing in the snubber is written as follows.

$$\frac{di_B}{dt} + \frac{1}{R_{Bs}C_{j0}} i_B = \frac{1}{R_{Bs}} \frac{dv_{DS}}{dt} \tag{21}$$

The KCL equation can be stated as follows.

$$i_D = C_{oss} \frac{dv_{DS}}{dt} = i_P - i_B \tag{22}$$

From Equation (19), we obtain the following equation.

$$V_{DD} = L_P \frac{d(i_D + i_B)}{dt} + v_{DS} \tag{23}$$

Substituting (21) by neglecting the term di_B/dt in Equation (23), we have:

$$L_P(C_{oss} + C_{j0}) \frac{d^2 v_{DS}}{dt^2} + v_{DS} = V_{DD} \tag{24}$$

It is then written in the standard form of the 2nd order system equation as follows.

$$\frac{d^2 v_{DS}}{dt^2} + {\omega_1}^2 v_{DS} = {\omega_1}^2 V_{DD} \tag{25}$$

where the resonant frequency is:

$$\omega_1 = \frac{1}{\sqrt{L_P(C_{oss} + C_{j0})}} \tag{26}$$

The rising time is assumed one tenth of the oscillation period time, which is approximately 36 degree phase forward.

$$t_r = \frac{1}{10 f_1} = \frac{1}{10} \frac{2\pi}{\omega_1} \tag{27}$$

The nominal values of the parameters and the calculation result is shown in Table 3.

Table 3. Parameters used to estimate the rising time.

Symbol	Original	Value	Unit
L_P	Measurement (LCR819)	400	µH
C_{oss}	Measurement (B1500A)	130 @ V_{DS} = 200 V	pF
C_{j0}	Measurement (Element)	10	pF
$f_1 = \omega_1/2\pi$	Equation (26)	670	kHz
t_r	Equation (27)	150	ns

2.6. Current Flowing on the Secondary Winding Phase

Referred to Figure 6, the output diode D_S start conducting as the $-v_P \geq av_O$. The transformer is transforming the voltage from the secondary winding back to the primary winding providing the equivalence $L_{Sm} = L_{Pm}/a^2$ and $i_{Sm} = a\ i_{Pm}$. It is important to note that the snubber diode is not a fast recovery diode, which will allow the reverse current through. Then the following equations are derived assuming that $C_B > 10\ C_{DS}$ and the core loss is neglected, which results in $i_B > 10\ i_D$. In addition, $L_{Pm} >> L_{Pl}$ is assumed during the derivation and the voltage drop on the leakage inductor is ignored. From Equation (3), we obtain that:

$$ai_P = -i_{Si} = i_{Sm} - i_S \tag{28}$$

In addition:

$$i_P = i_B = -C_B \frac{d(v_P + i_P R_{Bs})}{dt} = -C_B \frac{d\left(v_P + (i_{Sm} - i_S)\frac{R_{Bs}}{a}\right)}{dt} \tag{29}$$

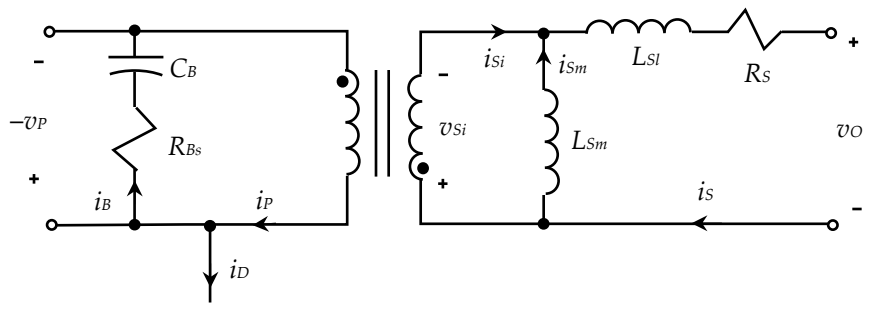

Figure 6. Equivalent circuit for the current flowing on the secondary winding phase.

On the secondary winding side, the current is:

$$L_{Sl}\frac{di_S}{dt} = -\frac{v_P}{a} - v_O \tag{30}$$

Substituting the above equation into Equation (28) then into (29), we have:

$$i_{Sm} - i_S = -aC_B\frac{dv_P}{dt} - C_B R_{Bs}\frac{di_{Sm}}{dt} + C_B R_{Bs}\frac{di_S}{dt} \tag{31}$$

Knowing that $di_{Sm}/dt = v_{Si}/L_{Sm} = a\ v_P/L_{Pm}$, we substitute Equation (30) into the Equation (31) to obtain that:

$$i_{Sm} - i_S = -aC_B\frac{dv_P}{dt} - aC_B R_{BS}\frac{v_P}{L_{Pm}} - \frac{C_B R_{BS}}{L_{Sl}}\left(\frac{v_P}{a} + v_O\right) \tag{32}$$

Taking time derivative to the above equation, we have:

$$C_B\frac{d^2v_P}{dt^2} + R_{Bs}C_B\left(\frac{1}{L_{Pm}} + \frac{1}{a^2L_{Sl}}\right)\frac{dv_P}{dt} + \left(\frac{1}{L_{Pm}} + \frac{1}{a^2L_{Sl}}\right)v_P = -\frac{v_O}{aL_{Sl}} \tag{33}$$

Considering the $L_{Pm} >> a^2\, L_{Sl}$, the above equation can be written into a standard form of a 2nd order differential equation as follows.

$$\frac{d^2 v_P}{dt^2} + 2\xi_2\omega_2\frac{dv_P}{dt} + {\omega_2}^2 v_P = -\frac{v_O}{a}{\omega_2}^2 \tag{34}$$

In the above equation, the natural frequency and the damping ratio are as follows.

$$\omega_2 = \frac{1}{a\sqrt{L_{Sl}C_B}} \tag{35}$$

$$\xi_2 = \frac{R_{Bs}}{2a}\sqrt{\frac{C_B}{L_{Sl}}} \tag{36}$$

It is worth to note that the damping ratio derived in the above equation is in the form for quality factor of the current amplification. That is to say the transformer is activating in this phase; the current on the primary winding will affect the current on the seconding winding. The nominal values of the parameters and the calculation results are shown in Table 4. Equation (34) is valid when the current i_P on the primary winding becomes negative until the current i_P becomes positive. At the time when the current i_P is zero, there is no more magnetization required on the secondary winding and Equation (30) will be revised into as follows.

$$L_S\frac{di_S}{dt} = v_O \tag{37}$$

Table 4. Parameters used to estimate the frequency of the current on secondary winding.

Symbol	Original	Value	Unit
C_B	Measurment (Element)	1	nF
a	Measurement (LCR819)	6.24	-
R_{Bs}	Measurment (Element)	33	Ohm
L_{Sl}	Measurement (LCR819)	270	nH
$f_2 = \omega_2/2\pi$	Equation (35)	500	kHz

Thus, the current i_S will immediately change from decreasing function into an increasing function as shown in Figure 7. Shortly when the current i_P on the primary winding becomes negative again after time t_d, Equation (34) is once again activated. The frequency of the current derived from the parameters of the transformer and the snubber, as shown in Table 4, indicates that the minimum time to complete the current hurdle is 2 µs. Thus, the maximum switching frequency f_S in the current arrangement shall be less than 500 kHz when the duty ratio is 50%.

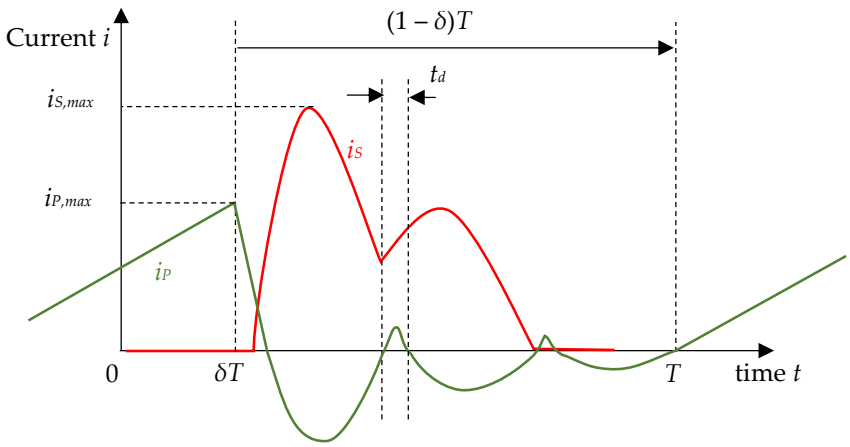

Figure 7. Response of the transformer current and the current on the secondary winding.

2.7. Zero Current in the Secondary Winding Phase and Zero Current Switching

As stated in the previous section that the necessary condition for the zero-voltage switching is $aV_O/V_{DD} \geq 1$. The snubber diode D_B simultaneously turns off when no current is flowing in in the secondary winding as shown in Figure 8. In this zero current in the secondary winding phase, assuming that i_B is negligibly small, the steady state voltage for v_{DS} is supposed V_{DD} when the initial value of v_{DS} is $V_{DD} + aV_O$.

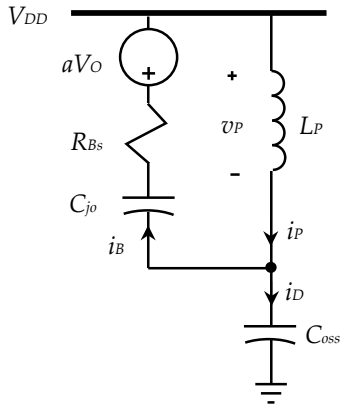

Figure 8. Equivalent circuit for the zero current in the secondary winding phase.

The capacitor C_{oss} withdraws the charge in according to the equation as follows.

$$i_D = C_{oss}\frac{dv_{DS}}{dt} \tag{38}$$

The KVL equation yields that:

$$L_P\frac{di_P}{dt} + v_{DS} = L_P\frac{d(i_D + i_B)}{dt} + v_{DS} = V_{DD} \tag{39}$$

Assuming that i_B is negligibly small compared with di_B/dt, Equation (21) yields that:

$$\frac{di_B}{dt} = \frac{1}{R_{Bs}}\frac{dv_{DS}}{dt} \tag{40}$$

We can reformulate Equation (39) as follows.

$$\frac{d^2v_{DS}}{dt^2} + 2\xi_3\omega_3\frac{dv_{DS}}{dt} + {\omega_3}^2 v_{DS} = {\omega_3}^2 V_{DD} \tag{41}$$

The resonant frequency is:

$$\omega_3 = \frac{1}{\sqrt{L_P C_{oss}}} \tag{42}$$

$$\xi_3 = \begin{cases} \frac{1}{2R_{Bs}}\sqrt{\frac{L_P}{C_{oss}}} & \text{when } i_B > 0 \\ 0 & \text{else} \end{cases} \tag{43}$$

The switch turns off when the first derivative of v_{DS} becomes zero is called ZCS. According to Equation (41), the time required to complete the half time period of resonance is defined as t_Z which can be expressed as follows.

$$t_Z = \frac{1}{2f_3} = \frac{\pi}{\omega_3} \tag{44}$$

We shall note that the damping ratio of Equation (43) is in a form of voltage amplification of resonance. The nominal values of the parameters and the calculation result is as shown in Table 5. As stated previously, the zero-voltage switching and further ZVS can be

successful only when we have a larger turn ratio a subjected to the same voltage output V_O. Thus, the transformer design is a critical issue to the flyback converter in order to achieve a high-power conversion efficiency.

Table 5. Parameters used to estimate the rising time.

Symbol	Original	Value	Unit
L_P	Measurement (LCR819)	400	μH
C_{oss}	Measurement (B1500A)	130 @ V_{DS} = 200 V	pF
$f_3 = \omega_3/2\pi$	Equation (42)	700	kHz
t_Z	Equation (44)	710	ns

3. Analysis

The analyses were used as tools to bridge the differences between the experiment and the derivations with assumptions. The first analysis is the SPICE analysis. The circuit parameters shown in the SPICE analysis are identical to those used in the experiment except the switch transistor, the input DC voltage V_{DD}, the switching frequency, the duty cycle and the load resistor. The second analysis based on the SPICE analysis is applied to verify the critical conditions for the DCM. The DCM operation is valid when the load resistor is large and the duty cycle of the switching is small. The corresponding analyses were also compared with the experiments. The satisfactory consistency allowed the designer to use the equations for verification of the DCM existence in different flyback converter designs.

3.1. SPICE Simulation Analysis

The flyback converter is simulated using the OrCAD, and the schematic diagram of the circuit is shown in Figure 9. During the simulation, parameters are considered the same as used for the above analysis. However, parasitic inductances are added at the input power supply ($L_{in,par}$) and switch ($L_{M1,par}$) to mimic their non-ideality due to the connecting wire and the lead of the switch, respectively. A voltage source is connected in series with the output capacitance to reduce the simulation time for achieving the steady-state. The steady-state waveform of the circuit is shown in Figure 10. The waveforms represent the gate voltage (v_G), switch voltage (v_{DS}), output diode current (i_S) and output voltage (V_O) with their respective colors, as shown in the schematic. It is observed that the i_S becomes zero within the $(1-\delta)T$ interval, which leads to ZCS of the switch. The capacitor C_o is provided with the initial condition (IC) of 56.3 VDC as the steady state output voltage and the SPICE simulation runs for only 1ms. We added a parasitic capacitance 50 pF to the primary winding of the transformer to increase the reality. The flyback converter result is for the purpose of comparing the analysis with the experiment and theoretical data using the identical circuit parameters, therefore it satisfies neither ZVS nor ZCS condition.

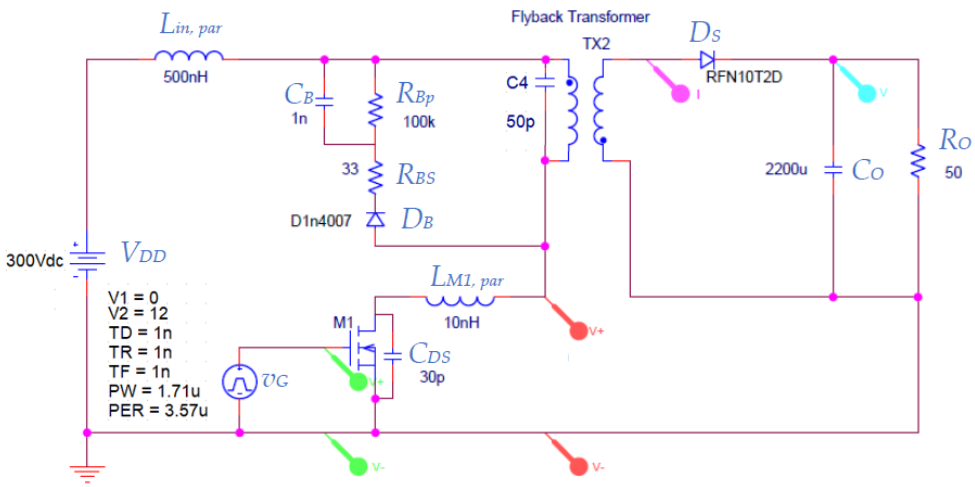

Figure 9. SPICE circuit for the equivalent flyback circuit.

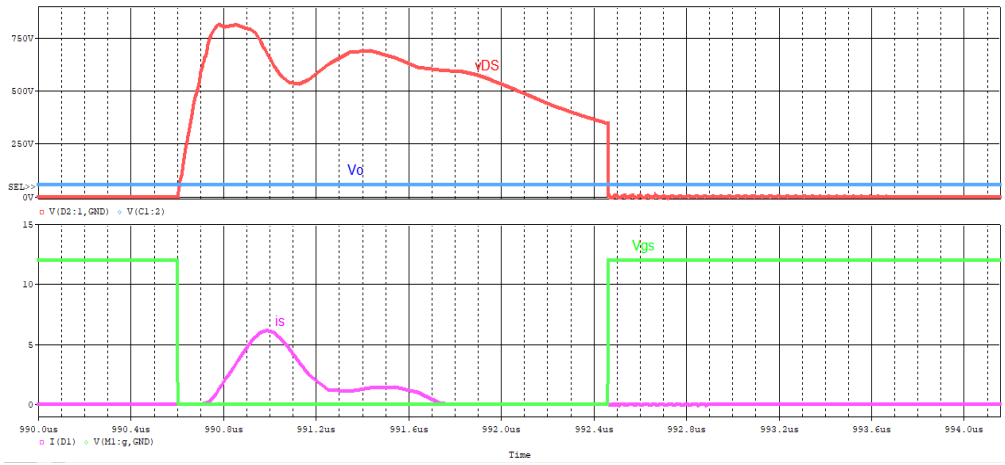

Figure 10. Simulation waveforms using the SPICE circuit (each time minor grid is 100 ns).

3.2. Critical Condition for DCM

The derivations provided in this section are based on the assumption that the power efficiency is 100%. The output voltage for the CCM is well-known as follows.

$$V_O = \frac{\delta}{a(1-\delta)} V_{DD} \tag{45}$$

According to Equation (9), the maximum current $I_{P,\max}$ on the inductor L_P can be written in terms of switching frequency f_s, duty cycle δ and input DC Voltage V_{DD} as follows.

$$I_{P,\max} = \frac{\delta V_{DD}}{L_P f_S} \tag{46}$$

According to Equation (17) providing the transformer peak current attenuation $\zeta = 1$, the output resistance R_O can be written in terms of switching frequency f_S, output voltage V_O, input DC Voltage V_{DD}, turn ratio a and duty cycle δ as follows.

$$R_O = 2L_P f_S \left(\frac{1}{\delta^2} \frac{V_O}{V_{DD}} \right) \frac{V_O}{V_{DD}} \tag{47}$$

Substituting Equation (45) into the above equation, we obtain the critical condition for output resistance R_O which locates at the border of CCM and DCM as follows.

$$R_O = 2 \frac{L_P f_S}{a\delta(1-\delta)} \frac{V_O}{V_{DD}} \tag{48}$$

Substituting Equation (46) into the above equation, we can rewrite the condition for DCM as follows.

$$R_O \geq 2 \frac{V_O}{a i_{P,\max}(1-\delta)} \tag{49}$$

According to Equation (45), if the output voltage V_O is higher than $\delta/a(1-\delta)V_{DD}$ then the output current which reduces the operation will become DCM. Thus, the duty cycle δ should follow also the equation below to achieve the DCM.

$$\frac{1-\delta}{\delta} \geq \frac{V_{DD}}{aV_O} \tag{50}$$

The SPICE circuit is operated at different V_{DD} and R_O to find out the boundary condition also known as critical condition. During the operation, the V_O and f_S are maintained constant 20 V and 150 kHz, respectively. The current i_S can be observed at different simulations to distinguish the kinds of operations. The simulation results

compared to the derivation in equation (50) and experiments are summarized in Figure 11. Afterward, the boundary condition between CCM and DCM operation is determined for the provided V_{DD} and R_O.

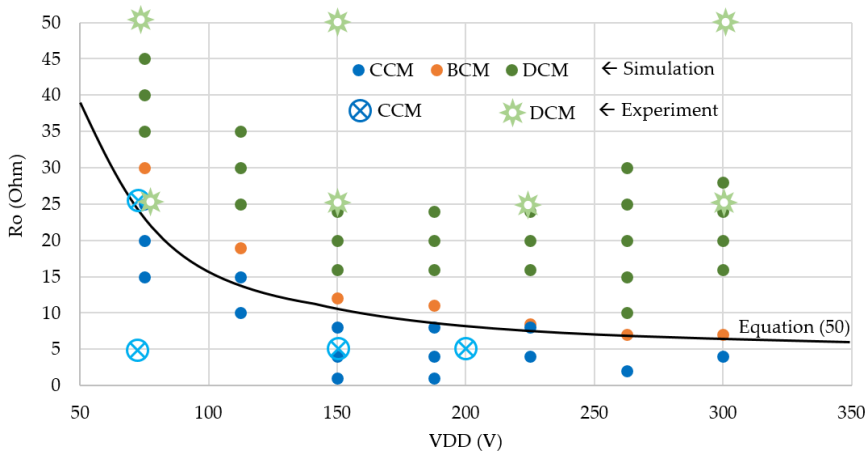

Figure 11. Determination of BCM using SPICE which is compared to Equation (50).

4. Results and Comparisons

In order to validate the proposed method, a medium voltage experimental setup is prepared as shown in Figure 12, and waveforms are shown in Figure 13. In the experiment, we used a D-mode GaN HEMT transistor fabricated by Elite advanced laser Co. The gate voltage in light blue color is switching from 0 to −12 V with the charge pump gate drive recommended in [48]. The circuit parameters follow the parameters provided in Tables 1–5. The circuit parameters follow the parameters provided in Tables 1–5. An operating condition ($V_{DD}, f_{S,}$ δ and R_O) is considered (150 V, 150 kHz, 66% and 50 Ohm), respectively. The measured V_O is found to be 53.4 V. The power output is 57 W under the efficiency 97.3% power conversion. The waveform matches closely to the theoretical waveform. As stated previously, at the time when the current i_P is zero, there is no more magnetization required on the secondary winding and Equation (30) will be revised into Equation (37), the current i_S will immediately change from decreasing function into an increasing function as shown in Figure 13. The dynamic waveforms due to the load change and different snubber designs are shown in Figure 14.

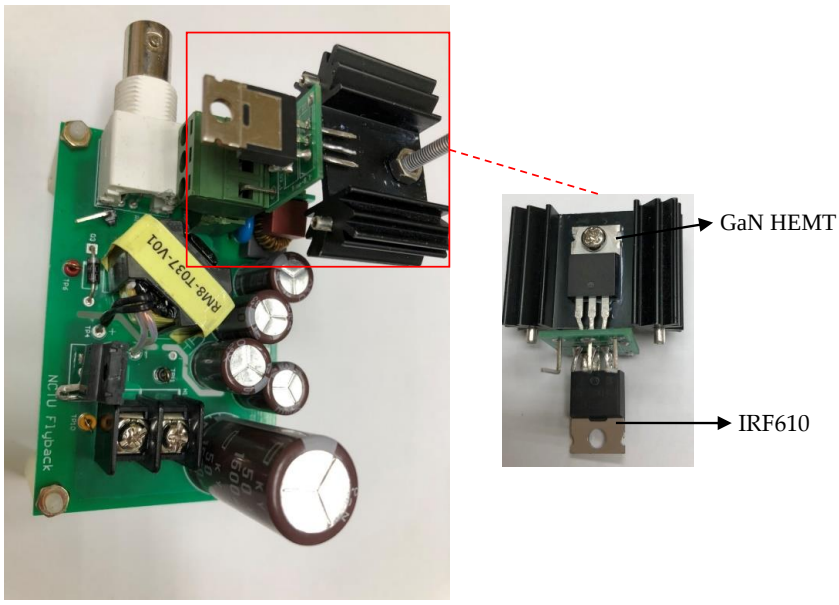

Figure 12. The Flyback experimental setup with cascode GaN HEMT power module.

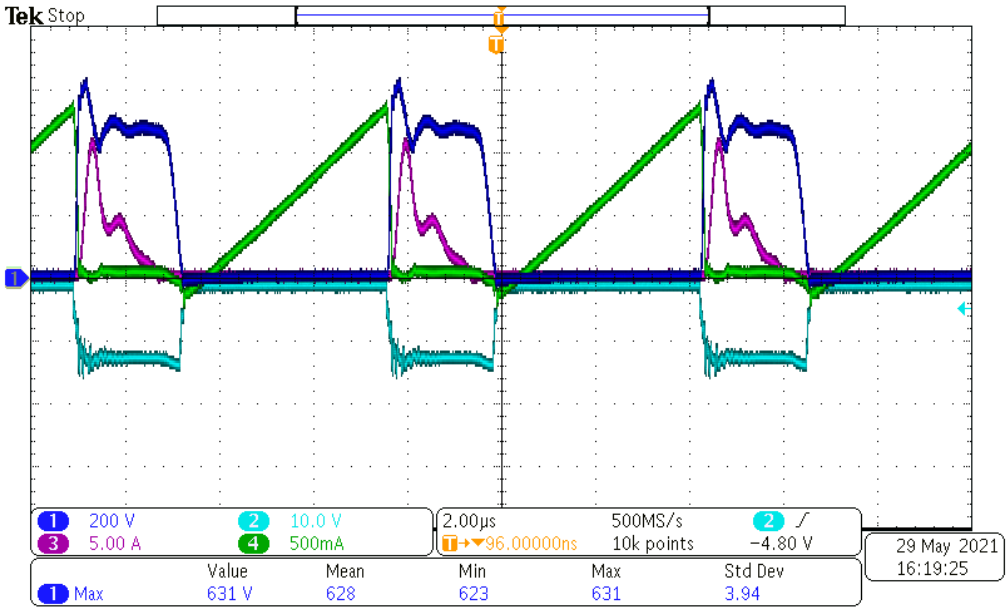

Figure 13. Experimentation waveforms at V_{DD} = 150 V, δ = 66%, f_S =150 kHz (T = 3.57 µs) and R_O = 50 Ohm.

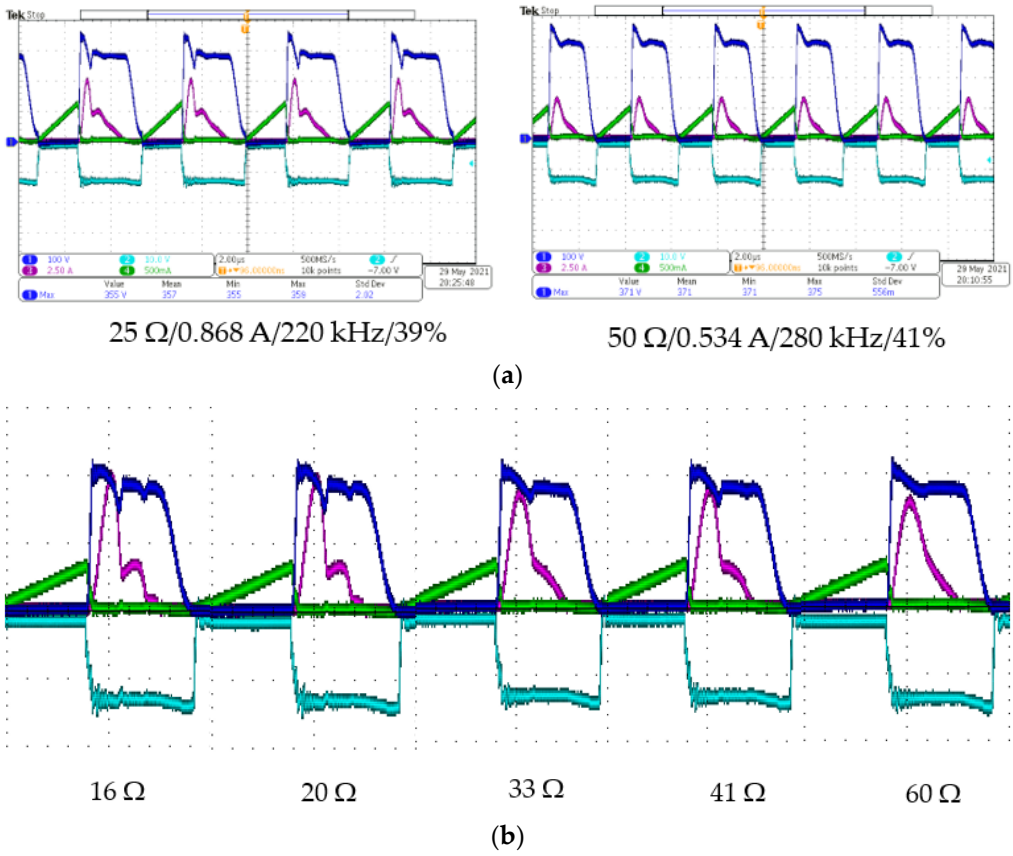

Figure 14. The dynamic waveforms due to (**a**) R_O changes (**b**) R_{Bs} changes (150 V, 250 kHz, 47% and 50 Ohm).

The other high voltage experimental setup yields waveforms are shown in Figure 15. An operating condition (V_{DD}, f_S, δ and R_O) is considered (300 V, 280 kHz, 48% and 50 Ohm), respectively. The measured V_O is found to be 56.3 V. The detailed key parameters comparison among the theoretical, OrCAD analysis, and experimental results are provided in

Table 6. From Table 6, it is observed that the t_{CC} obtained from the theoretical is higher than both the SPICE analysis and experiment. The reason for the differences due to the oscillation waveform of the i_S of the SPICE analysis is somehow different from the other two. The oscillation causes the peak of i_S to reach a value higher than $ai_{P,max}$. Therefore, the time required for the transformer to transfer the same amount of energy to the output side is less. The t_r parameter from the theoretical, SPICE analysis and experiment are found to be 150 and 130 ns, respectively. This is because the C_{DS} value during the simulation might be less than that of the experiment. The f_2 frequency obtained from the SPICE is twice higher than the theoretical, whereas the value obtained from the experiment is 1.6 times higher. The t_Z parameter obtained from the theoretical, SPICE and experiment are 710, 700 and 530 ns, respectively. The reason for having less t_Z time during the experiment because the t_{CC} time is larger. In summary, the theoretical yields values, a bit closer to the experiment than the SPICE does, however the total period of switching time was obtained incorrectly from the theoretical. The switching time period of the experiment is 3.57 µs. It is incorrect when we add up the t_{CC} and t_Z in the "theoretical" column of Table 6; the switch turn-off time of the theoretical became 2.2 µs which is supposed 1.86 µs subjected to the duty ratio 48%. On the other hand, the SPICE analysis can yield closer match to the experiments on the timing.

Table 6. Parameters comparison between SPICE analysis and experimentation.

Symbol	Description	Theoretical	SPICE Figure 10	Experiment	Unit
f_S	Switching Frequency	-	-	280	kHz
δ	Duty cycle of switching	-	-	48%	-
t_{CC}	Continuous Current Time	1.5 in Table 2	1.05	1.25	µs
t_r	Current rise time in secondary winding	150 in Table 3	130	130	ns
f_2	Natural frequency of the current resonance in secondary winding	500 in Table 4	1000	800	kHz
t_Z	Zero current time in secondary winding	710 in Table 5	700	530	ns

The power efficiency of the result shown in Figure 15 is 96.2% for 65 W output power. The power input is calculated by average the multiplication on the 10,000 samples, from the purple curve in Figure 15a, for 6 to 10 periods of switching as follows.

$$P_{in} = (\sum i_D)\ V_{DD}/10{,}000$$

The power input is calculated by average the multiplication on the 10,000 samples, from the green curve in Figure 15a, for 6 to 10 periods of switching as follows.

$$P_{out} = (\sum i_S)\ Vo/10{,}000$$

The power efficiency is calculated from the equation as follows.

$$Efficiency\ (\%) = P_{in}/P_{out} \times 100\%$$

Even though we demonstrated the efficiency without considering the EMI filter with AC/DC converter. However, with input AC voltage being 220 V can convert AC into the DC V_{DD} = 300 V, the EMI filter will only consume less than 0.1 W from the total power of 65 W. The overall efficiency is still higher than 96%. It is also worth to note that the output diode with average 1 A go through it will consume 1 W. Thus, other circuit elements including the snubber circuit consumes only 1.5 W.

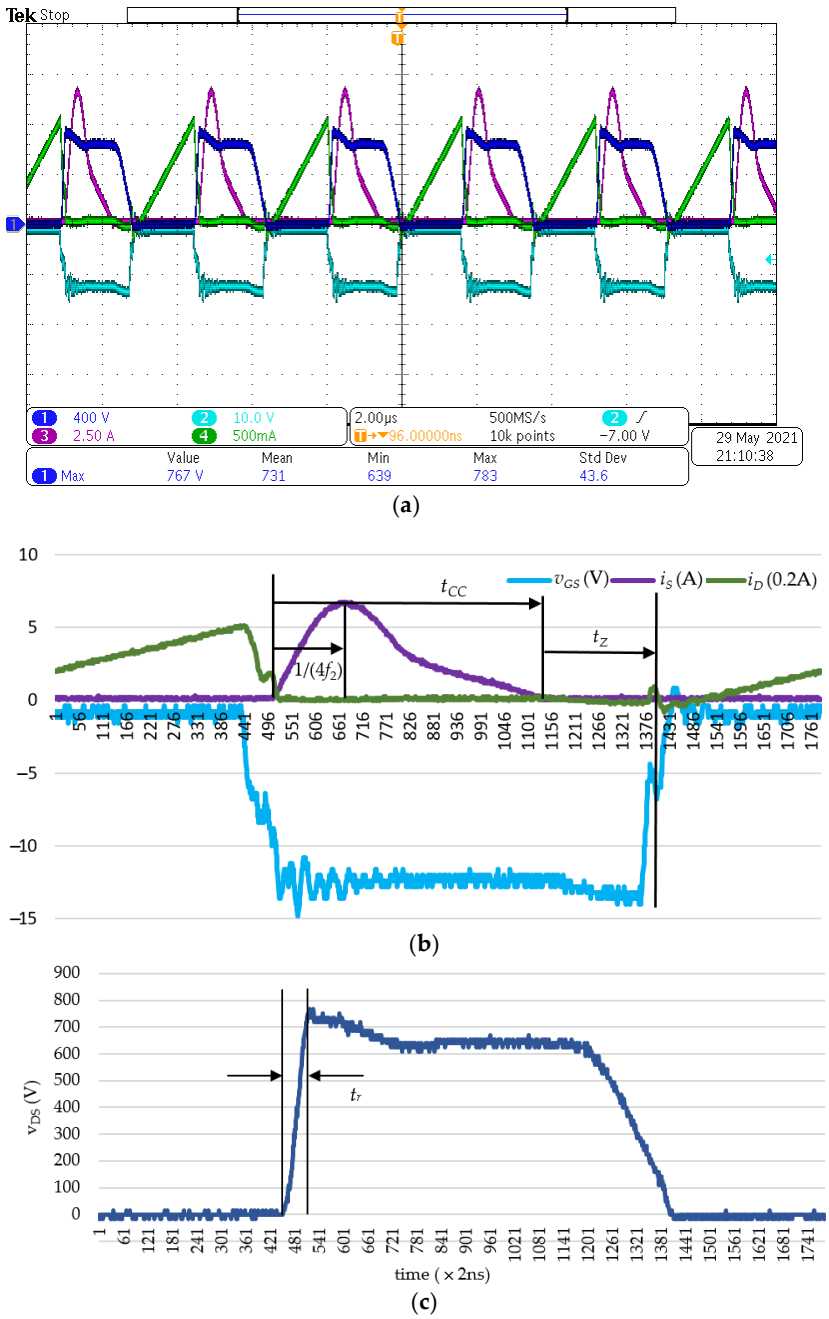

Figure 15. (**a**) Experimentation waveforms at V_{DD} = 300 V, δ = 48%, f_S = 280 kHz (T = 3.57 µs) and R_O = 50 Ohm, (**b**) t_{CC} = 1.25 µs, t_Z = 530 ns, (**c**) t_r = 130 ns.

Many other experiments have been performed to examine the ZCS performance for the flyback converter which are summarized as shown in Figure 16. It is observed from the experiments that the output power increases with the increasing input DC voltage as shown in Figure 16a. The maximum power efficiency occurs at around V_{DD} = 150 V which is equivalent to the AC input voltage 110 V that is commonly adopted in America, Canada, Japan and Taiwan. The maximum power output is at higher AC input voltage which yields higher DC output V_{DD} from the AC/DC converter. It is also observed from the experiments that both the power and power efficiency will be degraded subjected to the snubber resistor quality or precision as shown in Figure 16b, however not much. The result as depicted in Figure 16c shows that the duty cycle is rather linearly decreasing with the increasing switching frequency. In order to adjust the output voltage in the closed loop control of flyback converter, we need to adjust the switching frequency according to Equation (17).

The algorithm is quite simple to implement in the logic ICs or microprocessors due to the linearity of the duty cycle vs. switching frequency. It may be naming the ratio between duty cycle vs. switching frequency as the duty line equation as follows.

$$\delta = \delta_0 - Df_S \tag{51}$$

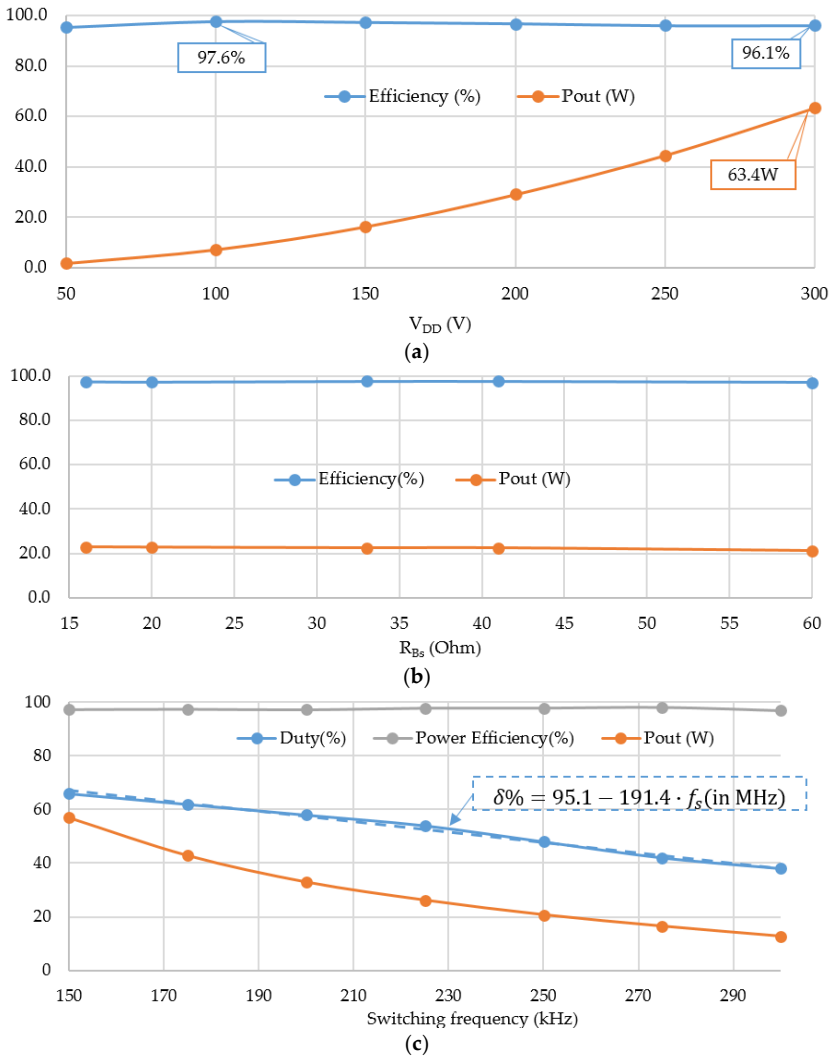

Figure 16. Experiment summaries (**a**) power efficiency versus input voltage V_{DD}, (**b**) output efficiency due to the snubber resistance adjustment and (**c**) the duty cycle versus the switching frequency.

The corresponding D as shown in Figure 16c is 191.4, which implies that for the current circuit parameters does not allow the circuit to be switching in the frequency higher than 500 kHz. The result is in consistent with the f_2 in Table 4. Equation (17) can then be rewritten as follows providing that the efficiency is assumed 100%.

$$\Delta V_O = \frac{-\Delta f_S}{{f_S}^{1/2}}\left(\frac{3}{2}\frac{\delta_0}{f_S} + \frac{1}{2}D\right)\sqrt{\frac{R_O}{2L_P}}V_{DD} \approx -\Delta f_S \frac{DV_O}{2(\delta_0 - Df_S)} \tag{52}$$

Equation (52) indicates that the output voltage is decreasing with the increasing switching frequency, which is in consistent with the output power decreasing as shown in Figure 16c. The circuit allows the designer to adjust the switching frequency and the duty cycle are recommended in variable frequency pulse width modulation (VFPWM) [49]. With the VFPWM, we are able to control both the switching frequency and the duty cycle through simple voltage inputs separately. The DCM with ZCS fulfillment can then be achieved.

5. Analysis and Discussion

The design methodology of the DCM control directly relates to the determination of the switching frequency and the duty. The target is to achieve the best efficiency through the proper selection of transformer and snubber circuit parameters. The low switching loss strategy proposed in this paper can yield a high efficiency in the DCM operation for a conventional flyback converter with high switching frequency using GaN HEMT. Our method is simply achieved by having ZVS with ZCS occurred simultaneously in the instance of switching. The step-by-step design methodology is depicted in Figure 17. In this method we started from studying the flyback converter specifications which include mainly the input voltage (typically 150/300 V), the power density (W/cc), the output power (W) and the output voltage (V). From the specifications, the output load (Ohm), the input voltage, the output voltage and the switching frequency together determines the critical condition for CCM or the BCM. It is then using the transformer turn ratio and input voltage to determine the minimum breakdown voltage for the GaN HEMT as well as the current rating required. After the transistor has been verified in its feasible working range, then ZVS and ZCS are determined from the equations stated in Section 2. According to either the PSpice simulation or experiments, we then determine the redesign of the snubber or the selection of transformers.

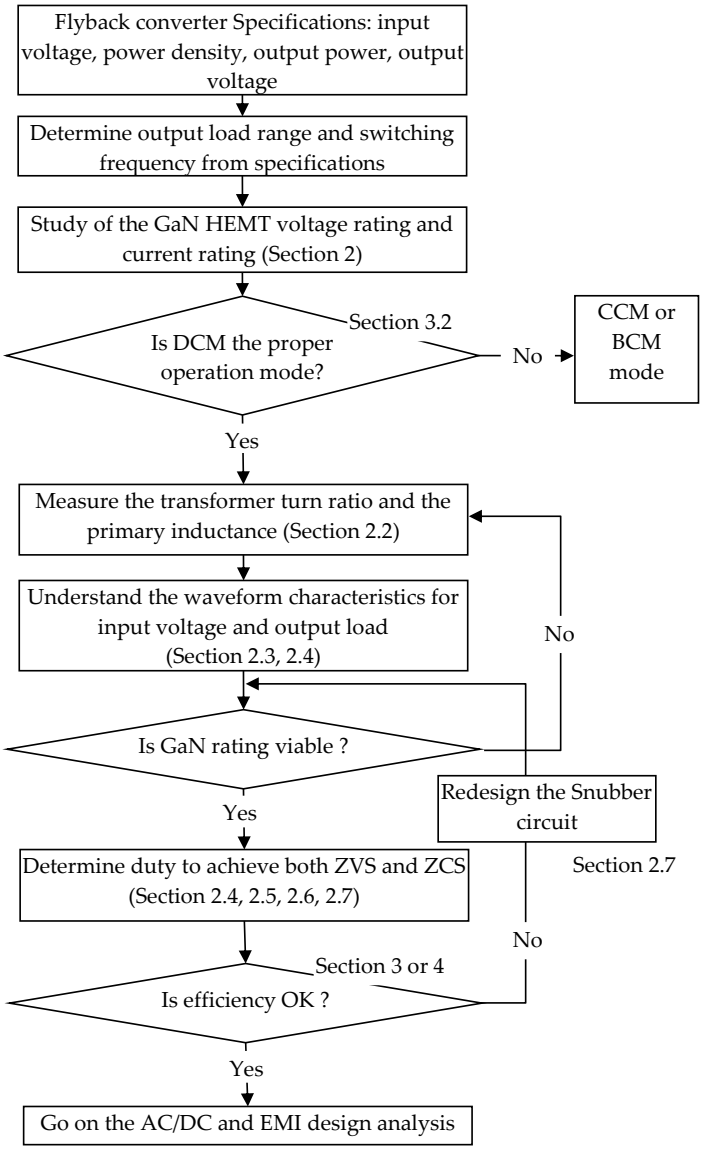

Figure 17. The step-by-step design methodology.

6. Conclusions

The flyback converter can yield higher power efficiency during the DCM than that of the CCM for less than 100 W low power output. The new knowledges that are conveyed in this paper including the DCM resonance mechanism and the relation among switching frequency, duty, ZVS and ZCS. The understanding of the DCM resonance mechanism is the key to fulfill ZVS and ZCS simultaneously and thus the switching loss of the flyback converter can be reduced. This paper provides an insight of the DCM mechanism. The current jumps to its first maximum after the switch turns off and bumps back, later on, to its second maximum. This paper explains the reason why the current bumps back and how that prolongs the current flowing time. The precise calculation of the current flowing time proceeds the drain-source voltage of the switch to swing down toward zero voltage. This paper shows that the drain-source voltage swing on the switch is critical to the ZVS. The condition enabling the ZVS to occur is to increase the turn ratio a of the transformer. In contrast with the quasi-resonant fly back converter wherein it makes use of the parasitic elements to manipulate the inductor voltage partially resemble a resonance action. The DCM resonant behaves as a nature from the current in its secondary winding. The control of the DCM can be implemented by controlling the switching frequency. The duty cycle following the switching frequency change can be adjusted in a linear way achieved by using the VFPWM that the authors have presented before. Nevertheless, the output resistance on the load is an important factor that affects the output voltage. For the heavy load application, the transformer made with small inductance is preferred in order to allow the DCM to occur. This paper demonstrated the particular applications own as high as 97.6% power efficiency. The high-power efficiency for fast charging application may be targeting at the 99% efficiency. This can be accomplished by further redesign the transformer, use the AMR (active MOS rectifier) or ideal diode on the secondary winding to replace the normal FRD (fast recovery diode), and/or integrate the power module together with the gate drive into a SiP (system in chip) packaging. These possibilities to promote the power efficiency to its extreme will be included in our future work.

Author Contributions: Conceptualization, E.-Y.C. and W.-H.C.; methodology, R.K. and C.-C.W.; software, C.-C.W.; validation, C.-Y.L., Y.-L.H. and R.K.; formal analysis, R.K.; resources, Y.-L.H. and R.K.; writing—original draft preparation, W.-H.C.; writing—review and editing, R.K. and C.-C.W.; visualization, C.-Y.L.; supervision, E.-Y.C.; project administration, W.-H.C.; funding acquisition, W.-H.C. and Y.-L.H. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Ministry of Science and Technology, R.O.C, grant number MOST(NSC) 110-2622-8-009-018-SB.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data sharing is not applicable.

Acknowledgments: This work was supported by the Ministry of Science and Technology, R.O.C. The authors also thank You-Chen Weng of the CSD Lab for fabricating the D-Mode MIS-HEMT chips and IMLab graduate students Guo-Bin Wang and Yueh-Tsung Shieh for their help in the experimental setup, also Kun-Chuan Lin andJin-Hsiang Liu from Elite Advanced Laser Corporation for their help on advising on the experimental result.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

Symbol	Abbreviation
L_P	inductance of primary winding
L_{Pm}	magnetization inductance of primary winding
L_{Pl}	leakage inductance of primary winding
L_S	inductance of secondary winding
L_{Sl}	leakage inductance of secondary winding
k	coupling coefficient of transformer
a	turn ratio of transformer
C_m	coupling capacitance of transformer
C_{DS}	drain-source parasitic capacitance of the switch
C_{oss}	output parasitic capacitance of the switch
v_{DS}	drain-source voltage of the switch
C_B	snubber capacitance
t_{CCM}	continuous current mode time
D_S	diode on secondary winding
D_B	diode of the snubber
δ	duty cycle of the switching
ω	natural frequency of response
ξ	damping ratio of response
C_O	output capacitance
R_O	output resistance

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