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Adaptive Impedance-Conditioned Phase-Locked Loop for the VSC Converter Connected to Weak Grid †

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† This paper is an extension of our paper "Analysis of steady-state power transfer capability and dynamic performance of VSC-HVDC with impedance-compensated synchronisation method connected to weak AC grid", here we proposed Adaptive Impedance-Conditioned Phase-Locked Loop.

Abstract: In this paper, an adaptive version of the impedance-conditioned phase-locked loop (IC-PLL), namely the adaptive IC-PLL (AIC-PLL), is proposed. The IC-PLL has recently been proposed to address the issue of synchronisation with a weak AC grid by supplementing the conventional synchronous reference frame phase-locked loop (SRF-PLL) with an additional virtual impedance term. The resulting IC-PLL aims to synchronise the converter to a remote and stronger point in the grid, hence increasing the upper bound on the achievable power transfer achieved by the VSC converter connected to the weak grid. However, the issue of the variable grid strength imposes another challenge in the operation of the IC-PLL. This is because the IC-PLL requires impedance estimation methods to estimate the value of the virtual impedance part. In AIC-PLL, the virtual impedance part is estimated by appending another dynamic loop in the exciting IC-PLL. In this method, an additional closed loop is involved so that the values of the virtual inductance and resistance are internally estimated and adapted. Hence, the VSC converter becomes effectively viable for the case of the grid strength variable, where the estimation of the grid impedance becomes unnecessary. The results show that the converter that relies on AIC-PLL has the ability to transfer power that is approximately equal to the theoretical maximum power while maintaining satisfactory dynamic performance.

Keywords: phase-locked loop (PLL); vector current control; VSC-HVDC; weak grid

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1. Introduction

The integration of renewable energy sources, which are usually located in remote areas, is often realised using high voltage direct current (HVDC) based on voltage sources converter (VSC) technology [1]. In the operation of the VSC converter, the phase angle of the AC grid voltage at the point of common coupling is considered to be critical to ensure correct synchronisation of the connected power converter with the grid. Through synchronisation, only information of the fundamental component is extracted and provided to the converters [2]. This information is typically obtained using the so-called phase-locked loop (PLL). When the PLL is locked, the output signal of the PLL synchronises with the input signal, where both signals oscillate at the same frequency with a particular value of a phase shift [3]. In addition, the phase angle of the grid voltage is utilised to transform the sinusoidally varying AC quantities into quasistationary dq-axis quantities by means of the Park transformation. Hence, three-phase AC currents are transformed into their corresponding active and reactive components that can then be controlled independently using standard PI/PID regulators [4–6]. Therefore, the ability of the PLL to accurately synchronise with the grid and estimate the phase angle of the grid voltage at the point of common coupling directly impacts the performance of the overall closed-loop system, and, in particular, its ability to independently control the exchange of active and reactive power

with the AC grid at the point of common coupling. Hence, if PLL loses synchronisation with the grid, then, as a consequence, the corresponding VSC converter will also lose synchronisation with the AC system to which it is connected [7].

The renewable energy sources are usually integrated into grids with long transmission lines, which leads to a large value of the Thevenin equivalent AC grid impedance, and such a system is called a "weak grid" [8,9]. Typically, the strength of the grid is measured by the short circuit ratio (SCR). According to [10,11], the SCR is the ratio of the short circuit capacity to DC link rated power, and it is mathematically defined as

$$\mathrm{SCR} = \frac{S_{ac}}{P_{dc}} = \frac{U^2}{Z_g P_{dc}}. \tag{1}$$

where S_{ac} is the short circuit capacity of the AC system at the point of common coupling and P_{dc} is the rated DC power of the HVDC link. If the voltage at PCC is assumed to be identical to the base value, and the rated power of the HVDC is used as the base power of the AC system, Equation (1) can be further simplified as

$$\mathrm{SCR} = \frac{U^2}{Z_g P_{dc}} = \frac{U^2}{Z_g \frac{U_{base}^2}{Z_{base}}} = \frac{1}{Z_g(p.u.)} \tag{2}$$

where U_{base} and Z_{base} are the base values of the voltage and impedance, respectively, and $Z_g(p.u.)$ is the value of the impedance in per unit. Based on [10], the strength of the AC system is strong if SCR > 3, $2 <$ SCR < 3 for a weak grid and SCR < 2 for a very weak grid.

Weak grid connections impose challenges on the operation of the VSC-HVDC system. The voltage at the PCC becomes more sensitive to power variations in the case of the weak grid connections; this, in turn, will affect the stability and dynamic performance of the system [12,13]. The high sensitivity to power variations leads to high voltage fluctuations. Therefore, the utilised PLL needs to be sufficiently fast to lock with the variations in the voltage. However, fast PLL, i.e., large bandwidth, leads to high frequency components and noise to propagate through the system and causing system instability [14]. In addition, there is a theoretical limitation for each value of SCR on the maximum power that the VSC-HVDC system can transmit to or from the AC system [10,15]. Another challenge emerges when the converter connected to the weak AC grid, which is the mutual coupling in controlling the active power and voltage. The interactions between the active power control and voltage control increase as the value of the grid impedance increases [16]. Therefore, it is essential to consider the PLL both in terms of the static (steady-state) power transfer and the dynamic performance of the power converter.

Hence, several modifications in the PLL are suggested to deal with this problem. In [17,18], the voltage sensorless technique was proposed. In this method, a virtual flux concept is utilised to synchronise the converter with the grid at the point of synchronisation without any needing for the physical sensor, where PLL uses flux instead of the voltage to generate the angle of the point of synchronisation. However, this technique needs for advanced estimation method for providing the information of the grid impedance. Another approach that is suggested to deal with a weak grid problem is modifying the SRF-PLL by attaching a damping factor term in order to suppress the oscillation that exhibits in the voltage at PCC due to the weak grid connections [19]. It was shown that with a certain value of the damping factor, the system stability is enhanced. However, this approach is limited to a weak grid with a $SCR > 1.83$.

In [20,21], the impedance-conditioned phase-locked loop (IC-PLL) is proposed to address the issue of synchronisation with weak AC grid by supplementing the conventional synchronous reference frame phase-locked loop (SRF-PLL) with additional virtual impedance term. As a result, increasing the upper bound on the achievable power transfer achieved by the VSC converter connected to the weak grid [21]. However, this approach requires for the grid impedance to be estimated accurately so that the virtual impedance

branch compensates the high-value grid impedance. Hence, the VSC converter is synchronised to the point at the infinite bus voltage, where the voltage operates in a relatively robust manner concerning the perturbations that happen in the voltage at PCC. Refs. [22,23] show that the value of the virtual impedance has an impact on the dynamic performance of the system. The system provides the optimal dynamic response when the value of the virtual impedance equal to the value of the grid impedance. The task of grid synchronisation becomes particularly challenging in the cases where the grid impedance is varied, which is the case that IC-PLL needs for adapting the value of the virtual impedance so that the VSC converter maintains the synchronisation with the infinite bus voltage.

In the literature, the approaches that are used to estimate the value of the grid impedance is based on the deliberate creation of a disturbance at the PCC, and the value of impedance is calculated based on the grid response to this distortion. These disturbances can be based on power variation in both active and reactive power at the PCC [24] and a current spike at PCC [25]. However, the accuracy of the estimation depends on the size of the disturbances, which may become challenging in the case of a weak grid system. In addition, these approaches require for additional signal processing method to deal with the influence of the nonlinear loads connected close to PCC.

Therefore, the proposed AIC-PLL has the ability to estimate the value of the grid impedance so that the VSC converter maintains the synchronisation with the infinite bus voltage, without any requirements for the sophisticated methods of the impedance value estimation. Furthermore, this method does not require any source of disturbance, which is essential in the other methods, for the estimation of the accurate value of the grid impedance. Therefore, the VSC converter that uses AIC-PLL has the ability to transfer power equals to maximum theoretical power with a satisfactory dynamic performance in the case of the grid impedance variation.

The paper is organised as follows. In Section 2, we provide a general description of the studied system. In Section 3, we explain the operation limits of the VSC-HVDC system, where the maximum theoretical power and the maximum power that the VSC-HVDC system can transfer are explained. Descriptions about different types of PLL, including the proposed AIC-PLL, are provided in Section 4. A study about stability limits for an AIC-PLL-based converter is provided in Section 5; in this section, a comparison between AIC-PLL and IC-PLL (virtual impedance equals to grid impedance) with the theoretical maximum power is given for a range of grid impedance. In Section 6, dynamic performance studies for AIC-PLL- and IC-PLL-based converters are given considering various parameters. The impact of the AIC-PLL low pass filter on the dynamic performance of the system is described in Section 7. Finally, in Section 8, we provide the conclusion.

2. Overview of the General System Configuration

The studied system is shown in Figure 1. The overall system consists of two main parts: the upper part, which represents the AC network (in this part, R_c and L_c represent the converter resistance and inductance), and R_g and L_g represent the grid resistance and inductance, respectively. The C_f represents the AC capacitor connected to the filter bus. The symbols $\boldsymbol{v}$, $\boldsymbol{u}$ and $\boldsymbol{e}$ represent the voltage vector of the VSC converter, the filter bus and AC source, respectively. V, U and E are their corresponding voltage magnitudes. The AC source is considered as the voltage reference, and it is a constant-frequency stiff voltage source. The phase angle of $\boldsymbol{v}$, $\boldsymbol{u}$ are θ_v and θ_u, respectively. The symbols P and Q are the active and reactive powers from the VSC to the AC system. The quantity i_c is the current vector of the phase reactor, and i_g is the current vector to the AC source.

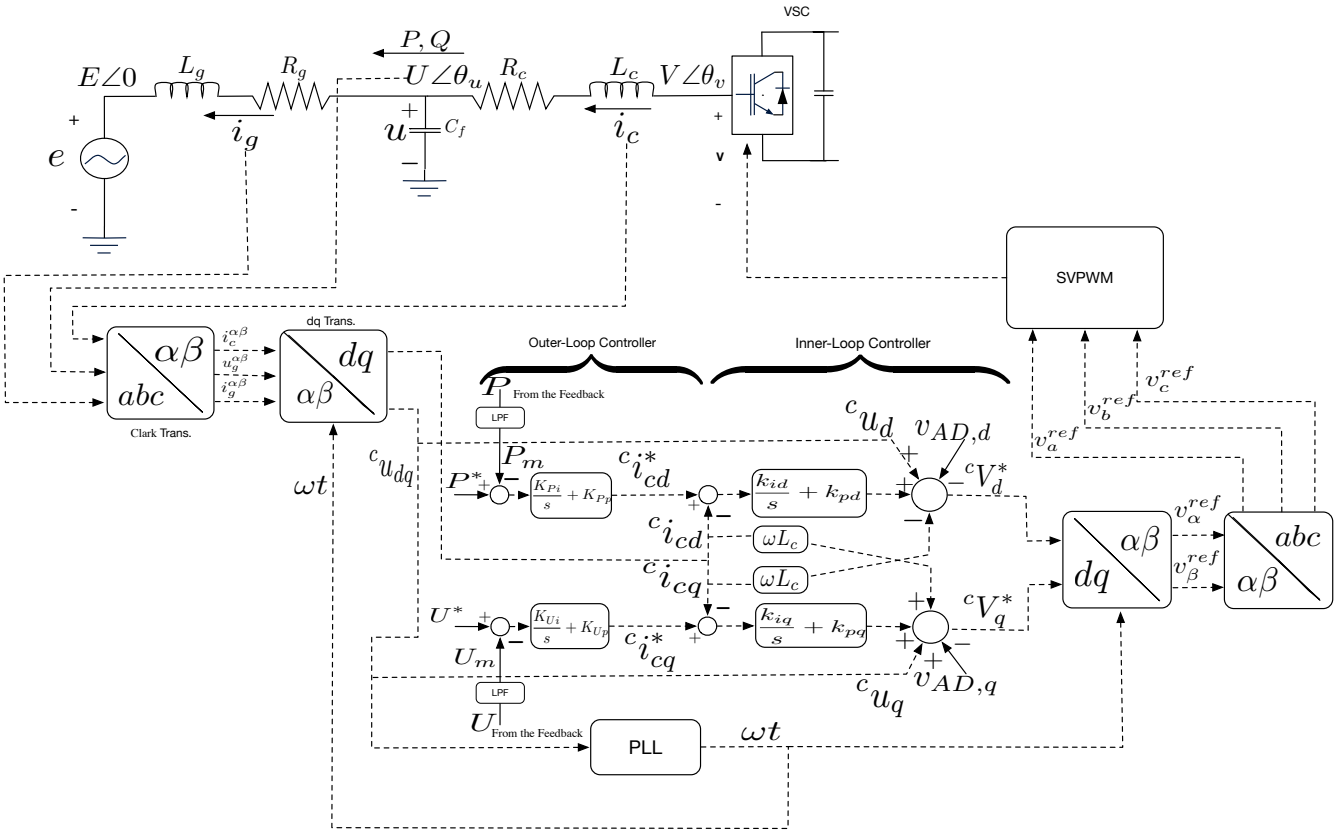

Figure 1. Closed Loop for VSC-HVDC system.

In this system, the active power and voltage magnitude are controlled at the point of common coupling through outer loop controller, by which the desired value of the converter current i_c^* is manipulated. The presuperscript c for any quantity refers to the converter side for that quantity, and postsubscripts d and q refer to d and q components.

3. Operation Limits of the VSC-HVDC System

The operation limit is defined in terms of the maximum power that the VSC converter can transfer in steady-state while maintaining the stability of the system. For a general power system consisting of two voltage sources given by U and E, interconnected via impedance $Z_g = R_g + jX_g$, as shown in Figure 2, there is a theoretical maximum power that is considered the theoretical operation limit that cannot be exceeded [26]. This theoretical maximum power is given by

$$\overline{P}_{max}(p.u.) = \frac{U \cdot E}{|Z_g|} \pm U^2 \frac{R_g}{|Z_g|^2}, \tag{3}$$

where all the values of the voltages and the AC circuit parameters are in per-unit quantities, and the sign '+' is for the inverter operation and '-' is for the rectifier operation.

However, the VSC-HVDC system may not be able to transfer power equals to the theoretical maximum power $\overline{P}_{max}$, which is due to the presence of the feedback element, where the dynamic of this element may affect on the stability of the system. Therefore, in the case of the VSC-HVDC system shown in Figure 1, P_{max} represents the maximum power that is transferred between the voltage u at PCC and the voltage e at the infinite bus and $P_{max} \leq \overline{P}_{max}$.

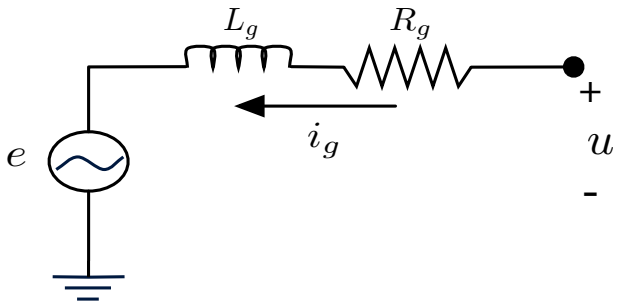

Figure 2. Simplified AC circuit model.

4. Grid Synchronisation Techniques for Converter Connected to Weak Grid

In the following subsections, two types of grid synchronisation methods are presented. The first one is IC-PLL, which is presented in general. The second one is the proposed AIC-PLL, where this method is described in detail.

4.1. Impedance-Conditioned PLL (IC-PLL)

In this section, an impedance-conditioned PLL (IC-PLL)-based system is considered. In this technique, the converter is not synchronised to the voltage at the point of common coupling (PCC); it is instead synchronised to the virtual remote point in the stiff grid. Hence, this provides better synchronisation (as a result, better stability), as the converter is synchronised to a virtual point near to the infinite bus so that the PLL receives a signal with less fluctuation than the signal that is received by PLL in the case of synchronising to the weak grid point [21]. The location of the virtual point depends on the value of the virtual impedance. When this value increases, the virtual point shifts from PCC to infinite bus.

The IC-PLL consists of SRF-PLL, which is the upper part in Figure 3, and the virtual impedance as indicated in the lower part in the figure. In the IC-PLL, the dq components of the voltage at the virtual point is obtained by subtracting the dq components of the voltage u at PCC from the voltage drop across the virtual impedance. The virtual impedance can be defined as

$$Z_g^v = R_g^v + j\omega_{PLL} L_g^v,$$

and the virtual voltage, which is indicated in Figure 3 by its dq components u_d^v u_q^v, can be defined as

$$\begin{aligned} u_d^v &= {}^c u_d - {}^c i_{gd} R_g^v + \omega_{PLL} L_g^{vc} i_{gq}, \\ u_q^v &= {}^c u_q - {}^c i_{gq} R_g^v - \omega_{PLL} L_g^{vc} i_{gd}. \end{aligned} \tag{4}$$

where the additional inputs to the PLL is the grid side current i_g in the dq frame [20],

The mathematical model of the IC-PLL is defined as

$$\frac{d\theta_{PLL}}{dt} = \omega_b K_{pPLL} tan^{-1} \frac{u_{qf}^v}{u_{df}^v} + \omega_b K_{iPLL} \gamma_{PLL}, \tag{5}$$

where $\gamma_{PLL} = \int_0^t tan^{-1} \frac{u_{qf}^v}{u_{df}^v} d\tau$,

θ_{PLL} is the phase angle deviation between the PLL orientation and the grid voltage.

The mathematical model of the low pass filter of the IC-PLL is defined as in Equation (6).

$$\begin{aligned} \frac{du_{df}^v}{dt} &= -\omega_{FLPLL} u_{df}^v + \omega_{FLPLL} u_d^v, \\ \frac{du_{qf}^v}{dt} &= -\omega_{FLPLL} u_{qf}^v + \omega_{FLPLL} u_q^v. \end{aligned} \tag{6}$$

where $\omega_{FL,PLL}$ is the angular frequency of the PLL low pass filter.

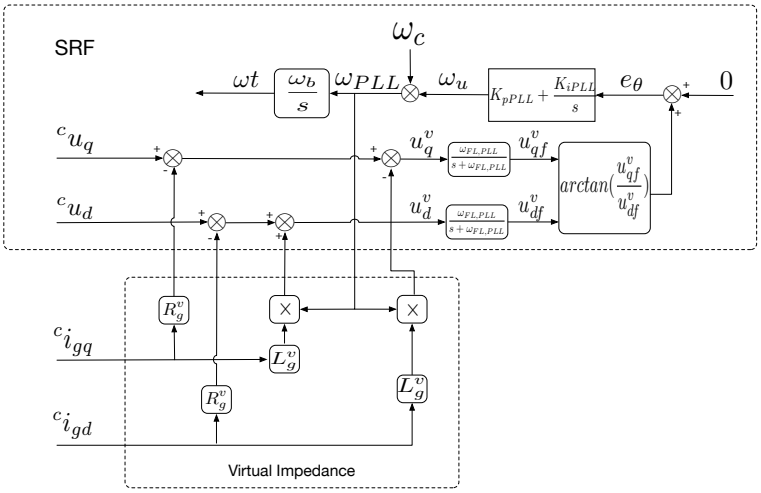

Figure 3. Block diagram of the impedance-conditioned PLL.

4.2. Adaptive Impedance-Conditioned PLL (AIC-PLL)

The exiting IC-PLL is modified so that another closed loop is included in order to adapt the value of the virtual resistance and inductance of the virtual impedance part. As it is shown in Figure 4, the value of θ_{PLL} is fed into two compensators $H_L(s)$ and $H_R(s)$, in order to generate the virtual inductance and resistance values $\hat{L_v}$ and $\hat{R_v}$, respectively. To understand how the AIC-PLL functions in terms of the phase angles of the voltages, the block diagram in Figure 4 is simplified to be represented as in Figure 5.

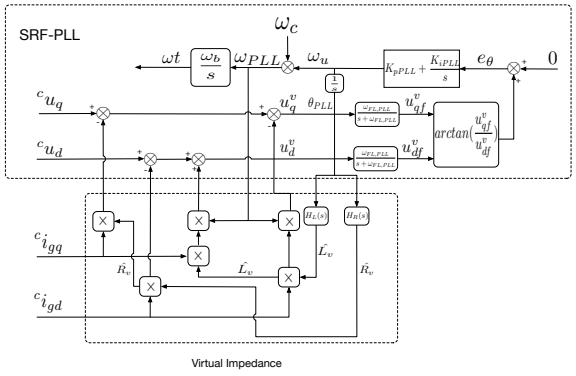

Figure 4. Schematic diagram of the AIC-PLL system.

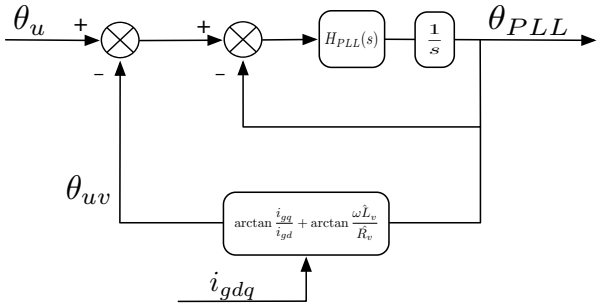

Figure 5. Simplified model of the AIC-PLL.

In Figure 5, two feedback closed loops simplify the AIC-PLL in Figure 4, where:

- The inner loop represents the linearised version of the conventional SRF-PLL, in which the transfer function $H_{PLL}(s) \simeq H_{FL,PLL}(s) \cdot H_C(s)$, where $H_{FL,PLL}(s)$ and $H_C(s)$ are the transfer functions of the PLL low pass filter and PLL compensator, respectively, providing that the angle $arctan(\frac{u_{qf}^v}{u_{df}^v}) \simeq 0$.
- The outer loop depicts the virtual impedance part, where $\hat{L}_v = \theta_{PLL} \cdot H_L(s)$ and $\hat{R}_v = \theta_{PLL} \cdot H_R(s)$.
- The value of θ_{uv} is the phase angle of the virtual voltage, which is the voltage across the virtual impedance.

In the outer loop, the value of the $\theta_{uv} \longrightarrow \theta_u$ through manipulating the values of $\hat{L}_v$ and $\hat{R}_v$ where $\hat{L}_v \longrightarrow L_g$, $\hat{R}_v \longrightarrow R_g$. The angle $(\theta_u - \theta_{uv})$ is the phase angle of the voltage at the point of synchronisation, which is $(\theta_u - \theta_{uv} = 0)$ when the converter is synchronised to the infinite bus voltage. By the inner loop, which represents the traditional SRF-PLL, the estimated angle value θ_{PLL} converges to the point of synchronisation angle, where $\theta_{PLL} \longrightarrow (\theta_u - \theta_{uv})$. As a result of this and in the steady-state, the VSC converter is synchronised to the infinite bus voltage, where $\theta_{uv} = \theta_u$ and $\theta_{PLL} = 0$. In order to demonstrate how the voltages and currents are manipulated in the AIC-PLL, the vector diagram is plotted in Figure 6.

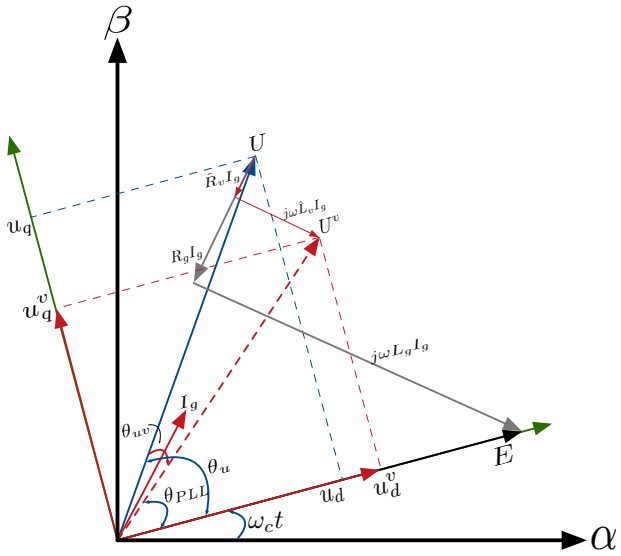

Figure 6. Vector diagram of the AIC-PLL.

In Figure 6, the symbol U^v is the magnitude of the voltage u^v across the virtual impedance with its phase angle θ_{uv}, and this angle is measured with respect to the voltage u at PCC. The voltage u^v is aligned with the voltage u when the value of the virtual impedance is equal to zero ($\hat{R}_v = 0$, $\hat{L}_v = 0$). In this case, the value of the angle $\theta_{uv} = 0$, i.e., the converter is synchronised to the voltage at PCC. Hence, the value of $\theta_{PLL} = \theta_u$ which is fed into compensators $H_L(s)$ and $H_R(s)$ to generate $\hat{L}_v$ and $\hat{R}_v$, respectively. As these values increase the voltage u_v shifts away from voltage u toward voltage E (as shown in Figure 6), and as result of this, $\theta_{uv} \to \theta_u$ and $\theta_{PLL} \to 0$.

The modelling of the VSC-HVDC system utilises AIC-PLL is the same as that one utilises IC-PLL with considering the following model of the AIC-PLL

$$u_d^v = {}^c u_d - {}^c i_{gd}\hat{R}_v + \omega_{PLL}\hat{L_v}{}^c i_{gq}, \tag{7}$$

$$u_q^v = {}^c u_q - {}^c i_{gq}\hat{R}_v - \omega_{PLL}\hat{L_v}{}^c i_{gd}, \tag{8}$$

where

$\hat{L_v} = \pm(H_L(s) \cdot \theta_{PLL})$,
$\hat{R_v} = \pm(H_R(s) \cdot \theta_{PLL})$.

$H_L(s) = \frac{K_{Lvi}}{s} + K_{Lvp}$, $H_R(s) = \frac{K_{Rvi}}{s} + K_{Rvp}$.

where the sign (+) is for the inverter operation and (-) is for the rectifier operation. The reason for that is the voltage u at the PCC leads the voltage E at the infinite bus in the case of the inverter operation, i.e. the phase angle θ_{PLL} is positive, while in the case of the rectifier operation, the voltage u lags the voltage E, which results in the phase angle θ_{PLL} to be negative.

5. Stability Limits of AIC-PLL-Based VSC Converter

In order to study the stability of the system for various types of PLLs, the operating points of the system are obtained first. The operating points are calculated by solving $\mathbf{f}(\mathbf{x_0}, \mathbf{u_0}) = \mathbf{0}$ for $\mathbf{x_0}$ numerically, where the $\mathbf{f}(\mathbf{x}, \mathbf{u})$ is the set of the nonlinear Equation (A16) that are provided in the Appendix B. The maximum theoretical power that is calculated by Equation (3) for a certain value of the grid impedance is approximately equal to the maximum power by which the nonlinear equations return a real solution. However, the system may not be able to operate according to the calculated operating points, i.e., these operating points are unstable. The operating points $\mathbf{x_0}$ are considered stable if all the eigenvalues of the matrix A, which is provided in the Appendix C, has negative real parts, where this method is referred as the first method of Lyapunov [27].

The results of the small signal stability analysis for different types of PLLs are shown in Figure 7, where $U^* = 1$ p.u. for $Z_g = [0.1, 2]$ p.u. and $\omega_{FL,PLL} = 400$ rad/s.

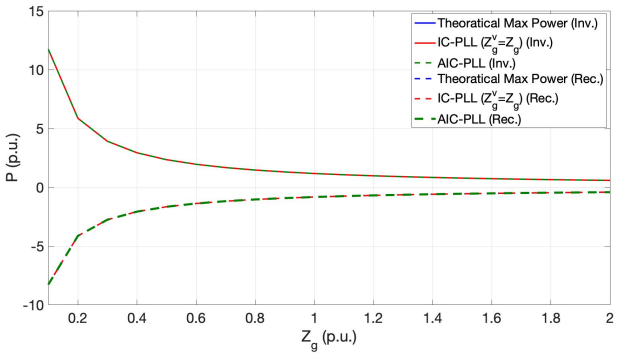

Figure 7. Steady-state power transfer stability limits of VSC-HVDC system for different types of PLL.

Figure 7 shows the maximum transferred power in per unit for two VSC converters utilising two types of PLLs, IC-PLL with $Z_g^v = Z_g$ and AIC-PLL, for a range of values of grid impedance Z_g and for the inverter and rectifier operations. It can be observed that the values of the maximum active power at which the system maintains stable for both types of the IC-PLL- and AIC-PLL-based converters are equal, and they are approximately equal to the theoretical maximum power. Therefore, the converter that utilises AIC-PLL is capable of reaching the maximum theoretical power transfer in the same way that the IC-PLL does, in spite the fact that the AIC-PLL does not require any information about the value of the grid impedance. Moreover, it can be concluded from this result that the AIC-PLL is able to imitate the IC-PLL with $Z_g^v = Z_g$ in terms of the power transfer capability, as the converter that utilises AIC-PLL is also synchronised to the infinite bus voltage E. Therefore, the AIC-PLL possibly replaces the IC-PLL in the case that the maximum power transfer is demanded, and the estimation of the value of the grid impedance is challenging, in particular, the grid strength changes.

6. Dynamic Performance Study for AIC-PLL-Based VSC Converter

In this section, the dynamic performance of the AIC-PLL-based converter is investigated for different points in the grid strength. The performance of the AIC-PLL-based system is studied by examining the dynamic response of the system to the changing in the value of the grid impedance and the value of the active power. For each point of the grid impedance, an experiment is conducted, and two step changes are applied. The

first step is on the grid impedance, and this is to simulate the variation that may occur in the grid impedance value in the real system, and how the AIC-PLL has the ability to recover the changing in this value. The second step change is for the active power, and this is to examine the effectiveness of the AIC-PLL-based converter in terms of dealing with variation in active power. In order to demonstrate the effectiveness of the proposed method, the time-domain response of the active power for the AIC-PLL-based converter is compared with two cases of the IC-PLL-based converters. The first one is the IC-PLL with a constant value of the virtual impedance, i.e., the value of Z_g^v does not change according to the changing in the grid impedance. The second case is when the value of the Z_g^v is changing according to the changing in the grid impedance; hence, the relation $Z_g^v = Z_g$ is maintained during the operation of the system.

The first experiment is when the value of the grid impedance changes from $Z_g = 1 \rightarrow 1.1$ p.u. in the inverter operation; then, another step change in active power is applied which is $P^* = 0.9 \rightarrow 1$ p.u. Figures 8–10 show the responses of active power and θ_{PLL}, respectively.

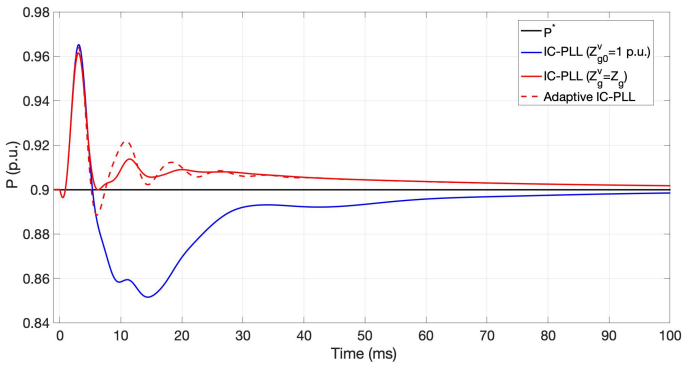

Figure 8. Time-domain response of the active power for different types of PLLs for step change in $Z_g = 1 \rightarrow 1.1$ p.u. and for $\omega_{FL,PLL} = 400$ rad/s (inverter operation).

Figure 8 shows the result of the time-domain response of the active power for different converters utilise different types of PLLs. It is clear from the figure the converter that utilises the IC-PLL with $Z_g^v = Z_g$ has the optimal response as it shows less oscillation than the other two approaches with less settling time. However, for the system that relays on the IC-PLL without updating the value of the virtual impedance (IC-PLL $Z_{g0}^v = 1$ p.u.), the result shows that the time-domain response exhibits the highest oscillatory response. In the case that the system uses the proposed method AIC-PLL, the result shows that the time-domain response of the active power suffers far less oscillation than the IC-PLL with $Z_g^v = 1$ p.u., and it has slightly more oscillation amplitude than the case of IC-PLL with $Z_g^v = Z_g$. Therefore, from this result, it can be concluded that the proposed AIC-PLL has the ability to recover the changing that occurs in the grid impedance.

Figure 9 shows the time-domain response of the active power for the applied step change in the active power for the VSC converters with different types of PLLs for the same above experiment at a different time where the value of the grid impedance $Z_g = 1.1$ p.u.

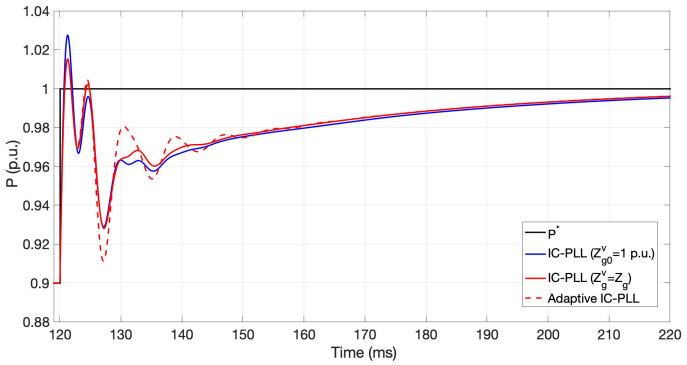

Figure 9. Time-domain response of the active power for different types of PLLs for step change in active power and for $\omega_{FL,PLL} = 400$ rad/s, $Z_g = 1.1$ p.u. (inverter operation).

It can be seen from Figure 9 that the dynamic response for the case of IC-PLL with ($Z_g^v = 1$) exhibits higher overshoot than the other two cases. However, for the case of the converter that utilises AIC-PLL, the results in Figure 9 show that the response exhibits relatively higher oscillation amplitude than the other two cases. It can be concluded from the results in Figures 8 and 9 that the proposed AIC-PLL has the ability to deliver the maximum power with satisfactory dynamic performance.

Figure 10 shows the response of the phase angle θ_{PLL} that is generated by different types of PLLs. In this figure, two y-axes for the phase angle θ_{PLL} are included; the left y-axis is for the IC-PLL ($Z_g^v = 1$ p.u.), as it generates a larger phase angle scale than the other two cases. For the other two cases of the PLLs, the right y-axis is devoted. It is clear from the figure that the time-domain response that is generated by IC-PLL ($Z_g^v = 1$ p.u.) exhibits higher oscillatory with higher settling time than the other two cases. In addition, the value of θ_{PLL} in the case of IC-PLL ($Z_g^v = 1$ p.u.) does not converge to zero. However, the result shows that the response of the θ_{PLL} for the IC-PLL with ($Z_g^v = Z_g$) has more oscillatory than the case of AIC-PLL. This is because in the second case, another closed loop is involved in the AIC-PLL (Figure 4) where the θ_{PLL} is considered as the control signal in this loop, and this is not the case for IC-PLL.

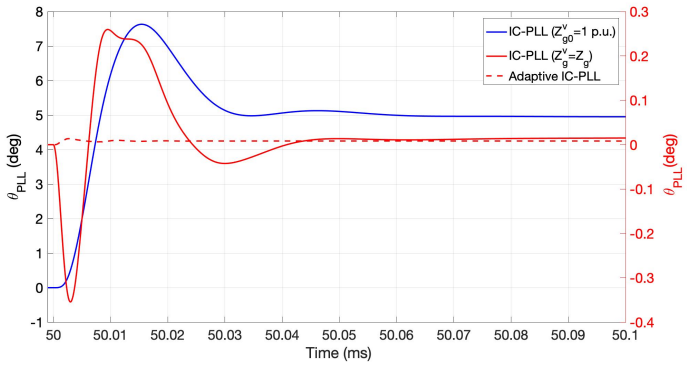

Figure 10. Time-domain response of the θ_{PLL} for different types of PLLs for step change in $Z_g = 1 \rightarrow 1.1$ p.u. and for $\omega_{FL,PLL} = 400$ rad/s (inverter operation).

The experiment is reconducted for the different step change where the value of the grid impedance change is $Z_g = 1.7 \rightarrow 2$ p.u., and the results are provided in Figures 11–13.

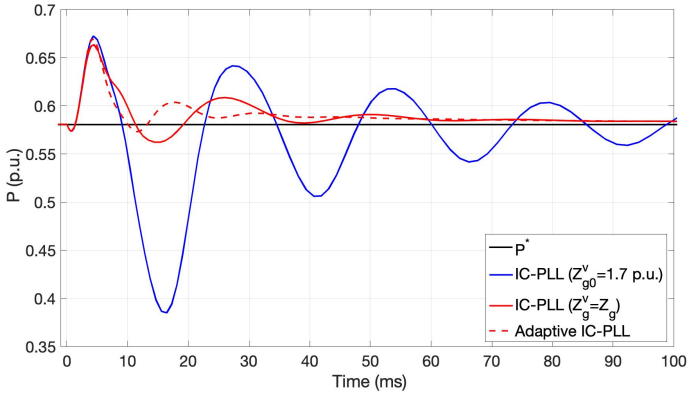

Figure 11. Time-domain response of the active power for different types of PLLs for step change in $Z_g = 1.7 \rightarrow 2$ p.u. and for $\omega_{FL,PLL} = 400$ rad/s (inverter operation).

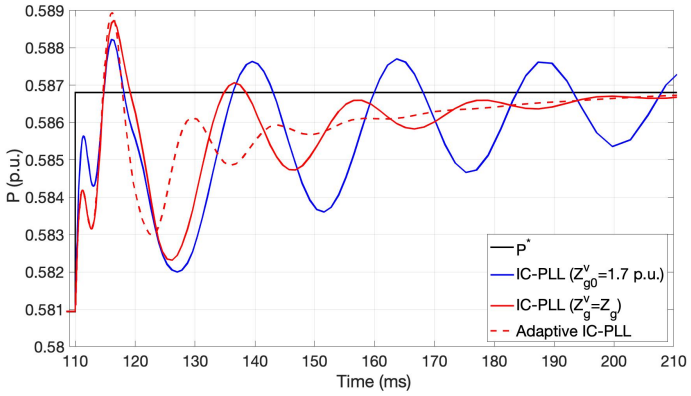

Figure 12. Time-domain response of the active power for different types of PLLs for step change in active power and for $\omega_{FL,PLL} = 400$ rad/s, $Z_g = 2$ p.u. (inverter operation).

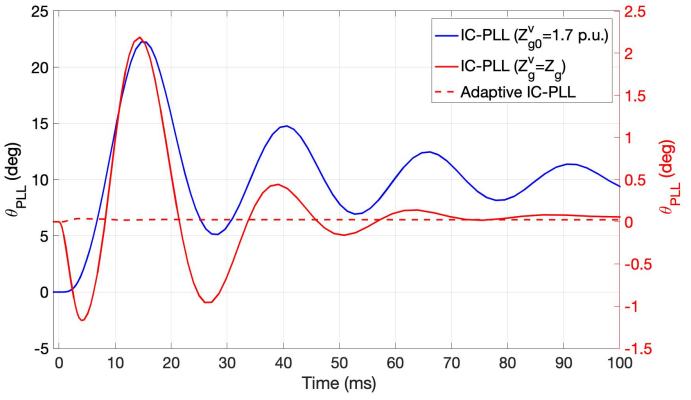

Figure 13. Time-domain response of the θ_{PLL} for different types of PLLs for step change in $Z_g = 1.7 \rightarrow 2$ p.u. and for $\omega_{FL,PLL} = 400$ rad/s (inverter operation).

Figures 11 and 12 show the response of the active power for the step change in the grid impedance ($Z_g = 1.7 \rightarrow 2$ p.u.), and the step change in the value of the active power, respectively. It can be observed that the responses of the active power for the cases of IC-PLL with ($Z_g^v = Z_g$) and the AIC-PLL have far better responses than the case of IC-PLL with ($Z_g^v = 1.7$ p.u.), as the first two cases provide lower oscillatory and settling time than the second case. Figures 11 and 12 also show that the response of the active power in the case of AIC-PLL is slightly better than the case of IC-PLL with ($Z_g^v = Z_g$), as the former case provides less oscillatory and settling time than the latter case. Therefore, it can be concluded that in the case of the weak grid, the converter that utilises AIC-PLL has the

ability to replace the ideal IC-PLL in the case of the grid variation where the estimation of the grid is complicated. Figure 13 is the time domain response for the produced angle of the three types of PLL.

From the result in Figure 13, it can be concluded that the response of the phase angles for different types of PLLs have the same indication as for the result in Figure 10. In addition, By comparing Figures 10 and 13, it is clear that the dynamic response of the angle in the case of IC-PLL with ($Z_g^v = Z_g$) has a higher oscillatory amplitude in the case of the second experiment than the first experiment. It reaches 2 degrees for the second experiment while it reaches about 0.5 degree in the first case, which is due to the larger value of the grid impedance in the second case. The dynamic response of the angle θ_{PLL} has an impact on the dynamic response of the active power, and the larger the value of the angle, the higher impact on the response of the active power. As a result of this, the response of the active power in the case of the AIC-PLL is relatively better than the case of the IC-PLL ($Z_g^v = Z_g$) for the larger value of the grid impedance, which is evident in Figures 11 and 12.

For further validation and reliability of the proposed AIC-PLL, experiments for different values of operating points and different values of the changing in the value of the grid impedance are conducted and the values of the sum of square of error (SSE) for the active power tracking are calculated. Two different operating points are chosen, 50% and 100% of the maximum transferred power of different values of the grid impedance. A step change in the active power is applied which is 1% of the selected operating point. Other experiments are also conducted, where the value of the active power is the maximum and the step change in the grid impedance is applied. Different step change percentages are applied and they depend on the value of the grid impedance, the larger the value of the grid impedance the smaller the value of the step change. The results of this experiment are presented in Figures 14, 16 and 18 for the inverter operation and Figures 15, 17 and 19 for the rectifier operation.

In Figures 14–17, bar charts represent the values of the SSE. A line graph represents the relative errors between the value of SSE of IC-PLL and SSE of AIC-PLL. It is clear from the results that both methods are approximate equals in terms of the dynamic responses, which indicates by the inconsiderable value of the relative error. In the case of the inverter operation, it can be concluded from the results in Figures 14 and 16 that the dynamic response of the IC-PLL-based converter is better than the AIC-PLL-based one for the strong grid. This difference in the dynamic response is reduced as the value of the grid impedance increases to become positive for the value of the $Z_g \geq 1.8$ p.u. However, in the case of the rectifier operation, the results in Figures 15 and 17 show that the converter that relies on the AIC-PLL provides a better dynamic response than the case of the IC-PLL-based converter for the whole range of the grid impedance. This is indicated by the value of the relative error, which is positive.

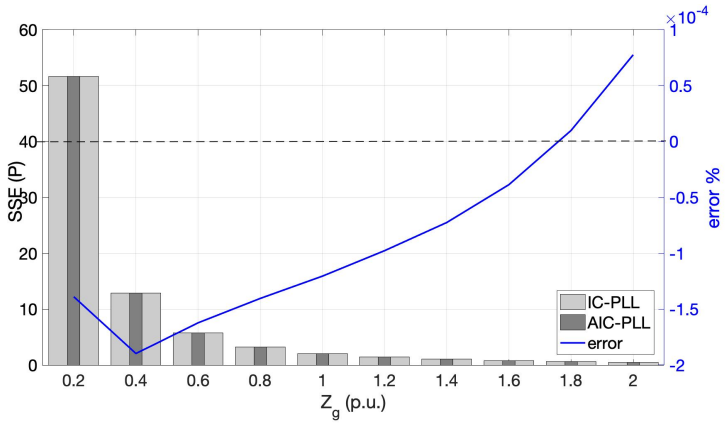

Figure 14. SSE for the active power tracking for the IC-PLL- and AIC-PLL-based system for half value of the maximum power (inverter operation).

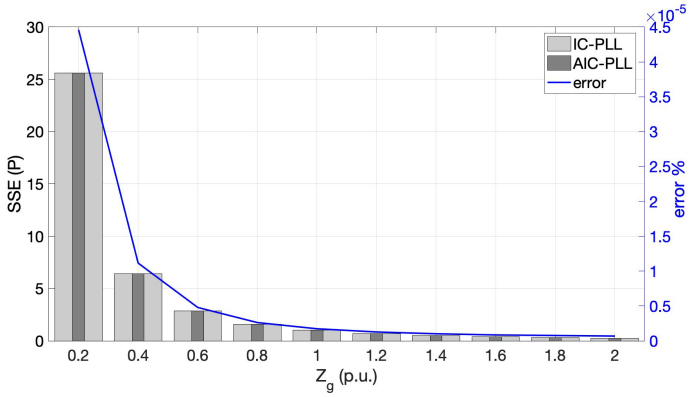

Figure 15. SSE for the active power tracking for the IC-PLL- and AIC-PLL-based system for half value of the maximum power (rectifier operation).

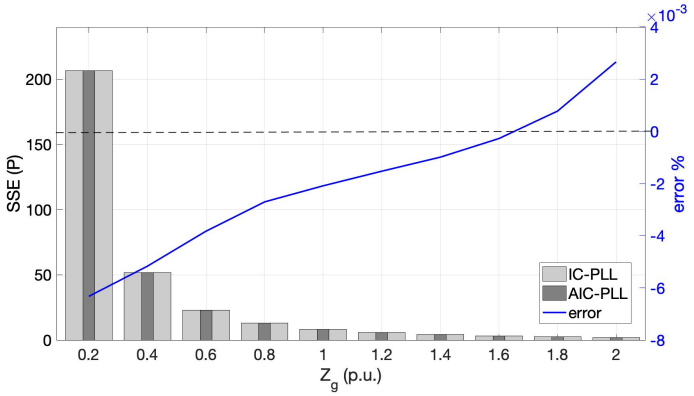

Figure 16. SSE for the active power tracking for the IC-PLL- and AIC-PLL-based system for the maximum power (inverter operation).

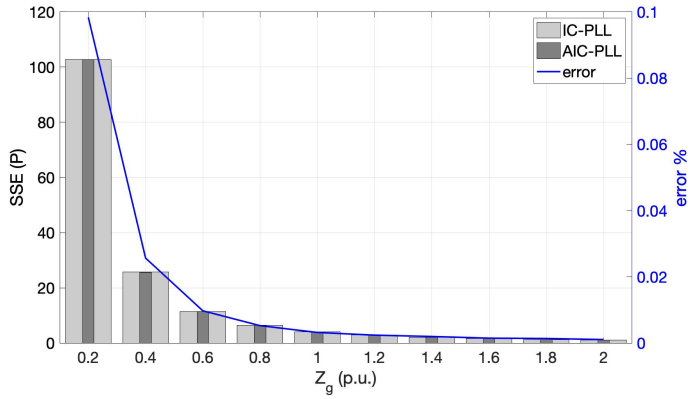

Figure 17. SSE for the active power tracking for the IC-PLL- and AIC-PLL-based system for the maximum power (rectifier operation).

Figures 18 and 19 represent the results of the value of SSE for both types of PLLs-based converters when the value of the grid impedance is changing for the inverter and rectifier operations, respectively. The values of these changes are $\Delta Z_g = [0.5\ 0.5\ 0.3\ 0.3\ 0.3\ 0.3\ 0.25\ 0.25\ 0.2\ 0.2] \cdot Z_g$, where $Z_g = [0.2\ 0.4\ 0.6\ 0.8\ 1\ 1.2\ 1.4\ 1.6\ 1.8\ 2]$ p.u. The value of the relative errors are also presented as a line graph in order to show the difference between the SSE values of the IC-PLL and AIC-PLL for the range of the grid impedance.

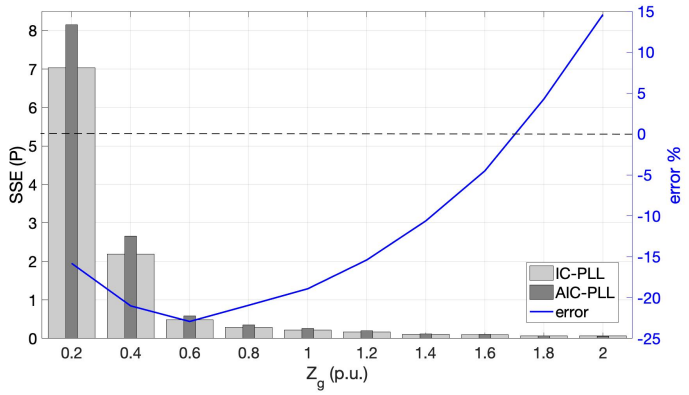

Figure 18. SSE for the active power tracking for the IC-PLL- and AIC-PLL-based system for different change in the values of the grid impedance (inverter operation).

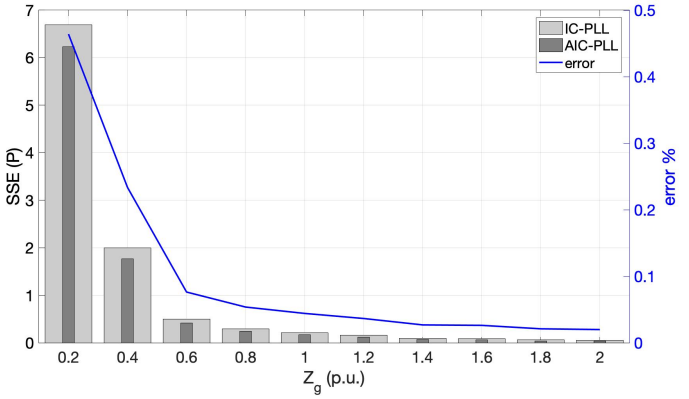

Figure 19. SSE for the active power tracking for the IC-PLL- and AIC-PLL-based system for different change in the values of the grid impedance (rectifier operation).

In the case of the inverter operation, Figure 18 shows that the values of SSE for the IC-PLL-based converter is less than the value of SSE for the case of the AIC-PLL-based converter for $Z_g \leq 1.6$ p.u., which is indicated by the value of the error. The results also show that the error is positive for $Z_g \geq 1.8$ p.u., which indicates that the proposed method has the ability to provide better dynamic performance as the value of the grid impedance increases. In the case of the rectifier operation, Figure 19 shows that the converter that utilises AIC-PLL has the ability to provide better dynamic performance than the case of the system that uses IC-PLL for the whole range of the grid impedance. This is clear from the relative error line graph, which is positive for the whole range of the grid impedance value.

7. The Impact of Changing the Value of PLL Bandwidth on the AIC-PLL Dynamic Performance

In this section, the effect of changing the value of the PLL bandwidth $\omega_{FL,PLL}$, which is related to the PLL compensator bandwidth, on the dynamic performance of the converter is considered. The compensator bandwidth is 55% of the bandwidth of the PLL low pass filter [21]. Therefore, when the value of the $\omega_{FL,PLL}$ changes, the controller parameters change accordingly. In order to understand how the impact of changing the value of $\omega_{FL,PLL}$ on the dynamic performance of the system, the root locus of the closed-loop system's poles in the s-domain is examined by sweeping the $\omega_{FL,PLL} = 50 \rightarrow 2000$ rad/s, and the results are plotted in Figure 20. The participation matrix are then calculated, and the states that have the highest participation factors to the plotted eigenvalues are revealed.

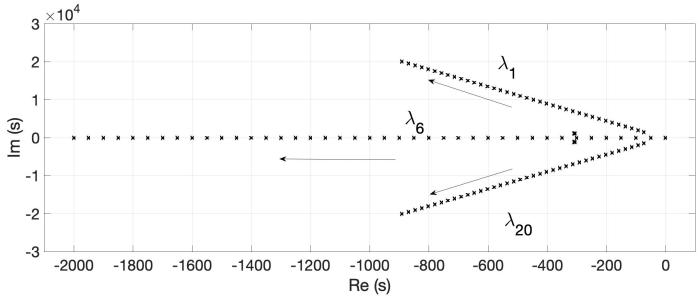

Figure 20. Loci of the closed-loop system poles for the range of $\omega_{FL,PLL} = 50 \rightarrow 2000$ rad/s.

In Figure 20, the only eigenvalues $\lambda_{1,20,6}$ are included, since they have the highest rates of change in their positions than other eigenvalues. From the participation matrix (the participation matrix are provided in Appendix D), these eigenvalues have the highest participation factors to the states that are related to the PLL. These states are the phase angle θ_{PLL}, the augmented state of the PLL's PI controller γ_{pll} and the virtual voltage $u^v_{d,q}$. It is clear from the result that all the positions of the eigenvalues are shifted towards the left as the value of the PLL bandwidth increases. This indicates that for the case of the AIC-PLL the value of the PLL bandwidth does not have an impact on the stability and the dynamic performance of the system. This is because the value of θ_{PLL} is minimal, which is due to the including of the estimation closed-loop. Therefore, this will not have an obvious impact on the dynamic performance of the active power. In order to understand this effect, the time-domain responses of the active power and the phase angle θ_{PLL} for different values of $\omega_{FL,PLL} = 100, 2000$ rad/s are plotted in Figures 21 and 22,

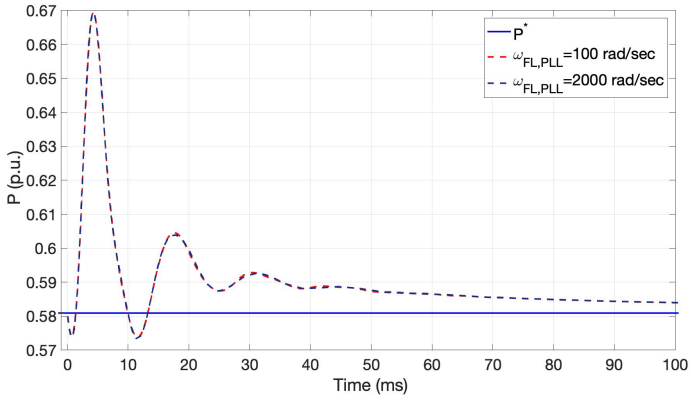

Figure 21. Time domain response of the active power for AIC-PLL for step change in $Z_g = 1.7 \rightarrow 2$ p.u. and for different values of the $\omega_{FL,PLL}$.

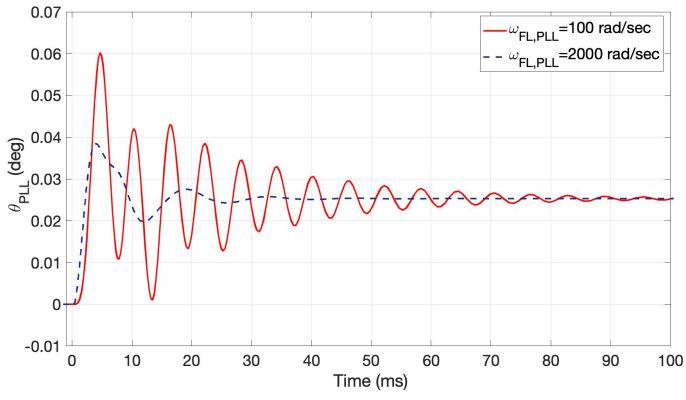

Figure 22. Time domain response of the θ_{PLL} for AIC-PLL for step change in $Z_g = 1.7 \rightarrow 2$ p.u. and for different values of the $\omega_{FL,PLL}$.

It is clear from Figure 21 that the dynamic response of the active power for the converter that utilises AIC-PLL with different values of $\omega_{FL,PLL}$ are approximately identical, which indicates the fact that changing the value of PLL bandwidth does not have any impact on the response of the active power. Figure 22 shows the time-domain response of the phase angle θ_{PLL} for different value of $\omega_{FL,PLL}$, and it is clear that as the value of the bandwidth increases the θ_{PLL} has a better response in terms of the oscillatory and the settling time. This is due to the increase in the value of the PI compensator parameters, which in turn, increases the speed of the PI controller. In addition, the result in Figure 22 shows that the range of the variation is inconsiderable to have an impact on the response of the active power.

8. Conclusions

In this paper, an adaptive impedance-conditioned phase-locked loop (AIC-PLL) is proposed. In the AIC-PLL, another dynamic closed loop is included, in which the generated phase angle is utilised to generate the estimated values of the grid resistance and inductance. By this technique, the need for the estimation method in order to estimate the value of the grid impedance becomes redundant, which is important in the case of the grid impedance variable. The nonlinear mathematical model of the system is developed and the model is linearised in order to be used in the analytical study. The steady-state power transfer capability and the dynamic performance of the AIC-PLL-based converter are also considered in this paper. The results show that the converter that relies on AIC-PLL is capable of transferring an amount of power that is approximately equal to the theoretical maximum power. In terms of the dynamic performance, the results demonstrate that the AIC-PLL-based VSC converter provides a satisfactory dynamic response for different values of the grid impedance. Therefore, the AIC-PLL has the ability to replace the traditional IC-PLL in the case of grid variation.

Author Contributions: Supervision, O.M. and J.C.; Writing—original draft, M.A.H. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A. The Electrical and Control Parameters of the Studied System

This appendix gives the technical data of the studied VSC-HVDC system,

Appendix A.1. The Electrical System Parameters

Parameter	Value
Rated power	1200 MVA
Rated voltage U	220 kV
Grid frequency	50 Hz
Converter inductance L_c	0.08 p.u.
Converter resistance R_c	0.003 p.u.
Filter capacitance c_f	0.074 p.u.
Gird voltage E	1 p.u.
Grid impedance angle	80°

Appendix A.2. The Control System and PLL Parameters

Parameter	Value
Power controller gains K_{Pp}, K_{Pi}	1, 50
Voltage controller gains K_{Up}, K_{Ui}	0.1, 5
Current controller gains $k_{pd} = k_{pq}, k_{id} = k_{iq}$	1.27, 14.25
Power measurement filter ω_P	200 rad/s
AC voltage filter ω_U	10 rad/s
The active damping gain K_{AD}	10
The active damping cutoff frequency ω_{AD}	200 rad/s
Rated angular frequency ω_b	$2\pi \times 50$ Hz

Appendix B. Nonlinear Mathematical Model of the Over All System

The overall system represented in Figure 1 can be redemonstrated in terms of a block diagram shown in Figure A1. The mathematical model of each block is provided below, and the overall nonlinear mathematical model is finally obtained.

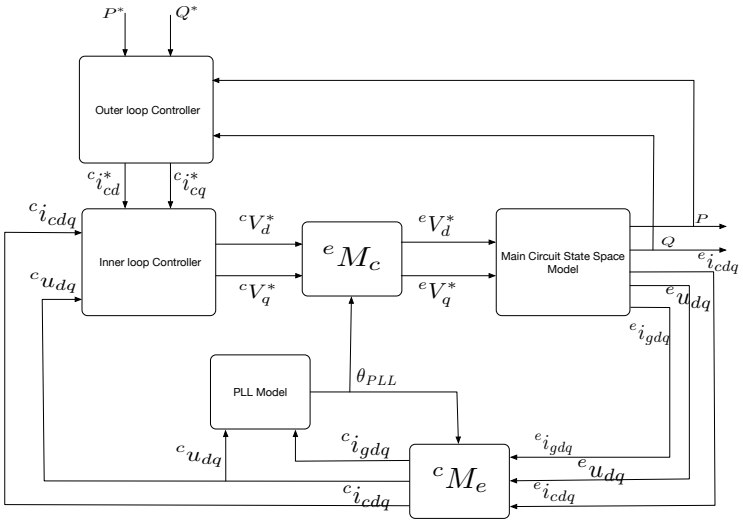

Figure A1. Block diagram for the nonlinear mathematical model.

The mathematical model of the main circuit model is

$$\dot{\bar{\mathbf{x}}} = \bar{\mathbf{f}}(\bar{\mathbf{x}}, \bar{\mathbf{u}}), \quad \bar{\mathbf{y}} = \bar{\mathbf{h}}(\bar{\mathbf{x}}) \tag{A1}$$

where,

$$\bar{\mathbf{f}}(\bar{\mathbf{x}}, \bar{\mathbf{u}}) = \begin{bmatrix} \frac{1}{L_c}{}^e V^*_d - \frac{1}{L_c}{}^e u_d - \frac{R_c}{L_c}{}^e i_{cd} + \omega^e i_{cq} \\ \frac{1}{L_c}{}^e V^*_q - \frac{1}{L_c}{}^e u_q - \frac{R_c}{L_c}{}^e i_{cq} - \omega^e i_{cd} \\ \frac{1}{C_f}{}^e i_{cd} - \frac{1}{C_f}{}^e i_{gd} + \omega^e u_q \\ \frac{1}{C_f}{}^e i_{cq} - \frac{1}{C_f}{}^e i_{gq} - \omega^e u_d \\ \frac{1}{L_g}{}^e u_d - \frac{1}{L_g} E - \frac{R_g}{L_g}{}^e i_{gd} + \omega^e i_{gq} \\ \frac{1}{L_g}{}^e u_q - \frac{R_g}{L_g}{}^e i_{gq} - \omega^e i_{gd} \end{bmatrix},$$

$$\bar{\mathbf{h}}(\bar{\mathbf{x}}) = \begin{bmatrix} P & U \end{bmatrix}^T$$

and,

$$P = {}^{e}u_d {}^{e}i_{gd} + {}^{e}u_q {}^{e}i_{gq}, \quad U = \sqrt{{}^{e}u_d^2 + {}^{e}u_q^2},$$

$$\bar{\mathbf{x}} = [{}^{e}i_{cd} \quad {}^{e}i_{cq} \quad {}^{e}u_d \quad {}^{e}u_q \quad {}^{e}i_{gd} \quad {}^{e}i_{gq}].$$

Appendix B.1. Outer Loop Controller

The function of the outer loop is to control the active and reactive/ voltage magnitude at PCC by manipulating the value of the dq components of the converter current i_c, where in this paper the case of controlling voltage magnitude is chosen. As it is shown in Figure 1, the reference input signals of this controller are the reference active power P^* and reference voltage magnitude U^*, and they are fed with the feedback of the active power P_m and voltage magnitude U_m into two PI controllers. These controllers produce two current reference signals ${}^{c}i_{cd}^{*}$ for the active power and ${}^{c}i_{cq}^{*}$ for the voltage magnitude, to be fed into the inner loop controller. Low pass filters are also applied to the signals of the power and the voltage flow of the feedback. The following set of mathematical equations represent the model of the outer loop controller [21]; The PI controller of the active power is

$${}^{c}i_{cd}^{*} = K_{Pp}(P^* - P_m) + K_{Pi} \cdot \gamma_P \tag{A2}$$

and,

$$\gamma_P = \int_0^t (P^* - P_m) d\tau. \tag{A3}$$

The model of the low pass filter that is applied to the feedback signal of the active power is

$$P_m = \int_0^t (\omega_P \cdot P - \omega_P \cdot P_m) d\tau. \tag{A4}$$

The PI controller of the voltage amplitude is

$${}^{c}i_{cq}^{*} = -K_{Up}(U^* - U_m) - K_{Ui} \cdot \gamma_U \tag{A5}$$

and

$$\gamma_U = \int_0^t (U^* - U_m) d\tau. \tag{A6}$$

The model of the low pass filter that is applied to the feedback signal of the voltage amplitude is

$$U_m = \int_0^t (\omega_U \cdot U - \omega_U \cdot U_m) d\tau. \tag{A7}$$

The produced ${}^{c}i_{dq}^{*}$ are the control input signals represent the set-points for the inner loop controller which is explained in the next subsection.

Appendix B.2. Inner-Loop Controller

The function of the inner loop is to control the value of the converter's currents by manipulating the values of the converter voltages ${}^{c}V_{d,q}^{*}$, which are fed into the switching device, as it is shown in Figure 1. The inner loop controller consists of two PI controllers and the cross-coupling terms $\omega \cdot L_c$. The function of the cross-coupling terms is to control the d, q components of the converter current ${}^{c}i_c$ independently. An active damping algorithm is

also included in the inner loop controller in order to attenuate the oscillation in the voltage at PCC [28]. The following set of the mathematical equations represent the model of the inner loop controller [20,28];

The mathematical model of the reference converter voltage V_d is

$$\begin{aligned} {}^{c}V_d^* = {}^{c}u_d - \omega \cdot L_c \cdot {}^{c}i_{cq} + k_{pd}({}^{c}i_{cd}^* - {}^{c}i_{cd}) + \\ k_{id} \cdot \gamma_d - v_{AD,d}, \end{aligned} \tag{A8}$$

where

$$\gamma_d = \int_0^t ({}^{c}i_{cd}^* - {}^{c}i_{cd}) d\tau. \tag{A9}$$

The mathematical model of the active damping part can be defined as

$$v_{AD,d} = K_{AD}({}^{c}u_d - \phi_d), \tag{A10}$$

where

$$\phi_d = \int_0^t (\omega_{AD} \cdot {}^{c}u_d - \omega_{AD} \cdot \phi_d) d\tau. \tag{A11}$$

The mathematical model of the reference converter voltage V_q is

$$\begin{aligned} {}^{c}V_q^* = {}^{c}u_q + \omega \cdot L_c \cdot {}^{c}i_{cd} + k_{pq}({}^{c}i_{cq}^* - {}^{c}i_{cq}) + \\ k_{iq} \cdot \gamma_q - v_{AD,q}, \end{aligned} \tag{A12}$$

where

$$\gamma_q = \int_0^t ({}^{c}i_{cq}^* - {}^{c}i_{cq}) d\tau. \tag{A13}$$

The mathematical model of the active damping part can be defined as

$$V_{AD,q} = K_{AD}({}^{c}u_q - \phi_q), \tag{A14}$$

where

$$\phi_q = \int_0^t (\omega_{AD} \cdot {}^{c}u_q - \omega_{AD} \cdot \phi_q) d\tau. \tag{A15}$$

The Park and inverse Park Transformation can be modelled as a rotation matrices as bellow

$${}^{e}M_c^{-1} = {}^{c}M_e = \begin{bmatrix} \cos\theta_{PLL} & \sin\theta_{PLL} \\ -\sin\theta_{PLL} & \cos\theta_{PLL} \end{bmatrix}.$$

Finally, the nonlinear state space model for the overall system can be defined as

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, \mathbf{u}), \quad \mathbf{y} = \mathbf{h}(\mathbf{x}) \tag{A16}$$

where

$$\mathbf{f}(\mathbf{x},\mathbf{u}) = \begin{bmatrix} \bar{\mathbf{f}}(\bar{\mathbf{x}},\bar{\mathbf{u}}) \\ {}^{c}i_{cd}^{*} - {}^{c}i_{cd} \\ {}^{c}i_{cq}^{*} - {}^{c}i_{cq} \\ \omega_b(K_{pPLL} tan^{-1}\frac{u_{qf}^{v}}{u_{df}^{v}} + K_{iPLL}\gamma_{PLL}) \\ tan^{-1}\frac{u_{qf}^{v}}{u_{df}^{v}} \\ -\omega_{FLPLL}u_{df}^{v} + \omega_{FLPLL}u_{d}^{v} \\ -\omega_{FLPLL}u_{qf}^{v} + \omega_{FLPLL}u_{q}^{v} \\ P^{*} - P_m \\ U^{*} - U_m \\ \omega_{AD}\cdot {}^{c}u_d - \omega_{AD}\cdot\phi_d \\ \omega_{AD}\cdot {}^{c}u_q - \omega_{AD}\cdot\phi_q \\ \omega_P \cdot P - \omega_P \cdot P_m \\ \omega_U \cdot U - \omega_U \cdot U_m \end{bmatrix},$$

$$\mathbf{h}(\mathbf{x}) = \begin{bmatrix} P & U \end{bmatrix}^{T}.$$

For the case of AIC-PLL, two more terms are included in $\mathbf{f}(\mathbf{x},\mathbf{u})$ which are $f_{19,1}(x,u) = K_{Rvi}\theta_{PLL}$ and $f_{20,1}(x,u) = K_{Lvi}\theta_{PLL}$.

Therefore, the state variables of the overall system is

$$\mathbf{x} = [{}^{e}i_{cd} \quad {}^{e}i_{cq} \quad {}^{e}u_d \quad {}^{e}u_q \quad {}^{e}i_{gd} \quad {}^{e}i_{gq} \quad \gamma_d \quad \gamma_q \quad \theta_{PLL} \quad \gamma_{PLL} \quad u_{df}^{v} \quad u_{qf}^{v} \quad \gamma_P \quad \gamma_U \quad \phi_d \quad \phi_q \quad P_m \quad U_m]$$

For the case of utilising AIC-PLL, $x_{19} = \gamma_{vd}$ and $x_{20} = \gamma_{vq}$, where

$$\gamma_{vd} = \int_0^t (K_{Rvi}\theta_{PLL})d\tau,$$
$$\gamma_{vq} = \int_0^t (K_{Lvi}\theta_{PLL})d\tau.$$

Appendix C. Developing the Small Signal State Space Model

The small signal state space mathematical model of the overall system is developed by finding the Jacobian matrix $\mathbf{J}$ of the function $\mathbf{f}(\mathbf{x},\mathbf{u})$, where $A = \mathbf{J}_{x=x_0}$. The Jacobian matrix can be defined as

$$\mathbf{J} = [\tfrac{\partial \mathbf{f}}{\partial x_1} \cdots \tfrac{\partial \mathbf{f}}{\partial x_n}]. \tag{A17}$$

where $n = 18$ for the case of the IC-PLL and $n = 20$ for the case of the AIC-PLL. The small signal state space model can be given as

$$\Delta\dot{x} = A\cdot\Delta x + B\cdot\Delta u,$$
$$\Delta y = C\cdot\Delta x + D\cdot\Delta u.$$

where

$$B = \begin{bmatrix} \frac{1}{L_c}k_{pd}K_{Pp}\cos\theta_{PLL0} & \frac{1}{L_c}k_{pd}K_{Pp}\sin\theta_{PLL0} & 0\,0\,0\,0\,K_{Pp} & 0 & 0\,0\,0\,0\,1\,0\,0\,0\,0\,0 \\ \frac{1}{L_c}k_{pq}K_{Up}\sin\theta_{PLL0} & -\frac{1}{L_c}k_{pq}K_{Up}\cos\theta_{PLL0} & 0\,0\,0\,0 & 0 & -K_{Up}\,0\,0\,0\,0\,1\,0\,0\,0\,0 \end{bmatrix}^{T},$$

$$C = \begin{bmatrix} 0\,0\,i_{gd0}\,i_{gq0}\,u_{d0}\,u_{q0}\,0\,0\,0\,0\,0\,0\,0\,0\,0\,0 \\ 0\,0\,\frac{u_{d0}}{U_0}\,\frac{u_{q0}}{U_0}\,0\,0\,0\,0\,0\,0\,0\,0\,0\,0\,0 \end{bmatrix},$$

$D = \tilde{D}$.

$$A = \begin{bmatrix}
a_{1,1} & a_{1,2} & -\frac{K_{AD}}{L_c} & 0 & 0 & 0 & \alpha_5 & -\alpha_6 & a_{1,9} & 0 & 0 & 0 & \frac{k_{pd}K_{Pi}\alpha_5}{k_{id}} & \frac{k_{pq}K_{Ui}\alpha_6}{K_{iq}} & \frac{K_{AD}\alpha_5}{k_{id}} & (-\frac{K_{AD}\alpha_6}{k_{iq}}) & (-\frac{k_{pd}K_{Pp}\alpha_5}{k_{id}}) & (-\frac{k_{pq}K_{Up}\alpha_6}{k_{iq}}) \\
a_{2,1} & a_{2,2} & 0 & -\frac{K_{AD}}{L_c} & 0 & 0 & \alpha_6 & \alpha_5 & a_{2,9} & 0 & 0 & 0 & \frac{k_{pd}K_{Pi}\alpha_6}{k_{iq}} & (-\frac{k_{pq}K_{Ui}\alpha_5}{k_{id}}) & \frac{K_{AD}\alpha_6}{k_{iq}} & \frac{K_{AD}\alpha_5}{k_{id}} & (-\frac{k_{pd}K_{Pp}\alpha_6}{k_{iq}}) & (\frac{k_{pq}K_{Up}\alpha_5}{k_{id}}) \\
\frac{1}{C_f} & 0 & 0 & \omega & -\frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{C_f} & -\omega & 0 & 0 & -\frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{L_g} & 0 & -\frac{R_g}{L_g} & \omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{L_g} & -\omega & -\frac{R_g}{L_g} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-\alpha_{10} & -\alpha_9 & 0 & 0 & 0 & 0 & 0 & 0 & a_{7,9} & 0 & 0 & 0 & K_{Pi} & 0 & 0 & 0 & 0 & 0 \\
\alpha_9 & -\alpha_{10} & 0 & 0 & 0 & 0 & 0 & 0 & a_{8,9} & 0 & 0 & 0 & 0 & -K_{Ui} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \omega_b K_{iPLL} & -\alpha_{14} & \alpha_{15} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{\alpha_{14}}{\omega_b K_{pPLL}} & \frac{\alpha_{15}}{\omega_b K_{pPLL}} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \omega_{FLPLL}\alpha_{10} & \omega_{FLPLL}\alpha_9 & \alpha_{18} & \alpha_{19} & 0 & 0 & \alpha_{16} & 0 & -\omega_{FLPLL} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\omega_{FLPLL}\alpha_9 & \omega_{FLPLL}\alpha_{10} & -\alpha_{19} & \alpha_{18} & 0 & 0 & \alpha_{17} & 0 & 0 & -\omega_{FLPLL} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\
0 & 0 & \omega_{AD}\alpha_{10} & \omega_{AD}\alpha_9 & 0 & 0 & 0 & 0 & \alpha_{12} & 0 & 0 & 0 & 0 & 0 & -\omega_{AD} & 0 & 0 & 0 \\
0 & 0 & -\omega_{AD}\alpha_9 & \omega_{AD}\alpha_{10} & 0 & 0 & 0 & 0 & \alpha_{13} & 0 & 0 & 0 & 0 & 0 & 0 & -\omega_{AD} & 0 & 0 \\
0 & 0 & \omega_P {}^e i_{gd0} & \omega_P {}^e i_{gq0} & \omega_P {}^e u_{d0} & \omega_P {}^e u_{q0} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\omega_P & 0 \\
0 & 0 & \frac{\omega_U {}^e u_{d0}}{\sqrt{{}^e u_{d0}{}^2 + {}^e u_{q0}{}^2}} & \frac{\omega_U {}^e u_{q0}}{\sqrt{{}^e u_{d0}{}^2 + {}^e u_{q0}{}^2}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\omega_U
\end{bmatrix},$$

and

$a_{1,1} = \alpha_1 \cos\theta_{PLL0} - \alpha_2 \sin\theta_{PLL0} - \frac{R_c}{L_c}$,
$a_{1,2} = \alpha_3 \cos\theta_{PLL0} - \alpha_4 \sin\theta_{PLL0} + \omega$,
$a_{2,1} = \alpha_1 \sin\theta_{PLL0} + \alpha_2 \cos\theta_{PLL0} - \omega$,
$a_{2,2} = \alpha_3 \sin\theta_{PLL0} + \alpha_4 \cos\theta_{PLL0} - \frac{R_c}{L_c}$,
$a_{7,9} = {}^e i_{cd0} \sin\theta_{PLL0} - {}^e i_{cq0} \cos\theta_{PLL0}$,
$a_{8,9} = {}^e i_{cq0} \sin\theta_{PLL0} + {}^e i_{cd0} \cos\theta_{PLL0}$,
$\alpha_1 = \omega \sin\theta_{PLL0} - \frac{1}{L_c} k_{pd} \cos\theta_{PLL0}$,
$\alpha_2 = \omega \cos\theta_{PLL0} + \frac{1}{L_c} k_{pq} \sin\theta_{PLL0}$,
$\alpha_3 = -\omega \cos\theta_{PLL0} - \frac{1}{L_c} k_{pd} \sin\theta_{PLL0}$,
$\alpha_4 = \omega \sin\theta_{PLL0} - \frac{1}{L_c} k_{pq} \cos\theta_{PLL0}$,
$\alpha_5 = k_{id} \frac{1}{L_c} \cos\theta_{PLL0}$,
$\alpha_6 = k_{iq} \frac{1}{L_c} \sin\theta_{PLL0}$,
$a_{1,9} = \frac{1}{L_c}(\cos\theta_{PLL0}(\partial^c V_d^* / \partial\theta \mid_{x=x_0}) - ({}^c V_d^* \mid_{x=x_0}) \sin\theta_{PLL0} - \sin\theta_{PLL0}(\partial^c V_q^* / \partial\theta \mid_{x=x_0}) - ({}^c V_q^* \mid_{x=x_0}) \cos\theta_{PLL0})$,
$a_{2,9} = \frac{1}{L_c}(\sin\theta_{PLL0}(\partial^c V_d^* / \partial\theta \mid_{x=x_0}) + ({}^c V_d^* \mid_{x=x_0}) \cos\theta_{PLL0} + \cos\theta_{PLL0}(\partial^c V_q^* / \partial\theta \mid_{x=x_0}) - ({}^c V_q^* \mid_{x=x_0}) \sin\theta_{PLL0})$,
$\alpha_9 = \sin\theta_{PLL0}$,
$\alpha_{10} = \cos\theta_{PLL0}$,
$\alpha_{12} = \omega_{AD}(-{}^e u_{d0} \sin\theta_{PLL0} + {}^e u_{q0} \cos\theta_{PLL0})$,
$\alpha_{13} = \omega_{AD}(-{}^e u_{q0} \sin\theta_{PLL0} - {}^e u_{d0} \cos\theta_{PLL0})$,
$\alpha_{14} = K_{pPLL}\omega_b \frac{u_{qf0}^v}{u_{df0}^v(\frac{u_{qf0}^{v2}}{u_{df0}^{v2}}+1)}$,
$\alpha_{15} = K_{pPLL}\omega_b \frac{1}{u_{df0}^v(\frac{u_{qf0}^{v2}}{u_{df0}^{v2}}+1)}$,
$\alpha_{16} = \omega_{FLPLL}({}^c u_{q0} - R_g^{vc} i_{gq0} - \omega_{PLL0} L_g^{vc} i_{gd0})$,
$\alpha_{17} = \omega_{FLPLL}(-{}^c u_{d0} + R_g^{vc} i_{gd0} - \omega_{PLL0} L_g^{vc} i_{gq0})$,
$\alpha_{18} = \omega_{FLPLL}(-R_g^v \cos\theta_{PLL0} - \omega_{PLL0} L_g^v \sin\theta_{PLL0})$,
$\alpha_{19} = \omega_{FLPLL}(-R_g^v \sin\theta_{PLL0} + \omega_{PLL0} L_g^v \cos\theta_{PLL0})$.

For the case of the AIC-PLL, the matrices of the state space model are given as the same as for the case of IC-PLL with considering the following:

$$A_{AIC-PLL} = \left[\begin{array}{cc|cc} & & 0_{10\times 2} & \\ & & -\omega_{FLPLL}{}^{c}i_{gd0} & \omega_{PLL0}\omega_{FLPLL}{}^{c}i_{gq0} \\ A & & -\omega_{FLPLL}{}^{c}i_{gq0} & -\omega_{PLL0}\omega_{FLPLL}{}^{c}i_{gd0} \\ & & 0_{6\times 2} & \\ \hline 0_{2\times 8} & \begin{matrix} K_{Rvi} \\ K_{Lvi} \end{matrix} & 0_{2\times 11} & \end{array}\right]$$

$$\begin{aligned} \alpha_{18} &= \omega_{FLPLL}(-\hat{R}_{v0}\cos\theta_{PLL0} - \omega_{PLL0}\hat{L}_{v0}\sin\theta_{PLL0}), \\ \alpha_{19} &= \omega_{FLPLL}(-\hat{R}_{v0}\sin\theta_{PLL0} + \omega_{PLL0}\hat{L}_{v0}\cos\theta_{PLL0}), \\ \alpha_{16} &= \omega_{FLPLL}({}^{c}u_{q0} - \hat{R}_{v0}{}^{c}i_{gq0} - K_{Rvp}{}^{c}i_{gd0} + \\ &\quad \omega_{PLL0}(K_{Lvp}{}^{c}i_{gq0} - \hat{L}_{v0}{}^{c}i_{gd0})), \\ \alpha_{17} &= \omega_{FLPLL}(-{}^{c}u_{d0} + \hat{R}_{v0}{}^{c}i_{gd0} - K_{Rvp}{}^{c}i_{gq0} + \\ &\quad \omega_{PLL0}(K_{Lvp}{}^{c}i_{gd0} + \hat{L}_{v0}{}^{c}i_{gq0})). \end{aligned}$$

In addition, the C and D matrices, adding other $0_{2\times 2}$ to the ends of the two matrices.

Appendix D. Participation Matrix for the AIC-PLL-Based System, $\omega_{FL,PLL} = 400$ rad/s and $Z_g = 2$ p.u.

The contribution of each eigenvalue on each state of the closed loop system can be demonstrated by calculating the participation matrix, which can be given by [15]

$$\mathbf{P} = [\mathbf{p}_1\mathbf{p}_2\cdots\mathbf{p}_n], \tag{A18}$$

with

$$\mathbf{p}_i = \begin{bmatrix} p_{1i} \\ p_{2i} \\ \vdots \\ p_{ni} \end{bmatrix} = \begin{bmatrix} \phi_{1i}\psi_{i1} \\ \phi_{2i}\psi_{i2} \\ \vdots \\ \phi_{ni}\psi_{in} \end{bmatrix} \tag{A19}$$

and

$$\Phi = [\boldsymbol{\phi}_1\,\boldsymbol{\phi}_2\cdots\boldsymbol{\phi}_n], \tag{A20}$$

$$\Psi = [\boldsymbol{\psi}_1\,\boldsymbol{\psi}_2\cdots\boldsymbol{\psi}_n] \tag{A21}$$

where $\boldsymbol{\phi}_i \ni R^{n\times 1}$ and $\boldsymbol{\psi}_i \ni R^{n\times 1}$ are the right and left eigenvector for the matrix A. The element $p_{ki} = \phi_{ki}\psi_{ik}$ is called the participation factor; it shows how the kth state variable is related to the ith eigenvalue, and vice versa. The participation matrix for the overall closed loop systems that use AIC-PLL are provided in Table A1.

Table A1. Participation matrix for the AIC-PLL.

	λ_1	λ_2	λ_3	λ_4	λ_5	λ_6	λ_7	λ_8	λ_9	λ_{10}	λ_{11}	λ_{12}	λ_{13}	λ_{14}	λ_{15}	λ_{16}	λ_{17}	λ_{18}	λ_{19}	λ_{20}
${}^{e}i_{cd}$	0	0.0005	0.0001	0	0.5424	0	0.0003	0	0	0	0	0	0	0	0	0.5424	0	0.0001	0.0005	0
${}^{e}i_{cq}$	0	0.0002	0.0003	0	0.5424	0	0.0002	0.0001	0	0	0	0	0	0	0	0.5424	0	0.0003	0.0002	0
${}^{e}u_{d}$	0.0002	0.3029	0.1971	0.0003	0.0006	0	0.027	0.0078	0	0	0.0001	0.0009	0	0	0	0.0006	0.0003	0.1971	0.3029	0.0002
${}^{e}u_{q}$	0.0006	0.2161	0.2766	0.0008	0.0006	0	0.068	0.0063	0	0	0	0.0001	0	0	0	0.0006	0.0008	0.2766	0.2161	0.0006
${}^{e}i_{gd}$	0.0001	0.2622	0.1789	0.009	0	0	0.1334	0.0019	0	0	0.005	0.0125	0.0062	0	0	0	0.009	0.1789	0.2622	0.0001
${}^{e}i_{gq}$	0	0.2277	0.3655	0.0035	0	0	0.2297	0.1072	0	0	0	0.0068	0.0001	0	0	0	0.0035	0.3655	0.2277	0
γ_d	0	0.0016	0.0017	0.8482	0	0	0.0123	0.0008	0	0	0.2016	0.1421	0	0	0	0	0.8482	0.0017	0.0016	0
γ_q	0	0.0008	0.006	0.0413	0	0	0.0077	0.0057	0	0	0.7034	0.2134	0	0	0	0	0.0413	0.006	0.0008	0
θ_{PLL}	0.5008	0.0003	0.0001	0	0	0	0	0	0	0.001	0	0	0	0	0	0	0	0.0001	0.0003	0.5008
γ_{PLL}	0.0056	0	0	0	0	0	0	0	0	1.0009	0	0	0	0	0	0	0	0	0	0.0056
u_{df}^{v}	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
u_{qf}^{v}	0.5005	0.0003	0.0001	0	0	0	0	0	0	0.0001	0	0	0	0	0	0	0	0.0001	0.0003	0.5005
γ_P	0	0.0036	0.026	0.833	0	0	0.0385	0.0315	0	0	0.0005	0.0435	0.0636	0	0	0	0.833	0.026	0.0036	0
γ_Q	0	0	0.0003	0.0411	0	0	0.0002	0	0	0	0.0011	0.0476	1.0738	0	0	0	0.0411	0.0003	0	0
Φ_d	0	0.0199	0.0736	0.0016	0	0	0.1284	1.0282	0.0143	0	0.01	0.0092	0	0	0	0	0.0016	0.0736	0.0199	0
Φ_q	0	0.0142	0.1034	0.0041	0	0	0.3244	0.8358	0	0	0.002	0.0011	0	0	0	0	0.0041	0.1034	0.0142	0
P_m	0	0.0879	0.2398	0.0259	0	0	0.5663	1.0237	1.0143	0	0.0003	0.0038	0	0	0	0	0.0259	0.2398	0.0879	0
Q_m	0	0.0004	0.0031	0.0282	0	0	0.0014	0.0002	0	0	0.1085	0.9215	0.0039	0	0	0	0.0282	0.0031	0.0004	0
γ_{vd}	0	0	0	0	0	0	0	0	0	0	0	0	0	0.2149	0.7851	0	0	0	0	0
γ_{vq}	0	0	0	0	0	0	0	0	0	0	0	0	0	0.7851	0.2149	0	0	0	0	0

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