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Asymmetric Split-Gate 4H-SiC MOSFET with Embedded Schottky Barrier Diode for High-Frequency Applications

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Abstract: 4H-SiC Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) with embedded Schottky barrier diodes are widely known to improve switching energy loss by reducing reverse recovery characteristics. However, it weakens the static characteristics such as specific on-resistance and breakdown voltage. To solve this problem, in this paper, an Asymmetric 4H-SiC Split Gate MOSFET with embedded Schottky barrier diode (ASG-MOSFET) is proposed and analyzed by conducting a numerical TCAD simulation. Due to the asymmetric structure of ASG-MOSFET, it has a relatively narrow junction field-effect transistor width. Therefore, despite using the split gate structure, it effectively protects the gate oxide by dispersing the high drain voltage. The Schottky barrier diode (SBD) is also embedded next to the gate and above the Junction Field Effect transistor (JFET) region. Accordingly, since the SBD and the MOSFET share a current path, the embedded SBD does not increase in $R_{ON,SP}$ of MOSFET. Therefore, ASG-MOSFET improves both static and switching characteristics at the same time. As a result, compared to the conventional 4H-SiC MOSFET with embedded SBD, Baliga′s Figure of Merit is improved by 17%, and the total energy loss is reduced by 30.5%, respectively.

Keywords: 4H-SiC; asymmetric; split gate; body diode; switching loss

1. Introduction

4H-SiC is a wide bandgap material and has material properties such as high critical electric field and thermal conductivity [1]. With these characteristics, the use of 4H-SiC enables the implementation of MOSFETs, which significantly improves the switching characteristics compared to the conventional Si IGBT [2,3]. Therefore, 4H-SiC Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) are considered to be promising candidates for high-voltage and high-frequency applications. In particular, high-voltage and high-frequency power devices are expected to be applied in applications requiring high-power density, such as high-power converters and traction drives [4,5]. However, most commercially available SiC power MOSFETs are for 1200 V and 1700 V applications. In response to these industry demands, SiC MOSFETs for 3300 V are being actively researched [6,7]. Recently, various studies into trench MOSFETs have been conducted due to the high channel mobility and the small cell pitch of trench MOSFETs. However, trench MOSFETs suffer from electric field concentrations at the trench gate oxide corners exceeding 3 MV/cm, the gate oxide reliability limit of SiC MOSFETs [8]. Therefore, for high voltage applications, research mainly focuses on planar MOSFETs.

To achieve fast switching speeds and low switching energy losses for high frequency, the gate—drain capacitance (C_{GD}) must be minimized [9]. A well-known method to reduce C_{GD} of the planar MOSFET is a split gate MOSFET, which reduces the overlapped region between gate and drain through the split active gate [10]. However, in this structure, the electric field is concentrated at the corner of the split gate oxide, so there is a problem in that the reliability of the gate oxide cannot be guaranteed. In particular, this problem becomes more serious as the high-voltage device increases. Therefore, the split gate structure is difficult to apply to high voltage applications (>3.3 kV).

Another way to improve the switching characteristic is to improve the reverse recovery characteristics. Because the body diode of SiC MOSFETs has a high reverse recovery charge, a high reverse recovery current is generated during the turn on transient in the switching operation [11]. The reverse recovery current increases the peak drain current, resulting in high switching energy loss. To handle the reverse recovery current, an external Schottky barrier diode (SBD) is widely used as a freewheeling diode to suppress the action of the body diode [12]. However, an external SBD increases the active chip area and package cost. In high voltage applications, the active chip area of external SBD increases as the size of the external SBD increases to withstand the high voltage in the off state [13]. Recently, to improve the reverse recovery characteristics of SiC MOSFETs without using an external SBD, research into embedding SBD in SiC MOSFET has been actively conducted. A conventional 4H-SiC MOSFET with embedded SBD (C-MOSFET) greatly improves reverse recovery characteristics without external SBD [14]. However, embedded SBD increases the cell pitch, decreasing the channel density and thus increases the specific on-resistance ($R_{ON,SP}$). Moreover, in the off state, due to the increased mesa region, the voltage concentrated on the p+ base is also increased, reducing the Breakdown Voltage (BV). That is, the SBD embedded in the mesa region improves the reverse recovery characteristic but is accompanied by a deterioration of the static characteristics.

In this paper, we propose an asymmetric split gate 4H-SiC MOSFET with embedded SBD (ASG-MOSFET) to simultaneously improve both the switching and static characteristics. In ASG-MOSFET, the SBD is embedded next to the active gate and above the junction field effect transistor (JFET) region. Accordingly, the embedded SBD does not degrade the $R_{ON,SP}$ of MOSFET because the MOSFET and SBD share the current path in the on state. In addition, since the ASG-MOSFET is an asymmetric structure, it has a narrow JFET width (W_{JFET}). Therefore, it has a high channel density through a small cell pitch, thus reducing the $R_{ON,SP}$ despite the narrow W_{JFET}. This narrow W_{JFET} also forms a large depletion region, creating a small depletion capacitance (C_{DEP}). Moreover, the split gate structure of ASG-MOSFET reduces the overlapping area between gate and drain, thereby reducing gate oxide capacitance (C_{OX}). Therefore, ASG-MOSFET significantly reduces C_{GD} through the reduced C_{OX} and C_{DEP}.

This study was conducted by a Sentaurus TCAD simulation tool. In this simulation, the used models include the Fermi–Dirac statistics, band narrowing, anisotropic material properties, Shockley-Read-Hall, Auger recombination. A Hatakeyama model is used to consider the impact of ionization behavior. Mobility models, such as doping dependent, high field saturation, surface roughness, and acoustic phonon scattering at the SiC/SiO$_2$ interface are involved [15]. The incomplete ionization model is also considered and the nonlocal tunneling model and Schottky barrier lowering model are used for the tunneling current at the Schottky contact [16]. The fixed charge concentration at the SiC/SiO$_2$ interface is considered as 3×10^{12} cm^{-2}.

2. Device Structure and Optimization

2.1. Proposed Device Structure

Figure 1 is a cross-sectional view of the C-MOSFET and the proposed ASG-MOSFET. In Figure 1, the cells used for the simulation are marked with a red dotted line. In Figure 1, the C-MOSFET and the ASG-MOSFET have the SBD embedded over the mesa region and the JFET region, respectively.
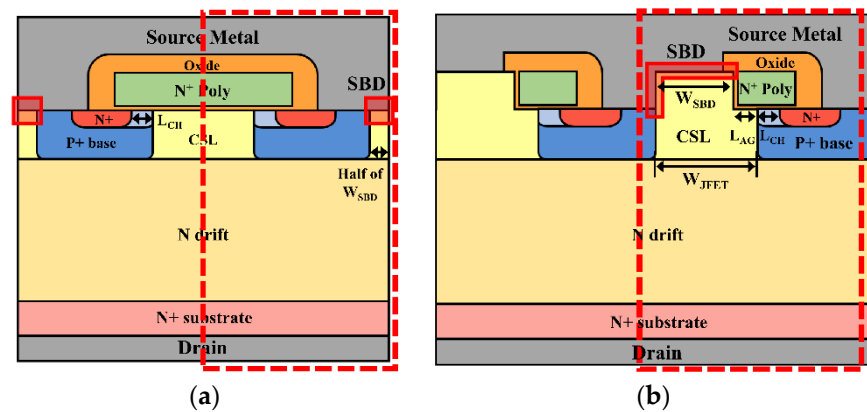
Figure 1. Schematic cross-sectional views (**a**) conventional MOSFET with embedded SBD (C-MOSFET) and (**b**) asymmetric split gate MOSFET with embedded SBD (ASG-MOSFET).

For the two device structures, the channel length and gate oxide thicknesses are 0.5 μm and 50 nm, respectively, and the doping concentration in the channel region is 2×10^{17} cm^{-3}. Considering the simultaneous formation of ohmic and Schottky contacts using Ni as a source metal, the work function of the Schottky metal was set to 5.05 eV [17]. The electron mobility is set at about 20–50 cm^{2}V^{-1}S^{-1} in the 15 nm range below the SiC/SiO$_2$ interface. A P+ base region doping concentration of 2×10^{18} cm^{-3}, an N-drift layer of 30 μm, an N-drift doping concentration of 3×10^{15} cm^{-3}, and a Channel Spread Layer (CSL) doping concentration of 2×10^{16} cm^{-3} were used. A heavily doped 1×10^{20} cm^{-3} N-type Poly Si was adopted as the active gate. The W_{JFET} of C-MOSFET was set to 2.0 μm in consideration of static characteristics such as $R_{ON,SP}$, and *BV*. The gate oxide thickness of the two structures was considered to be 50 nm.

2.2. Key Parameter Optimization

In this section, optimization of the two structures was performed considering $R_{ON,SP}$ and turn on voltage of embedded SBD ($V_{F,SBD}$) of C-MOSFET and ASG-MOSFET. As previously mentioned, the C-MOSFET improves the reverse recovery characteristic through the embedded SBD, but it accompanies the degradation of the static characteristic. Therefore, the SBD width (W_{SBD}) of C-MOSFET was designed considering $R_{ON,SP}$ and $V_{F,SBD}$. Figure 2 shows $R_{ON,SP}$ and $V_{F,SBD}$ according to W_{SBD} change in C-MOSFET. As W_{SBD} increases, $V_{F,SBD}$ decreases while $R_{ON,SP}$ increases. This is because the embedded SBD in the mesa region increases the cell pitch of the C-MOSFET, reducing the channel density. Therefore, considering both $R_{ON,SP}$ and $V_{F,SBD}$, 2.0 μm with the most appropriate performance was determined as the W_{SBD}.
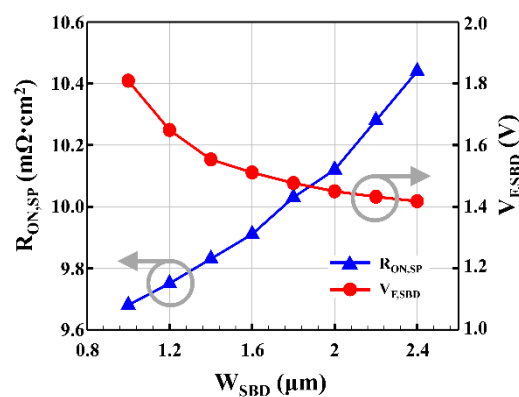

Figure 2. Trade-off between $R_{ON,SP}$ and $V_{F,SBD}$ of C-MOSFET according to W_{SBD}.

For a fair comparison between C-MOSFET and ASG-MOSFET, the W_{JFET} of ASG-MOSFET is designed such that the BV of the ASG-MOSFET has a BV similar to that of the C-MOSFET. In the ASG-MOSFET, the W_{JFET} consists of W_{SBD}, the active gate length (L_{AG}) and the gate oxide thickness (T_{OX}). The L_{AG} and T_{OX} of ASG-MOSFET is fixed to 0.2 μm and 50nm. Therefore, the W_{JFET} of the ASG-MOSFET was optimized by adjusting the W_{SBD}.

Figure 3 shows the effect of W_{JFET} on static characteristics of the ASG-MOSFET. In Figure 3a, unlike C-MOSFET, when W_{SBD} increases, $V_{F,SBD}$ and $R_{ON,SP}$ decrease simultaneously. In other words, the embedded SBD of the ASG-MOSFET does not degrade the $R_{ON,SP}$ characteristic of the ASG-MOSFET. This is because the MOSFET channel and the embedded SBD share a current path through the JFET region in their respective on state. Meanwhile, from Figure 3b, in the off state, as the W_{JFET} increases, the BV decreases due to the reduction of the screening effect by the JFET region. As a result, 1.4 μm, the condition with the most similar BV to that of C-MOSFET, was determined as W_{JFET}. Therefore, W_{SBD}, L_{AG}, and T_{OX} of the optimized ASG-MOSFET were designed to be 1.4 μm, 0.2 μm, and 50 nm, respectively.
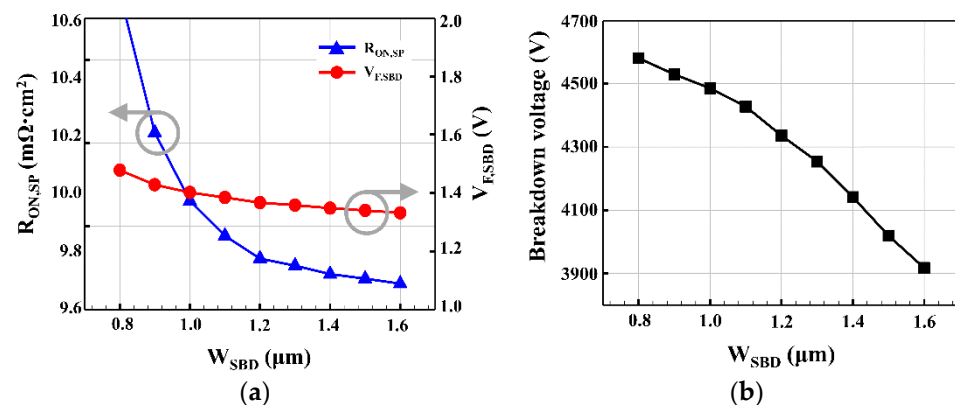

Figure 3. Static characteristics of ASG-MOSFET according to W_{SBD} (**a**) $R_{ON,SP}$ and $V_{F,SBD}$ characteristics and (**b**) *BV*.

3. Electrical Characteristics Analysis

3.1. Static Characteristics

In this section, to verify the excellent electrical properties of the proposed ASG-MOSFET, the electrical properties of the two structures were compared and analyzed through TCAD simulation.

Figure 4 shows output curves and *BV* characteristics of the C-MOSFET and ASG-MOSFET. According to the results optimized in Section 2.2, C-MOSFET and ASG-MOSFET have similar BV of 4094 V and 4141 V, respectively. Whereas, The $R_{ON,SP}$ of both structures are 10.12 mΩ·cm² and 8.85 mΩ·cm², respectively. ASG-MOSFET has higher JFET resistance than C-MOSFET due to smaller W_{JFET}, but $R_{ON,SP}$ of ASG-MOSFET is 12.5% smaller than C-MOSFET. This is because the ASG-MOSFET has a smaller cell pitch, which increases the channel density. As a result, the *BFOM* calculated by $BV^2/R_{ON,SP}$ improved by 17 %, respectively, compared to C-MOSFET.

The electric field distributions of C-MOSFET and ASG-MOSFET when V_{DS} = 3000 V are plotted in Figure 5a,b, respectively. The C-MOSFET has the highest gate oxide electric field (E_{OX}) in the center of the gate oxide because the W_{JFET} is wide. On the other hand, in ASG-MOSFET, the split gate corner is most vulnerable to electric field. However, because the ASG-MOSFET has an asymmetric structure, the gate oxide is more effectively protected by forming a wide depletion region in the JFET region through a narrow W_{JFET}. As a result, the maximum E_{OX} of C-MOSFET and ASG-MOSFET is 2.74 MV/cm and 2.02 MV/cm, respectively, so ASG-MOSFET has a more superior gate oxide reliability.
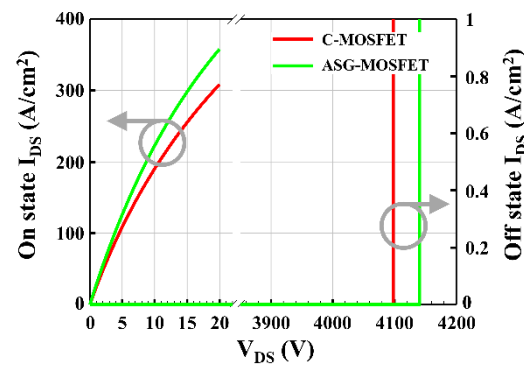
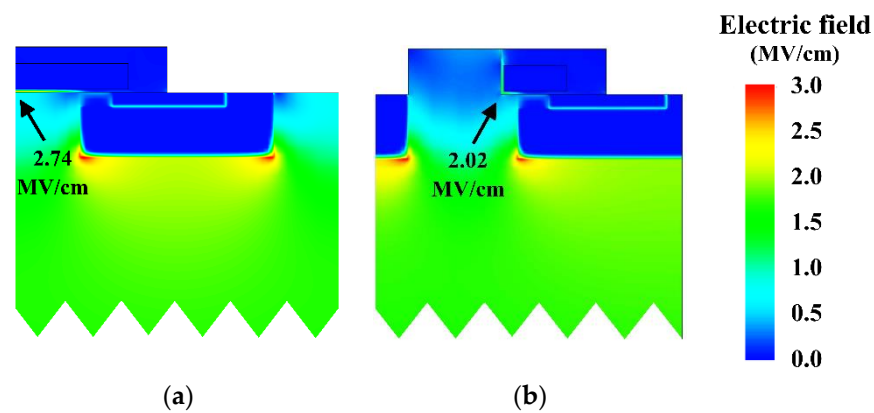**Figure 4.** Output curve and *BV* characteristics of C-MOSFET and ASG-MOSFET.

Figure 5. Electric field distribution of (**a**) C-MOSFET and (**b**) ASG-MOSFET when V_{DS} = 3000 V.

Figure 6 shows the forward conduction characteristics of the body diode. The forward conduction characteristics were extracted by sweeping V_{DS} from 0 V to −10 V when V_{GS} = −5 V. In Figure 6, the $V_{F,SBD}$ is defined as the V_{DS} when the drain current reaches −80 A/cm². Meanwhile, the knee point means the point at which the body diode is turned on [18]. As a result, $V_{F,SBD}$ of C-MOSFET is 1.45 V, whereas $V_{F,SBD}$ of ASG-MOSFET is 1.35 V. Therefore, the ASG-MOSFET more effectively suppresses the turn on of the body diode. The static characteristics of the two devices, including $R_{ON,SP}$, *BV*, maximum E_{OX}, $V_{F,SBD}$ and turn on voltage of body diode ($V_{F,Body}$), are summarized in Table 1. In addition, Baliga′s Figure of Merit (*BFOM*), which is the static characteristic indicator considering $R_{ON,SP}$ and *BV*, was calculated and listed.
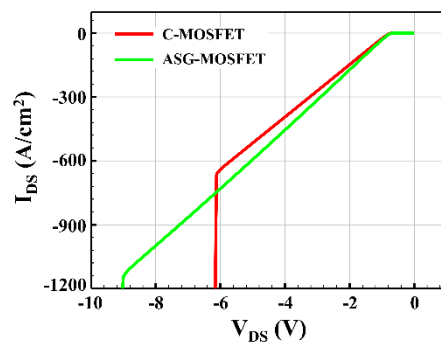

Figure 6. Forward conduction of the body diode of C−MOSFET and ASG−MOSFET.

Table 1. Dynamic characteristics of two devices.

	C-MOSFET	ASG-MOSFET
$R_{ON,SP}$ (mΩ·cm^2)	10.12	8.85
BV (V)	4098	4141
$BFOM$ (MW/cm^2)	1659.5	1937.6
Maximum E_{OX} (MV/cm)	2.74	2.02
$V_{F,SBD}$ (V)	1.45	1.35
$V_{F,Body}$ (V)	6.12	9.0

3.2. Dynamic Characteristics

The capacitance simulation results of two devices are depicted in Figure 7. In the capacitance simulation, the capacitance was extracted by sweeping the drain voltage from 0 V to 1500 V when V_{GS} = 0 V, and the AC small signal was set to 1 MHz. In addition, the active area of two devices of two devices is set to 1 cm^2.
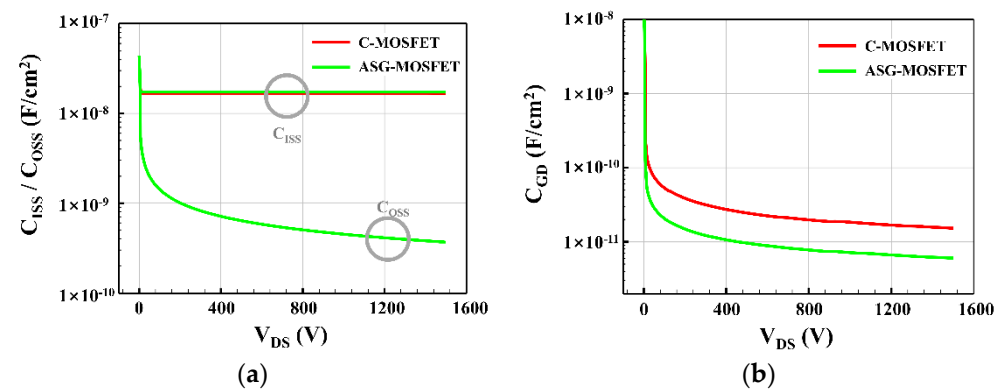

Figure 7. Capacitance of C-MOSFET and ASG-MOSFET (**a**) Input and output capacitance and (**b**) Gate–drain capacitance.

From Figure 7a, it can be seen that the input capacitance (C_{ISS}) and the output capacitance (C_{OSS}) of two structures are very similar. In the Figure 7b, the ASG-MOSFET has a significant improvement in C_{GD} over C-MSOFET. The C_{GD} of ASG-MOSFET is 6.04 pF/cm^2, which is improved by 60.4% compared to 15.24 pF/cm^2 of C-MOSFET. This is because the ASG-MOSFET greatly reduces the C_{OX} and C_{DEP} constituting C_{GD}. The C_{GD} is a series connection of C_{OX} and C_{DEP} [9]. The split-gate structure of ASG-MOSFET effectively reduces the overlapping area between gate and drain, reducing the C_{OX}. In addition, narrow W_{JFET} of ASG-MOSFET forms a wide depletion region between gate and drain, which also reduces C_{DEP}. Therefore, the ASG-MOSFET has significantly reduced C_{GD}. Based on the $R_{ON,SP}$ and C_{GD} results, High-Frequency Figure of Merit (*HFFOM*), which is commonly used as the high frequency performance indicators is calculated [2]. As a result, owing to the reduced $R_{ON,SP}$ and C_{GD}, the *HFFOM* of the ASG-MOSFET is 53.45 mΩ·pF, which is a 65% improvement compared to the 154.23 mΩ·pF of the C-MOSFET.

Figure 8 shows the switching waveforms of both devices when used as a device under test (DUT) in a half-bridge circuit. Figure 8a shows this during the turn on transient and turn off transient, respectively, and Figure 8b appears to show the half bridge circuits used for the double pulse test simulation. In Figure 8b, the gate resistance is set to 10 Ω and the gate voltage switched from −5 V to 20 V. In order to proceed with the double pulse test of the 3.3 kV device, V_{DD} was set to 1700 V. Furthermore, to set the load current to 100 A/cm^2 in the test circuit, the time period of the first pulse and load inductance are set to 10 μs and 170 μH, respectively, considering the V_{DD} and the rate of di/dt, and a parasitic inductance is assumed to 10 nH. In addition, the same MOSFET as the lower arm MOSFET was used for the upper arm MOSFET to handle the freewheeling current in the half-bridge circuit, and V_{GS} of the upper arm MOSFET was applied to −5V to maintain the off state of the

upper arm MOSFET. The SBD connected in parallel to the MOSFET in a half-bridge circuit appears in the SBD, which is embedded into the MOSFET.
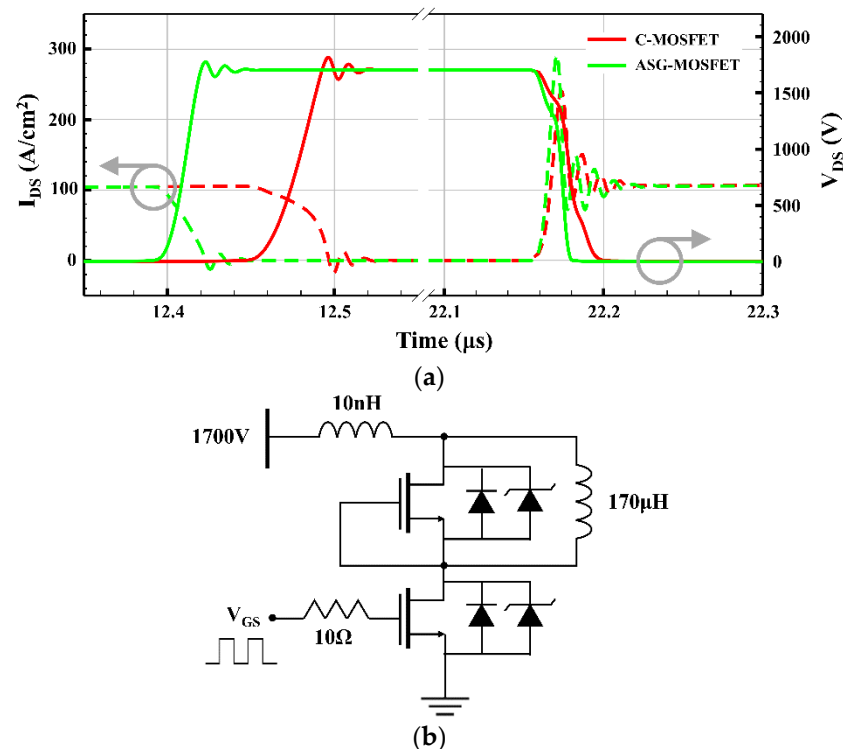

(a)

(b)

Figure 8. (**a**) Switching waveforms of C-MOSFET and ASG-MOSFET during turn off transient and turn on transient and (**b**) half-bridge circuit used for double pulse test simulation.

In Figure 8a, the ASG-MOSFET has a shorter Miller plateau and a faster switching speed than C-MOSFET during the switching transients, which is consistent with the C_{GD} results. Meanwhile, although SBD of ASG-MOSFET has lower $V_{F,SBD}$ than C-MOSFET, the peak current during switching transient is larger. This is because the fast-switching time of the ASG-MOSFET results in a higher overshoot current [19].

Figure 9 shows the current waveform of upper arm MOSFET during the turn on transient of lower arm MOSFET when the C-MOSFET and ASG-MOSFET are used as DUT in half-bridge circuit. From Figure 9, the ASG-MOSFET has a slightly larger reverse recovery charge (Q_{RR}) compared to the C-MOSFET. This is because the reduced C_{GD} of the ASG-MOSFET causes a larger overshoot current, resulting in a higher peak current.
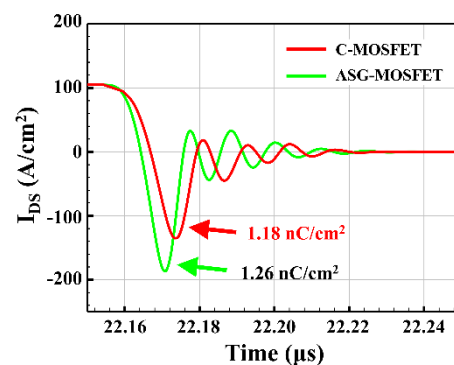

Figure 9. Current waveform of upper arm MOSFET during the turn on transient of lower arm DUT.

The ASG-MOSFET has a slightly larger Q_{RR}, but more superior the switching characteristics than the C-MOSFET. Figure 10 shows the total switching energy loss (E_{Total}) of two

devices during the switching transient. The E_{Total} of the ASG-MOSFET is still lower than that of the C-MOSFET shown in Figure 10 due to its fast-switching speed. Based on the double pulse test simulation results, the turn off loss (E_{OFF}) and the turn on loss (E_{ON}) of ASG-MOSFET are 0.84 mJ/cm^2 and 3.19 mJ/cm^2, respectively, whereas the C-MOSFET has an E_{OFF} of 1.79 mJ/cm^2 and an E_{ON} of 4.01 mJ/cm^2, the E_{Total} of ASG-MOSFET is 4.03 mJ, which is 30.5% lower than that of C-MOSFET with E_{Total} of 5.80 mJ. As a result, the switching characteristics, including the parasitic capacitance and reverse recovery characteristics of the two devices, are summarized in Table 2.
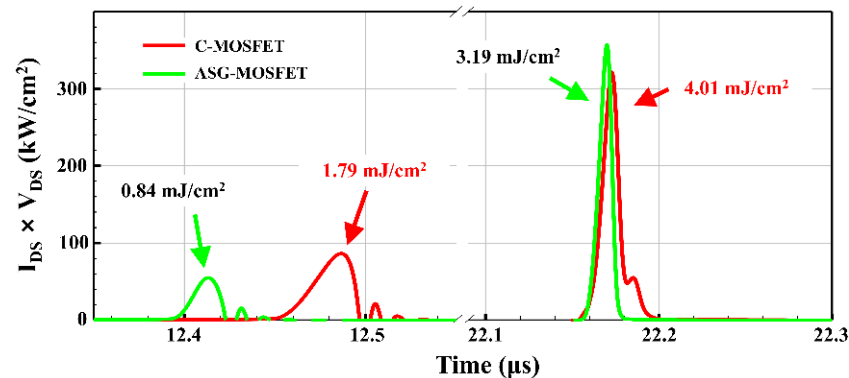

Figure 10. Switching energy loss during turn off and turn on transients.

Table 2. Dynamic characteristics of two devices.

	C-MOSFET	ASG-MOSFET
C_{ISS} (nF/cm^2)	16.79	17.34
C_{OSS} (pF/cm^2)	369.79	369.71
C_{GD} (pF/cm^2)	15.24	6.04
Q_{RR} (nC/cm^2)	1.18	1.26
E_{OFF} (mJ/cm^2)	1.79	0.84
E_{ON} (mJ /cm^2)	4.01	3.19
E_{Total} (mJ/cm^2)	5.80	4.03

4. Proposed Fabrication Process

Considering the feasibility of the proposed MOSFE, the fabrication process of ASG-MOSFET is proposed as shown in Figure 11. The N- drift and Channel Spread Layer are grown on an n+ substrate by epitaxial process, and the CSL layer is etched to remove the CSL layer, except for the Schottky contact region. N+ source, P+ base and P channel region are formed by the implantation process. The chemical vapor deposition is performed at 800 °C to form an oxide with a uniform thickness of 50 nm [20]. Poly Si is deposited by the low-pressure chemical vapor deposition (LPCVD) and is etched by reactive ion etching to form a split gate structure [21]. Interlayer dielectric oxide is deposited through LPCVD and is etched to open the Ohmic and Schottky contact region [22]. After Ni is deposited, rapid thermal annealing (RTA) is performed at 900 °C [23]. RTA at 900 °C after Ni deposition allows Ni to serve as a multifunctional metal that simultaneously forms Ohmic and Schottky contacts. Finally, an Ni layer is patterned, and a thick Al layer is deposited to form a metal pad.
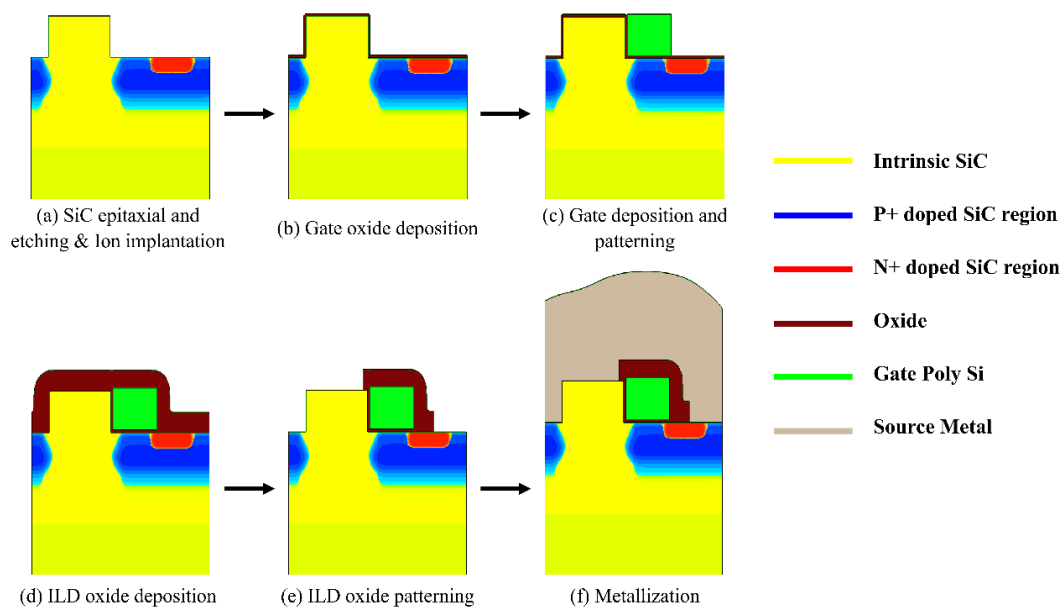
Figure 11. Proposed process flow of ASG-MOSFET. (**a**) Epitaxial N-drift layer and CSL on N+ substrate and Form the P+ base, P channel and N+ source by implantation (**b**) gate oxide deposition (**c**) Poly Si deposition and patterning (**d**) ILD deposition (**e**) ILD patterning (**f**) Ni metal deposition to form the ohmic and Schottky contact.

5. Conclusions

In this paper, based on the TCAD simulation results, we propose and analyze an asymmetric 4H-SiC split-gate MOSFET with embedded SBD (ASG-MOSFET). ASG-MOSFET has narrower W_{JFET} than C-MOSFET due to its asymmetric structure. The narrower W_{JFET} forms a wide depletion region, causing a better shielding effect of the JFET region. Therefore, the split gate structure of ASG-MOSFET is effectively protected without degradation of BV and gate oxide reliability. ASG-MOSFET also has lower $R_{ON,SP}$ than C-MOSFET. Unlike C-MOSFET, in ASG-MOSFET, the SBD is embedded above the JFET region so that the embedded SBD does not degrade the $R_{ON,SP}$ and the ASG-MOSFET has a smaller cell pitch, increasing channel density. In addition, since narrow W_{JFET} due to asymmetric structure effectively reduces C_{DEP}, ASG-MOSFET effectively improves switching characteristics through split gate, narrow W_{JFET} due to its asymmetric structure, and embedded SBD. As a result, ASG-MOSFET improved *BFOM* and switching energy loss by 17% and 30.5%, respectively, compared to C-MOSFET. Therefore, ASG-MOSFET is more suitable for high voltage and high frequency applications.

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