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Analyses and Comparisons of Generic and User Writing Models of HVDC System Considering Transient DC Current and Voltages

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Abstract: Analyses and comparisons of generic models and a novel modeling method of line-commutated converter (LCC)-based high voltage direct current (HVDC) systems are presented for the power system simulator for engineering (PSS/E) simulation tool. The main purposes are to describe the dynamics of the DC voltage and current of HVDC system and to improve estimation of the maximum values using the generic and proposed HVDC models when AC line-to-ground faults are occurred. For the generic HVDC models, the characteristics and limitations as well as parameter investigations are conducted. Three modules are also are developed for the proposed HVDC model, which are composed of (a) AC/DC conversion; (b) controller selection; and (c) DC line model. Case studies were conducted considering the real-operated HVDC system in Korea under the PSS/E and power systems computer aided design (PSCAD) simulation environments. The simulation results were compared with measured data from the real-operated HVDC system and the results from the PSCAD HVDC models considering single- and three-phase line-to-ground faults. The case study results show that a specific generic HVDC model in PSS/E can simulate the dynamics of the DC voltage and current after the AC line-to-ground faults. The case studies also showed that the proposed modeling method is effectively improves the estimation of the maximum DC voltage and current values for the AC line-to-ground faults.

Keywords: AC grid faults; dynamics of DC voltage and current; generic HVDC models; maximum DC voltage and current; modeling of HVDC system; PSS/E

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1. Introduction

High-voltage direct-current (HVDC) systems have install and operated continuously to transfer constant or fluctuant power between power networks in recent years. Concretely, about 191,000 MW power is delivered through 172 HVDC system around the world after the HVDC system was operated first in 1954 [1]. Although most HVDC projects have been utilized voltage-source converters (VSCs), a verified line-commutated converters (LCCs) are still installed and operated with higher capacities of HVDC system than current VSCs [2]. For example, Korea Electric Power Corporation (KEPCO) have installed and utilized two LCC-based HVDC systems, i.e., 180-kV, 300-MW and 200-kV, 250-MW, to transfer electrical power from the Korean mainland to the Jeju Island [3]. Moreover, the 200-kV LCC-based HVDC system installed by KEPCO has been used to transmit 300-MW electrical power from the Godduck substation to the Dangjin substation on the Korean mainland for improving stability and reliability of the Korea power grid against AC fault conditions [4].

Before installing and operating the HVDC systems, it is essential to analyze the transient- and steady-state stabilities of HVDC-linked AC transmission grids. For this,

several models of HVDC systems have been studied to analyze interactions between large-scale AC networks and the HVDC system against several AC network or HVDC system conditions [5–7]. For example, in [5], an LCC-based HVDC system was proposed using *dq*-reference quantities of an connected AC network to calculate DC voltage and current. In [6] and [7], an LCC-based HVDC system in multi-infeed HVDC systems was linearized to analyze the small-signal and network stability, respectively. However, these models of HVDC systems may be difficult or required adaptations to represent the operating features of real-operated HVDC systems, which needs a lot of time and effort considering modeling complexity.

Considering the difficulties of HVDC system modeling, the conseil international des grands reseaux electriques (CIGRE) benchmark model have been utilized to simulate HVDC systems and AC grids for the dynamic and steady-state stabilities in the several papers. In [8], comparative studies of the CIGRE benchmark model was conducted using different simulation tools. In [9,10], the responses of CIGRE benchmark model was explored when commutation failures occurred with respect to DC voltage variation and valve current variation, respectively. However, the CIGRE benchmark model may also require modifications to represent the operating characteristics of real HVDC systems. For example, in [11], additional extinction angle and DC current controllers at the rectifier and the inverter, respectively, were implemented to the CIGRE benchmark model to represent the HVDC system in the Taiwan. In [12], the Anshun-Zhaoqing HVDC system was modeled without consideration of the CIGRE benchmark model to represent the own operating characteristics of the system. Moreover, power systems computer aided design (PSCAD) and MATLAB/SIMULINK have been used as the simulation tools in [8–10]. However, only simplified voltage sources and equivalent impedances were used to represent the AC network models in these studies due to limited capabilities of the simulation tools for modeling of large-scale AC grids. Therefore, modeling of the real AC networks, such as Korea and Jeju grids, are restricted by these simulators; i.e., real-time simulations of the HVDC systems will have computational burden.

Quasi-steady-state (QSS) simulators such as Power System Simulator for Engineering (PSS/E), Positive Sequence Load Flow (PSLF) or PowerWorld are suitable simulation tools to model large-scale AC networks including HVDC systems. In particular, PSS/E is an appropriate QSS simulator to study AC networks and associated controllers. It assists transmission planning and operation engineers in designing and operating reliable AC networks by a broad range of methods. Therefore, PSS/E have been utilized to analyze large-scale power grids by many electric utilities [11,13]. Moreover, real data of power grid can be utilized in PSS/E to demonstrate interactions between the HVDC system and AC power network. For this, PSS/E also provides generic HVDC models such as CDC4T, CDC6T, and CDC7T instead of the CIGRE benchmark model [14]. In general, these HVDC models are used to represent real LCC-based HVDC systems when system operators analyze effects of the HVDC system on the AC power grid. For example, Western Electricity Coordination Council (WECC) have approved these HVDC models as generic models to simulate abnormal conditions, such as commutation failure or AC grid faults, for validating the real HVDC systems via PSS/E [15]. However, these models require numerous parameters whose characteristics and differences are not described to demonstrate operations of the real HVDC system at the abnormal conditions. In addition, a few real HVDC systems may be restricted to depict operations via these models because of their own characteristics. Therefore, some grid operators or utility companies may request new PSS/E models of practical HVDC systems to analyze effects of the HVDC system on the AC power grid, for example we focus on the Jeju-Haenam HVDC system in Korea.

In the meantime, LCC-based HVDC systems are cautious to commutation failure under the abnormal operation due to AC line faults. This is because it is capable of interrupting power transfer or imposing stress on converter [16]. Therefore, there have been several papers about cognizance of commutation failure caused by AC network

faults [17] and alleviation of commutation failure by modifying controllers [18,19] or by including supplement components [13,14]. In [17], the maximum-allowable balanced voltage drop at an inverter bus was calculated to reduce commutation failure probability and to increase recovery speed of the DC system after the commutation failure. In [18], A larger commutation margin was achieved by advancing the firing angle at the inverter side immediately when AC voltage disturbance was detected. It was described that a diminution of rectifier current order can reduce commutated DC current when AC voltage disturbances are detected in [19]. In [13], it was depicted that possibility of commutation failures and power factor can be reduced and improved, respectively, by a capacitor-commutated converters (CCC). In [14], thyristor-based full-bridge module (TFBM) was used in the converter valve of LCC to improve commutation failure immunity. However, these papers discussed so far focused on the reduction of commutation failure possibilities caused by AC line-to-ground faults. The maximum DC voltage and current of HVDC systems during commutation failures due to the AC line-to-ground faults have not been investigated in these papers. In practice, the maximum fault current and voltage are major concerns for the HVDC systems as well as AC networks because parameters of converter valves, DC-line capacity, and protection relays are affected by these values [20–22].

This paper investigates generic LCC-based HVDC system models and proposes a novel modeling method for an LCC-based HVDC system in the PSS/E simulation. In this paper, the characteristics and limitations as well as parameter investigations of generic HVDC models (e.g., CDC4T, CDC6T, and CDC7T) are conducted to indicate the maximum DC voltage and current of the HVDC systems in the abnormal condition, i.e., commutation failure due to AC line-to-ground faults. Moreover, the proposed modeling method, which composed of three modules, i.e., (a) AC/DC conversion; (b) controller selection; and (c) DC line model, is presented to calculate the maximum DC voltage and current of the HVDC system in the abnormal condition. Furthermore, the real HVDC system and the real power network are used as an example. The DC voltage and current of generic and proposed models are compared with measured data from the real-operated HVDC system to manifest differences between the generic and proposed models. The main contributions of this paper are summarized below:

- Analyses of characteristics, limitations, and parameter for the generic HVDC models in PSS/E are conducted to describe dynamic DC current and voltage of HVDC systems when AC line-to-ground faults occur.
- The HVDC system modeling method and procedure using PSS/E are proposed. The proposed modeling method calculates more precise maximum DC voltage and current of HVDC systems during the transient AC networks caused by AC grid faults.
- This paper describes transient DC voltage and current profiles compared with measured data for a single-phase fault from a real-operated HVDC systems using the proposed HVDC systems in PSS/E. Moreover, the DC voltage and current profiles of generic and proposed models are compared with those of HVDC system model developed using PSCAD considering a three-phase line-to-ground fault.

Section 2 explains analyses and comparisons of generic HVDC models in PSS/E simulation. The proposed HVDC modeling method using the real-operated HVDC system is stated in Section 3. The case studies for AC line-to-ground faults, e.g., single- and three-phase line-to-ground faults, are conducted in Section 4. Section 5 discusses conclusions.

2. Generic Models of HVDC System in PSS/E Simulation

PSS/E is one of the QSS-type simulation tools to simulate AC network at the fundamental grid frequency. It means that analyses of interaction between the HVDC systems and AC grid is more appropriate than analyses of detailed dynamics for converters using PSS/E. In particular, there are 12 examples of LCC-based HVDC system models in PSS/E for analyzing interaction between the HVDC system and AC transmission networks. Among these example models, 7 models (e.g., CDCABT, CEELT, CMDWAST, and etc.) represent actual operating HVDC models which have own additional controllers each,

for example frequency or runback controllers. The other models, on the other hand, are generally utilized to represent several HVDC systems having fundamental controllers, such as DC voltage, DC current, and firing angle controllers. For example, CDC4T, CDC6T and CDC7T models belong to these models, and are called the generic models. Following sections will explain characteristics and parameter analyses for the system operators to analyze HVDC system under an abnormal condition AC line faults.

2.1. Generic HVDC Models—CDC4T & CDC6T

A schematic control diagram for the CDC4T and CDC6T models is presented in Figure 1. The dc power reference P_{dc_ref} or the dc current reference I_{dc_ref} can be selected for the both models as input variables including the dc voltage reference V_{dc_ref}. When P_{dc_ref} is selected as an input variable, the dc current reference from the dc power reference $I^P{}_{dc\_ref}$ is chosen for the initial dc current reference $I^i{}_{dcr\_ref}$ rather than I_{dc_ref}. $I^P{}_{dc\_ref}$ is calculated by dividing P_{dc_ref} by the inverter dc voltage V_{dci} or rectifier dc voltage V_{dcr}. Note that V_{dci} or V_{dcr} is chosen by measure point for the dc voltage of the HVDC system. The dc current reference from voltage-dependent current order limit (VDCOL) function, $I^V{}_{dc\_ref}$, is also calculated using V_{dci}. The final dc current reference $I^f{}_{dc\_ref}$ is then selected either $I^i{}_{dc\_ref}$ or $I^V{}_{dc\_ref}$ by the minimum-select block. The final dc voltage reference $V^f{}_{dc\_ref}$ is calculated using V_{dc_ref}, $I^f{}_{dc\_ref}$ and the compounding resistance R_{comp}. V_{dci} and I_{dc} then calculated from $V^f{}_{dc\_ref}$ and $I^f{}_{dc\_ref}$ by the converter control block and transducer delay blocks, which have time constants T_{Vdc} and T_{Idc} each. Note that V_{dcr} can be calculated using V_{dci} and I_{dc} because a dc line is modeled by the dc-line resistor, R_{dc}, in the CDC4T and CDC6T models.

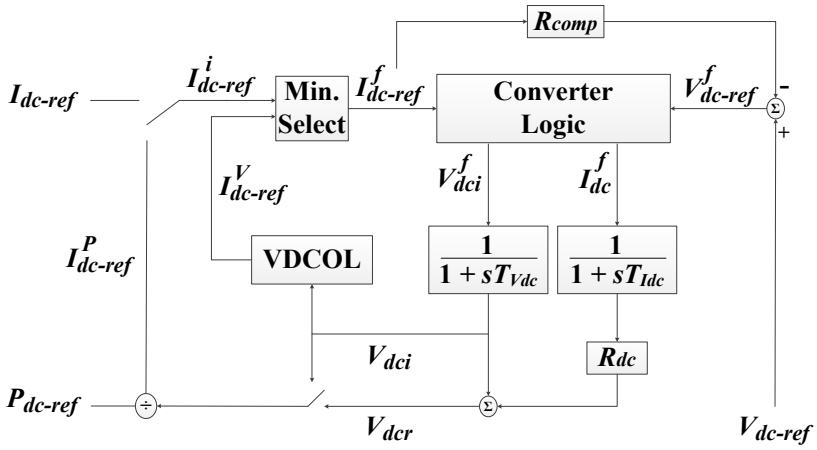


Figure 1. A control diagram for the CDC4T and CDC6T.

The primary aim of the converter control block is to obtain the V_{dci} and I_{dc} of the HVDC system from final input variables $V^f{}_{dc\_ref}$ and $I^f{}_{dc\_ref}$. Each converter control block is controlled by a simple feedback loop that adjusts firing delay to control the dc current to reference signal. The transfer function for the feedback loop depends on details of the bridge design. This feedback controller is able to force the dc current rapidly to the reference point by transient overadjustment of the rectifier dc voltage. This rapid forced response of the feedback control block is completed in a time that is generally shorter than the shortest time interval that can be recognized within the bandwidth of PSS/E simulation environment. This means that CDC4T and CDC6T models treat dc converter pairs as if they move instantaneously to their reference points when any of their input signals or ac feed voltages are changed. Therefore, these models are not concerned with the internal dynamic behavior of converters. The dc current and voltage from converter control block follows with transducer delay blocks which time constant determined by inductance of converter transformer and dc-link line.

The CDC4T and CDC6T models have 22 and 32 parameters which users can decide for investigation of interactions between HVDC systems and AC network. These parameters

can be classified into two groups. One group is parameters given by manufacturers to represent their own individual HVDC characteristics. For example, the minimum alpha and gamma parameters (i.e., AFLDY and GAMDY) or the dc voltage and current transducer time constants (i.e., TVDC and TIDC) in CDC4T and CDC6T models are parameters given by manufacturer for representing their own HVDC system. These parameters are difficult for system operator to change. The other is parameters which can be changed by the system operators to validate HVDC system models against the real operating profiles for some network events, such as three-phase ground fault and dc-line block, or to modify HVDC models for making operating strategies of HVDC systems. For example, inverter dc bypassing voltage (VBYPAS), voltage recovery rate (VRAMP), and VDCOL parameters in CDC4T and CDC6T models are parameters can be included to this group. Table 1 shows the parameters given by the manufacturers (i.e., Group A) and the parameters can be modified (i.e., Group B) of CDC4T and CDC6T models. Specially, example values of parameters for CDC4T model are also provided in the PSS/E manual [23].

Table 1. Parameters given by manufacturers (Group A) and modified by user (Group B) of CDC4T and CDC6T.

Parameters	Descriptions	Groups	Sample Values
AFLDY	minimum alpha for dynamics [deg]	A	5
GAMDY	minimum gamma for dynamcis [deg]	A	15
TVDC	dc voltage transducer time constant [s]	A	0.05
TIDC	dc current transducer time constant [s]	A	0.05
VBLOCK	rectifier ac blocking voltage [pu]	B	0.6
VUNBL	rectifier ac unblocking voltage [pu]	B	0.65
TBLOCK	minimum blocking time [s]	B	0.1
VBYPAS	inverter dc bypassing voltage [kV]	B	0.6
VUNBY	inverter ac unbypassing voltage [pu]	B	0.65
TBYPAS	minimum bypassing time [s]	A	0.1
RSVOLT	minimum dc voltage following block [kV]	A	200
RSCUR	minimum dc current following block [A]	A	500
VRAMP	voltage recovery rate [pu/s]	B	5
CRAMP	current recovery rate [pu/s]	B	5
C0	monimum current demand [A]	A	400
V1, C1	voltage, current limit point 1 [kV, A]	B	300, 1000
V2, C2	voltage, current limit point 2 [kV, A]	B	500, 3000
V3, C3	voltage, current limit point 3 [kV, A]	B	500, 3000
TCMODE	minimum time stays in switched mode [s]	A	0.1

Both CDC4T and CDC6T models have block and bypass functions to protect against the abnormal condition of HVDC system due to AC grid faults. For example, when the ac voltage at the rectifier side falls below the setting value (i.e., VBLOCK), the rectifier and inverter are both blocked. The only inverter, on the other hand, is bypassed while the rectifier continues to maintain dc current at the scheduled value when the inverter dc voltage falls below the setting value (i.e., VBYPAS). Note that low DC voltage at the rectifier does not cause blocking of the HVDC system unless AC voltage at the rectifier is also low. Similarly, low AC voltage at the inverter does not cause blocking or bypassing unless DC voltage at the inverter is also low. If the HVDC system is blocked, the rectifier remains block for a minimum second (i.e., TBLOCK) and then restarts when the AC voltage at the rectifier rises to a value of VUNBL. In the same manner, if the HVDC system is bypassed, the inverter remains bypass for a minimum second (i.e., TBYPAS) and then reestablishes when the AC voltage at the inverter rises to a value of VUNBY.

Moreover, CDC6T model has additional 10 parameters for the block of bypass functions to protect the HVDC system in detail from the AC faults causing the commutation failure, as listed in Table 2. This model allows for delayed automatic blocking of the HVDC system based on low AC voltage at the rectifier. For example, if the AC voltage at the rectifier is below the set value (i.e., VDEBLK) during the set seconds (i.e., TREBLK), the

HVDC system is then blocked. Following this block, the HVDC system cannot restart until several seconds (i.e., TREBLK) after the AC voltage at the rectifier goes above the set value (i.e., VUNBY). Furthermore, the CDC6T model allows a low AC voltage at the inverter to send a signal via a communication channel to the rectifier for blocking the HVDC system. This function is modeled by the instantaneous AC voltage at the inverter for blocking and the time delay (i.e., VINBLK and TCOMB). The HVDC system will stay blocked until the set period (i.e., TINBLK) after the AC voltage at the inverter goes above VUNBY. Note that TINBLK should include the communication delay in getting the signal from the inverter to the rectifier. Besides, if the AC voltage at the inverter goes below the set value (i.e., VACBYP) during the set seconds (i.e., TDEBYP), the inverter is then bypassed. The inverter will clear the bypass the set time seconds later (i.e., TUNBY) when the AC voltage at the inverter goes above VUNBY. Figure 2 shows differences of bypass and block functions between the CDC4T and CDC6T models.

Table 2. Additional parameters for CDC6T model.

Parameters	Descriptions, Sample Values
VDEBLK	rec. ac voltage that causes a block if remains for time TDEBLK, 0.1 pu
TDEBLK	time delay for block, 99 s
TREBLK	time delay after rec. ac voltage recovers above VUNBL before line unblocks, 0.1 s
VINBLK	inv. ac voltage that cause block after communication delay TCOMB, 0.65 pu
TCOMB	communication delay to signal rec. to block because of low inv. voltage, 0.05 pu
VACBYP	inv. ac voltage that causes bypass if remains for time TDEBYP, 0.1 pu
TDEBYP	time delay for bypass, 0.01 s
TINBLK	time delay after inv. ac vol. recovers above VUNBY before line unblocks, 0.05 s
TINBYP	time delay after inv. ac vol. recovers above VUNBY before line unbypasses, 0.05 s
TVRDC	rec. dc voltage transducer time constant, 0.05 s

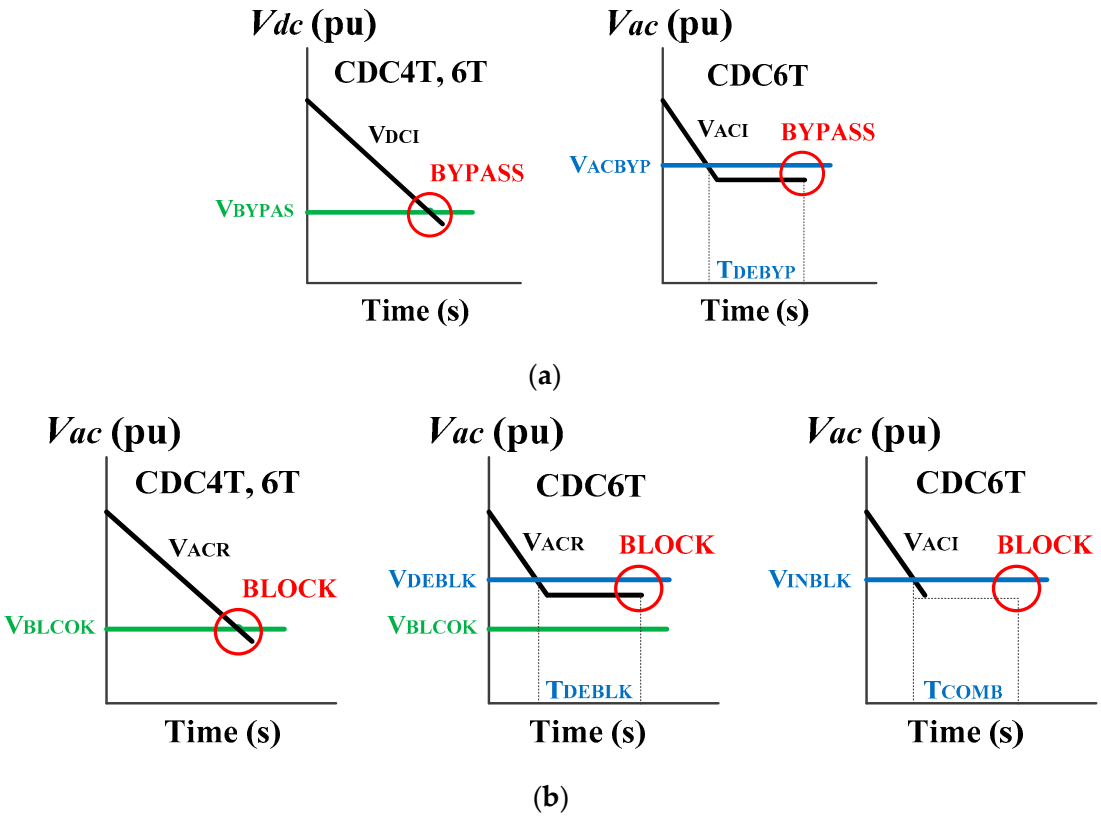


Figure 2. Differences of protection functions between the CDC4T and CDC6T: (**a**) bypass; (**b**) block.

2.2. Generic HVDC Model—CDC7T

The CDC7T model can simulate dynamics of DC line in the HVDC systems, which is a significant difference in other generic models, such as CDC4T or CDC6T models. The latter models assume that the HVDCs system have an instantaneous response to disturbance coming from the adjacent grid without internal dynamics of converters. These models also have block and bypass functions using some threshold AC and DC voltages to protect against the abnormal condition of HVDC system due to AC grid faults. The CDC7T model, on the other hand, can be utilized to analyze dynamic operations of the DC line and converter controllers. At the same time, the CDC7T model uses general converter controllers and typical configuration of DC line for modeling of several real-operated HVDC systems.

Figure 3 show a configuration of DC line circuit for the CDC7T model. The DC line of CDC7T model consists of overhand lines and cables from the rectifier to inverter. Both overhead lines and cables are represented by DC resistances and equivalent inductances. Note that the cable has also a capacitance and a small resistance to represent the cable damping which is place in series with the cable capacitance. The CDC7T model has no elements affected by frequencies for the overhead lines and cables. Therefore, a fundamental frequency is used for the equivalent inductances and capacitances in the DC line circuit. The CDC7T model also allows to simulate faults in the DC system by adding three fictitious shunt RL to the model as shown in Figure 3. These shunt parameters for simulation of DC line fault should be set to large numbers to have almost zero current flowing through these shunt elements during the normal operation. It means that both inductance and resistance of the shunt elements should be declined for DC line fault simulations; faults on the (1) rectifier DC terminal, (2) inverter DC terminal, and (3) in the center of DC line. Note that L/R ratio for the DC line fault simulations should be 0.1 [23].

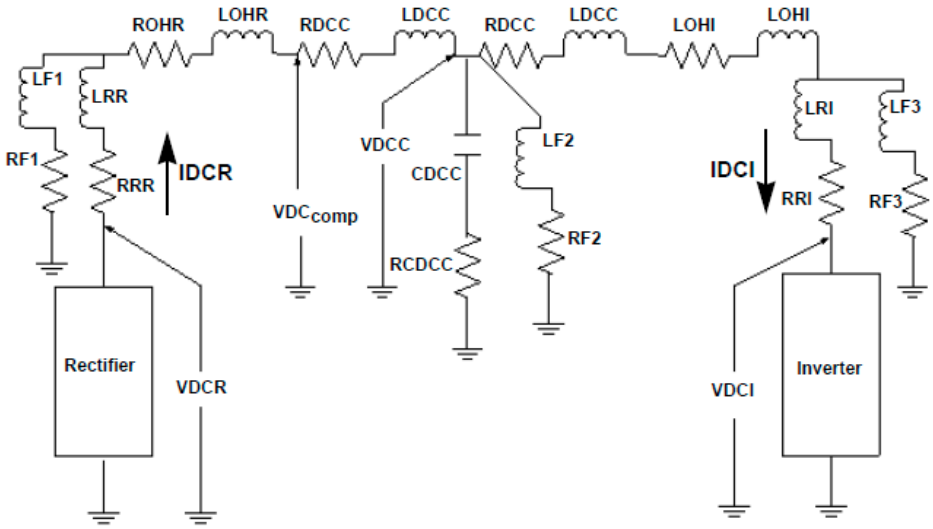


Figure 3. A DC line circuit arrangement of CDC7T [23].

The CDC7T model provides the following three major configurations of converter controls which numerous exiting HVDC systems have; (1) DC current and extinction angle (i.e., gamma) control at the rectifier and inverter, respectively, (2) DC current and voltage control at the rectifier and inverter, respectively, and (3) DC voltage and current control at the rectifier and inverter, respectively. Some real-operated HVDC systems, such as the first-operated and Jeju–Haenam HVDC systems, utilize the control configuration (1). The configuration (2) is general composition for present HVDC systems which have long overhead DC lines or relatively short cables. The control configuration (3) is more appropriate to the HVDC systems having long cables. Figure 4 shows a control diagram of both converters in the CDC7T model, which includes three controllers; (1) DC current, (2) DC voltage, and (3) gamma controllers. The outputs from these three controllers enter

the maximum and minimum selector for the rectifier and inverter side, respectively. The output of mode selector is utilized as an input signal for a PI controller, and then the final output is a firing angle order (i.e., an alpha order). In particular, the DC voltage and gamma controllers in the inverter have extra signal from the Current Error Control (CEC), which proportional to the DC current error to improve stability when AC voltages at the both sides vary. Note that CEC is look-up table composed of non-linear gains which determined to be advantageous to change-slope of the converter characteristic near the operating point. The CDC7T model also has the Voltage Dependent Current Order Limit (VDCOL) algorithm. The compounded DC voltage (i.e., Vdcomp) enters a lag controller which time constant determined by the DC voltage, and then multiplied by a non-linear gain. Note that the time constant of the lag controller is set to up and down value considering increment and reduction of DC voltage, respectively. The non-linear gain for the rectifier and inverter in the VDCOL is look-up table composed of the V_d-I_d characteristics. Finally, a smaller value between the output of the VDCOL and the current order is selected as the input for the DC current controller.

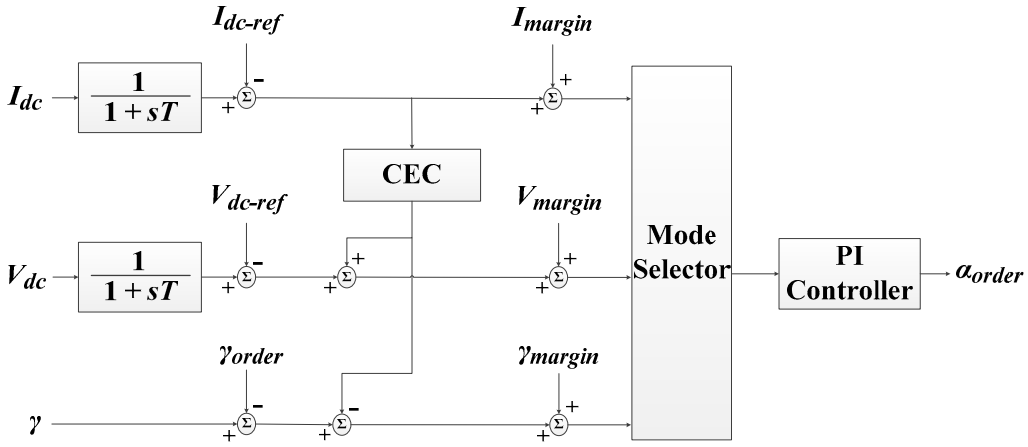


Figure 4. A control diagram of both converters in the CDC7T.

The CDC7T model has 75 parameters which are much more than that of the CDC4T or CDC6T models. However, most of parameters are given by manufacturers for representing their own HVDC system, which is difficult to by modified by the system operator (i.e., Group A). For example, all parameters in the DC line circuit, which is shown in Figure 3, are provided by the manufacturers. Table 3 shows the parameters can be modified by the system operators to validate HVDC system models against the real operating profiles (i.e., Group B). Specifically, shunt inductances and resistances for simulation of DC system faults (i.e., LF1–RF3 in Table 3) are determined by comparing DC current or voltage profiles of real operating HVDC system when DC faults are occurred using trial and error method. This is because these parameters are considerably affected by adjacent grids connected to the HVDC system. The 5 pairs of parameters for VDCOL in both-side converters and time constants for Vdcomp (i.e., Vd1–Id5 and VDCompeR–VDCompI in Table 3) are decided by the HVDC system operation strategies at the abnormal conditions due to commutation failures or AC grid faults. In addition, parameters of DC current order change-rates for blocking and unblocking are set by the system operators based on the HVDC system operation strategies.

2.3. Comparisons with CDC4T & 6T and CDC7T

Table 4 lists functions implemented in the CDC4T, CDC6T, and CDC7T models to describe the HVDC system under the abnormal condition due to AC grid faults. The CDC6T model has delayed block and bypass functions considering communication delays as well as includes all functions of CDC4T. This enables the CDC6T model to block or bypass converter due to AC faults at the other converter side, which is not implemented in the CDC4T model. Both CDC4T and CDC6T models have the VDCOL function and can set

the change-rates of DC voltage and current. Therefore, the system operators can describe recovery times of the DC voltage and current to the rated values, which similar to the those of real HVDC systems, after the AC faults are cleared using the both models. However, both models depict the DC voltage and current profiles briefly without oscillations under the abnormal operation (i.e., commutation failure) caused by the AC grid faults. This is because converter and DC line models are simplified without considering the dynamics for the abnormal operation of the HVDC system. In other words, it is difficult to describe oscillations of DC voltage or current and to identify the maximum DC voltage and current of the HVDC system under the abnormal operation using these models.

Table 3. CDC7T Parameters which can be modified by the system operators (Group B).

Parameters	Descriptions
LF1, RF1	dc fault shunt inductance and resistance at rectifier side [mH, Ohm]
LF2, RF2	dc fault shunt inductance and resistance at mid-line [mH, Ohm]
LF3, RF3	dc fault shunt inductance and resistance at inverter side [mH, Ohm]
VDCompR_Tdown	VDComp down time constant for VDCOL at rectifier [s]
VDCompR_Tup	VDComp up time constant for VDCOL at rectifier [s]
VDCompI_Tdown	VDComp down time constant for VDCOL at inverter [s]
VDCompI_Tup	VDComp up time constant for VDCOL at inverter [s]
GPGR, TIGR	PI-controller proportional and integrator gains at rectifier
GPGI, TIGI	PI-controller proportional and integrator gains at inverter
BLOCK_RATE	rate of current order change when blocking [A/s]
UNBLOCK_RATE	rate of current order change when unblocking [A/s]
$V_{d1\text{-}5}$, $I_{d1\text{-}5}$ (rec, inv)	Parameter of VDCOL function at rectifier and inverter

Table 4. Functions implemented in the CDC4T, CDC6T, and CDC7T to describe the HVDC system under the abnormal condition due to AC grid faults.

Functions	CDC4T	CDC6T	CDC7T
VDCOL	O	O	O
change-rate of DC voltage	O	O	O
change-rate of DC current	O	O	O
minimum alpha, gamma	O	O	O
maximum alpha, gamma			O
BLOCK, BYPASS	O	O	
BLOCK, BYPASS considering delays		O	
converter controller			O
DC-line			O

The CDC7T model, on the other hand, has a DC line model and converter controllers for DC current, DC voltage, and gamma via PI controllers. It means that the CDC7T model is capable to identify the maximum DC voltage and current of the HVDC system when AC faults occur. The CDC7T model can also simulate that both DC voltage and current are restored to the rated values gradually by modifying the change-rate of DC voltage and current as well as VDCOL. This means that the CDC7T model is more suitable for describing the DC voltage and current dynamics of the HVDC system under the abnormal condition due to AC faults than CDC4T or CDC6T models.

3. Proposed Model of HVDC System for Describing Dynamics of DC Voltage and Current

Figure 5 shows a flowchart of the proposed modeling procedure of the HVDC system to enhance calculation of DC voltage and current during the commutation failure caused by AC grid faults. It is integrated with the *Dynamic Simulation* (DS) module in PSS/E. The state variables of various dynamic power devices, including not only the HVDC system but also thermal generators, wind turbines, and synchronous condensers, are initially set to the PSS/E data that are pre-determined based on their actual parameters and operating

conditions. The AC power flow is then calculated in the *Power Flow Calculation* (PFC) module using the initial values. The differential and algebraic equations characterizing the time-varying operations of the dynamic devices are solved for the period of Δt_{step}, based on the power flow calculation results. Specifically, the proposed model consists of the three modules for the AC/DC conversion, controller selection, and DC line model. The variation in the DC current ΔI_{dc} is calculated in the DC-line modeling module, based on the DC-line voltage V_{dc}, the converter firing angle α, and the AC voltage V_{ac} of the converter transformers. In addition, α is updated to α_{new} in the control-mode selection module using V_{dc} and I_{dc}. In the equation conversion module, I_{dc} is updated to $I_{dc,new} = I_{dc} + \Delta I_{dc}$, and V_{dc} is calculated to $V_{dc,new}$ by using $I_{dc,new}$ and α_{new}. The algebraic equations are then solved to update the AC currents I_{ac} that are injected to the AC buses where the HVDC converters are connected. The variables are then used to update I_{ac} to $I_{ac,new}$ for the AC power flow calculation. This iterative process continues until the total simulation time $t_{simulation}$.

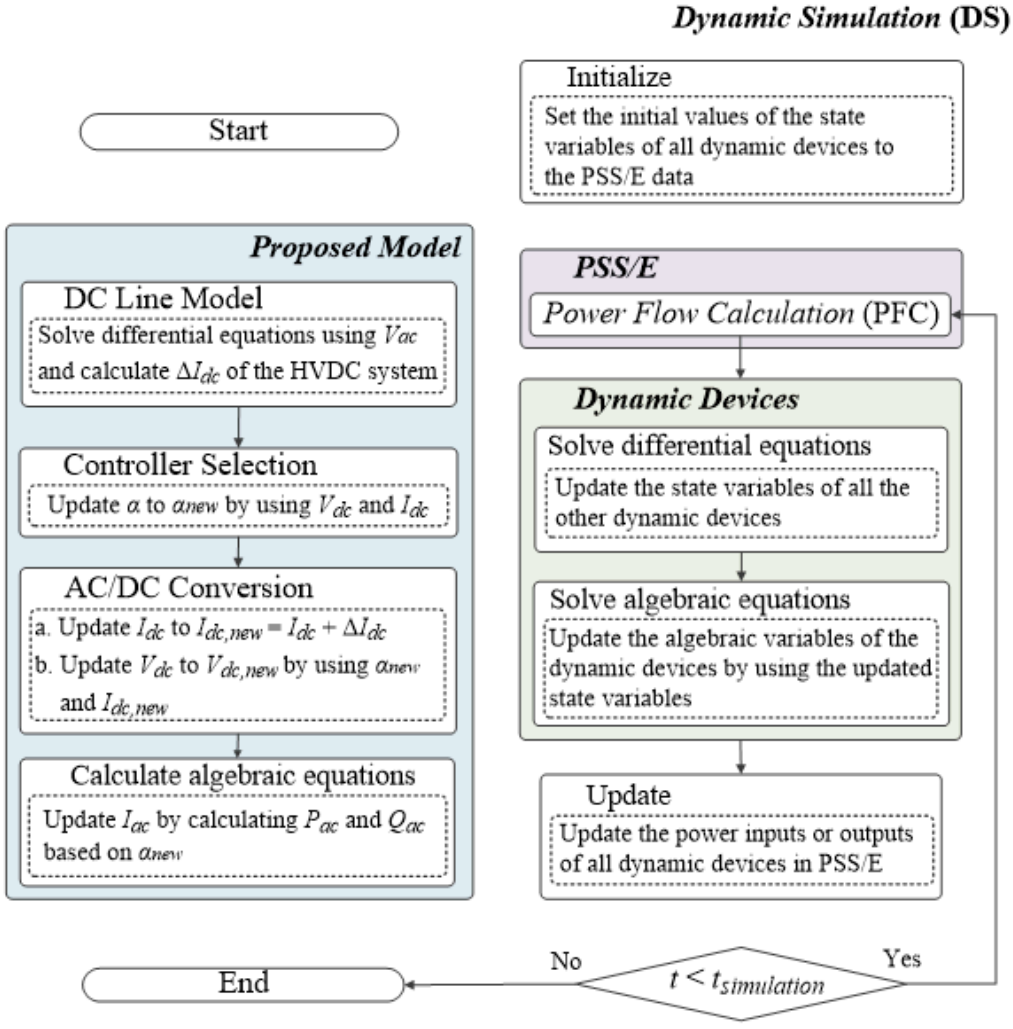


Figure 5. Flowchart of the proposed method for HVDC system modeling to enhance calculation of the DC voltages and current during the AC grid faults.

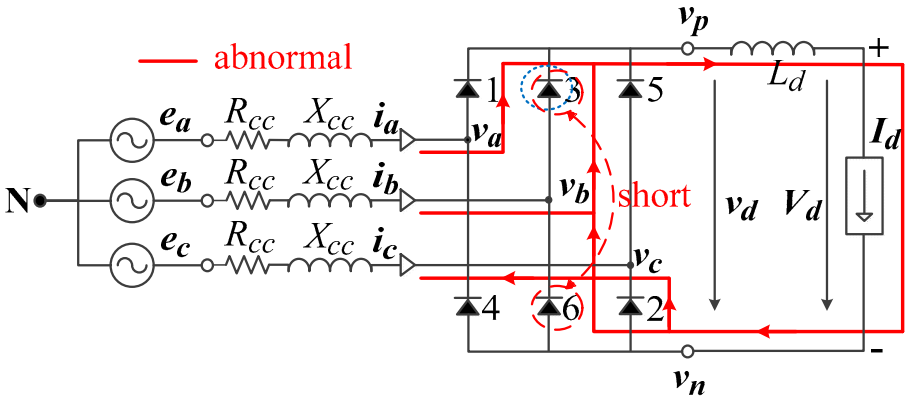
3.1. AC/DC Conversion Module

The main aim of AC/DC conversion module is to calculate the DC voltage of the HVDC system. This module also calculates the active and reactive AC power at the both-side converters to estimate injected AC current flowing into the AC network from the HVDC system during the normal and abnormal HVDC operations. This paper concentrates HVDC system on the abnormal operation caused by the commutation failure. The commutation failure can be occurred when the extinction angle γ is smaller than γ_{min} or when

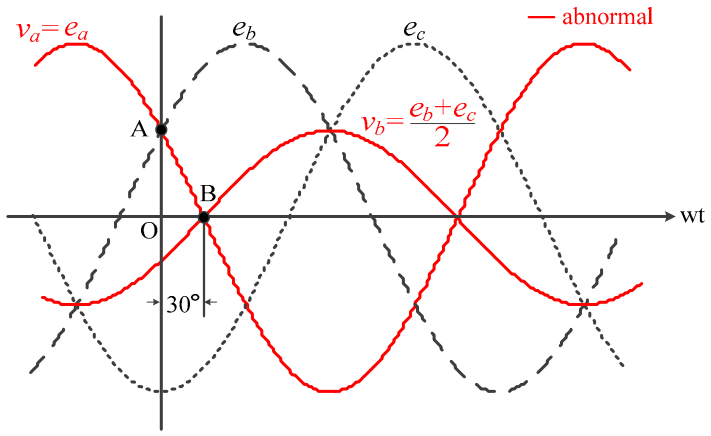
μ is larger than 60° [22,24]. If μ is greater than 60°, the next commutation will commence prior to completion of the current commutation, which results in a short circuit as shown in Figure 6a. In other words, v_a and v_b are same to e_a and $(e_b + e_c)/2$, respectively, as shown in Figure 6b. Therefore, the DC voltage and current can be expressed as Equations (1) and (2), respectively, during the abnormal operation of HVDC system. Note that α is calculated by the controller selection module.

$$V_{dc} = N_c \left(\frac{3\sqrt{6}}{2\pi} E_{acc} (\cos(\alpha - 30) + \cos(\delta + 30)) \right) \tag{1}$$

$$I_{dc} = \frac{1}{\sqrt{6}(X_{cc} + \frac{2\pi}{9} R_{cc})} E_{acc} (\cos(\alpha - 30) - \cos(\delta + 30)) \tag{2}$$



(**a**)



(**b**)

Figure 6. (**a**) Schematic diagram and (**b**) instantaneous voltages of the three-phase converter during the abnormal operation.

V_{dc} then can be obtained using Equation (3) by substituting Equation (2) into Equation (1). Moreover, γ, power factor angle ϕ, and the active power P_{ac} can be calculated using the updated V_{dc}, α, and μ, expressed as Equations (4)–(6), respectively. The reactive AC power Q_{ac} is also calculated by Equation (7) and the injected AC current from the HVDC system to AC grid, which utilized for power flow calculation (PFC), can be obtained using Equations (6) and (7). Using these equations, the proposed method can obtain more accurate DC voltage and current as well as injected AC current flowing from the HVDC system to the AC network during the abnormal HVDC operation cause by the commutation failure. It is

noticeable that the generic models (i.e., CDC4T, CDC6T, and CDC7T) in PSS/E do not consider these equations.

$$V_{dc} = N_c\left(\frac{3\sqrt{6}}{\pi}E_{acc}\cos(\alpha - 30) - \frac{9X_{cc}I_{dc}}{\pi} - 2R_{cc}I_{dc}\right) \tag{3}$$

$$\gamma = \arccos\left(\cos(\alpha - 30) - \frac{\sqrt{6}I_{dc}X_{cc}}{E_{acc}}\right) - 30 \tag{4}$$

$$\tan(\phi) = \frac{2\mu + \sin(2(\alpha - 30)) - \sin(2(\gamma + \alpha))}{\cos(2(\alpha - 30)) - \cos(2(\gamma + 30))} \tag{5}$$

$$P_{ac} = \frac{3N_cE_{acc}^2}{4\pi X_{cc}}(\cos(2(\alpha - 30)) - \cos 2(\gamma + 30)) \tag{6}$$

$$Q_{ac} = \frac{3N_cE_{acc}^2}{4\pi X_{cc}}(2\mu + \sin(2(\alpha - 30)) - \sin(2(\gamma + 30))) \tag{7}$$

3.2. Controller Selection Module

The controller selection module calculates α for the HVDC converters, which can change from DC current control mode to DC voltage control mode, and vice versa, according to converter AC voltages. However, this module is difficult to be implemented using the CIGRE benchmark HVDC model or individual HVDC model having exclusive controllers because of several different *V-I* characteristics of HVDC systems. Therefore, a simple and intuitive HVDC controller is developed to analyze dynamics of the DC voltage and current comfortably in this paper. Note that the proposed controller can be applied to other HVDC systems easily with slight modifications. For example, KEPCO has applied the controller to the Jeju-Jindo HVDC system model [25].

Figure 7 shows a simplified schematic diagram of the proposed controller selection module at the rectifier and inverter side of the Jeju-Haenam HVDC system, as an example. Figure 8 shows a *V-I* characteristic curve for the HVDC system. The proposed controller selection scheme decides the control mode which having the smallest difference between the reference and present DC voltage and current values. For example, in Figure 7a, there are two PI controllers having restricted maximum and minimum output values at the rectifier. If the rectifier operates the DC voltage control mode under the normal operation (i.e., the point X in Figure 8), then the operated DC voltage and current of the rectifier are quite close to V_{dcr} = 1.0 pu and I_{dcr} = 0.5 pu, respectively. In the meantime, the DC voltage and current orders at the rectifier side are V_{dcr_order} = 1.0 pu and I_{dcr_order} = 1.3 pu, respectively, as shown in Figure 8. Therefore, the difference between V_{dcr_order} and V_{dcr} is small and the output value of the rectifier controller $\alpha_{r\_voltage}$ is close to the current firing angle α_r. On the contrary, the DC current controller reduces the output value $\alpha_{r\_current}$ so as to adjust I_{dcr} to I_{dcr_order}. This is because I_{dcr} is obtained from the difference between V_{dcr} and the DC voltage at the middle of DC line. Note that V_{dcr} is proportional to $cos\ \alpha_r$. It means that I_{dcr} increases by reducing α_r which is same to increasing V_{dcr}. Therefore, an updated α_r is same to $\alpha_{r\_voltage}$ because the maximum selector chooses $\alpha_{r\_voltage}$, which is larger than $\alpha_{r\_current}$.

In addition, for the point Y in Figure 8, the rectifier operates the DC current controller when the AC voltage is reduced. The rectifier DC voltage and current are close to V_{dcr} = 0.55 pu and I_{dcr} = 1.3 pu, respectively. V_{dcr_order} and I_{dcr_order} are then same to 1.0 and 1.3 pu, respectively, as discussed above. Therefore, the DC voltage controller decreases $\alpha_{r\_voltage}$ so as to increase V_{dcr} up to V_{dcr_order}. $\alpha_{r\_current}$, on the other hand, is close to current α_r because difference between I_{dcr_order} and I_{dcr} is very small. Consequently, $\alpha_{r\_current}$ from the DC current controller is selected to the updated α_r.

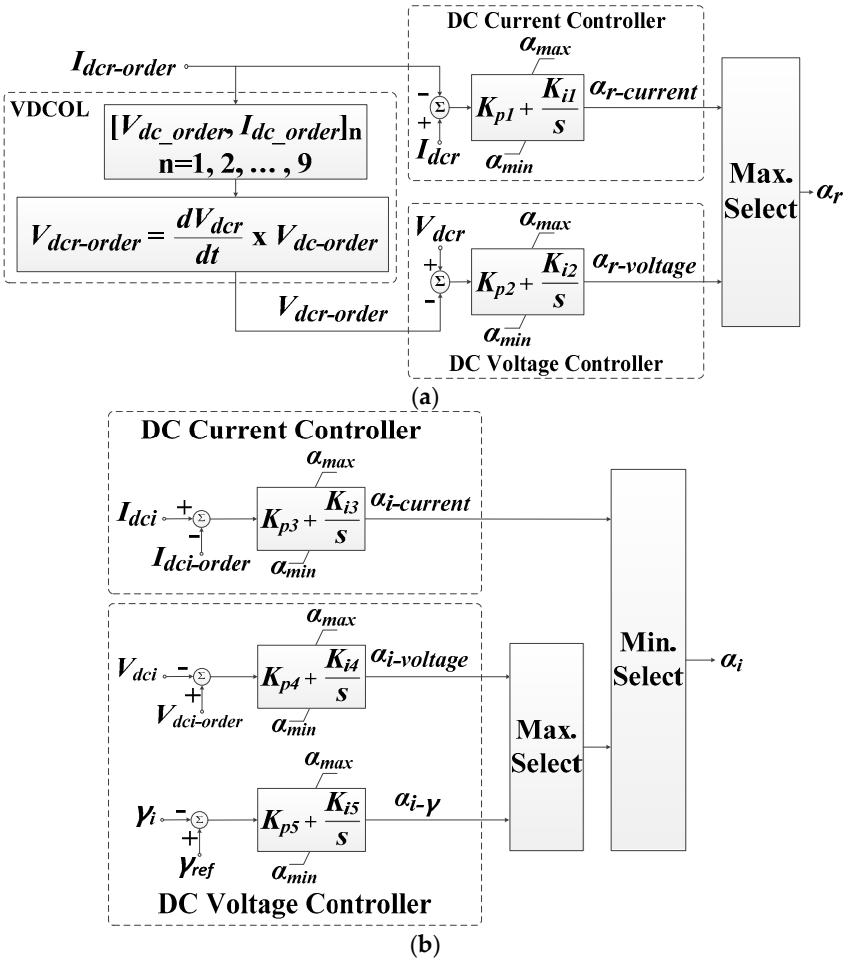


Figure 7. Schematic diagrams of the controller selection module at (**a**) the rectifier and (**b**) the inverter.

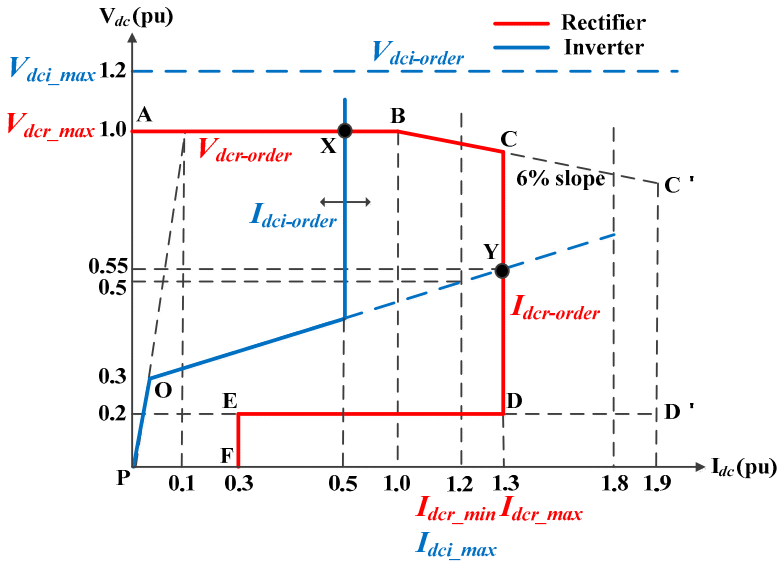


Figure 8. Characteristic V-I curve of the Jeju-Haenam HVDC system.

In particular, the DC voltages at the rectifier and inverter of the Jeju-Haenam HVDC system are controlled to be gradually restored to the nominal value of 1 pu (i.e., $dV_{dcr}/dt \approx 0.2$ pu/s), after the AC line fault is cleared. This is to protect the Jeju AC grid from a sudden variation in the DC power flow during the time period when the HVDC system is recovering from the fault. Therefore, the proposed model includes an additional function for the VDCOL

with a gradual restoration parameter (i.e., dV_{dcr}/dt) in the rectifier controller, as shown in Figure 7a.

The controller selection of the inverter side is analogous to that of the rectifier side, besides the extra PI controller for the γ selection, as shown in Figure 7b. For the point X in Figure 8, the inverter DC voltage and current are quite close to V_{dci} = 1.0 pu and I_{dci} = 0.5 pu, respectively. In addition, V_{dci_order} and I_{dci_order} are same to 1.2 pu and 0.5 pu, respectively. Therefore, the difference between I_{dci_order} and I_{dcr} is quite small that the output value of the inverter controller $\alpha_{i\_current}$ is adjacent to the current inverter firing angle α_i. However, the output value $\alpha_{i\_voltage}$ is increased by the DC voltage controller to increase V_{dci} up to V_{dci_order}; V_{dci} is proportional to cos (π-α_i). Therefore, $\alpha_{i\_voltage}$ from the DC voltage controller is selected to the updated α_i by the minimum selector because $\alpha_{i\_voltage}$ is smaller than $\alpha_{i\_current}$. Analogously, for the point Y in Figure 8, the inverter controls the DC voltage. The supplementary γ controller is not explained for brevity.

3.3. DC Line Model Module

In the DC line model module, the rectifier and inverter DC currents are obtained using the updated DC voltages (i.e., Equation (8)) during the abnormal operating conditions, as well as α_r and α_i for every time-step Δt_{step}. Figure 9 shows a general schematic diagram of the proposed DC line model using N π-sections.

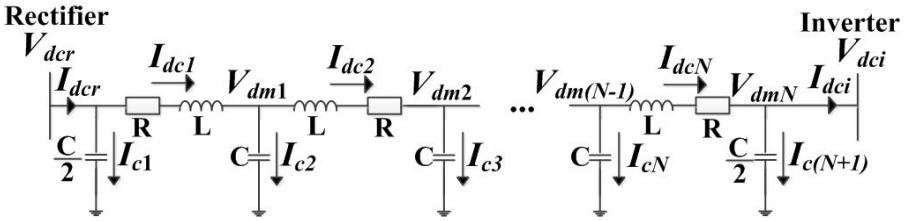


Figure 9. A schematic diagram of proposed DC line model using N π-sections.

The conventional DC-line model (i.e., T-equivalent model) have been used in previous papers [26,27] because of its simplicity. However, the model may lead to over-estimation of the fault current, particularly when a commutation failure occurs due to AC grid faults such as single- or three-phase line-to-ground faults. Specifically, in the conventional DC-line model, the DC voltages at the middle point V_{dm} and V_{dci} are used to calculate the fault current. In the proposed model, on the other hand, it is affected mainly by the difference between $V_{dm(n\text{-}1)}$ and V_{dmn}, as shown in Figure 9. The difference between $V_{dm(n\text{-}1)}$ and V_{dmn} can result in more accurate fault current than that between V_{dm} and V_{dci}. This is because the actual DC line has a uniformly distributed resistance R, inductance L, and capacitance C. Therefore, the DC voltage and current are affected by the several sections punctuated in the DC line.

However, as the number of π-sections increases, the number of differential equations for calculating I_{dci} also increases and, consequently, it makes it difficult to set the PI gains (e.g., K_{p3} and K_{i3} in Figure 7) in the both-sides controllers. Therefore, in this paper, three π-section lines (i.e., N = 3) was utilized considering both precision of DC line model and computational complication.

4. Case Studies and Results

4.1. Test System and Simulation Conditions

Figure 10 shows a simplified schematic diagram of the entire AC network of Korea as a test grid. The test system includes the mainland and Jeju Island; the corresponding PSS/E data were used for simulation case studies. Note that the PSS/E data for the Korea grid in 2015 haves 382 generators, 1275 loads, and 1834 buses, which was comprehensively discussed in [28]. Table 5 summarizes the detailed parameters of the Jeju-Haenam HVDC system. All the parameters were obtained considering the various operating features of the real-operated Jeju-Haenam HVDC system [29]. Note that the DC-winding resistance

R_{cc} of the converter transformer has been set to zero for simplicity in this paper because it remains unknown. The reactance X_{cc} of the converter transformer more significantly affects the transient responses of the HVDC converters than R_{cc} [30].

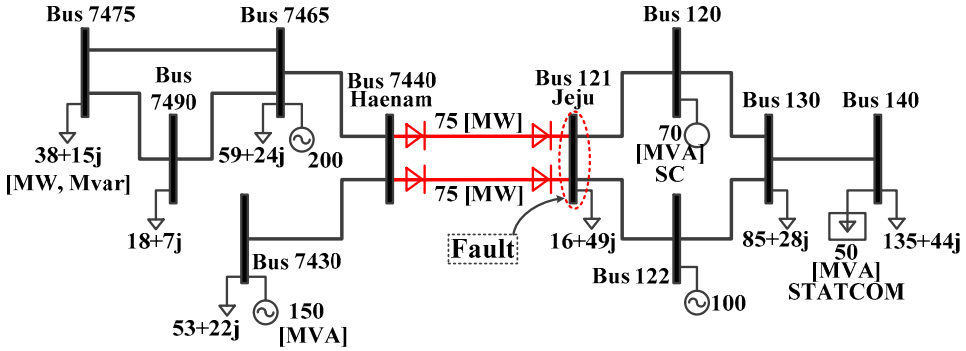


Figure 10. Simplified schematic diagram of the AC network and the Jeju-Haenam HVDC system.

Table 5. Detailed parameters of the Jeju–Haenam HVDC system.

	Parameter	Value	Parameter	Value
Parameters for PSS/E	P_{rated} (MW)	75	V_{rated} (kV)	184
	N_c	2	R	0.744
	X_{cc}	7.99	L	133.33
	R_{cc}	0	C	27
Parameters for the proposed model	V_{dcr_max} (pu)	1	V_{dci_max} (pu)	1.2
	I_{dcr_min} (pu)	1.2	I_{dcr_max} (pu)	1.3
	I_{dci_max} (pu)	1.2	α_{max} (°)	165
	α_{min} (°)	5	γ_{ref} (°)	18
	K_{p1}	0.01	K_{i1}	0.001
	K_{p2}	1.3	K_{i2}	2.5
	K_{p3}	1.42	K_{i3}	5.5
	K_{p4}	0.01	K_{i4}	0.01
	K_{p5}	0.1	K_{i5}	0.01

The generic, conventional, and proposed HVDC system models were comprehensively tested and analyzed for the case where the AC line fault occurred in the weak Jeju AC network. Note that the conventional model does not consider the abnormal condition in the equation conversion module and uses T-model for the DC-line. Specifically, the AC single- and three-phase line-to-ground faults are selected for the events because these faults affect the power grid operation most frequently and seriously, respectively [31]. The SCR and effective SCR (ESCR) of the Jeju AC network are estimated as 4.0 and 2.3, respectively [25,32]. Therefore, operations of the HVDC system were investigated when AC line faults occurred at the inverter side (i.e., Bus 121 in Figure 10) in the case studies. The simulation results for the generic and proposed HVDC models were compared with the measured data from the real-operated Jeju-Haenam HVDC system. These were also compared with the simulation results acquired using the comprehensive HVDC system model in PSCAD [32]. The CDC6T and CDC7T models are utilized as generic models of the HVDC system and some parameters of the models, discussed in Section 2, were modified to describe the actual operating data. Note that Δt_{step} was set to 8.30 ms, 4.15 ms and 70 µs in the generic and proposed models and the PSCAD model, respectively. For comparison with the real measured data, the single-phase line-to-ground fault was occurred during 0.015 s at the inverter side of the HVDC system at t = 0.5 s. For comparison with the PSCAD simulation result, it was assumed that a three-phase line-to-ground fault occurred during 0.1 s at the inverter side at t = 0.5 s. Table 6 lists modified values of the generic models for describe the real measured data from the real-operated Jeju-Haenam HVDC system.

Table 6. Modified values of the generic models for the Jeju-Haenam HVDC system.

Model	Parameters	Values
CDC4T, CDC6T	VBYPAS	300
	VRAMP	0.4
	V1, V2	200, 250
CDC6T	VDEBLK	0.7
	TDEBLK	0.1
	TREBLK	0.1
	VACBYP	0.7
	TDEBYP	0.1
	TINBLK	0.1
	TINBYP	0.1
CDC7T	VDCompR_Tdown	0.01
	VDCompR_Tup	4.15
	VDCompI_Tdown	0.01
	VDCompI_Tup	0.15
	GPGR	2.1
	TIGR	0.02
	GPGI	0.5
	TIGI	0.1

4.2. Single-Phase Line-to-Ground Fault

Figure 11 shows the inverter DC voltages for the proposed, conventional, comprehensive, and real-operated HVDC models, respectively, when a single-phase line-to-ground fault occurred in the inverter side network (i.e., the Jeju grid). In particular, the red line in Figure 11 shows the real-measured data on the DC voltage at the inverter side when an A-phase line-to-ground fault occurred at the Jeju station on 6 February 2015. The inverter DC voltage rapidly increased to 141 kV with a short time-delay after the fault, mainly because of a smoothing reactor on the DC line. The inverter DC voltage then slowly reduced to the rated voltage. Analogously, the inverter DC voltage also increased to 145 kV after the fault occurred using the proposed model, which is very close to the peak value in the real-measured data. In the conventional model, on the other hand, the inverter DC voltage increased to 238 kV after the fault occurred, which is much larger than the peak value in the real-measured data. This is because the proposed modeling method improved the estimation of the DC voltage by calculating (3) under the single-phase line-to-ground fault situation. However, the conventional model calculated the inverter DC voltage in the AC/DC conversion module without considering the abnormal HVDC operation (i.e., Equation (3)). In addition, the inverter DC voltages of the real-operated and proposed HVDC systems are almost same in the steady-state situation after the fault cleared. In Figure 11, the proposed and conventional HVDC model restored the inverter DC voltage faster than the real-operated HVDC system after the fault cleared (particularly after t = 0.6 s). This is mainly because in the PSS/E, the valve or firing control was calculated using Equation (4) for simplicity rather than obtained using physical model. In the real system, the firing controller has time delays of 5–10 ms. The time delays of the firing controller were implemented in the proposed HVDC system model using PSCAD. It can be seen in Figure 11 that the DC voltage of the comprehensive PSCAD model recovered slowly, consistent with the real operating data. The maximum DC voltage was equal to 144 kV in the comprehensive model. Therefore, the proposed model can estimate the maximum DC voltage similar to the real-operated system as well as the comprehensive PSCAD models.

Figure 12 shows the comparisons between the DC currents at the inverter side for the real-measured data and the three different models. The corresponding maximum fault currents are summarized in Table 7. For the proposed model, the maximum fault current was 2375 A, which is almost similar to that for the real-operated system and PSCAD model, i.e., 2380 A and 2363 A, respectively. However, the maximum value of inverter DC current was 3120 A in the conventional model, which is much higher than the maximum value from

the real-operated system. This is mainly because the proposed model used 3 π-sections for the DC line model while the conventional DC-line model used the T-equivalent model. In other words, the voltage difference between V_{dm} and V_{di} in Figure 9 of the proposed model was smaller than that of the conventional model. Note that the maximum fault current is one of the important values to decide appropriate set-parameters of protection relay, DC line capacity, and AC/DC converter valve capacity [20,21]. The case study shows that the proposed model can calculate more accurate maximum DC current as well as DC voltage, and therefore the proposed HVDC model can be effectively utilized to analyze AC networks connected to HVDC systems considering AC grid faults.

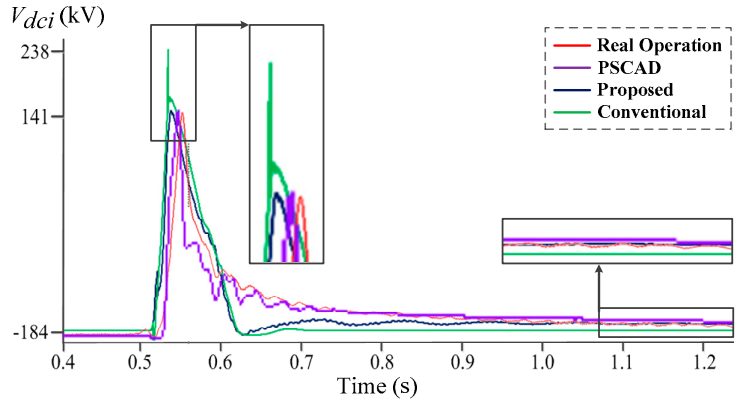


Figure 11. Inverter DC voltage for a single-phase line-to-ground fault.

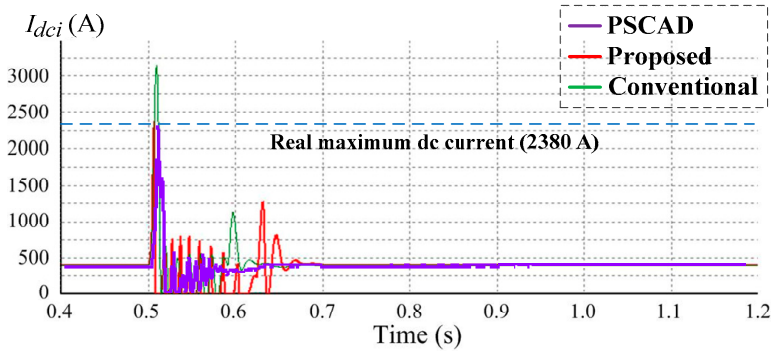


Figure 12. Inverter DC current for a single-phase line-to-ground fault.

Table 7. Summary of the maximum DC voltages and currents at the inverter for the single-phase line-to-ground fault.

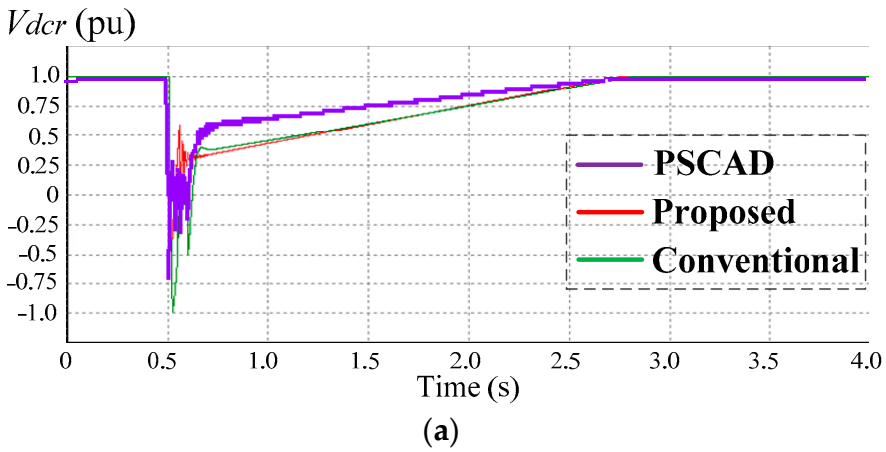
Key Factors	Real Data	PSCAD		Proposed		Conventional	
		Value	Error (%)	Value	Error (%)	Value	Error (%)
V_{dci} (kV)	141	144	2.1	145	2.8	238	68.8
I_{dci} (A)	2380	2363	0.7	2375	0.2	3120	31.1

4.3. Three-Phase Line-to-Ground Fault

Figure 13 shows the rectifier DC voltage and current when the three-phase line-to-ground short-circuit fault occurred in the inverter side at t = 0.5 s during 0.1 s. As shown in Figure 13a, the comprehensive PSCAD model and the proposed model both resulted in similar DC voltage profiles and the minimum DC voltage (i.e., −126.4 kV and −121.1 kV, respectively) at the rectifier side during the fault, whereas the conventional model resulted in larger peak values (i.e., −180.5 kV). This is mainly because the proposed model considered the abnormal operation of the HVDC system in the AC/DC conversion module. In Figure 13a, the DC voltage of the three models increased gradually after the

fault-clear at t = 0.6 s. This is because the real-operated HVDC system are designed to restore the DC voltage slowly (around 0.2 pu/s) after the fault-clear to protect the inverter-side week grid (i.e., Jeju Island). This was reflected in the proposed model controller so that the DC voltage is restored gradually to the rated voltage after the fault-clear (i.e., during 0.6 < t < 2.7 s). During the period of the HVDC system recovery, the slopes of the DC voltage variations slightly differed for the PSCAD and proposed models. This is mainly attributed to the fact that the DC voltages in the proposed models were estimated using (3), where the time delay of the firing control units was not reflected. In Figure 13b, the rectifier DC voltage of the CDC6T model decreased sharply and maintained zero without oscillations during the fault. This is because the CDC6T model does not consider the internal dynamic behavior by modeling the converter using simple transducer delay blocks. In other words, the CDC6T model cannot describe the internal dynamic behavior of converters. The CDC7T model, on the other hand, had DC voltage drop and oscillations after the fault because the DC circuit and converter controllers are implemented in the CDC7T model as shown in Figure 13c. However, the minimum DC voltage of the CDC7T model (i.e., −147.2 kV) during the fault was relatively differ from the value of proposed and PSCAD models because the AC/DC converting equations for the abnormal operation are not applied to the CDC7T model. The gradual increases of the DC voltage were also depicted by the generic models using the VDCOL function. Note that the maximum DC voltage is mainly considered in case studies because it is utilized to calculate the maximum fault current, and consequently designing protective relays, transmission line capacities, and converter values. Therefore, the proposed model can be utilized effectively for designing these elements.

In addition, Figure 14 shows the comparison between the inverter DC current for the PSCAD, proposed, conventional, and generic models. Both the PSCAD and proposed models had analogous peak currents of approximately 3.6 pu, whereas the conventional and generic CDC7T models resulted in larger and smaller peak of 3.9 pu and 2.4 pu, respectively. The inverter DC current for the CDC4T and CDC6T models decreased sharply and maintained 0.3 pu and zero, respectively, without peak value during the fault. This is because the both models do not consider the internal dynamic behavior in the converter. In Figure 14b, the difference of DC currents between two models was caused by the additional protection functions for the CDC6T model, as discussed in Section 2.1. It is notable that the rectifier DC current of the CDC7T recovered gradually after the fault, which is differ to the PSCAD and the proposed models, because the DC current is affected by the DC voltage via VDCOL in the CDC7T model. It implies that the CDC7T model is more suitable to estimate the peak value of the DC current roughly than to investigate recover trend of the DC current accurately.



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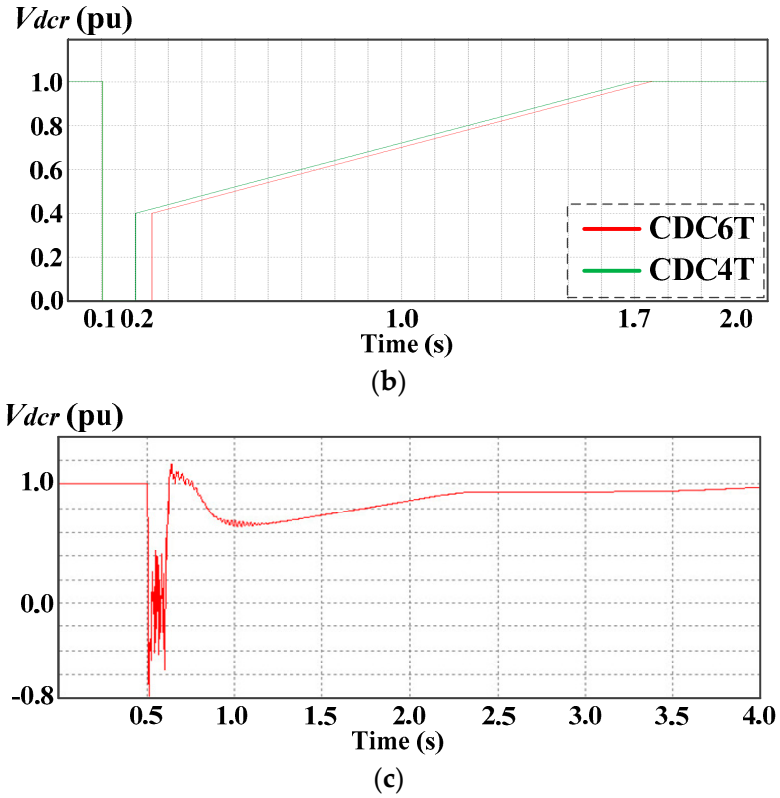

Figure 13. Rectifier DC voltage for a three-phase ground fault: (**a**) PSCAD, proposed, and conventional; (**b**) CDC4T and CDC6T; (**c**) CDC7T.

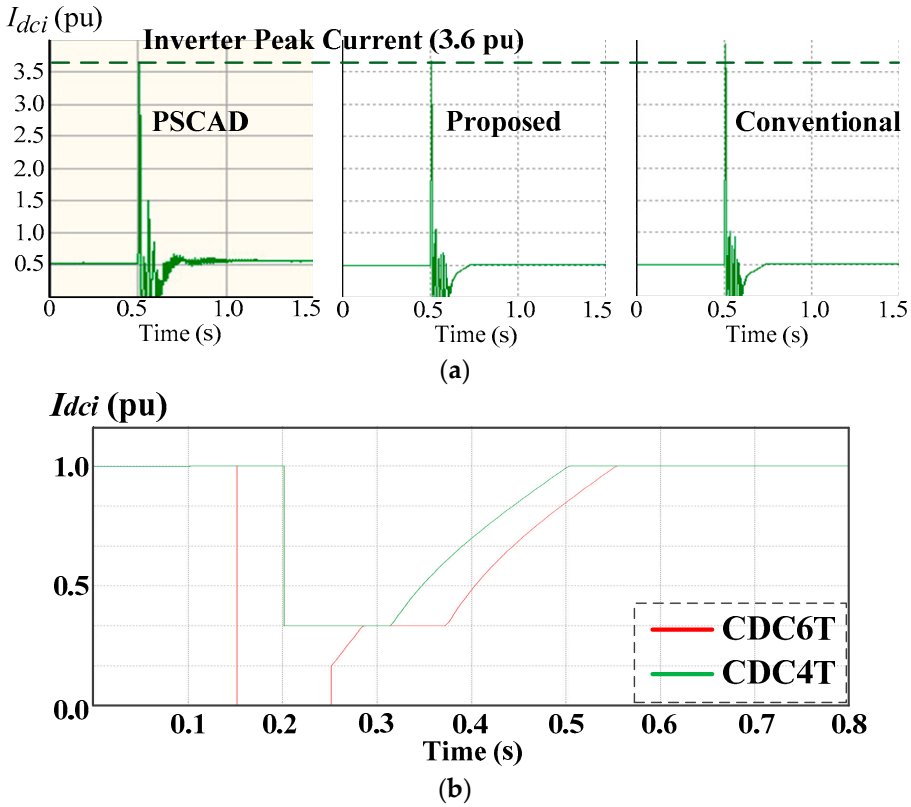

Figure 14. *Cont.*

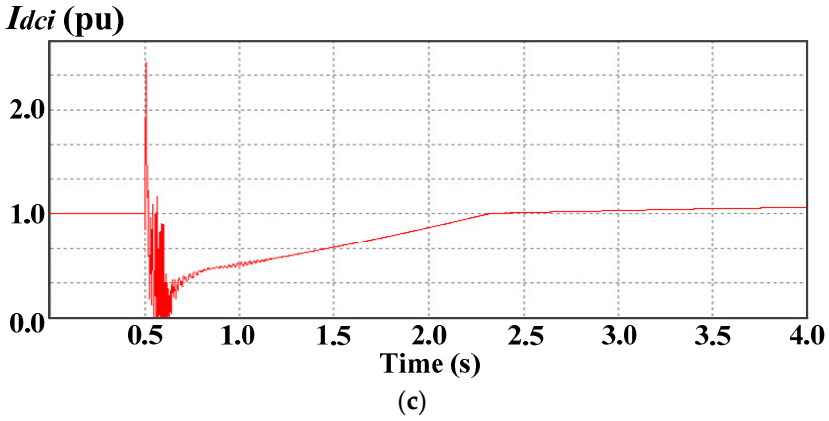

Figure 14. Inverter DC current for a three-phase ground fault: (**a**) PSCAD, proposed, and conventional; (**b**) CDC4T and CDC6T; (**c**) CDC7T.

Table 8 summarizes the minimum (or maximum) DC voltage and current for the four different HVDC models. It can be seen that the difference between the comprehensive PSCAD model and the proposed model small compared to the CDC7T model. The simulation results show that the proposed model is appropriate to analyze the DC voltage and current dynamics during the fault and to estimate the maximum values of DC voltage and current. In addition, the CDC7T model can simulate the dynamics of the DC voltage and current after the fault, however the difference of the maximum (or minimum) value to the PSCAD model are larger than the proposed model. Note that the CDC6T model is difficult to simulate the dynamics of DC voltage and current, which resulted in largest errors. Table 9 summarizes the characteristics of the proposed and generic HVDC models in PSS/E to analyze HVDC systems under abnormal operation caused by the AC grid faults.

Table 8. Summary of the maximum DC voltages and currents at the inverter for the three-phase line-to-ground fault.

Key Factors	PSCAD		Proposed		Conventional		CDC7T	
	Value	Error (%)	Value	Error (%)	Value	Error (%)	Value	Error (%)
V_{dcr} (kV)	−126.4	-	−121.1	4.2	−180.5	42.8	−147.2	16.4
I_{dci} (A)	1465	-	1469	0.3	1546	5.5	976	33.4

Table 9. Summary of characteristics for the proposed and generic HVDC models in PSS/E to analyze HVDC systems under abnormal operation cause by the grid faults.

Characteristics	Proposed	Conventional	CDC4T	CDC6T	CDC7T
Converter	normal/ abnormal	normal	none (time delay)	none (time delay)	normal
DC line	N π-sections	T-equivalent	none	none	T-equivalent
Controller	V_{dc}, I_{dc}, γ	V_{dc}, I_{dc}, γ	V_{dc}, I_{dc}	V_{dc}, I_{dc}	V_{dc}, I_{dc}, γ
Converter dynamics	O	O	X	X	O
Slow V_{dc} restoration	O	O	O	O	O
Fast I_{dc} restoration	O	O	X	X	X
Estimation max. V_{dc}, I_{dc}	O	O	X	X	O
Max. error max. V_{dc}, I_d	4.2%	42.8%	-	-	33.4%

5. Conclusions

This paper described analyses of generic LCC-based HVDC system models and proposed a novel modeling method for an LCC-based HVDC system in the PSS/E simulation. In this paper, the characteristics and limitations as well as parameter investigations of generic HVDC models (e.g., CDC4T, CDC6T, and CDC7T) were conducted to indicate the

maximum DC voltage and current of the HVDC system in the abnormal operation, i.e., commutation failure due to AC line-to-ground faults. The CDC6T model has additional protection schemes compared to the CDC4T model, and both CDC4T and CDC6T models are not concerned with the internal dynamic behavior of converters. The CDC7T model, on the other hand, can be utilized to analyze dynamic operations of the DC line and converter controllers. Furthermore, the proposed modeling method had three modules developed for the AC/DC conversion, controller selection, and DC line model. In particular, the AC/DC conversion module was developed considering the abnormal operation of HVDC system. The DC line was modeled using multiple π-sections for accurate estimation of the DC voltages and currents. The case study results showed that the specific generic HVDC models in PSS/E (i.e., CDC7T) can simulate the dynamics of the DC voltage and current after the fault, however, the maximum values of the DC voltage and current can be differed from the real-measured data. The case study results also showed that the proposed modeling method effectively improves the estimation of the DC voltage and current variations for single-phase and three-phase line-to-ground faults. In addition, the simulation results showed that the proposed model has a limitation for describing time delays of the firing controller in the converter due to restriction of simulation time-steps for PSS/E. Further work will focus on implementing various real-operated LCC-based HVDC systems which have different size and control types by using the proposed modeling method. Moreover, applications of the proposed method to VSC-based HVDC systems are required for the future work.

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