energies

MDPI

Article

Variable Speed Drive DC-Bus Voltage Dip Proofing

Freeman Chiranga and Lesedi Masisi *

School of Electrical and Information Engineering, University of the Witwatersrand, Johannesburg 2000, South Africa; 2288056@students.wits.ac.za
* Correspondence: Lesedi.Masisi@wits.ac.za

Abstract: This paper proposes a power electronic module that uses a switched capacitor for retaining the integrity of the dc-link voltage of a variable speed drive (VSD) during a 0.2 s short-term power interruption (STPI). Ride-through was achieved through switched capacitor onto the dc bus. However, this technique presents a challenge of the high inrush currents during a ride through compensation. In this work both analytical and experimental investigations were conducted in order to reduce the in-rush currents and its impact on the performance of the VSD during the STPI. Inrush peak currents were reduced by approximately 90%. Experimental results showed torque pulsations of 12.8% and 14.3% at the start and end of dc-link voltage compensation, respectively. A method for sizing the switched capacitor and the inrush limiting resistors is proposed. This methodology is based on the use of readily available nameplate information of the VSD and the electric motor. The proposed module can be retrofitted to existing VSDs that are based on v/f control.

Keywords: variable speed drive; short-term power interruption; ride-through; dc-link; inrush current; voltage compensation

Citation: Chiranga, F.; Masisi, L. Variable Speed Drive DC-Bus Voltage Dip Proofing. *Energies* **2021**, *14*, 8257. https://doi.org/10.3390/en14248257

Academic Editor: Santiago de Pablo

Received: 7 October 2021
Accepted: 16 November 2021
Published: 8 December 2021

1. Introduction

Electricity supply in developing economies is characterized by low generation and dominated by frequent faults and outages owing to lack of financial resources, old infrastructure and poor maintenance [1–3]. Voltage dip sensitive equipment including variable speed drives (VSD) are negatively affected by such frequent faults and outages leading to voltage dip-related trips. This results in disruptions of critical processes, loss of production and revenue [4]. Various transmission grid codes have a common way of defining which grid disturbances have to be tolerated. They also specify frequency of occurrence of these disturbances. VSDs are used to drive critical processes in power generation equipment and they are required to be able to ride-through a 0.2 s short-term power interruption (STPI) [5,6]. Studies carried out by numerous researchers to analyse the behaviour of a VSD during a voltage dip, have identified the dc-link under voltage as the main reason for the VSD tripping during a voltage dip [7–9]. There is an abundant number of VSDs on the market of different makes and models which gives rise to differences in susceptibility and response to voltage dips and STPI [9]. Existing VSD topologies can be modified to enhance their ride-through capability. Most modifications to existing topologies would require close collaboration with different manufacturers to access design base technical information. Such arrangements present challenges due to intellectual property which is closely guarded by manufacturers and thus not readily available for access by users of VSDs. Modifications to the drives must then be limited to an electrical connection only between the existing VSDs and ride-through enhancing module. This results in limited options available for enhancing ride-through capability for existing VSDs.

A VSD with a passive front end diode rectifier has limited response possibilities during a voltage disturbance which makes it sensitive to voltage dips [10–12]. Reference [13] developed a stacked switched capacitor for energy buffer on the dc bus and developed a switching scheme for the buffer switches. Voltage fault ride through is achieved in [12]

through the use of field-oriented control. Various researchers have investigated alternatives of improving the ride-through capability of a VSD to voltage dips [10,11,14–16]. These alternatives can be grouped into those that allow ride-through for a total loss of power under an STPI and those that do not. Invariably, those that can offer ride-through for a STPI incorporate an energy storage device. Several STPI ride-through improvement alternatives incorporating energy storage are available to provide the required additional dc-link power. These include either ordinary or super-capacitors, battery based back-up systems, flywheel based energy storage, motor-generator sets, storage based on super conducting magnetic energy and fuel cells [14,17–20].

The simplest alternative for improving STPI ride-through involves increasing the overall dc-link capacitance. Most VSDs are equipped with an electrolytic capacitor on the dc-link. This capacitor is used primarily for filtering the dc-link voltage, providing limited energy storage for a VSD to ride-through minor voltage dips and providing a low impedance path for high frequency inverter currents [19]. Typical capacitance values are between 75–360 μF/kW [15]. Although a larger capacitor is preferred in order to strongly hold the dc link voltage for longer during a STPI, big capacitance tend to cause harmonic pollution onto the supply.

To be able to ride through a STPI, a sufficient energy reserve is required. A variety of energy storage technologies are candidates for providing the required power during a STPI. Battery backup systems, supercapacitors, motor-generator sets, flywheel energy storage systems, superconducting magnetic storage and fuel cells are some examples of these technologies [7]. For low voltage (<1000 V), low power (10 kW) applications, ordinary capacitors, super-capacitors and batteries are suitable candidates [14]. A boost converter maintains the dc-link voltage to a set point during the dip. The boost converter can be connected to the dc-link of a VSD, but more commonly is connected in parallel to the VSD. It uses the remaining voltage during a dip, to supply the dc-link. They do not use an energy storage device. Boost converters can be integrated into new drives between the rectifier and the dc-link capacitors or retrofitted as an add-on module [11,14]. During a voltage dip, the boost converter will sense a drop in the dc-link voltage and begin to regulate the dc-link to a minimum voltage required by the inverter. However, when the supply is completely lost due to a fault, the boost converter loses capability for ride through dip voltage. This paper proposes the use of a switched capacitor onto the VSD dc bus for a 0.2 s STPI ride through capability. Since the additional capacitor is only introduced during a dc bus voltage dip the power quality of the supply is not compromised during the healthy supply of power to the VSD. The power electronic module used to switch the capacitor onto the dc bus is equipped with the necessary inrush current limiting technique. The impact of switching a capacitor onto the dc bus was investigated based on motor performance and the dc bus performance. The work also proposes power electronic module sizing methodology based on the motor and VSD nameplate data.

The paper is organized as follows, Section 2 provides the behavior of the VSD under STPI and Section 3 proposes dc-link voltage dip compensation module. Section 4 is concerned with proposed sizing methodology for voltage dip compensation module, Section 5 with simulation results and analysis, Section 6 with experimental results, Section 7 with the overall analysis of results, and Section 8 with the conclusion.

2. Variable Speed Drive under Short-Term Power Interruption (STPI)

A voltage dip or STPI on the incoming AC supply of a VSD causes a drop in the dc-link voltage. If supply restoration is delayed, this can lead to a low dc-link voltage protection trip. VSDs are equipped with protection mechanism to guard against low dc-link voltage in order to guarantee good control and avoid damage to equipment. A number of studies have been carried to assess the tolerance of VSDs to voltage dips and STPIs [5,10,21]. Results indicate that most VSDs are most sensitive to three-phase dips and STPIs, less sensitive to two-phase dips and least sensitive to single phase dips. To ride through a STPI will depend on the size of the VSD dc link capacitor. The challenge is that in several

industries, VSDs were designed for certain STPI duration. A comparison of VSDs from different manufactures indicates that most VSDs can only survive a STPI of up to 0.05 s. The energy within a VSD-motor-load system during a STPI can be represented by (1),

$$E_L = E_c + E_{kin} \quad (1)$$

where E_L is the total load energy, E_C is the energy supplied by the capacitor and E_{kin} is the kinetic energy in the rotating masses. During a STPI, the capacitor and rotating masses provide energy E_L to the load, resulting in the reduction of capacitor voltage and motor performance. E_L can be expressed as in (2),

$$E_L = \frac{C}{2}\Delta V_c^2(t) + \frac{J_l}{2}\Delta\omega^2(t) = \int_{t_1}^{t_2} T_l \omega \delta t \quad (2)$$

where T_l is the load torque, J_l is inertia, C is the dc-link capacitance, V_C is capacitor voltage, ω is speed of rotating assembly and t_2–t_1 is the duration of the STPI. From (2), it can be concluded that the behavior of a VSD during a STPI is influenced by three main parameters: C which determines the electric energy E_C stored in the dc-link, J_l which determines the kinetic energy E_{kin} stored in the rotating parts and the motor load T_l. For the same load torque, a VSD with a large capacitance driving a load with a high inertia has a better chance of riding through a voltage dip as compared to lower capacitance and motor inertia.

At the end of the STPI, i.e., when supply is restored, large inrush currents can be experienced due to reduced VSD dc link capacitor voltage. If not controlled, this inrush current can cause nuisance tripping of protective devices, damage VSD components and cause undesirable torque pulsations. The magnitude of inrush current is largely dependent on the capacitor voltage at the end of the STPI. A lower capacitor voltage results in a higher inrush charging current. Low dc-link voltage protection is incorporated to ensure that the capacitor does not discharge excessively which would otherwise lead to high inrush currents. During initial powering, inrush current is limited by use of a pre-charge resistor based circuit [22].

3. Proposed DC-Link Voltage Dip Compensation

The proposed voltage dip compensating module (module) was developed to ensure a 0.2 s ride-through capability of a 1.5 kW VSD while striving to sustain demanded motor load. This work only focus on V/f controlled VSDs as they are predominantly used in industry. The proposed module was required to be active only during an STPI and when charging in order to minimize harmonic pollution onto the grid associated with an increased capacitance on the dc link. Ride-through requirements are listed in Table 1.

Table 1. Ride-through requirements.

Ride-through duration	0.2 s
Voltage dip	STPI
Minimum acceptable dc-link voltage	0.85 V_{dc}
Maximum permissible discharge current [1]	4.1 A
Maximum permissible charging current [2]	8.4 A

[1] VSD (variable speed drive) maximum output current; [2] VSD inrush current.

Figure 1 shows the proposed module developed for retaining the dc bus voltage using a switched capacitor C_a. C_e is the existing VSD dc bus capacitor. The switches T_c and T_d controlled the charging and discharging of C_a, respectively. The diodes (D_c and D_d) were installed to prevent IGBT freewheeling diodes from conducting whenever the respective IGBT was switched off and thus allowed the flow of power in one direction in each of the charging and discharging circuits. The resistor R_C, that was installed on the charging leg of C_a limited inrush current to be within VSD rectifier device ratings during charging of C_a.

Resistor R_d installed on the discharging leg limited the inrush current when module was activated as C_a charged C_e.

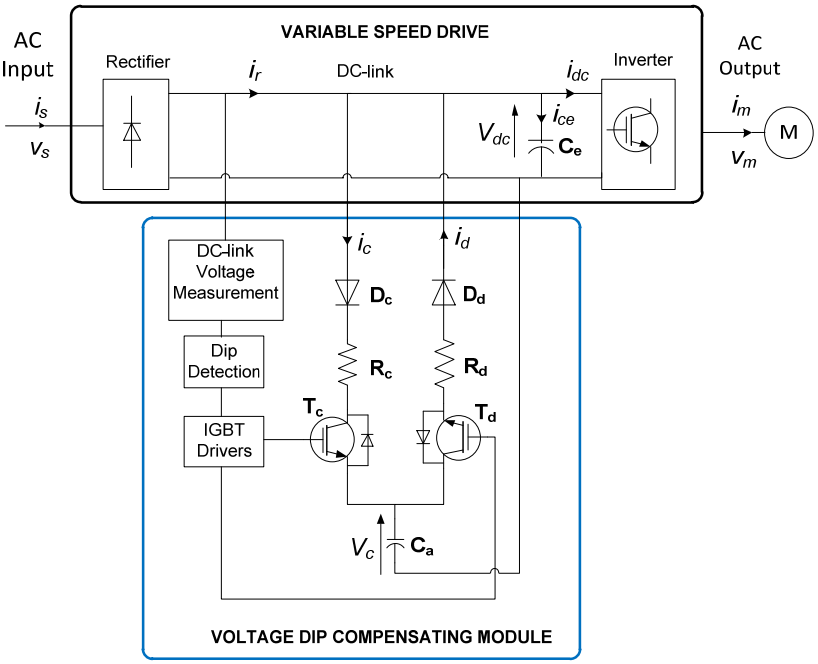

Figure 1. Proposed voltage dip compensating module.

Charging of C_a was conducted using the rectifier of the VSD through the dc bus. The detection circuit sensed the STPI and controlled the switching of IGBTs, T_c and T_d which ensured that the voltage dip compensation module (VDCM) was switched onto the dc bus when required i.e., during the dip and taken out once the voltage STPI had cleared and C_a fully charged.

3.1. DC-Link during Compensation

Let us assume a low inertia load and a negligible energy contribution from rotating masses. During the period after the start of the STPI and before C_a is switched onto the dc-link, C_e provides energy required by the load. Thus, when C_a eventually is switched onto the dc-link, it charges up C_e and provides power to the load during the STPI. Figure 2 represents the dc-link during compensation. R_{Ca} is the capacitor internal resistance, R_{Td} is the IGBTs on state internal resistance, R_{Dd} is resistance of the diode during conduction, R_d is the discharge current limiting resistor, R_{Ce} is the internal resistance of the VSD capacitor and P_{inv} is the VSD inverter input power. Relating capacitance and input power demand can be described in (3),

$$C = \frac{2P\Delta t}{V_{Ca}^2 - V_{Ca\_min}^2} \tag{3}$$

where V_{Ca} and V_{Ca_min} are the capacitor voltages at start and end of compensation respectively, P is the total power demand and Δt is STPI duration, V_{Ca} can be represented as in (4) based on Figure 2,

$$V_{Ca} = i_d\,(R_{Td} + R_{Dd} + R_d) + V_{dc} = V_{Rdisch} + V_{dc} \tag{4}$$

where V_{Rdisch} is the voltage drop across IGBT switch, diode D_d and resistor R_d. Substituting V_{Ca} from (3) into (4) results in (5),

$$C = \frac{2P\Delta t}{V_{Ca}^2 - \left(V_{dc_{min}} + V_{Rdisch}\right)^2} \tag{5}$$

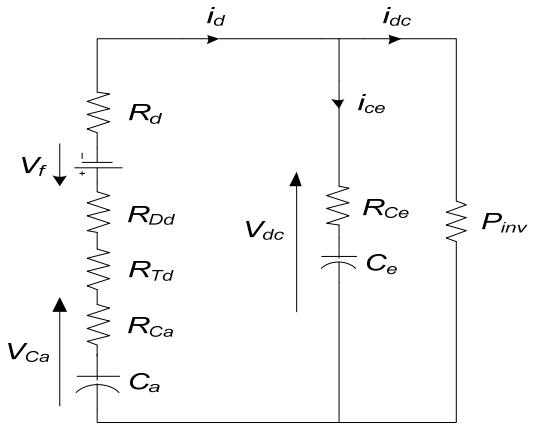

Figure 2. DC-link during compensation (discharge).

Inrush current at start of compensation,

$$i_{d\_max} = \frac{V_c - V_d - V_f}{R_{Ca} + R_{Td} + R_{Dd} + R_d + R_{Ce}} \quad (6)$$

where V_{dc} is the dc-link voltage at start of compensation.

3.2. DC-Link during Charging

The DC-link during charging is shown in Figure 3, Inrush charging current i_c at the start of charging can be obtained from (7),

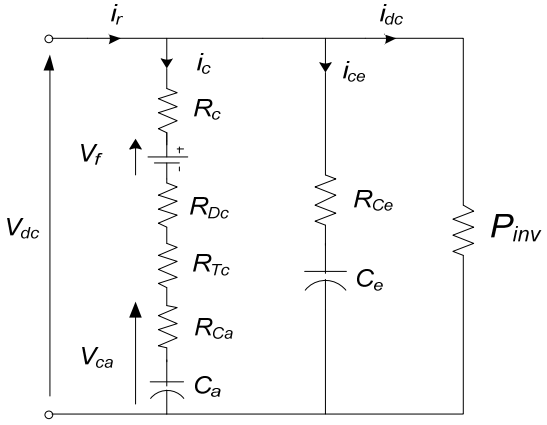

Figure 3. DC-link during charging.

Inrush charging current i_c at the start of charging can be obtained from,

$$i_{c\_max} = \frac{V_{dc} - V_{Ca\_min} - V_f}{R_{Td} + R_{Dd} + R_c} \quad (7)$$

where V_{Ca_min} is the capacitor C_a voltage after compensation.

4. Sizing Methodology: Voltage Dip Compensating Module

A sizing methodology based on readily available data such as the motor and VSD name plate information is developed. Figures 4–6 show the proposed sizing methodologies for inrush current limiting resistors R_d, R_c and capacitor C_a. For Figure 4, this algorithm works backwards from motor size to the dc link of the VSD or inverter. The motor full load current and the motor power factor can be obtained from the motor name plate. These values will then be used to calculate the input inverter dc current (i_{dc_n}). The inverter

output transient current or peak current can be obtained from the inverter nameplate. Once this is obtained the inverter peak dc bus current can be calculated (i_{dc_max}). Then this will allow for the maximum discharge current to be calculated (i_{d_max}). Since i_{d_max} will be calculated, and given a set voltage where compensation should start (V_{dc_trig}), diode forward voltage (V_f) and the capacitor voltage (V_{ca}), it then becomes possible to calculate the total resistance in the capacitor discharge leg. Given the knowledge of the IGBT internal resistance and that of the diode, the current limiting resistor can then be calculated (R_d) including its power rating. Figure 4 shows the analytical progress of obtaining the size of the current limiting resistor when switching the additional capacitor onto the dc bus.

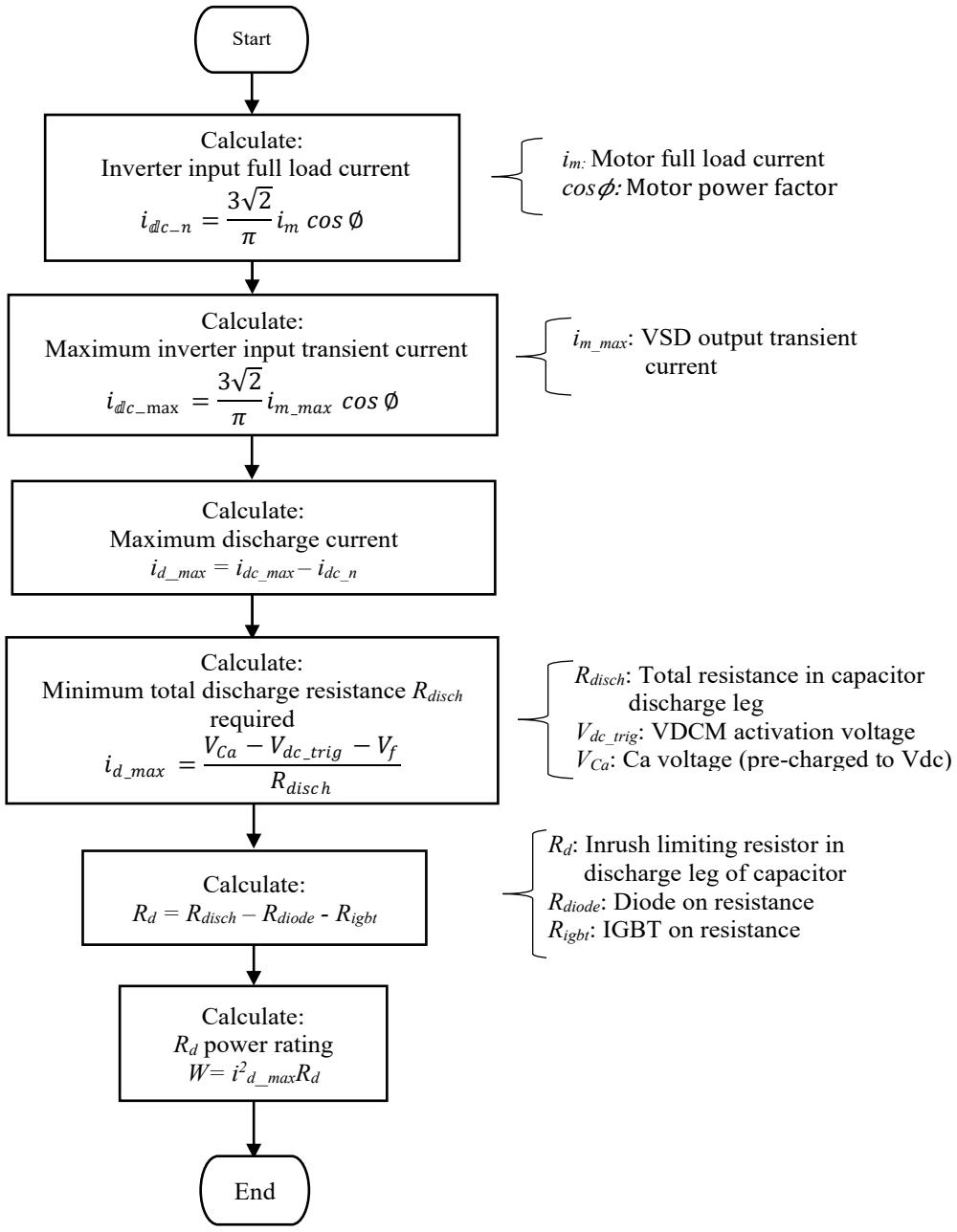

Figure 4. Discharge inrush current limiting resistor sizing flow chart.

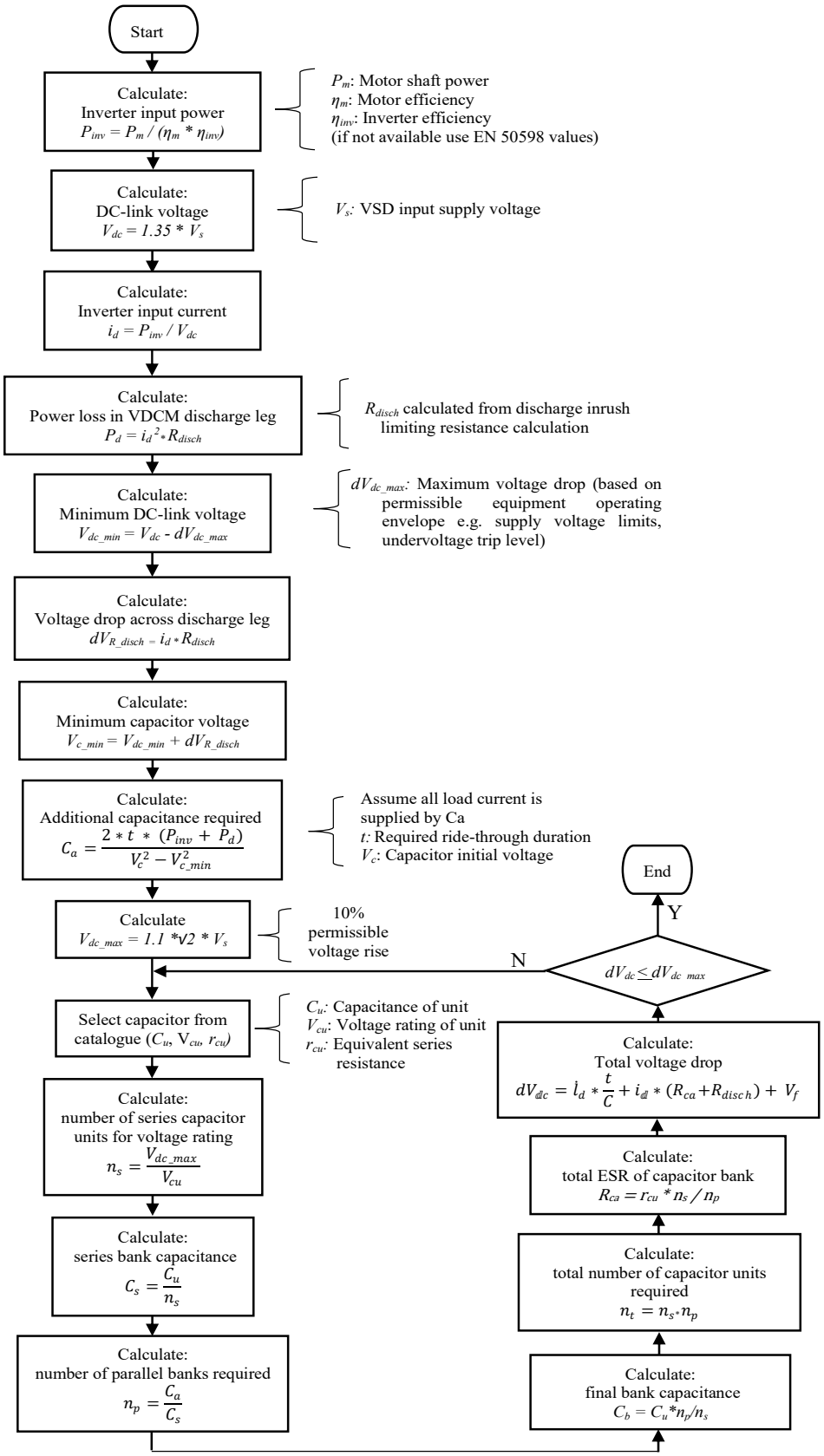

Figure 5. Switched capacitor sizing flowchart.

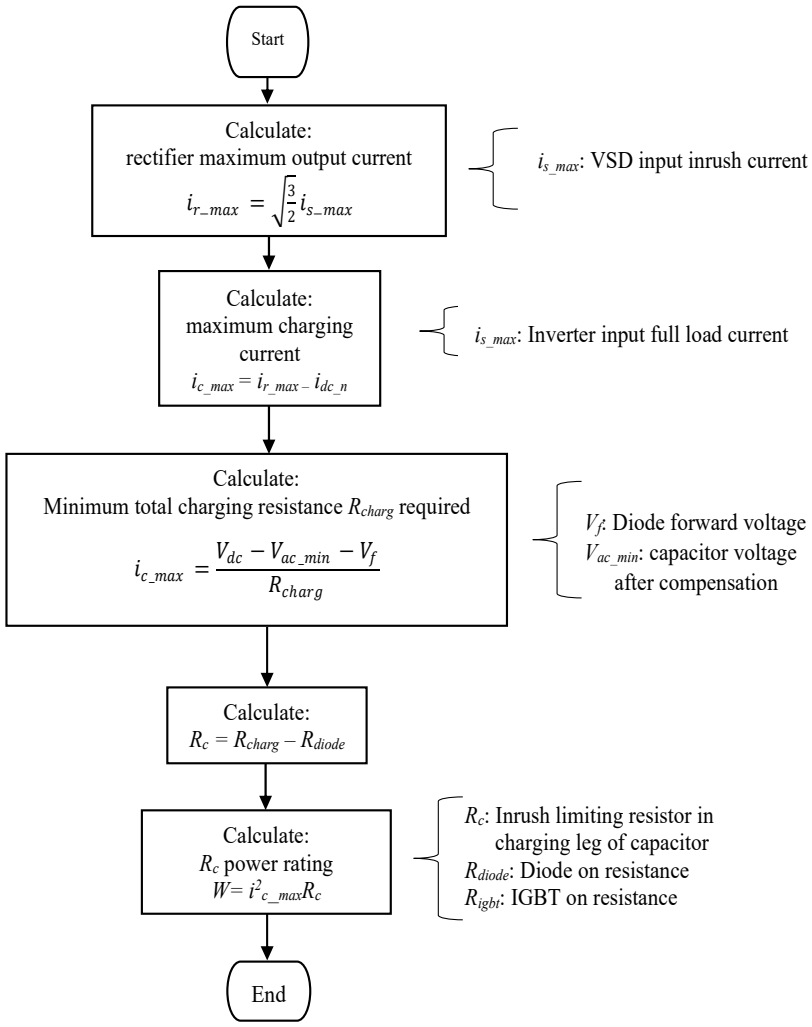

Figure 6. Charging inrush current limiting resistor sizing flowchart.

Figure 5 shows the additional switched capacitor sizing. Given the motor shaft power, motor efficiency and inverter efficiency from their nameplates the inverter input power can be calculated. The additional capacitor is calculated based on the assumption that full load current would be produced by this capacitor. This is because the additional capacitor will be used to supply the full load during a STPI. Given the known capacitance (from calculations) and the dc bus voltage, the appropriate capacitor can be chosen from the started capacitor units. Once the equivalent series resistor is calculated, the expected voltage drop on the dc bus can be calculated based on the chosen capacitor. If the voltage drop calculated is smaller than the set desired voltage drop (V_{dc_max}) then the loop ends. This will mean that the chosen standard capacitor will satisfy the conditions to not drop the dc bus voltage beyond (V_{dc_max}) during a STPI.

In Figure 6, a charging limiting resistor is calculated. Having obtained the VSD input inrush current by calculations. The rectifier maximum output current can be calculated. Once the minimum charging resistance is obtained, the inrush charging limiting resistor can be calculated including its power rating. It should be noted that during the charging scenario, the additional capacitor voltage would be minimal.

Sizing of the additional capacitor C_a and inrush current limiting resistors R_d and R_c was conducted for an induction motor with parameters shown in Appendix A, Tables A1 and A2. Using the proposed sizing methodology, the calculated values for C_a, R_d and R_c obtained were 15.1 mF, 6.91 Ω and 8.15 Ω, respectively.

5. Simulation Results and Analysis

To validate the operation of the proposed module and assess its impact on VSD and motor behavior, simulation studies were carried out. The simulation model comprised a v/f PWM controlled inverter driving an induction motor rated at 1.5 kW. This study is only concerned with v/f control based VSDs. The VSD simulation parameters are listed in Table A3 in Appendix A.

5.1. Simulation Results without DC-Link Voltage Compensation

When a 0.2 s STPI was simulated on the VSD supply, the dc-link voltage started decaying at a constant rate from an initial value of 556 V whereas the dc-link capacitor of the VSD supplied all the power required by the motor as shown in Figure 7. There was a gradual reduction in speed and torque as the dc-link voltage decayed. The dc-link voltage continued to drop until 300 V which is the under-voltage trip setting at which stage the VSD tripped. This is indicated by the flattening of the dc-link voltage curve and a loss in motor torque. There was an increase in the rate of speed reduction as load torque decelerated the motor-drive rotating assembly. After VSD tripped, for a brief period, the motor switched to an induction generator as the load acted as the prime over and stator windings acted as a current source allowing self-excitation of the motor. Once stator current decayed to zero, developed torque decays to zero. After the STPI was cleared over a period of 0.2 s, there is a sudden buildup of inrush current as shown in Figure 7. This results from low resistance of the VSD capacitor which is now experiencing a sudden high voltage after the STPI.

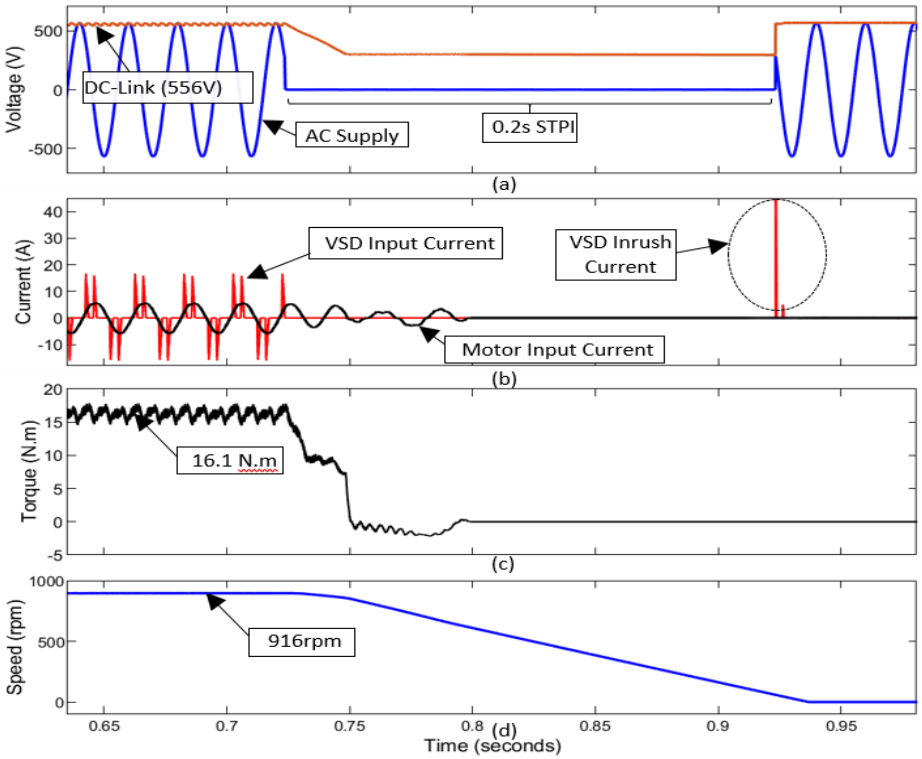

Figure 7. Simulation results without compensation of the dc-link, (**a**) supply and the dc bus voltage, (**b**) dc-link current and moto input current, (**c**) load torque and (**d**) motor speed.

5.2. Simulation Results with DC-Link Voltage Compensation

Figure 8 shows simulation results for the same 0.2 s STPI test with dc-link voltage compensation utilizing a 16 mF electrolytic capacitor bank.

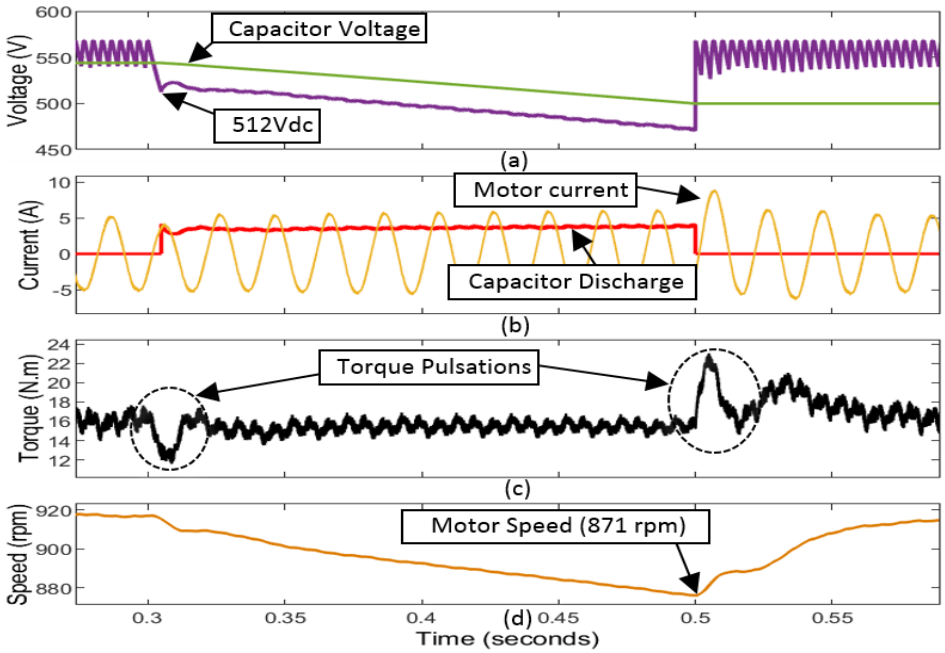

Figure 8. Simulation results with dc-link voltage compensation, (**a**) dc-link and capacitor voltage, (**b**) Motor and capacitor discharge current (**c**) torque and (**d**) speed response.

There was a decrease in the dc-link voltage when the supply was lost. At the point where the dc-link voltage dropped below the trigger set point voltage of 512 V, the dc-link voltage compensating device was initiated. The additional capacitor bank was switched onto the dc link and started supplying additional power. This is evidenced by the sudden halt in the "dc-link voltage" rate of decay and an increase in the dc-link voltage from 512 V to 524 V. The halting of the "dc-link voltage" decay was accompanied by a sudden increase of the current from the additional capacitor since the capacitor started to inject power into the dc-link i.e., delivering power to the motor as shown in Figure 8. Table 2 shows the summary of the simulation results.

Table 2. Key simulation results.

Parameter	At Start of Short Term Power Interruption(STPI)	At End of Short Term Power Interruption (STPI)	% Change [1]
DC-link voltage	556 V	471 V	−15.3%
Capacitor voltage	544 V	500 V	−8.1%
Speed	916 rpm	871 rpm	−4.5%
Torque	16.1 Nm	15.8 Nm	−1.9%

[1] negative sign indicates a reduction in the measured parameter.

The "dc-link voltage" continued to drop at a lower rate due to the influence of the additional capacitor. The start and end of compensation had a minor impact on the current drawn by the motor. There was, however, a steady increase in current drawn as the voltage decayed due to the need to maintain a constant power. Once supply was restored after 0.2 s and the "dc-link voltage" was retained from a minimum of 467 V to approximately 566 V, the capacitor bank was switched off from the "dc-link".

Torque pulsations were observed when the compensating module was connected and disconnected respectively from the dc-link at STPI clearance. These torque pulsations were as a result of transients in the dc-link voltage at the start and end of compensation.

Once STPI had cleared and the dc-link voltage stabilized, charging of C_a from the dc-link commenced. Figure 9 shows the simulation results obtained. To avoid continuous and

excessive loading of the dc-link due to charging action, pulse charging was adopted. This can be seen from the pulsed charging current trend. This approach resulted in minimum impact on the torque and speed of the motor.

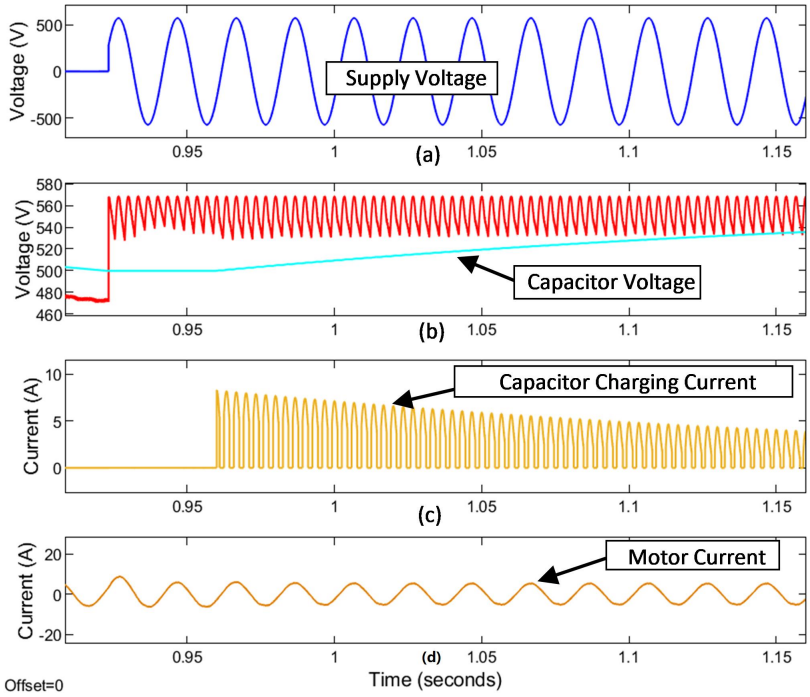

Figure 9. Simulation results for dc-link charging of capacitor Ca, (**a**) supply voltage, dc-link and (**b**) capacitor voltage, (**c**) capacitor charging current and (**d**) motor input current.

6. Experimental Set-Up and Results

Two induction machines were used for the experimental setup. One machine acted as a motor and the other as a generator in order to load the induction motor. The motor was driven by two-quadrant industrial VSD. Loading on the induction generator was driven through the 4 quadrant VSD. Figure 10, shows the experimental block diagram. The proposed voltage dip compensating module (VDCM) was interfaced to a two-quadrant VSD connected to a 1.5 kW induction motor. A 2.2 kW induction generator coupled to the induction motor provided the required loading of the induction motor. The SIEMENS S7 Programmable Logic Controller (PLC) was used for the generation of the logic signals used for controlling the power switches. These power switches were responsible for creating a voltage dip on the dc bus and switching the additional capacitor onto the dc bus. Since a PLC was used for the generation of the switching signals, the period of the short-term power interruption could be set to any desired value.

A variac transformer was used for the voltage dip generator on the dc bus of the 2 quadrant VSD. The variac allowed for any dc bus dip voltage needed to be achieved. Figure 11 shows the diagram of the voltage dip generator. When switch S1 is on S2 is open, the variac would be set to a lower supply voltage in order to emulate a fault on the supply and by switching on S2 for a particular period a voltage dip can be created on the dc bus of the VSD. Figure 12 shows the experimental set-up.

The motor speed and torque were measured by a torque transducer mounted between the motor and generator coupling. The torque transducer had a maximum error of 0.25%. The voltage transducers and the current transducers each had a maximum total error of +/−1%. Before the capacitor was put on standby for dc-link compensation, charging was carried out through a separately powered bridge rectifier as shown in Figure 12.

6.1. Experimental Test Conditions

The investigation involved assessing the behavior of the VSD without and with dc-link voltage compensation when subjected to a 0.2 s STPI. An industrial VSD was used and the investigation was carried out with the induction motor loaded to rated torque. To avoid damage to the VSD, key protection schemes including low dc-link voltage protection and overcurrent were left enabled. VSD dc-link voltage compensation, slip compensation and torque compensation control schemes were disabled to ensure alignment with the simulation model.

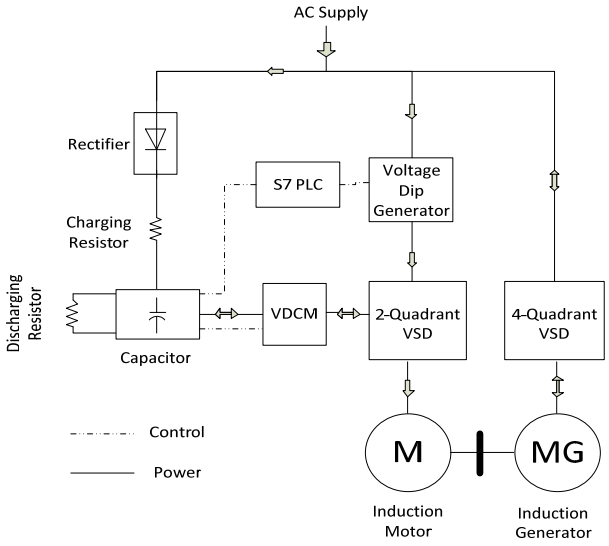

Figure 10. Block diagram of experimental set-up.

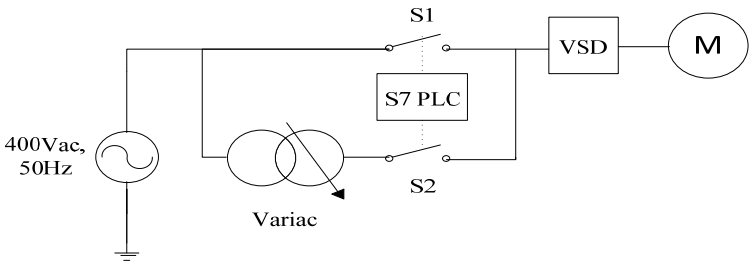

Figure 11. Voltage dip generator.

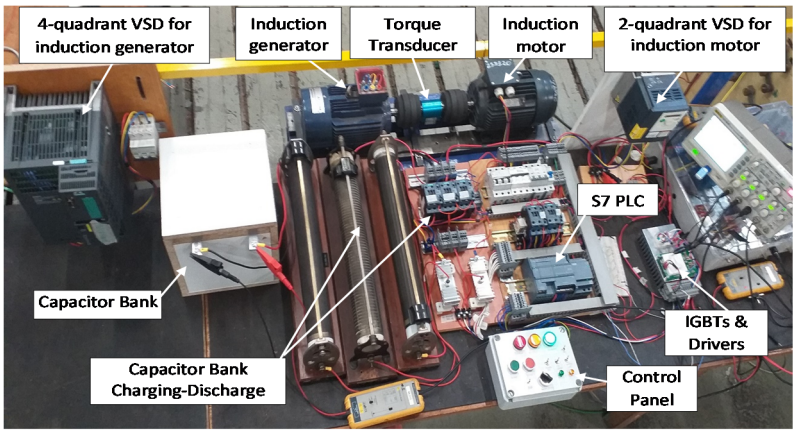

Figure 12. Laboratory experimental set-up.

6.2. Results without "DC-Link Voltage" Compensation

Figure 13 shows the results obtained when the two-quadrant VSD is subjected to a 0.2 s STPI. Once supply to the VSD was lost, the dc-link voltage immediately started decaying as the VSD dc-link capacitor supplied all the required motor power. The VSD tripped once the dc-link voltage had dropped to below the low dc-link trip setting of 288 V. This is indicated by the flattening of the dc-link voltage curve. Once supply was restored at the end of the dip, the dc-link voltage rapidly increased to its nominal level with some initial oscillations. The voltage dip clearance was followed by a current spike as the VSD dc-link capacitor started charging up.

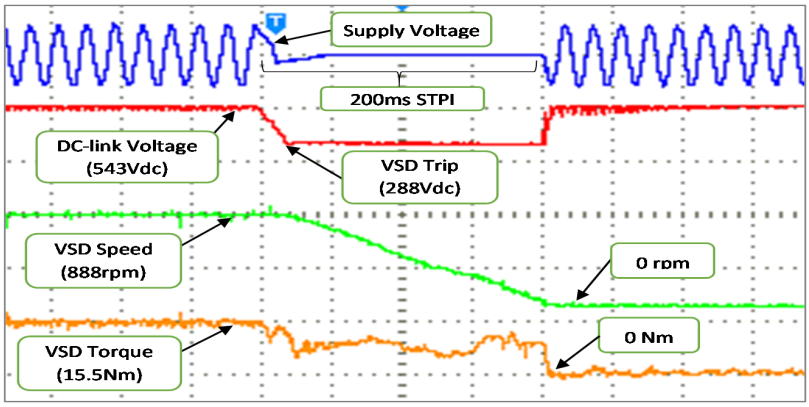

Figure 13. Experimental results without dc-link voltage compensation.

6.3. With "DC-Link Voltage" Compensation

The dc bus was operated at 556 V and the compensation capacitor was pre-charged to a voltage of 544 V as shown in Figures 14 and 15, respectively. During a fault the dc bus voltage started to drop. Once the voltage drops below 512 V, the trigger circuit was activated which then effectively switched the additional capacitor bank onto the "dc-link". Slight reductions in shaft speed including insignificant motor torque pulsations during the STPI were observed as shown in Figure 14. Figure 15 shows the instant increase of the discharge current from the additional capacitor drawn into the dc bus.

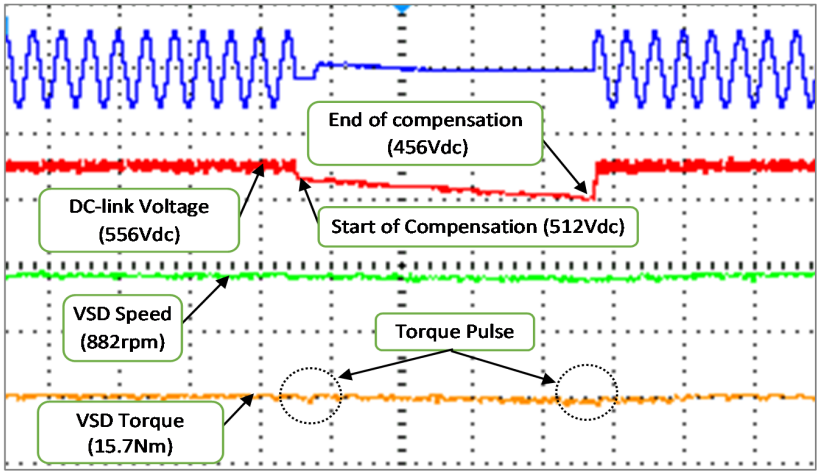

Figure 14. Experimental results with dc-link voltage compensation.

6.4. Compensation of Capacitor Charging from DC-Link

Figure 16 shows the results obtained of charging from the dc-link of the VSD. The charging circuit was configured to switch off once the dc-link voltage had dropped below a pre-set value. This was done to ensure that the dc-link was not excessively loaded by charging of the additional capacitor.

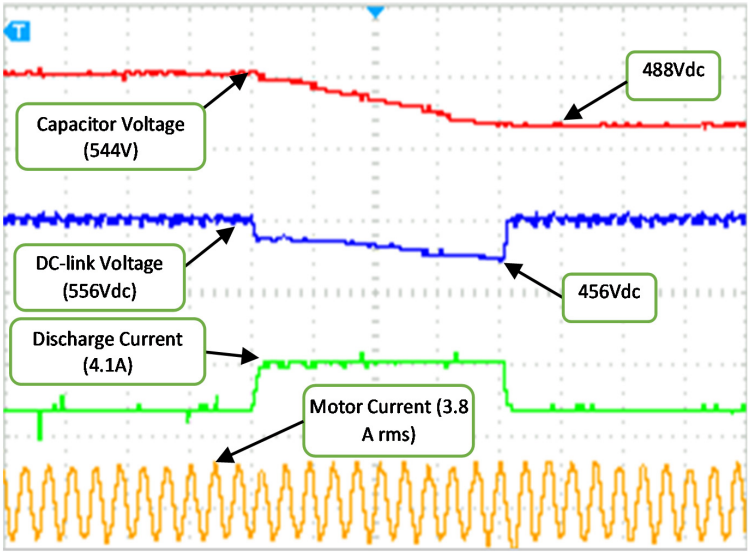

Figure 15. DC-link voltage variation during voltage compensation.

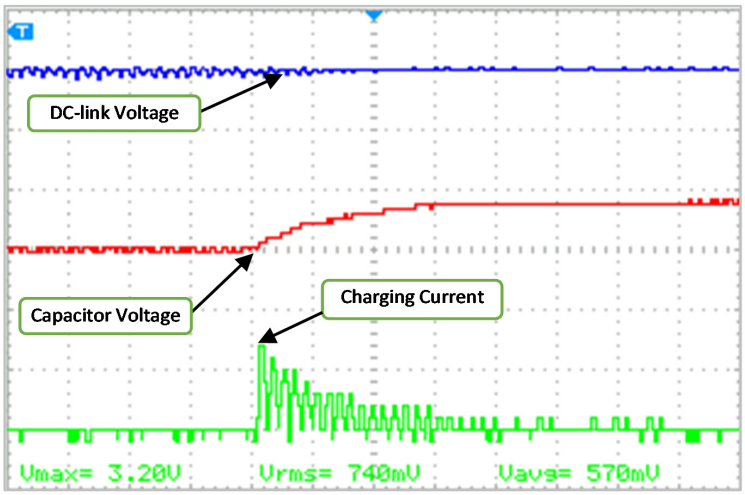

Figure 16. DC-link charging of capacitor Ca.

When charging was initiated, a considerable charging current was drawn, resulting in the dc-link voltage dropping below the charging threshold. This caused the charging IGBT to switch off. In this state, the dc-link voltage recovered resulting in the IGBT switching on. This repeated switching results in a pulsed charging current. Once the additional capacitor voltage had recovered to a value which did not trigger switching off the charging IGBT, continuous charging occurred till the capacitor was fully charged.

7. Analysis of Results

Table 3 summarizes the variations in the dc-link voltage and capacitor voltage during compensation.

Table 3. DC-link and capacitor voltage variation during compensation of a 1.5 kW induction motor.

Parameter	at Start of STPI	at End of STPI	% Change [1]
DC-link voltage	556 V	456 V	−18.0%
Capacitor Voltage	544 V	488 V	−10.3%

[1] negative sign indicates a reduction in the measured parameter.

The voltage drop across the capacitor is less than that of the dc-link. This is as a result of the voltage drop across the inrush limiting resistor during compensation. Table 4 shows the impact of the compensating module on torque and speed.

Table 4. Impact on speed and motor torque.

Parameter	at Start of STPI	at End of STPI	% Change [1]
Speed	882 rpm	860 rpm	−2.5%
Torque	15.7 Nm	14.0 Nm	−10.3%

[1] negative sign indicates a reduction in the measured parameter.

A comparison of key parameters from calculation as per proposed sizing methodology, simulation and experimental results are summarised in Tables 5 and 6. There is a strong correlation between calculated values (as per sizing methodology), simulation and experimental results for the proposed voltage dip compensation.

Table 5. Comparison of key parameters.

Parameter	Change in Value as Per *		
	Sizing Methodology	Simulation	Experiment
DC-link voltage drop	15.0%	15.6%	18.0%
Cap voltage drop	7.7%	8.3%	10.3%

* refers to change in value at the end of compensation compared to value at start of compensation.

Table 6. Capacitor charging and discharging currents.

Parameter	Value Obtained as Per		
	Sizing Methodology	Simulation	Experiment
Discharge current (A)	4.2 A	4.2 A	4.1 A
Charging current (A)	8.4 A	8.3 A	9.5 A

To further test the proposed sizing methodology, a study was undertaken for a 7.5 kW motor. Data used for the 7.5 kW induction motor assessment is listed in Table A4 in Appendix A. The results of key parameters are shown in Tables 7 and 8.

Table 7. DC-link and capacitor voltage variation during compensation of a 7.5 kW induction motor.

Parameter	Value Obtained as Per		% Variance
	Sizing Methodology	Simulation	
DC-link voltage drop	83.4 V	82.8 V	0.7%
Cap voltage drop	54.0 V	51.2 V	5.3%

Table 8. Capacitor charging and discharging currents of a compensating module for 7.5 kw induction motor.

Parameter	Value Obtained as Per		% Variance
	Sizing Methodology	Simulation	
Discharge current (A)	27.89 A	28.17 A	1.0%
Charging current (A)	20.88 A	19.79 A	5.4%

Calculated and simulated results for dc-link voltage compensation for a 7.5 kW induction motor during a STPI are very comparable. The proposed sizing methodology can thus be used for different sized motors which are driven from a v/f controlled VSDs.

8. Conclusions

This paper investigated and developed inrush current mitigation schemes for a proposed dc bus voltage ride through a power electronic module. The paper can be summarized as follows:

- A switched capacitor can be used to improve voltage ride through for a dc bus voltage;
- There was a torque pulsation of 12.8 and 14.3% at the start and end of dc-link voltage compensation respectively;
- During voltage dip ride through (compensation) there was a 2.5% drop in the speed and 10.3% drop in the motor torque;
- A sizing methodology for the additional capacitor and discharge limiting resistor has been tested and validated. This methodology uses readily available motor and VSD nameplate information;
- The voltage ride through module was able to retain up to 82% of the dc bus voltage during 0.2 s STPI which avoided a trip on the VSD;
- There was good agreement between simulations and experimental results and, when comparing the two, there was a 2.4% voltage difference on the dc link voltage drop and 2% difference on the switched capacitor voltage drop during compensation. There was a 2.4% difference between simulations and experimental work on the amount of the discharge current;
- The proposed method whilst effective in improving ride-through capability of VSD resulted in an unwanted voltage drop and energy losses due to the inrush current limiting resistor, which led to reduced overall module efficiency;
- The observed behaviour of the VSD was based on a STPI which presents the worst-case scenario. Improved behaviour is expected for less severe voltage dips;
- The voltage compensation module can be added to existing VSDs that are based on V/f control in order to avoid operational breakdowns.

Author Contributions: F.C. contributed towards the write up of the paper, methodology, experimental work and validation. L.M. contributed towards the conceptualization of the research idea, review, editing of the paper, methodology and supervision. All authors have read and agreed to the published version of the manuscript.

Funding: This work was funded by the Eskom Power Plant Engineering Institute program and the national research foundation of South Africa under grant 118120.

Institutional Review Board Statement: Not Applicable.

Informed Consent Statement: Not Applicable.

Data Availability Statement: Not Applicable.

Acknowledgments: This project is part of the Eskom Power Plant Engineering Institute program at Wits University. Authors also acknowledge the support of the National Research Foundation of South Africa.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature/Abbreviations

E_L	Total load energy (Wh)
E_C	Energy supplied by capacitor (Wh)
E_{kin}	Kinetic energy in the rotating mass (Wh)
T_L	Load torque (N.m)
ω	Speed of rotating assembly (rad/s)
J_l	Inertia (kg·m^2)
V_c	Capacitor voltage (V)
C_a	Switched capacitor (F)

C_e	Invereter dc bus capacitance (F)
V_{dc}	dc bus voltage (V)
I_{dc}	dc link current (A)
I_S	Variable speed drive supply current (A)
V_s	Variable speed drive supply voltage (V)
R_{ca}	Internal resistance of the switched capacitor (Ω)
R_{Td}	The switch internal resistance (Ω)
R_{Dd}	The resistance of the diode during conduction (Ω)
R_d	The discharge current limtting resistor (Ω)
R_{ce}	The internal resistance of the VSD capacitor (Ω)
P_{inv}	The VSD inverter input power (W)
V_{Ca}	Initial capacitor voltage
V_{Ca_min}	Capacitor voltage at end of compensation
i_{d_max}	The initial inrush current (A)
i_c	Inrush charging current (A)
R_d, R_c	Inrush current limiting resistors (Ω)
R_{disch}	Total resistance in discharge led (Ω)
I_{dc_n}	Norminal dc bust current under full load condition (A)
i_m	Motor full load current (A)
I_{m_max}	VSD peack out transient current (A)
P_m	Motor shaft power (W)
Δt	Required ride through duration (s)
C_u	Standard capcitance value (F)
V_{cu}	Standard voltage (V)
ESR	Equivalent serries resistance (V)
V_f	Diode forward voltage (V)
V_{ac_min}	Capacitor voltage after compensation (V)
R_{charg}	Resistance during charging (Ω)
STPI	Short term power interuption
PWM	Pulse width modulation
VSD	Variable speed drive
VDCM	Voltage dischage compensation module

Appendix A

Table A1. The 1.5 kW induction motor parameters.

Motor Rating	1.5 kW, 400 V, 50 Hz, 3.84 A, 920 rpm, Cos ϕ: 0.75, η: 75.2%
Stator resistance	4.38 Ω
Stator leakage inductance	17.1 mH
Rotor resistance	4.11 Ω
Rotor leakage inductance	16.5 mH
Magnetizing inductance	476 mH
Rotor inertia	0.0014 kg·m^2

Table A2. VSD technical data.

Input Rating	380–500 V, 50 Hz, 6.4 A, Inrush: 10 A, Power loss: 61 W
Output Rating	380–500 V, 0.5–500 Hz, 4.1 A, Transient 6.2 A for 60 s

Table A3. VSD simulation parameters.

Rectifier	3-arm Diode Bridge
Inverter	3-arm IGBT/Diode Bridge
Inverter Control	V/f, 2-level PWM
Switching Frequency	4 kHz
Modulation Index	0.9
Sample Time	10 µs
DC-link Capacitor	250 µF

Table A4. Induction motor parameters.

Power	7.5 kW
Efficiency	89.3%
Power Factor	0.81
Pole Pairs	2
Rotor Speed	1450 rpm

References

1. Majodina, M.; Botai, J.O.; Rautenbach, H. The vulnerability of the South African electricity transmission network infrastructure to weather and climate: A review. *J. Energy South. Afr.* **2018**, *29*, 51–59. [CrossRef]
2. Pillot, B.; Muselli, M.; Poggi, P.; Dias, J.B. Historical trends in global energy policy and renewable power system issues in Sub-Saharan Africa: The case of solar PV. *Energy Policy* **2019**, *127*, 113–124. [CrossRef]
3. Minnaar, U.J.; Gaunt, C.T.; Nicolls, F. Characterisation of power system events on South African transmission power lines. *Electr. Power Syst. Res.* **2012**, *88*, 25–32. [CrossRef]
4. Buraimoh, E.; Davidson, I.E.; Martinez-Rodrigo, F. Fault Ride-Through Enhancement of Grid Supporting Inverter-Based Microgrid Using Delayed Signal Cancellation Algorithm Secondary Control. *Energies* **2019**, *12*, 3994. [CrossRef]
5. B Magoro The South African Grid Code-The Network Code-Version 9. Eskom Transmission Division, July 2014. Available online: http://www.nersa.org.za (accessed on 1 March 2021).
6. Hansen, A.D.; Das, K.; Sørensen, P.; Singh, P.; Gavrilovic, A. European and Indian Grid Codes for Utility Scale Hybrid Power Plants. *Energies* **2021**, *14*, 4335. [CrossRef]
7. Duran-Gomez, J.L.; Enjeti, P.N.; von Jouanne, A. An approach to achieve ride-through of an adjustable-speed drive with flyback converter modules powered by super capacitors. *IEEE Trans. Ind. Appl.* **2002**, *38*, 514–522. [CrossRef]
8. Bollen, M.H.J.; Zhang, L.D. Analysis of voltage tolerance of AC adjustable-speed drives for three-phase balanced and unbalanced sags. *IEEE Trans. Ind. Appl.* **2000**, *36*, 904–910. [CrossRef]
9. Zyl, A.V.; Spee, R.; Faveluke, A.; Bhowmik, S. Voltage sag ride-through for adjustable-speed drives with active rectifiers. *IEEE Trans. Ind. Appl.* **1998**, *34*, 1270–1277.
10. Narayanan, R.; Platt, D.; Perera, S. Improvements to Voltage Sag-Ride Through Perfomance of AC Variable Speed Drives. *Int. J. Eng. Sci. Technol.* **2010**, *2*, 7.
11. Enjeti, P.N. Method and System for Ride Through of an Adjustable Speed Drive for Voltage Sags and Short Term Power Interruption. U.S. Patent 6,005,362, 21 December 1999.
12. Pires, V.F.; Monteiro, J.; Silva, J.F. Dual 3-Phase Bridge Multilevel Inverters for AC Drives with Voltage Sag Ride-through Capability. *Energies* **2019**, *12*, 2324. [CrossRef]
13. Afridi, K.K.; Chen, M.; Perreault, D.J. Enhanced Bipolar Stacked Switched Capacitor Energy Buffers. *IEEE Trans. Ind. Appl.* **2014**, *50*, 1141–1149. [CrossRef]
14. von Jouanne, A.; Enjeti, P.N.; Banerjee, B. Assessment of ride-through alternatives for adjustable-speed drives. *IEEE Trans. Ind. Appl.* **1999**, *35*, 908–916. [CrossRef]
15. Stockman, K.; D'hulster, F.; Verhaege, K.; Didden, M.; Belmans, R. Ride-through of adjustable speed drives during voltage dips. *Electr. Power Syst. Res.* **2003**, *66*, 49–58. [CrossRef]
16. Klumpner, C.; Blaabjerg, F. Experimental evaluation of ride-through capabilities for a matrix converter under short power interruptions. *IEEE Trans. Ind. Electron.* **2002**, *49*, 315–324. [CrossRef]
17. Deswal, S.S.; Dahiya, R.; Jain, D.K. Enhance Ride-Through Capability of Adjustable Speed Drives by Maintaining DC-Link voltage. *Int. J. Comput. Electr. Eng.* **2009**, *1*, 142–148. [CrossRef]

18. Carnovale, D.J.; Biternas, J.; Dionise, T.J.; Shipp, D.D. Design, Development and Testing of a Voltage Ride-Thru Solution for Variable Speed Drives in Oil Field Applications. In Proceedings of the 2007 IEEE Petroleum and Chemical Industry Technical Conference, Calgary, AB, Canada, 17–19 September 2007; pp. 1–7.
19. Kavitha, V.; Subramanian, K. Review on DC link capacitor issues in variable frequency drives. In Proceedings of the 2017 International Conference on Innovations in Electrical, Electronics, Instrumentation and Media Technology (ICEEIMT), Coimbatore, India, 3–4 February 2017; pp. 216–218.
20. Kim, U.-J.; Oh, S.-G. New Sub-Module with Reverse Blocking IGBT for DC Fault Ride-Through in MMC-HVDC System. *Energies* **2021**, *14*, 1551. [CrossRef]
21. Wymann, T.; Jorg, P. Power loss ride-through in a variable speed drive system. In Proceedings of the 2014 Petroleum and Chemical Industry Conference Europe, Valparaíso, Chile, 22–26 March 2021; pp. 1–9.
22. Undeland, T.M.; Mohan, N. Overmodulation and loss considerations in high-frequency modulated transistorized induction motor drives. *IEEE Trans. Power Electron.* **1988**, *3*, 447–452. [CrossRef]