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A 1.2 kV SiC MOSFET with Integrated Heterojunction Diode and P-shield Region

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Abstract: A 1.2 kV SiC MOSFET with an integrated heterojunction diode and p-shield region (IHP-MOSFET) was proposed and compared to a conventional SiC MOSFET (C-MOSFET) using numerical TCAD simulation. Due to the heterojunction diode (HJD) located at the mesa region, the reverse recovery time and reverse recovery charge of the IHP-MOSFET decreased by 62.5% and 85.7%, respectively. In addition, a high breakdown voltage (BV) and low maximum oxide electric field (E_{MOX}) could be achieved in the IHP-MOSFET by introducing a p-shield region (PSR) that effectively disperses the electric field in the off-state. The proposed device also exhibited 3.9 times lower gate-to-drain capacitance (C_{GD}) than the C-MOSFET due to the split-gate structure and grounded PSR. As a result, the IHP-MOSFET had electrically excellent static and dynamic characteristics, and the Baliga's figure of merit (BFOM) and high frequency figure of merit (HFFOM) were increased by 37.1% and 72.3%, respectively. Finally, the switching energy loss was decreased by 59.5% compared to the C-MOSFET.

Keywords: SiC; MOSFET; heterojunction diode; p-shield region; split-gate; BFOM; HFFOM; switching energy loss; reverse recovery; gate-to-drain capacitance

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1. Introduction

Silicon carbide (SiC) is a wide bandgap (WBG) material that can withstand a higher electric field and has good thermal conductivity compared to silicon (Si), so it is in the spotlight as a next-generation power MOSFET material [1–4]. GaN and diamond are also in the spotlight as wide bandgap materials, but SiC is more advantageous compared to both materials in terms of fabrication process because it can utilize the existing silicon process. SiC MOSFETs are being actively studied because of their superior switching characteristics compared to Si IGBTs [5,6]. To improve the switching characteristics of SiC MOSFETs, the gate-drain capacitance (C_{GD}) must be reduced because switching power loss occurs mainly during the charging and discharging of the C_{GD} [7]. A well-known method to reduce the C_{GD} is a split-gate MOSFET [8]. However, split-gate MOSFETs have critical problems in that the high electric field is concentrated on the split-gate oxide corner and there is a degradation of static characteristics such as on-resistance (R_{ON}) and breakdown voltage (BV). Therefore, several structures, including an accumulation-mode split-gate MOSFET and a split-gate MOSFET with floating P+ polysilicon, have been proposed to solve these problems [8,9].

Another way to improve the switching characteristics of 4H-SiC MOSFETs is to improve the reverse recovery characteristics of the body diodes. The SiC MOSFETs have a parasitic PiN body diode composed of a P-base region and an N-drift region, which features high turn-on voltage (V_F) because of the wide energy bandgap. Therefore, the body diode of a SiC MOSFET increases the peak current and reverse recovery charge during switching turn-on transients, which increases the reverse recovery power dissipation [10]. In order to improve the reverse recovery characteristics, several device structures in which

the heterojunction diode- (composed of polysilicon and N-SiC) or Schottky barrier diode (SBD)-embedded SiC MOSFETs have been studied [11–15].

In this study, a novel 1.2 kV SiC MOSFET with an integrated heterojunction diode and p-shield region (IHP-MOSFET) was proposed and investigated through Sentaurus TCAD simulation. The P+ polysilicon was located at the mesa region of the IHP-MOSFET, and acted as a heterojunction diode (HJD). Due to the low turn-on voltage (V_F) of the HJD, the proposed device significantly reduced the reverse recovery charge (Q_{RR}) and reverse recovery time (t_{RR}) compared to the conventional SiC MOSFET (C-MOSFET). The p-shield region (PSR) under the P+ polysilicon effectively dissipated the electric field, resulting in high breakdown voltage (BV) and low maximum oxide electric field (E_{MOX}). Moreover, the gate-to-drain capacitance (C_{GD}) of the proposed device was decreased by a factor of 3.9 because of the split-gate structure and PSR. As a result, the IHP-MOSFET attained better switching performance in terms of the switching time and switching energy loss.

2. Device Structures and Fabrication Procedures

2.1. Device Structures and Concept

Figure 1a,b show the schematic cross-sectional views of the C-MOSFET and IHP-MOSFET. Additionally, the equivalent circuits of both devices are shown in Figure 1c,d. In IHP-MOSFET, the integrated HJD shares source and drain electrodes with the parasitic body diode, so the HJD is connected to body diode in parallel as shown in Figure 1d. To achieve 1.2 kV BV class, the epi-layer thickness and N-drift doping concentration of the both devices were set to 10 μm and 8×10^{15} cm^{-3}, respectively. The channel length and doping concentration were 0.5 μm and 2×10^{17} cm^{-3}, respectively. The thickness of the gate oxide (t_{ox}) was set to 50 nm. To minimize the JFET resistance component, a current spreading layer (CSL) with a higher doping concentration (4×10^{16} cm^{-3}) was introduced to both devices [16,17]. In the case of the IHP-MOSFET, the CSL was placed above the PSR because the secondary epitaxy process was performed after forming the PSR through ion implantation. This wide CSL could help prevent serious degradation of R_{ON} due to the depletion region caused by the PSR. Moreover, the proposed device adopted a split-gate structure in order to reduce the C_{GD}. The PSR was placed under P+ polysilicon to protect the HJD and split-gate corner from a high electric field. As the floating p-shield region caused a dynamic degradation effect because of the stored negative charge in switching operations, the PSR must be grounded [18,19]. Therefore, the PSR was in contact with grounded P+ polysilicon to prevent dynamic degradation [20,21]. The detailed parameters for both devices are shown in Table 1.

To understand the operation of an HJD, Figure 1e shows the energy band diagram along line A-A′ in Figure 1b at thermal equilibrium. At a state of thermal equilibrium, the energy bands of P+ polysilicon and n-type 4H-SiC (CSL) differed as much as the built-in potential (e.g., electron barrier height Φ_{BN}). Moreover, due to the difference in energy bandgap between the two materials, a potential difference of 0.7 eV at the conduction band and 1.43 eV at the valence band occurred at the junction between the P+ polysilicon and CSL. When the forward bias was applied, the built-in potential began decreasing, and the conduction band of the CSL began rising. Therefore, this allowed the electrons in the CSL to easily migrate to the P+ polysilicon region. On the other hand, the valence band of the CSL also rose, but there was still a high energy barrier between the two materials, and the holes could not move from the P+ polysilicon to the CSL [22]. As a result, the HJD behaved as a unipolar device.

2.2. Proposed Fabrication Procedures

To demonstrate the feasibility of the IHP-MOSFET, the possible fabrication procedure was constructed, as shown in Figure 2. An N-drift is grown on an N+ substrate by an epitaxial growth and the PSR is formed by ion implantation (Figure 2a). After a second epitaxial process of the CSL, the N+ source, P+ base, and channel regions are formed by ion implantation as shown in Figure 2b. Then, the CSL is etched into the integrated HJD

(Figure 2c) [23]. In this step, the CSL and a portion of the PSR are etched to make the PSR grounded (source contacted). Next, the P+ polysilicon is deposited in the trench region (Figure 2d), and thermal oxidation is performed to form the gate oxide layer (Figure 2e). In this step, a nitride mask can be used to prevent the oxidation of the P+ polysilicon region. Next, N+ polysilicon is deposited and patterned to form the split-gate (Figure 2f). Finally, an interlayer dielectric (ILD) oxide is deposited (Figure 2g) by LPCVD, and the metallization process proceeds to form the source and drain the ohmic contacts (Figure 2h).

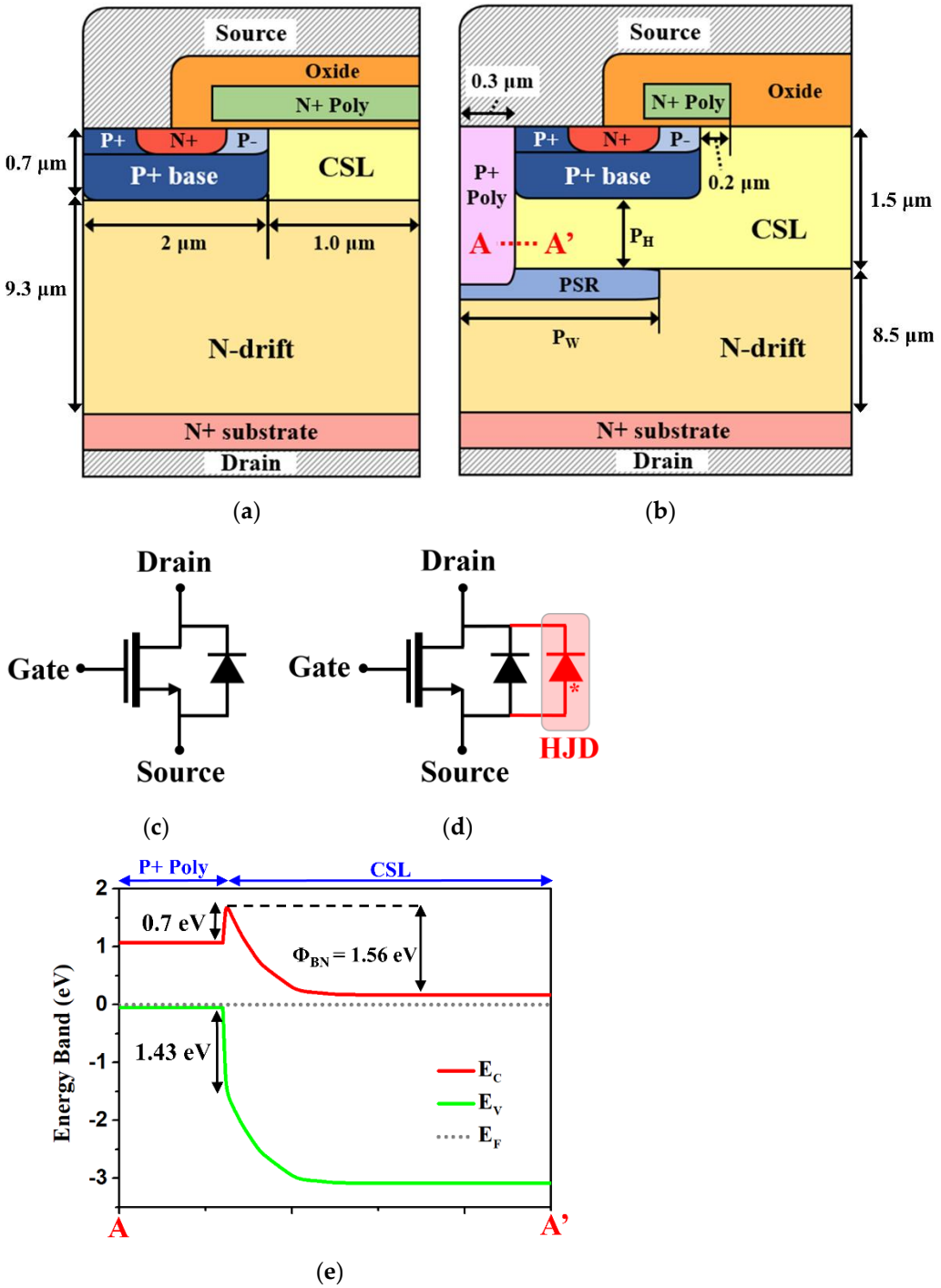

Figure 1. Schematic cross-sectional views of (**a**) C-MOSFET and (**b**) IHP-MOSFET. The equivalent circuits of (**c**) C-MOSFET and (**d**) IHP-MOSFET. (**e**) Energy band diagram along line A-A' in (**b**) at thermal equilibrium.

Table 1. Dimension and doping parameters of both devices.

Parameter	C-MOSFET	IHP-MOSFET	Unit
Epi-layer thickness	10	10	μm
N-drift doping	8×10^{15}	8×10^{15}	cm^{-3}
CSL doping	4×10^{16}	4×10^{16}	cm^{-3}
Length of the channel	0.5	0.5	μm
Channel doping	2×10^{17}	2×10^{17}	cm^{-3}
P+ base doping	5×10^{18}	5×10^{18}	cm^{-3}
N+ source doping	1×10^{19}	1×10^{19}	cm^{-3}
PSR doping	-	5×10^{17}	cm^{-3}
Width of P+ base	2	2	μm
Half-cell pitch	3	3.3	μm
Width of JFET	1	1	μm
Oxide thickness (t_{ox})	50	50	nm
Width of P+ polysilicon	-	0.3	μm
Width of PSR (P_W)	-	2	μm
Distance between P+ base and PSR (P_H)	-	0.8	μm
N+ substrate doping	1×10^{19}	1×10^{19}	cm^{-3}
N+ substrate thickness	100	100	μm

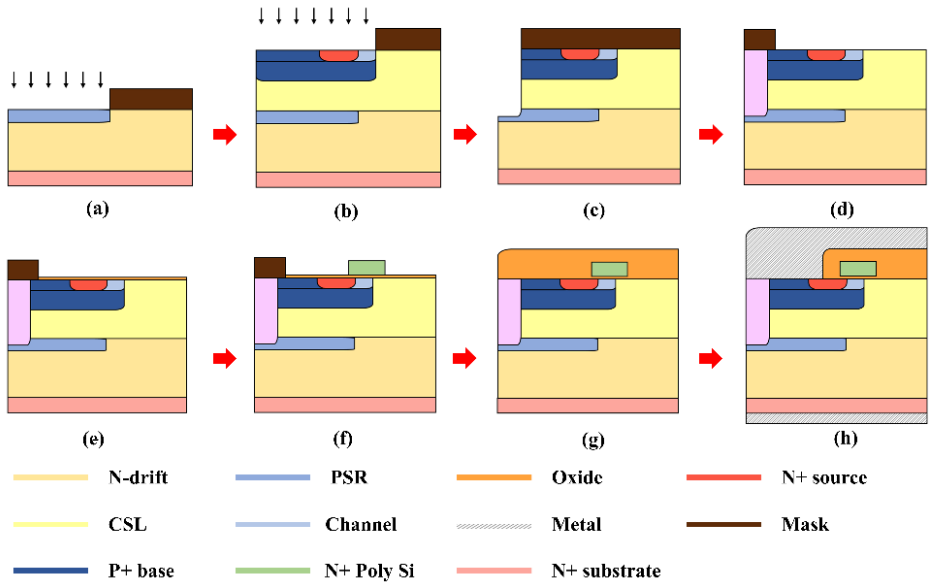

Figure 2. Proposed fabrication procedure of the IHP-MOSFET: (**a**) forming PSR by ion implantation, (**b**) forming P+ base, N+ source and channel regions on CSL, (**c**) CSL etching, (**d**) forming HJD, (**e**) thermal oxidation, (**f**) split-gate formation, (**g**) ILD deposition, and (**h**) ILD etching and metallization process.

3. Results and Discussions

3.1. Simulation Test Conditions

The two-dimensional (2D) SiC MOSFET devices were generated using the Synopsys Sentaurus Structure Editor tool (SDE) in which the doping profile, the dimension parameters, and the meshing of the device were set. The electrical characteristics of the device were simulated using Sentaurus Device (SDEVICE). The Poisson equation and the electron/hole continuity equations were solved by either a transient solution or quasi-stationary solution. The mixed-mode simulation was carried out for the reverse recovery characteristics and switching characteristics, in which multiple active and passive devices were connected to construct the power circuit. The TCAD simulation models (physics) used in this study referred to our previous work [24]. The Auger, SRH, doping-dependent, and temperature-

dependent recombination models were considered. In the case of the mobility model, the Arora, Lombardi, Enormal, and high field saturation models were considered [25]. Additionally, the bandgap narrowing and Fermi–Dirac statistics were considered. A fixed charge with a concentration of 1×10^{12} cm^{-2} was incorporated into the SiC/SiO_2 interface for both devices, which corresponded to a channel mobility of about 50 $cm^2/V{\cdot}s$ [26]. Finally, the interface trap charge with a concentration of 2×10^{10} cm^{-2} was considered in the SiC/polysilicon interface [27].

3.2. Optimization of the IHP-MOSFET

In power MOSFETs, the R_{ON} and BV are considered to be the most basic and important parameters. Figure 3 shows the influence of the width of the PSR (P_W) on R_{ON} and BV characteristics in the IHP-MOSFET. As the P_W increased, the current path decreased in the on-state but more of the electric field was dispersed by the PSR in the off-state. Therefore, an increase in P_W caused an increase in R_{ON} and BV, and it can be seen that there is a trade-off relationship. We chose the P_W = 2 μm result, which achieved the highest Baliga's figure of merit (BFOM = BV^2/R_{ON}). It is noteworthy that P_W shows a similar BFOM of over 1150 MW/cm^2 in the range of 1.8 to 2.2 μm, indicating sufficient process tolerances.

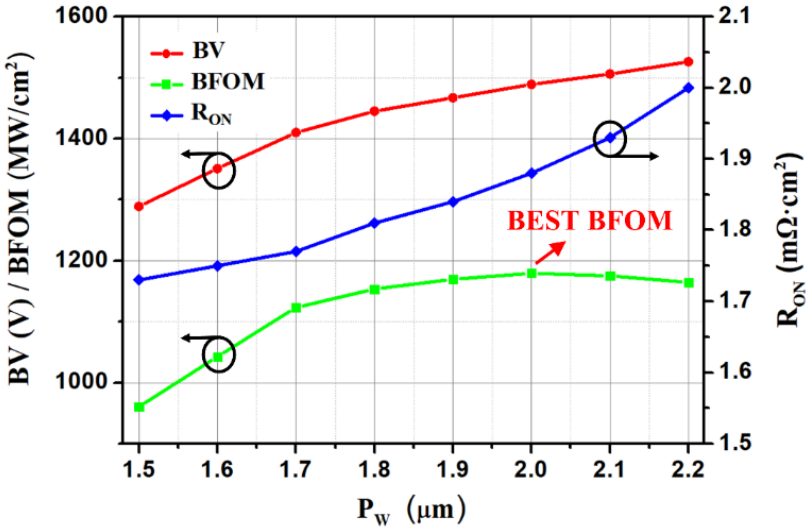

Figure 3. Influence of P_W on static characteristics in IHP-MOSFET when P_H = 0.8 μm. R_{ON} is obtained at V_{GS} = 15 V and I_{DS} = 100 A/cm^2. BV is obtained at V_{GS} = 0 V and I_{DS} = 1 $\mu A/cm^2$.

Next, the influences of the distance between the P+ base region and PSR (P_H) on blocking characteristics and reverse conduction characteristics are shown in Figure 4. The tables inserted in Figure 4 represent the changes in the BV and V_F according to changes in the P_H. Here, the V_F is obtained at V_{GS} = −5 V and I_{DS} = −100 A/cm^2. It can be seen that an increase in P_H caused a decrease in both V_F and BV. The reason for the decreasing BV was that the electric field became more concentrated in the PSR as the P_H increased. On the other hand, the V_F decreased owing to the increasing HJD area and a wider diode current path as the P_H increased. We chose P_H = 0.8 μm, which displayed the good trade-off relationship between the BV and V_F.

It can be seen that the IHP-MOSFET featured much higher BV compared to the C-MOSFET in all the cases shown in Figure 4a. For better understanding of the BV improvement of the IHP-MOSFET, the electric field distributions of both devices when V_{GS} = 0 V and V_{DS} = 1.2 kV are shown in Figure 5. The result shows that the PSR effectively dispersed the electric field, so that the maximum electric field of the P+ base region (3.08 MV/cm) was much lower than that of the C-MOSFET (3.77 MV/cm). Therefore, the IHP-MOSFET has a higher BV compared to the C-MOSFET in all cases in Figure 4a. In addition, it was confirmed that the proposed device had a lower E_{MOX} (2.78 MV/cm)

than the C-MOSFET (3.11 MV/cm), despite the split-gate structure, owing to the electric field dispersion effect of the PSR. It is well-known that low E_{MOX} helps improve oxide reliability [28].

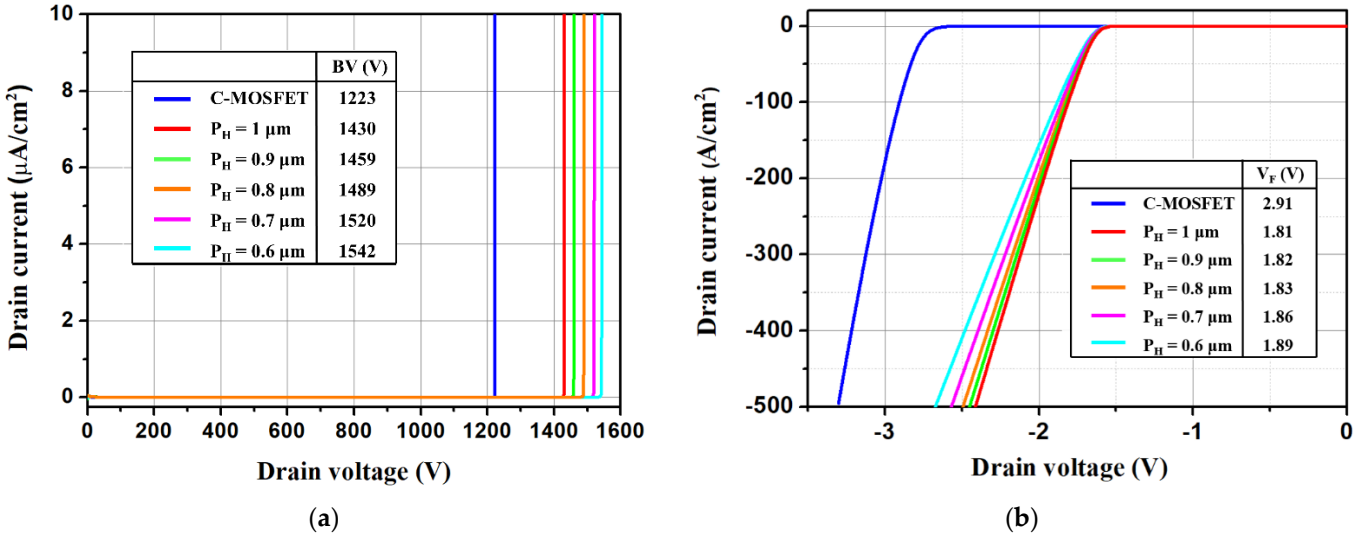

Figure 4. (**a**) Influence of P_H on forward blocking characteristics in IHP-MOSFET when P_W = 2 μm. The BV curve of the C-MOSFET is given for comparison. (**b**) Influence of P_H on reverse conduction characteristics in IHP-MOSFET when P_W = 2 μm. V_F is obtained at V_{GS} = −5 V and I_{DS} = −100 A/cm^2.

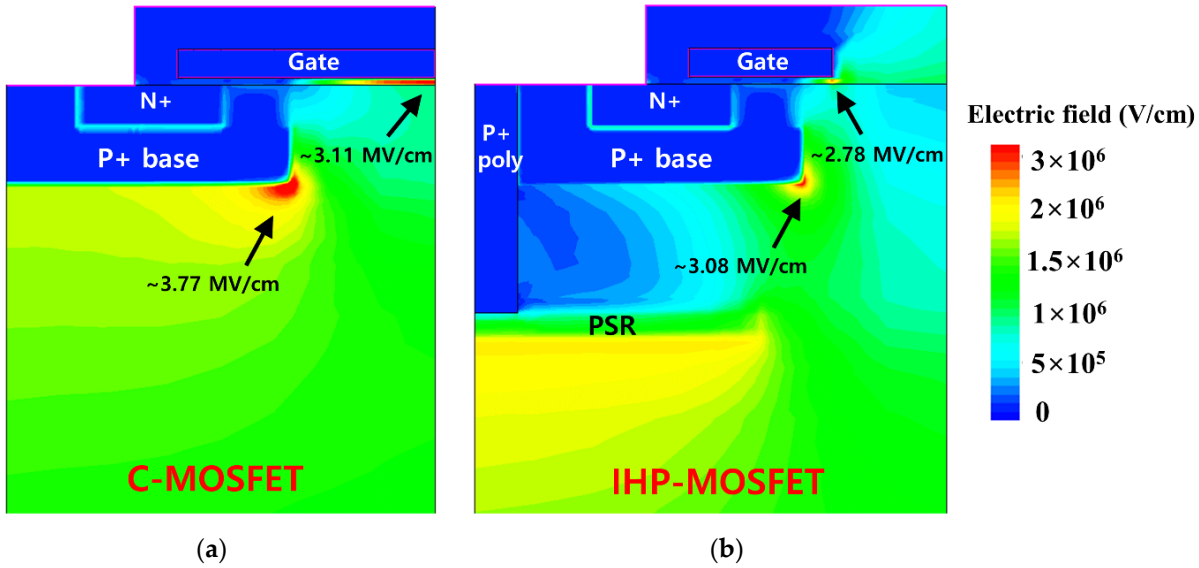

Figure 5. Electric field distributions of (**a**) C-MOSFET and (**b**) IHP-MOSFET when V_{GS} = 0 V and V_{DS} = 1.2 kV. The P_W and P_H of the IHP-MOSFET are 2 and 0.8 μm, respectively.

Moreover, electron and hole current density distributions of both devices are shown in Figure 6 to confirm the unipolar action of the HJD. In the case of the C-MOSFET, the electron current flowed mainly in the junction between the P-base and the CSL, indicating the activation of the PiN diode as shown in Figure 6b. On the other hand, the PiN diode was suppressed and the electron current only flowed to the HJD in the IHP-MOSFET (Figure 6a). As a result, it can be seen that the minority carriers (holes) induced by the PiN diode were effectively suppressed in the IHP-MOSFET (Figure 6c) compared to the C-MOSFET (Figure 6d).

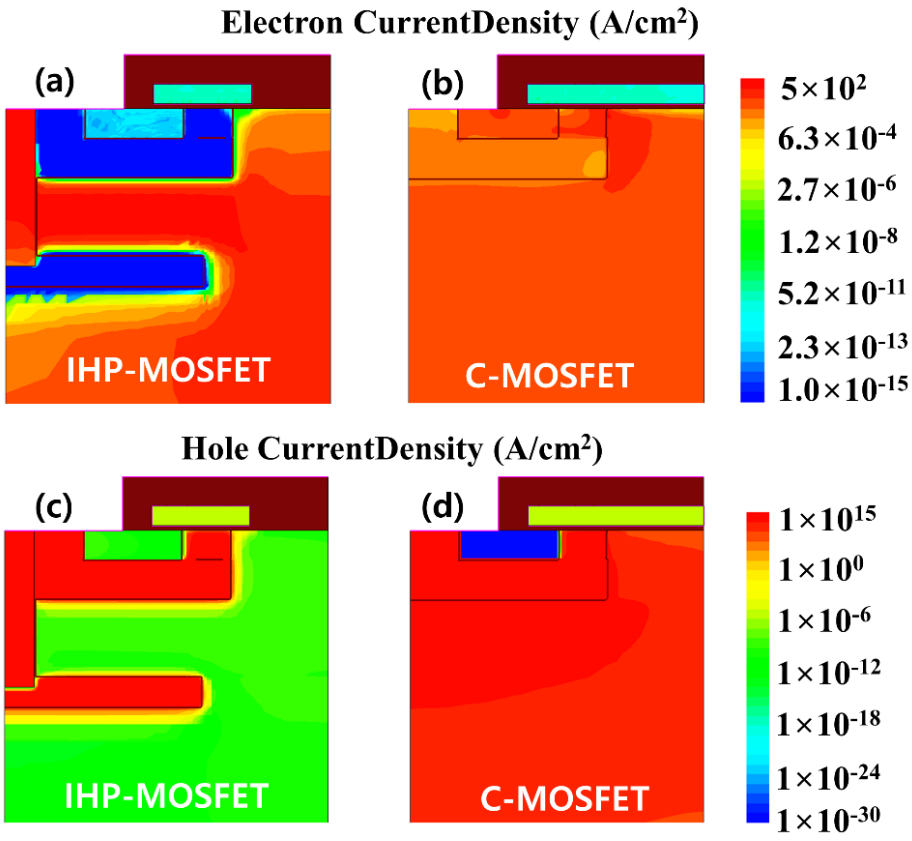

Figure 6. Electron current density distributions of (**a**) C-MOSFET and (**b**) IHP-MOSFET. Hole current density distributions of (**c**) C-MOSFET and (**d**) IHP-MOSFET when V_{GS} = −5 V and I_{DS} = −100 A/cm^2. The P_W and P_H of the IHP-MOSFET are 2 and 0.8 µm, respectively.

3.3. Device Performance Comparison of Both Devices

Figure 7 presents the forward conduction characteristics of the C-MOSFET and IHP-MOSFET. Due to the slightly increased cell pitch and the depletion region formed by the PSR, the proposed device had a slightly higher R_{ON} (1.88 mΩ·cm^2) compared to the C-MOSFET (1.74 mΩ·cm^2). However, the 8% increase in the R_{ON} was not insignificant and the ultimate increase in the BFOM (1179 MW/cm^2 in the IHP-MOSFET and 860 MW/cm^2 in the C-MOSFET) could cover this higher R_{ON} downside. The inset of Figure 7 shows the electron current density distributions of the IHP-MOSFET at V_{GS} = 15 V and V_{DS} = 20V. It can be seen that the HJD was safely turned off in the forward conduction.

Figure 8 shows the parasitic capacitance characteristics of the C-MOSFET and IHP-MOSFET. For the capacitance simulation conditions, the gate voltage was fixed at 0 V and the frequency of the AC small signal was set to 1 MHz. The output capacitance (C_{OSS}:C_{DS} + C_{GD}) was almost the same for both devices, but the input capacitance (C_{ISS}:C_{GD} + C_{GS}) and C_{GD} of the IHP-MOSFET were much lower than those of the C-MOSFET. To explain the reason for the reduction in the C_{GD}, the C_{GD} can be expressed by the following equation [29]:

$$C_{GD} = \frac{C_{OX}C_{dep}}{C_{OX} + C_{dep}} \quad (1)$$

where C_{OX} means the gate oxide capacitance and C_{dep} means the bulk depletion capacitance. The C_{OX} component of the IHP-MOSFET was reduced compared to the C-MOSFET because of the reduction in the active gate area. Moreover, the C_{dep} component of the proposed device decreased as the drain voltage increased because of the fast depletion in the N-drift region by the grounded PSR. Therefore, the C_{GD} of the IHP-MOSFET was reduced by 74.4% compared to the C-MOSFET. Finally, the reduction in C_{ISS} also originated from

the reduced active gate area. As a result, the IHP-MOSFET showed a 72.3% improvement in the high frequency figure of merit (HFFOM) compared to the C-MOSFET, indicating better dynamic performance.

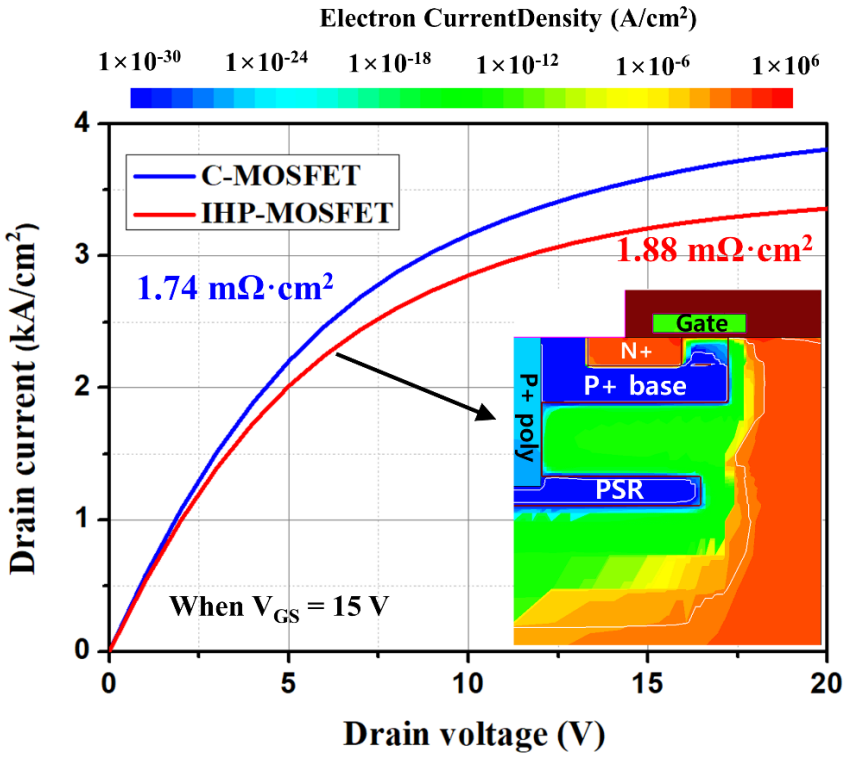

Figure 7. Forward conduction characteristics of the C-MOSFET and IHP-MOSFET. The inset in the figure represents electron current density distributions at V_{GS} = 15 V and V_{DS} = 20 V.

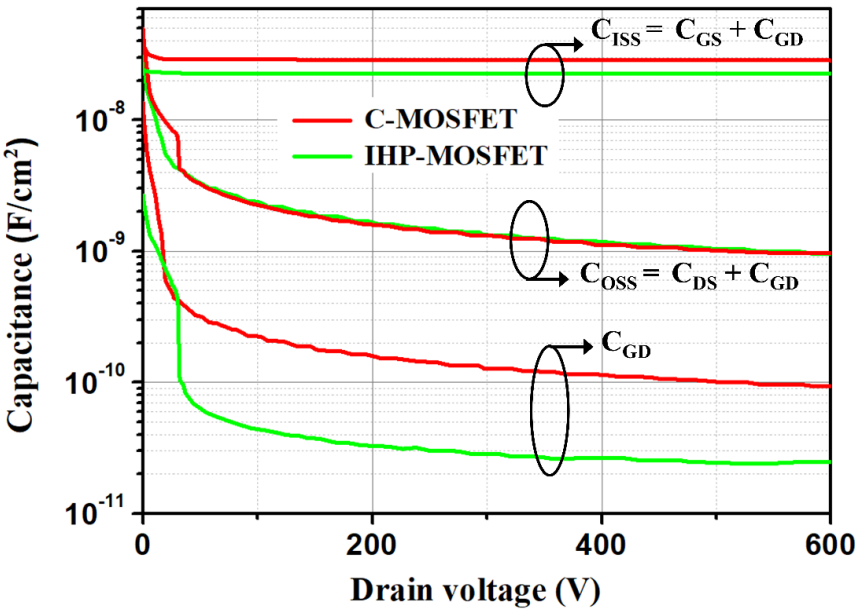

Figure 8. Parasitic capacitances of both devices as a function of drain voltage when V_{GS} = 0 V.

Figure 9a shows the reverse recovery characteristics of the body diodes of the C-MOSFET and IHP-MOSFET, and Figure 9b shows the double-pulsed test circuit (DPT) for the reverse recovery and switching characteristics. In Figure 9a, the body diode of the

IHP-MOSFET has a much smaller reverse recovery time (t_{rr}) and reverse recovery peak current (I_{RRM}) than the C-MOSFET. Since the body diode of the C-MOSFET operated as a bipolar device, the electrons and holes moved when the diode was turned on. On the other hand, since the diode of the IHP-MOSFET operated as a unipolar device, only the electrons moved from the N-drift to P+ polysilicon. Therefore, when the diode was turned off, the number of minority carriers remaining in the IHP-MOSFET was much smaller than that of the C-MOSFET, thereby having smaller t_{rr} and I_{RRM}. The reverse recovery charge (Q_{rr}) follows the equation:

$$Q_{rr} = \int_{t_1}^{t_2} I(t)\, dt \quad (2)$$

where t_1 is the first point at which the reverse recovery current becomes zero, and t_2 is the second point at which the reverse recovery current becomes 10% of the I_{RRM}. The results showed that the Q_{rr} of IHP-MOSET was 85.7% smaller than that of C-MOSFET. Table 2 summarizes the device characteristics of the C-MOSFET and IHP-MOSET.

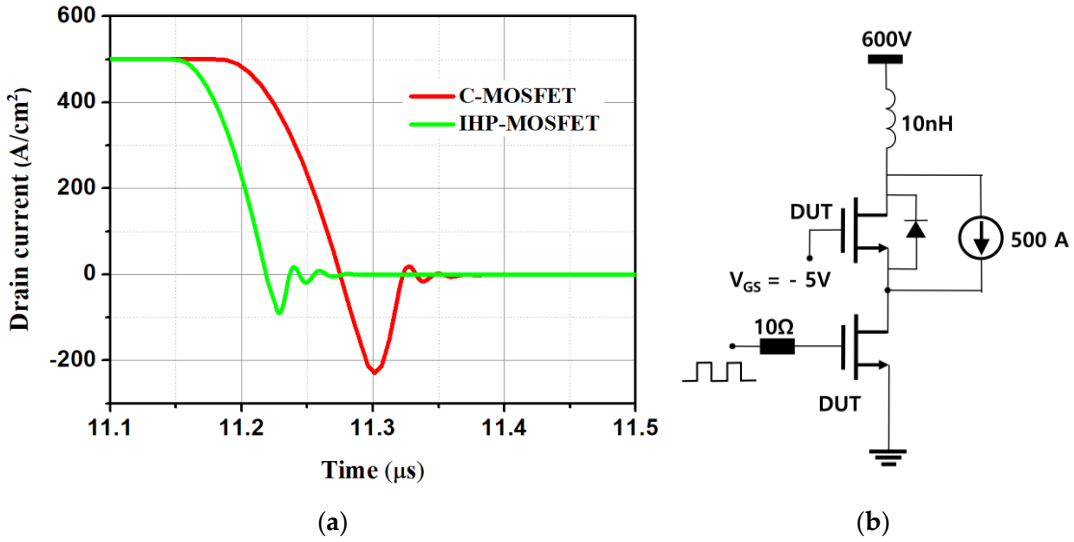

Figure 9. (**a**) Reverse recovery characteristics of the C-MOSFET and IHP-MOSFET. (**b**) Test circuit for reverse recovery characteristics.

Table 2. Device characteristics comparison.

	C-MOSFET	IHP-MOSFET	Unit
V_F [1]	2.91	1.83	V
BV [2]	1223	1489	V
R_{ON} [3]	1.74	1.88	mΩ·cm^2
BFOM (= BV^2/R_{ON})	860	1179	MW/cm^2
C_{ISS} [4]	28.48	22.51	nF/cm^2
C_{GD} [4]	93.25	23.89	pF/cm^2
C_{OSS} [4]	951.89	962.42	pF/cm^2
HFFOM (= $R_{ON} \times C_{GD}$)	162.26	44.91	mΩ·pF
I_{RRM}	230	90	A/cm^2
t_{rr}	48	18	ns
Q_{rr}	6220	890	nC/cm^2

[1] V_F was obtained at $V_{GS} = -5$ V and $I_{DS} = -100$ A/cm^2. [2] BV was obtained at $V_{GS} = 0$ V and $I_{DS} = 1$ μA/cm^2. [3] R_{ON} was obtained at $V_{GS} = 15$ V and $I_{DS} = 100$ A/cm^2. [4] Value of the parasitic capacitances was obtained at $V_{DS} = 600$ V.

Figures 10 and 11 show the switching waveforms and switching power losses of the two devices, respectively. The test circuit in Figure 9b was also used in the double-pulse switching simulation. In Figure 10, the IHP-MOSFET has the largest dV_{DS}/dt during turn-on and turn-off transients because of the smaller C_{GD} compared to the C-MOSFET.

In addition, the IHP-MOSFET showed a smaller peak current during switching turn-on transients. This was because of the improved reverse recovery characteristics of the proposed device. As a result, the IHP-MOSFET boasts much shorter switching time and smaller switching energy loss compared to the C-MOSFET. The switching characteristics of both devices are summarized in Table 3.

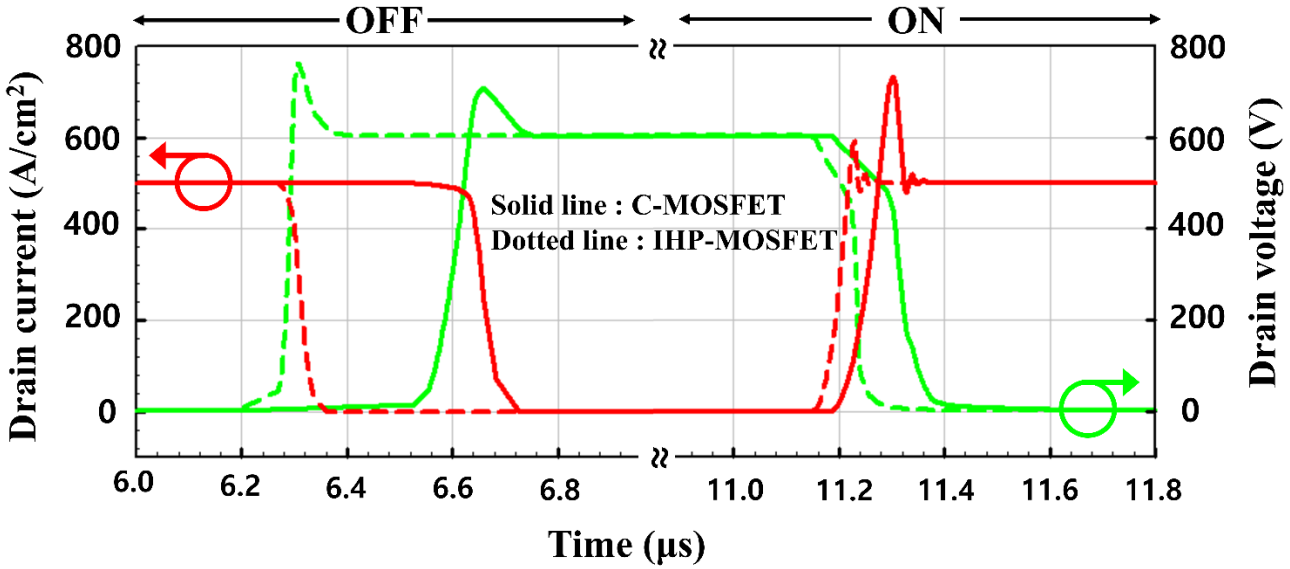

Figure 10. Switching waveforms of both devices.

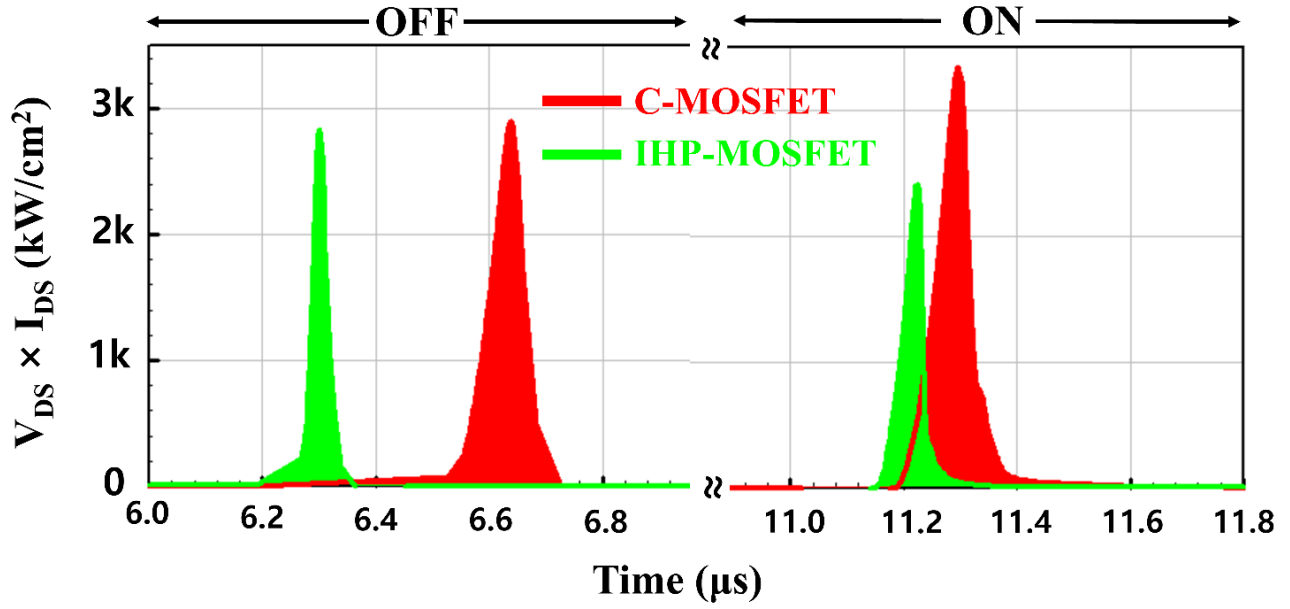

Figure 11. The switching energy losses of both devices.

Table 3. Switching characteristics comparison.

	C-MOSFET	IHP-MOSFET	Unit
T_{OFF}	544	244	ns
T_{ON}	303	197	ns
E_{OFF}	10.70	3.70	mJ/cm^2
E_{ON}	23.25	10.05	mJ/cm^2
E_{SW} (= E_{ON} + E_{OFF})	33.95	13.75	mJ/cm^2

4. Conclusions

A novel 1.2 kV class SiC IHP-MOSFET was proposed and investigated through numerical TCAD simulation. In addition, the possible fabrication procedures of an IHP-MOSFET were proposed to demonstrate the feasibility of the proposed device. Owing to the unipolar action of the HJD, composed of polysilicon and N-SiC, integrated in the mesa region, the proposed device featured superior reverse recovery characteristics compared to the C-MOSFET. The results showed that the t_{rr} and the Q_{rr} of the IHP-MOSFET were improved by 62.5% and 85.7%, respectively.

The PSR under the P+ polysilicon in the IHP-MOSFET effectively dissipated the electric field, resulting in a high BV and low E_{MOX}. Therefore, the BFOM of the proposed device was improved by 37%, indicating a great trade-off between R_{ON} and BV. Moreover, the C_{GD} of the IHP-MOSFET was reduced by a factor of 3.9 because of the split-gate structure and grounded PSR. Furthermore, the results showed that the IHP-MOSFET boasted a much lower switching energy loss and shorter switching time.

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