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A Bimodal Multichannel Battery Pack Equalizer Based on a Quasi-Resonant Two-Transistor Forward Converter

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Abstract: In the application of a long series battery group, an inter-pack imbalance is inevitable. No intra-pack cell equalizer can prevent pack-level over-discharge. A bimodal, multichannel battery pack equalizer based on a quasi-resonant, two-transistor forward converter is proposed to solve this problem and achieve a tradeoff between balancing efficiency and speed. This equalizer has two modes: pack-to-pack-group and pack-to-any-pack (P2PG&AP) mode and direct-pack-to-pack (DP2P) mode. In P2PG&AP mode, this equalizer can realize the full-switching-cycle (FSC) equalization through three balancing channels, and transfer energy from any pack to both the whole group and any pack inside the group. In addition, it can effectively clamp the transformer-induced voltage using a secondary side two-transistor magnetic reset structure (STMR) and reduce the total turns of transformer coil from 70 to 50 turns via a secondary side boost converter (SBC). In DP2P mode, this equalizer can realize zero voltage gap (ZVG) equalization. A prototype was tested at different switching frequencies and LC values to validate the theoretical analysis and optimize the bimodal hybrid operation. Experiment results including higher than 89.66% efficiency and minute-level balancing time under different pack voltage distributions show that the proposed topology demonstrates excellent balancing performance.

Keywords: FSC equalization; LC series quasi-resonator; Two-transistor forward converter; ZVG equalization

Citation: Wu, Q.; Gao, M.; Lin, H.; Dong, Z. A Bimodal Multichannel Battery Pack Equalizer Based on a Quasi-Resonant Two-Transistor Forward Converter. *Energies* **2021**, *14*, 1112. https://doi.org/10.3390/en14041112

Academic Editor: Branislav Hredzak

Received: 31 December 2020
Accepted: 14 February 2021
Published: 19 February 2021

1. Introduction

Nowadays, the application of clean energy is a trend. Lithium-ion batteries are being more and more widely used [1]. As the cell voltage of a lithium-ion battery is low, battery packs made of a certain number of battery cells in series are used. Although the consistency of lithium batteries is constantly improving, the imbalances caused by slight differences of batteries in capacity, internal resistance, self-discharge rate, etc., are still unavoidable during use [2,3]. At present, there are many studies on the balancing technology of battery cells [4–17].

However, electric vehicles [18], mobile robots [19], space rovers [20,21], smart energy storage devices [22], and other high-power applications always need large numbers of in-series cells. In order to reduce the complexity of the cell equalizer and improve the reliability, several modular battery packs are series connected to form a pack group. For example, the battery group of Tesla Model S is composed of 16 series packs, and each pack has 6 cell parallel modules in series [23]. Obviously, the intra-pack cell equalizer cannot purposefully eliminate the imbalance between the battery packs, especially the pack-level over-discharge. Pack-level over-discharge means that there is a certain number of over-discharged batteries in one battery pack at the same time, and the total discharge time of the single battery pack is insufficient, which will cause the entire battery pack group to stop working. The effective solution is to use a pack equalizer.

The balancing strategy of pack equalizer is similar to the cell equalizer, which can also be divided into passive and active methods.

The passive method realizes equalization by dissipating the energy of overcharged battery through parallel power resistor [24]. Obviously, the passive method comes at the cost of reducing the overall discharge time of battery pack group.

In contrast, the active method can transfer the energy of the battery instead of venting it. Many studies have focused on the active method applied to a cell equalizer. This method can be divided into five categories: single to group [4,5], group to single [6,7], adjacent type [8–11], direct type [12–15], and hybrid type [16,17]. The active method's energy transfer device can be an inductor, a capacitor, a transformer, or their combination. The disadvantages of active cell equalizers are higher cost and larger volume. Additionally, because of localized high temperature and complex EMI environment, the battery module's reliability decreases with a significant increase in the number of active cell equalizers used. However, if these structures are applied to pack equalizer, the reduction in the number of balancing objects changing from cells to packs and the significantly dropped ratio of equalizer's cost to power level are both obvious advantages.

According to different operation conditions, battery pack equalizers can be divided into cooperative and independent types. The cooperative type needs to cooperate with the intra-pack cell equalizer to perform its function [25–27]. It requires that the cell equalizer must have a cell-to-pack or pack-to-cell balancing function. Shang et al. [25] designed a modular multiwinding transformer to integrate the pack and cell equalizer. This integrated equalizer can achieve the balance between two or more designated battery packs by cooperating with cell equalization simultaneously, but at the cost of the transformer volume and leakage inductance loss. Farzan et al. [26] proposed a forward cell equalizer fed by a buck pack equalizer. This buck pack equalizer provides a DC bus for the pack-to-cell forward equalizer, and each cell equalizer is connected to the bus. The multiwinding forward transformer inside every pack realizes magnetic reset by the way of a parallel capacitor. Zhong et al. [27] used several 400V to 12 V DC-DC converters incorporating intra-pack BMSs and a low-voltage (LV) bus supply to realize the hierarchical model predictive control pack equalization.

The independent pack equalizer can balance battery packs independently, which means it can adapt to any structure of the lower cell equalizer [28,29]. This facilitates structure simplification and integration of the cell equalizer on a chip. Park et al. [28] introduced and compared a switch capacitor-based pack-to-pack equalizer and a flyback multiwinding transformer-based pack-to-pack equalizer respectively, and eventually chose a switched capacitor pack equalizer to reduce volume, cost, and energy consumption. However, its balancing speed is limited by the packs' voltage difference. Dong et al. [29] proposed a multi-layer adjacent equalizer which relies on an inductor as an energy transfer device. Its bottom layer can balance adjacent cells, and its upper layer is responsible for balancing adjacent multicells or packs.

In general, restricted by the performance and cost of the power switch, the existing independent equalizer structures were relatively simple, and the cooperative pack equalizers were more common. Nevertheless, with the rapid development of MODFET manufacturing technology and pack-level SOC estimation [30], the superiority of an independent active pack equalizer has emerged.

This paper proposes a new active independent pack equalizer and makes three original contributions.

1. Full-switching-cycle (FSC) equalization, which was verified by simulation and experimental waveforms, was innovatively realized by a quasi-resonant, two-transistor forward converter. This structure can not only limit the forward transformer's induced EMF without the forward transformer's magnetic reset coil, but also obtain three balancing channels in each switching cycle.

2. The bimodal hybrid control strategy was designed to achieve a tradeoff between balancing efficiency and speed, which can select the best operation mode according to the status of battery pack group.
3. The experimental data of the prototype, which was in good agreement with theoretical and simulation analysis, confirmed the proposed pack equalizer's ability to prevent pack-level over-discharge.

2. Proposed Pack Equalizer

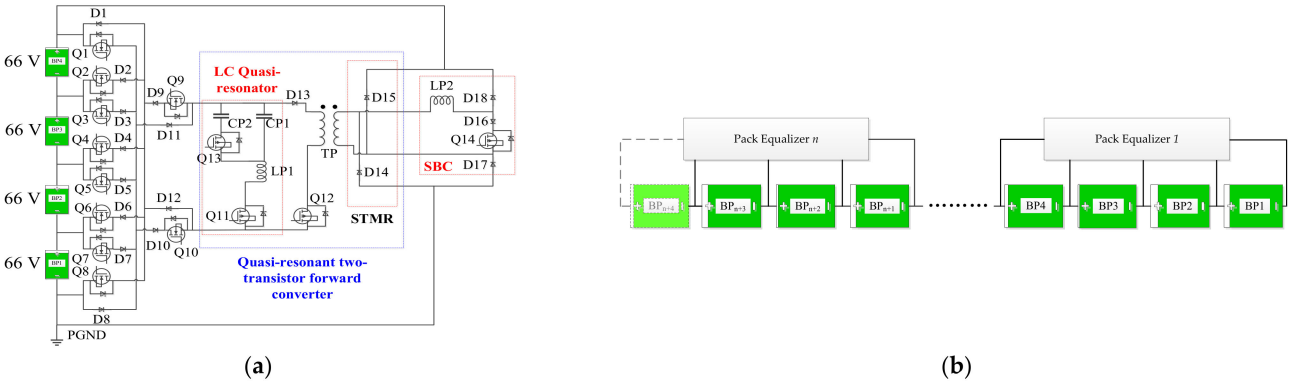
Before starting the system analysis, the abbreviations and explanations of all the special nouns in the paper are listed in Table 1.

Table 1. The abbreviations and explanations of all the special nouns.

Abbreviations	Explanations
P2PG&AP	pack-to-pack-group and pack-to- any-pack
DP2P	direct-pack-to-pack
STMR	secondary side two-transistor magnetic reset structure
SBC	secondary side boost converter
FSC	full-switching-cycle
ZVG	zero voltage gap
LC2AP	LC quasi-resonator to any pack

2.1. Pack Equalizer Configuration and Operation Principles

The proposed bimodal multichannel pack equalizer, which takes a high-voltage battery pack but not a low-voltage battery cell as an equalization object, consists of a switch array, a two-transistor forward converter, an LC quasi-resonator, and a side boost converter (SBC), as shown in Figure 1a. It can use other channels or switch to the other mode when one balancing channel fails. This is of great significance to improve the reliability of high-power, fast inter-pack equalization.



(**a**) (**b**)

Figure 1. The proposed pack equalizer. (**a**) The circuit diagram of the proposed pack equalizer. (**b**) The application in a larger battery pack group.

The switch array can minimize the number of transformers and their windings in the pack equalizer topology. Compared with multi winding transformer and multi transformer structure, it has great advantages in cost reduction and the low weight of high-power pack equalizer. However, the cost is that the two power switches at the top and bottom of array need to be able to bear the voltage of entire pack group [4].

The two-transistor forward converter, composed of the forward transformer TP and STMR, is mainly used in pack-to-pack-group and pack-to-any-pack (P2PG&AP) mode. When the primary circuit turns on, TP transfers energy to the whole pack group through SBC. After the primary circuit turns off, the main part of the remanence energy in TP is transferred to the whole pack group through two magnetic reset diodes at the secondary

side. This process realizes the voltage clamp of TP and FSC equalization simultaneously. The magnetic reset diodes are designed on the secondary side instead of the primary side. As a result, the primary coil-induced EMF of the off-state forward transformer can be further reduced by the effect of transformer turns ratio. Moreover, the other part of the remanence energy is stored in the capacitor CP1 to realize LC quasi-resonator to any pack (LC2AP) equalization. In DP2P mode, the primary circuit of TP is used as a part of the quasi-resonant loop to achieve ZVG equalization.

When SBC is not added, the turn ratio of transformer needs to be at least 1/6 to smoothly output the balancing current. This is because the turn-on resistance of MOSFETs and the forward turn-on voltage drop of diodes in the primary circuit will reduce the actual voltage of TP's primary coil. SBC can quickly extract part of the energy charged into TP when the forward switch is on, and transfer it to the boost inductor LP2. The sum of the induced EMF of the secondary coil and LP2 can effectively raise the output voltage. When the turn ratio of the transformer is 1/4, it can also turn on D17 and D18 to output the balanced current. This greatly reduces the total turn ratio of TP and makes the transformer design miniaturized. At the same time, D17 and D18 clamp the voltage on Q14 to the total voltage of the entire battery pack group.

The LC series quasi-resonator has two functions. In P2PG&AP mode, CP1 can absorb the peak voltage of the transformer at the moment when the forward circuit turns off, and transmit this part of energy to any battery pack through the switch array in reverse; this auxiliary equalization function means that the equalizer can not only equalize from a single battery pack to the whole pack group, but also selectively equalize to any pack in group simultaneously in each switching cycle. Additionally, the equalization speed is improved innovatively, which is not available in the conventional single to group mode. In DP2P mode, CP1 and CP2 act as the core energy transfer device together with LP1. Q13 is used to select different capacitance values for quasi-resonator. A large CP1 value in P2PG&AP mode limits the switching frequency rise for keeping Q11 in a nearly zero-current switching state. This is detrimental to equalizer's efficiency performance at high-power operation.

The proposed pack equalizer can cooperate with passive and chip intra-pack cell equalizers with the ability to prevent pack-level over-discharge. In the application of a long series battery group, this combination is simpler, lower cost, and smaller volume than the two-stage equalizers in [25–27]. The independent pack equalizer based on the switched capacitor in [28,29] can only achieve hour-level balancing speed, whereas the proposed pack equalizer can achieve minute level balancing speed.

Power Schottky diodes are used in the proposed pack equalizer. Their forward voltage drop is far lower than battery pack's terminal voltage, which is a guarantee of high energy efficiency.

Compared with the cell equalizer, the switching devices of the pack equalizer need a higher withstand voltage. It is a fact that under the condition of the same withstand current value, MOSFETs with higher withstand voltage have lower switching speed, while the power diode with a higher withstand voltage has a higher forward voltage drop. These are the main factors affecting the equalizer efficiency. Moreover, a MOSFET with higher power and faster speed has a higher price. Thereby, although the switch array in the proposed topology has no theoretical limit on balancing objects' number [4], in engineering, this number needs to achieve a compromise with energy efficiency and cost. In the following discussion of this paper, the balancing objects will be composed of four 20-series battery packs. In the application of a larger battery pack group, multiple proposed pack equalizers are used for inter-pack equalization, as shown in Figure 1b.

2.2. Operation Principles, Modeling, and Analysis of P2PG&AP Mode

In P2PG&AP mode, the proposed equalizer provides the first equalization path through TP during the on period of the forward switch. When the forward switch turns off, the equalizer generates the second equalization path through STMR to the whole group and the third equalization path from the LC quasi-resonator to a single pack. Differently

from the conventional equalizer structure, which can only use part of the switching cycle to transfer energy, the proposed equalizer realizes the multichannel FSC equalization to effectively improve the equalization speed.

The switch pair Qi and Q(i + 1) in the switch array are driven by the same forward PWM wave with an adjustable duty cycle. Switch Q12 is driven by another synchronous PWM wave with higher duty cycle. Switch Q11 and another switch pair Qj and Q(j + 1) are driven by the PWM wave complementary to Q12's PWM wave. The PWM signal of the SBC switch Q14 is obtained by superposition of two narrow pulse signals with identical duty cycles proportional to the forward PWM wave and the same frequency. Switches Q9, Q10, and Q13 are always off in this mode. The time sequence relationship of all PWM wave is shown in Figure 2a, and the period 0–t_{01} is the dead-time between forward switches and Q14. The relationship between the time points is as follows:

$$\begin{cases} t_{02} = t_{01} + D_B \cdot T_0 \\ t_{03} = t_{01} + 0.5D_F \cdot T_0 \\ t_{04} = t_{03} + D_B \cdot T_0 \\ t_{05} = D_F \cdot T_0 \\ t_{06} = (1 - D_{LC}) \cdot T_0 \end{cases} \quad (1)$$

where D_F is the duty cycle of forward PWM wave, D_B is the duty cycle of SBC PWM wave, and D_{LC} is the duty cycle of LC quasi-resonator PWM wave.

Figure 2b–e shows the operation principle when BP1 releases energy to the whole pack group, and BP3 obtains the reverse charging from LC quasi-resonator. In the following analysis of P2PG&AP mode, this state will be used as the example.

State I (0–t_{01}, Figure 2b): Q7, Q8, and Q12 are on simultaneously; the peak-induced voltage produced by TP's secondary coil turns on D17 and D18 to output balancing energy to the whole group; as the voltage of the secondary side drops, the balancing current of the secondary side decreases.

State II ($t_{01}-t_{02}$, Figure 2c): Q14 is on, and the energy of TP is transferred to LP2.

State III ($t_{02}-t_{03}$, Figure 2b): Q14 turns off, and Q7, Q8, and Q12 stay on. The inductances of the TP secondary coil and boost inductor LP2 generate induced voltage to turn on D17 and D18 to output balancing energy to the whole group again.

State IV (t_{03}–t_{04}, Figure 2c) and *state V* (t_{04}–t_{05}, Figure 2b): *State IV* and *state V* respectively repeat the processes of *state II* and *state III*. Q14 remains off after t_{04} in each switching cycle.

State VI (t_{05}–t_{06}, Figure 2d): Q7 and Q8 turn off at t_{05}, and Q12 remains in the on-state. Most of the remanence energy of TP charges to the whole pack group through D14 and D15. A small part of the remanence energy is stored in CP1 through Q12 and the body diode in Q11. The residual energy of LP2 continues to charge the whole pack group through D18 and D14 until the voltage of LP2 drops down.

State VII (t_{06}–T_0, Figure 2e): Q12 turns off, then Q11 turns on, the LC2AP equalization is activated. The energy of CP1 reversely charges to any battery pack selected by the controller through switch array. Additionally, the P2PG equalization through STMR continues until the remanence magnetic energy of the transformer is exhausted.

In the period of $0-t_{05}$, as shown in Figure 2b–c, the equalizer circuit meets the following expressions (ignoring C_{oss} of all MOSFETs and C_j of all diodes):

$$\begin{cases} E_1 = R_m \cdot (i_1 - i_{2\_B}) + L_m \cdot \frac{d(i_1 - i_{2\_B})}{dt} = V_{BP1} - L_{\sigma 1} \cdot \frac{di_1}{dt} - i_1 \cdot R_{eq1\_1} - \sum_{i=7,11,12,13} V_{F\_Di} \quad (0 < t \le t_{05}) \\ E_2 = 4E_1 = (L_{\sigma 2} + LP2) \cdot \frac{di_{2\_B}}{dt} + i_{2\_B} \cdot R_{eq2\_1} + \sum_{i=17,18} V_{F\_Di} + \sum_{i=1}^{4} V_{BPi} \\ \left(0 < t \le t_{01}, t_{02} < t \le t_{03}, \; and \quad t_{04} < t \le t_{05}\right) \\ E_2 = 4E_1 = (L_{\sigma 2} + LP2) \cdot \frac{di_{2\_B}}{dt} + i_{2\_B} \cdot R_{eq2\_2} + V_{F\_D16} (t_{01} < t \le t_{02}, t_{03} < t \le t_{04}) \end{cases} \quad (2)$$

where the explanations of parameters in Equation (2) are shown in Table 2. The positive direction and path of i_1 is indicated by the red arrows in Figure 2b,c. The positive direction and path of i_{2_B} is indicated by the purple arrows in Figure 2b,c,d.

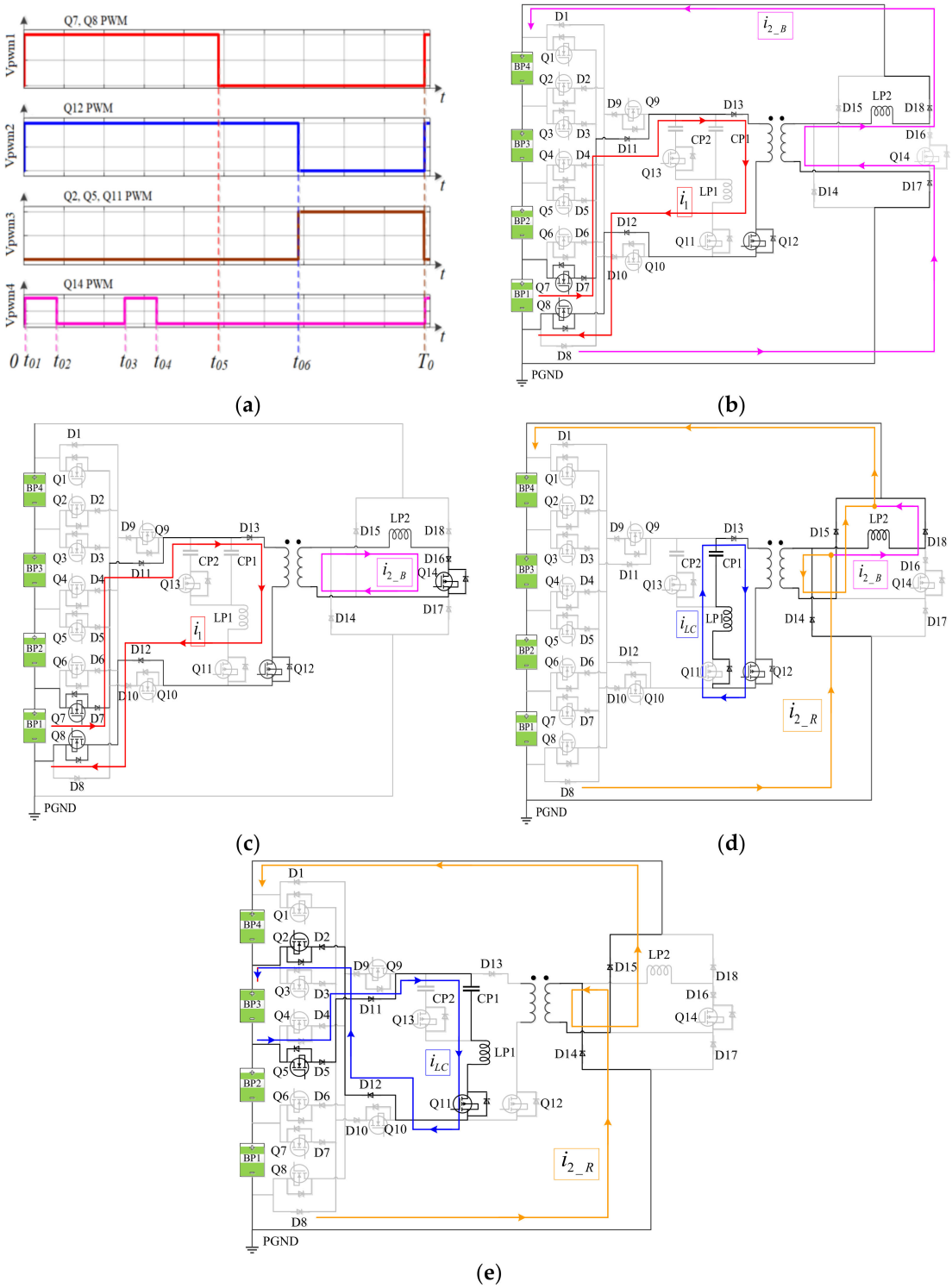


Figure 2. Operating principles of pack-to-pack-group and pack-to-any-pack (P2PG&AP) mode. (**a**) PWM wave sequence diagram of P2PG&AP mode. (**b**) *State I,III and V.* (**c**) *State II,IV.* (**d**) *State VI.* (**e**) *State VII.*

Table 2. Parameters and related explanations in the analysis of a pack equalizer.

Parameters	Explanations
E_1	the EMF value of TP's primary coil
E_2	the EMF value of TP's secondary coil
R_m	the excitation impedance value of TP
i_1	the current value of primary side electrified circuit under different switching states
i_2	the output current value of secondary coil under different switching states
i_{2_B}	the SBC current
i_{LC}	the quasi-resonator current
i_{2_R}	the STMR output current
L_m	the excitation inductance of TP
V_{BPi}	the voltage value of the battery pack BPi
$L_{\sigma 1}$	the leakage inductance of TP's primary coil
$L_{\sigma 2}$	the leakage inductance of TP's secondary coil
R_{eq1_1}	the total equivalent resistance of the primary side electrified circuit in Figure 2b,c
R_{eq1_2}	the total equivalent resistance of the primary side circuit in Figure 2d
R_{eq1_3}	the total equivalent resistance of the primary side circuit in Figure 2e
$\sum V_{F\_D}$	the sum of the forward voltage drop of diodes on the energized circuit
$LP1$	the inductance value of LC quasi-resonator
$LP2$	the boost inductance value of the secondary side
$CP1$	the capacitance value of LC quasi-resonator
C_{oss}	The output capacitance of MOSFET
C_j	The junction capacitance of power diode
R_s	The equivalent resistance of quasi-resonator
R_{eq2_1}	the total equivalent resistance of the secondary side electrified circuit in Figure 2b
R_{eq2_2}	the total equivalent resistance of the secondary side electrified circuit in Figure 2c
R_{eq2_3}	the equivalent resistance of SBC circuit in Figure 2d
R_{eq2_4}	the equivalent resistance of STMR in both Figure 2d, e

By solving Equation (1) with $i_1(0) = i_{2\_B}(0) = 0$ and ignoring R_m and all equivalent resistances, primary and secondary currents in the period of $0 < t \leq t_{01}$, $t_{02} < t \leq t_{03}$, and $t_{04} < t \leq t_{05}$ can be deduced as:

$$\begin{cases} i_1 = i_1(t_{0x}) - \frac{L_m \cdot (F+H) + F \cdot G - V_{BP1} \cdot (L_m + G)}{L_m \cdot L_{\sigma 1} + (L_m + L_{\sigma 1}) \cdot G} \cdot (t - t_{0x}) \\ i_{2\_B} = i_{2\_B}(t_{0x}) - \frac{H \cdot L_{\sigma 1} + L_m \cdot (F+H) - V_{BP1} \cdot L_m}{L_m \cdot L_{\sigma 1} + (L_m + L_{\sigma 1}) \cdot G} \cdot (t - t_{0x}) \end{cases} \quad (3)$$

Additionally, in the period of $t_{01} < t \leq t_{02}$, and $t_{03} < t \leq t_{04}$, they are:

$$\begin{cases} i_1 = i_1(t_{0x}) + \frac{V_{BP1} \cdot (L_m + G) - L_m \cdot (F+I) - F \cdot G}{L_m \cdot L_{\sigma 1} + (L_m + L_{\sigma 1}) \cdot G} \cdot (t - t_{0x}) \\ i_{2\_B} = i_{2\_B}(t_{0x}) + \frac{V_{BP1} \cdot L_m - I \cdot L_{\sigma 1} - L_m \cdot (F+I)}{L_m \cdot L_{\sigma 1} + (L_m + L_{\sigma 1}) \cdot G} \cdot (t - t_{0x}) \end{cases} \quad (4)$$

where $F = \sum_{i=7,11,12,13} V_{F\_Di}$, $G = (L_{\sigma 2} + LP2)/4$, $H = \sum_{i=17,18} V_{F\_Di}/4 + \sum_{i=1}^{4} V_{BPi}/4$, $I = V_{F\_D16}/4$, and t_{0x} is the initial moment of each switching state by turn.

According to Equations (3) and (4), when V_{BP1} increases, i_1 and i_{2_B} increase; when $LP2$ increases, i_1 and i_{2_B} decrease because $L_{\sigma 1}$ is smaller than L_m; when F, H, or I increases, i_1 and i_{2_B} decrease.

In period of t_{05}–T_0, as shown in Figure 2d, e, the equalizer circuit meets:

$$\begin{cases} E_1 = R_m \cdot (i_{LC} - i_{2\_R}) + L_m \cdot \frac{d(i_{LC} - i_{2\_R})}{dt} & (t_{05} < t \le t_{06}) \\ \quad = LP1 \cdot \frac{di_{LC}}{dt} + CP1^{-1} \cdot \int_{t_{05}}^{t_{06}} i_{LC} dt + i_{LC} \cdot R_{eq1\_2} + V_{F\_D13} + V_{F\_Q11} & \\ CP1^{-1} \cdot \int_{t_{06}}^{T_0} i_{LC} dt + LP1 \cdot \frac{di_{LC}}{dt} + i_{LC} \cdot R_{eq1\_3} + \sum_{i=2,5,11,12} V_{F\_D} + V_{BP3} = 0 & \\ & (t_{06} < t \le T_0) \\ E_2 = 4E_1 = L_{\sigma 2} \cdot \frac{di_{2\_R}}{dt} + i_{2\_R} \cdot R_{eq2\_4} + \sum_{i=14,15} V_{F\_Di} + \sum_{i=1}^{4} V_{BPi} & \\ & (t_{05} < t \le T_0) \\ LP2 \cdot \frac{di_{2\_B}}{dt} = i_{2\_B} \cdot R_{eq2\_3} + \sum_{i=14,15} V_{F\_Di} + \sum_{i=1}^{4} V_{BPi} & (t_{05} < t \le T_0) \end{cases} \quad (5)$$

where the explanations of parameters in Equation (5) are also shown in Table 2. The positive direction and path of i_{LC} is indicated by the blue arrows in Figure 2d,e. The positive direction and path of i_{2_R} is indicated by the yellow arrows in Figure 2d and e.

It can be found that the solution of Equation (5) is mathematically complex and not intuitive enough. MATLAB/Simulink simulation was done to verify the currents and the design parameters of the equalizer. The waveforms of currents are shown in Figure 3. Table 3 lists the relevant parameters of the simulation experiment.

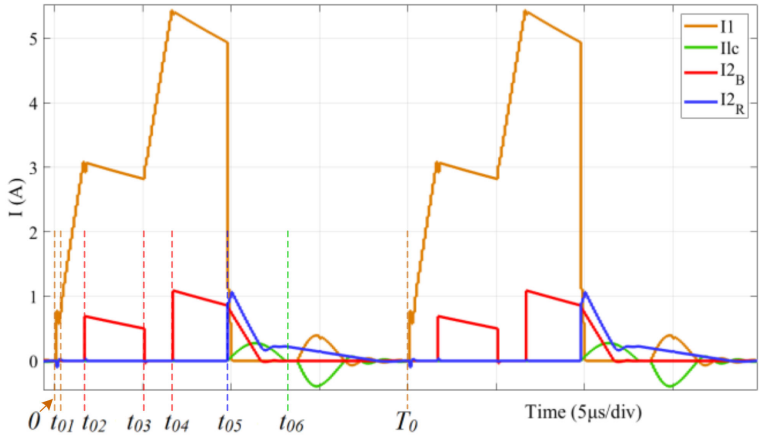


Figure 3. The simulation waveform of i_1, i_{LC}, i_{2_B}, i_{2_R} in P2PG&AP mode.

Table 3. Parameters of simulation experiment.

Parameter	Value
D_F	0.485
D_B	0.08
D_{LC}	0.315
L_m	360 μH
$LP1$	330 μH
$CP1$	3.3 nF
$LP2$	330 μH
$CP2$	150 nF
Turns ratio of TP	1/4

In Figure 3, the trends of i_1 and i_{2_B} conform to Equations (3) and (4) during 0–t_{05}. Furthermore, under suitable D_F and D_B, as shown in Table 3, the transformer is completely demagnetized when magnetic reset current drops to zero at the end of each cycle, and SBC works in discontinuous current mode. LC quasi-resonant current during t_{05}–T_0 is approximately sinusoidal.

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In the actual circuit design, we have to consider the fact that Q11 can not completely block the current of LC quasi-resonator during 0–t_{05} due to the output capacitance of Q11. This current can be described by the time domain expression of LC quasi-resonant current [12]:

$$\begin{cases} i_{LC} = \frac{2(V_{BP1\_U} - V_{BP1\_D})}{\pi \cdot R_s} \cdot \sin(2\pi \cdot f_{Qr} \cdot t) \cdot e^{\frac{-R_s}{2 \cdot LP1} \cdot t} \\ f_{Qr} = \sqrt{\frac{1}{LP1 \cdot C_{eq}} - \frac{R_s^2}{4LP1}} / 2\pi \\ C_{eq} = (CP1 + CP2 // C_{oss\_Q13}) // C_{oss\_Q11} \\ \quad \approx \frac{(CP1 + C_{oss\_Q13}) \cdot C_{oss\_Q11}}{CP1 + C_{oss\_Q13} + C_{oss\_Q11}} \end{cases} \quad (6)$$

where V_{BP1} is the average voltage value of BP1, V_{BP1_U} and V_{BP1_D} are upper and lower voltages of V_{BP1} fluctuation, C_{eq} is the equivalent capacitance of quasi-resonator, C_{OSS_Q11} and C_{OSS_Q13} are the output capacitance of Q11 and Q13, f_{Qr} is the frequency of quasi-resonator current in $0-t_{05}$.

It can be seen that a MOSFET with smaller C_{OSS} used as Q11 can effectively reduce the quasi-resonator current in $0-t_{05}$, but its on-state resistance will increase accordingly, which is detrimental to the energy efficiency of both P2PG&AP mode and DP2P mode.

2.3. Operation Principles, Modelling, and Analysis of DP2P Mode

The DP2P mode is just a three state quasi-resonator [8] with direct balancing topology, which is suitable for situations where the voltage difference between battery packs is close to zero. In this mode, the switch pair Qi and Q(i + 1) connected to donor battery pack are first on. Additionally, the switch pair Qj and Q(j + 1) (j ≠ i) connected to acceptor battery pack turn on together with Q9 and Q10 after Qi and Q(i+1) turn off. The PWM wave of switch Q12 turns on the quasi-resonance to realize ZVG equalization after Qj, Q(j + 1), Q9 and Q10 turn off. In DP2P mode, Q11 and Q13 are always on, and Q14 is always off. Figure 4 shows the operation principle when BP1 is donor battery pack, and BP3 is acceptor battery pack. In the following analysis of DP2P mode, this state will be used as the example.

State I ($0-t_{11}$, Figure 4b): After Q11 and Q13 turn on, Q7 and Q8 turn on simultaneously. BP1 charges the CP1, CP2, and LP1. The capacitor voltage increases from value V_{Cd} to V_{Cu}. At the same time, the discharge current of donor pack rises from 0, changes in the form of sine half wave. When the discharge current drops to 0, turn off the Q7 and Q8.

State II ($t_{11}-t_{12}$, Figure 4c): After Q7 and Q8 turn off, Q2, Q5, Q9, and Q10 turn on simultaneously, and the capacitor and inductor begin to release energy to BP3. The capacitor voltage decreases from value V_{Cu} to V_{Qr}. The trend of charge current is similar to that of discharge current, but the direction is opposite. When the charge current drops to 0, turn off the Q2, Q5, Q9 and Q10.

State III (t_{12}–T_1, Figure 4d): After Q2, Q5, Q9 and Q10 turn off, Q12 turns on, and the capacitor and inductor form a quasi-resonant circuit. As the quasi-resonant current first increases and then returns to zero, the capacitor voltage decreases to value V_{Cd}. This process increases the gap between the voltage of BP1 and the capacitor voltage, speeds up the charging speed of BP1 to the capacitor and inductor in *State I* of the next cycle, thereby realizing the ZVG equalization between battery packs.

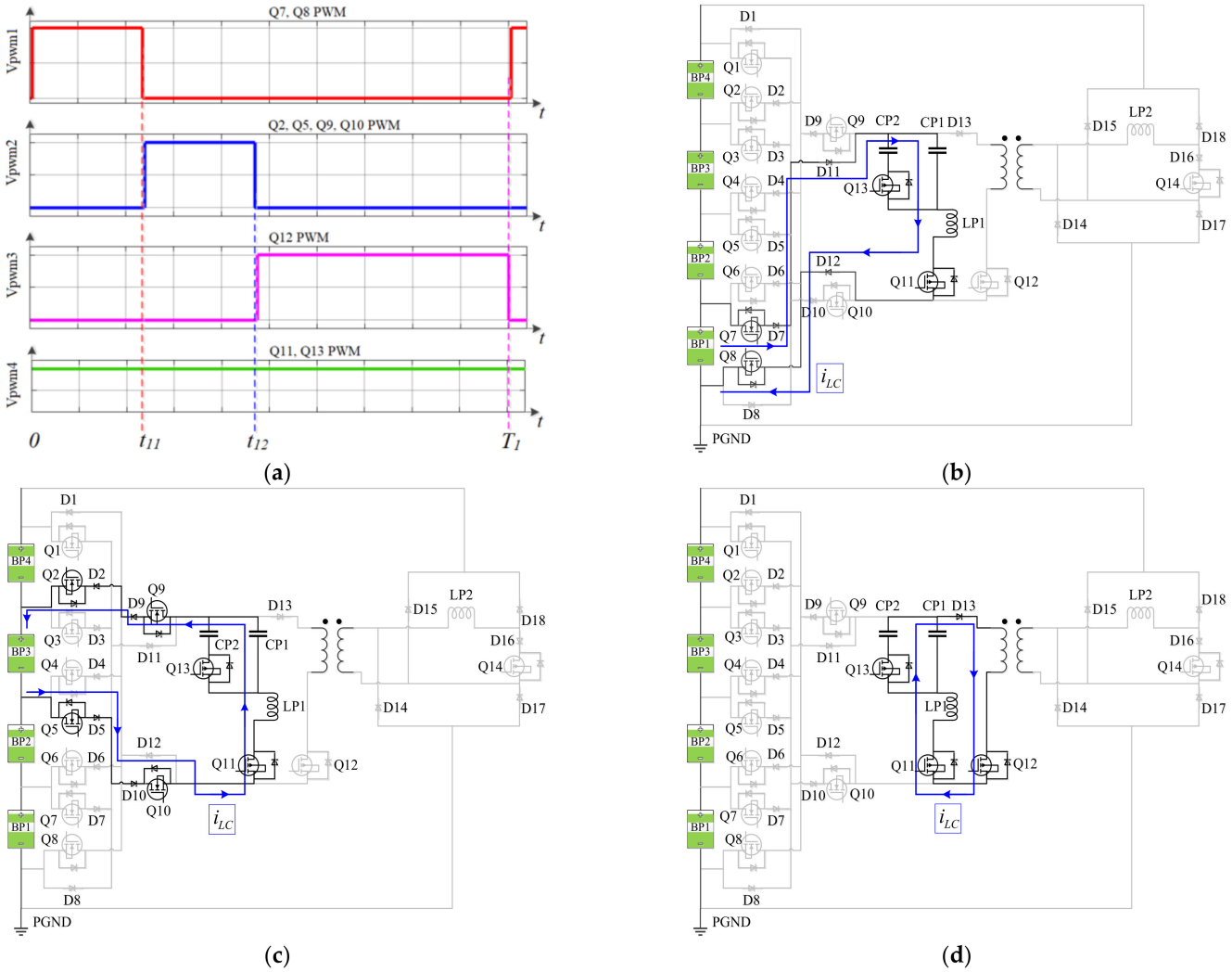

Figure 4. Operating principles of DP2P mode. (**a**) PWM wave sequence diagram of DP2P mode. (**b**) *State I*. (**c**) *State II*. (**d**) *State III*.

According to [8], the value of V_{Cd}, V_{Cu}, and V_{Qr} as shown in Figure 5 are:

$$\begin{cases} V_{Cd} = \frac{\alpha \cdot (\alpha \cdot V_{BP1} - V_{BP3})}{1-\alpha+\alpha^2} \\ V_{Cu} = \frac{V_{BP1} + \alpha^2 \cdot V_{BP3}}{1-\alpha+\alpha^2} \\ V_{Qr} = \frac{(1-\alpha) \cdot V_{BP3}}{1-\alpha+\alpha^2} \end{cases} \tag{7}$$

where R_s is the equivalent resistance of quasi-resonator, α and δ are defined as follows:

$$\begin{cases} \alpha = \frac{e^{-\pi\delta/\sqrt{1-\delta^2}}}{\sqrt{1-\delta^2}} \\ \delta = \frac{R_s}{2\sqrt{LP1/(CP1+CP2)}} \end{cases} \tag{8}$$

The simulation waveforms in Figure 5 are obtained when $V_{BP1} = V_{BP3} = 66V$ with the same parameters in Table 3. This illustrates that the capacitor voltage can reduce to negative in the third stage of quasi-resonant process, and ZVG equalization can be achieved.

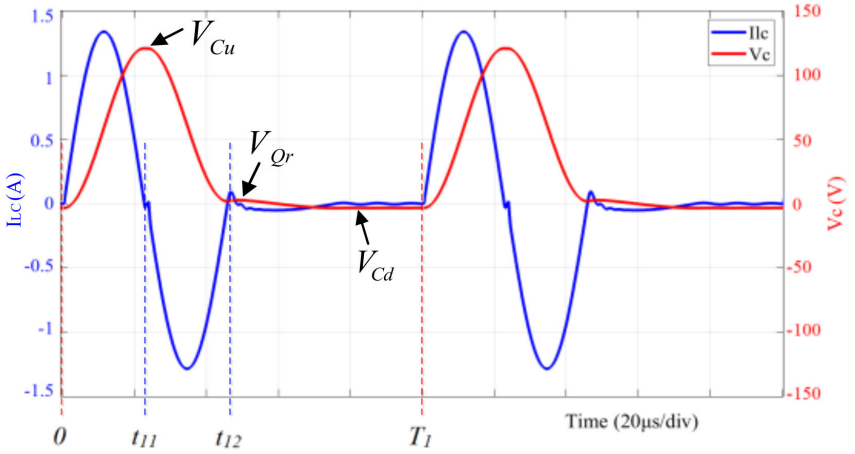

Figure 5. The waveform of capacitor voltage and quasi-resonant current.

2.4. Equalizer Efficiency and Loss Analysis of P2PG&AP Mode

In this mode, the input power of the equalizer is the power provided by the donor battery pack:

$$P_{in} = p_{prim} + p_{LCQr} + P_{TP\_prim} = \frac{1}{T_0}\int_0^{t_{05}} V_{BP1} \cdot i_1 dt \quad (9)$$

where the explanations of parameters in (9) are shown as Table 4.

Table 4. Parameters and related explanations in the efficiency and loss analysis.

Parameters	Explanations
P_{in}	The total input power of pack equalizer
p_{prim}	the conduction and switching loss of all primary lines
p_{LCQr}	the average power loss of LC quasi-resonator caused by output capacitance of Q11 in $0-t_{05}$
P_{TP_prim}	the primary input power of transformer TP
P_{out}	the total output power of pack equalizer
P_{SBC_out}	the average power output from SBC to the whole pack group in $0-t_{05}$
P_{STMR_out}	the average power output from STMR to the whole group in $t_{05}-T_0$
P_{LC_out}	the average power of the LC quasi-resonator reversely charging into the acceptor battery pack in t_{06}–T_0
$\eta_{P2PG\&AP}$	the equalizer energy efficiency of P2PG&AP mode
η_{SBC}	the ratios of output powers from SBC to input power of equalizer
η_{STMR}	the ratios of output powers from STMR to input power of equalizer
η_{LC}	the ratios of output powers from LC quasi-resonator to input power of equalizer
p_{cond}	The circuit conduction loss of equalizer
R_{eq1_4}	the total equivalent resistance of the primary side circuit in Figure 4b
R_{eq1_5}	the total equivalent resistance of the primary side circuit in Figure 4c
R_{eq1_6}	the total equivalent resistance of the primary side circuit in Figure 4d
p_{sw}	The switching loss of equalizer
p_{core}	The core loss of equalizer's transformer
p_{open}	the turn-on losses of power switch
p_{close}	the turn-off losses of power switch
f_{sw}	the switching frequency
V_{open}	the withstand voltage of the power switch before it turns on
V_{close}	the withstand voltage of the power switch before it turns on
I_{close}	the turnoff current of MOSFET
t_{fall}	the falling time of MOSFET
I_{rr}	the reverse recovery current of power diode
t_{rr}	the reverse recovery time of power diode

In this mode, the output power of the equalizer is composed of three parts, including P_{SBC_out}, P_{STMR_out}, and P_{LC_out}, and their explanations are shown as in Table 4:

$$\begin{aligned} P_{out} &= P_{SBC\_out} + P_{STMR\_out} + P_{LC\_out} \\ &= \tfrac{1}{T_0} \cdot \left(\int_0^{t_{05}} \sum_{i=1}^{4} V_{BPi} \cdot i_{2\_B} dt + \int_{t_{05}}^{T_0} \sum_{i=1}^{4} V_{BPi} \cdot i_{2\_R} dt + \int_{t_{06}}^{T_0} V_{BP3} \cdot i_1 dt \right) \end{aligned} \tag{10}$$

Therefore, the energy efficiency $\eta_{P2PG\&AP}$ is as follows:

$$\eta_{P2PG\&AP} = P_{SBC\_out}/P_{in} + P_{STMR\_out}/P_{in} + P_{LC\_out}/P_{in} = \eta_{SBC} + \eta_{STMR} + \eta_{LC} \tag{11}$$

where the explanations of η_{SBC}, η_{STMR} and η_{LC} are shown in Table 4.

Otherwise, the loss of equalizer mainly comes from the power loss of LC quasi-resonator, the circuit conduction loss, the switching loss, and the core loss of transformer.

According to Equation (6), the average power loss of LC quasi-resonator in $0-t_{05}$ can be calculated as follows:

$$\begin{cases} p_{LCQr} = \frac{1}{T_0} \cdot \int_0^{t_5} v_{BP1} \cdot i_{LC} dt \approx V_{BP1} \cdot I_{LC} \\ I_{LC} = \frac{2(V_{BP1\_U} - V_{BP1\_D})}{\pi^2 \cdot R_s} \cdot \left(1 - \frac{R_s^2 \cdot C_{eq}}{4LP1}\right) \cdot \left(1 + e^{\frac{-R_S \cdot \pi}{2\sqrt{\frac{LP1}{C_{eq}} - \frac{R_S^2}{4}}}}\right) \end{cases} \tag{12}$$

where v_{BP1} is the real time value of donor pack voltage, I_{LC} is the average value of LC quasi-resonant current.

It can be seen that p_{LCQr} in $0-t_{05}$ is determined by pack voltage fluctuation and LC parameter. Moreover, the LC resonant frequency in $0-t_{05}$ is several times of the switching frequency in the design below.

The circuit conduction loss p_{cond} is:

$$\begin{cases} p_{cond} = p_{cond1} + p_{cond2} \\ p_{cond1} = \frac{1}{T_0} \cdot \left[\int_0^{t_{05}} i_1^2 \cdot R_{eq1\_1} dt + R_{eq2\_1} \cdot \left(\int_0^{t_{01}} i_{2\_B}^2 dt + \int_{t_{02}}^{t_{03}} i_{2\_B}^2 dt + \int_{t_{04}}^{t_{05}} i_{2\_B}^2 dt \right) \right. \\ \quad \left. + R_{eq2\_2} \cdot \left(\int_{t_{01}}^{t_{02}} i_{2\_B}^2 dt + \int_{t_{03}}^{t_{04}} i_{2\_B}^2 dt \right) \right] \qquad (0 < t \le t_{05}) \\ p_{cond2} = \frac{1}{T_0} \cdot \left[\int_{t_{05}}^{t_{06}} \left[i_1 \cdot (V_{F\_D13} + V_{F\_Q11}) + i_1^2 \cdot R_{eq1\_2} \right] dt \qquad (t_{05} < t \le T_0) \right. \\ \quad \left. + \int_{t_{06}}^{T_0} \left(i_1 \cdot \sum_{i=2,5,11,12} V_{F\_Di} + i_1^2 \cdot R_{eq1\_3} \right) dt + \int_{t_{05}}^{T_0} \left(i_{2\_R} \cdot \sum_{i=14,15} V_{F\_Di} + i_{2\_R}^2 \cdot R_{eq2\_4} + i_{2\_B}^2 \cdot R_{eq2\_3} \right) dt \right] \end{cases} \tag{13}$$

According to Equation (13), the conduction loss is mainly affected by primary current, secondary current, equivalent resistance, and forward voltage drop of diodes. Under the same balancing power level, the duty cycle of the equalizer is adjusted accordingly when the switching frequency changes. This means the peak and average value of primary current and the pack voltage fluctuation change little with switching frequency. Therefore, if the effect of other losses is not considered, the switching frequency has little effect on the above two kinds of losses in theory.

The switching loss p_{SW} is:

$$\begin{cases} p_{sw1} = \sum_{i=7,8,14} p_{sw\_Qi} + \sum_{i=7,11,12,16,17,18} p_{sw\_Di} + p_{open\_Q12} + p_{open\_D13} \\ p_{sw2} = \sum_{i=2,5,11} p_{sw\_Qi} + \sum_{i=2,5,11,12,14,15} p_{sw\_Di} + p_{close\_Q12} + p_{close\_D13} \\ p_{sw} = p_{sw1} + p_{sw2} \end{cases} \tag{14}$$

Additionally, the switching loss of MOSFET and diode are [31]:

$$\begin{cases} p_{sw\_Qi} = p_{open\_Qi} + p_{close\_Qi} \\ \qquad = 0.5 f_{sw} \cdot C_{oss} \cdot V_{open}^2 + 0.5 f_{sw} \cdot V_{close} \cdot I_{close} \cdot t_{fall} \\ p_{sw\_Di} = p_{open\_Di} + p_{close\_Di} \\ \qquad = 0.5 f_{sw} \cdot C_j \cdot V_{open}^2 + 0.5 f_{sw} \cdot V_{close} \cdot I_{rr} \cdot t_{rr} \end{cases} \tag{15}$$

where p_{sw_Qi} and p_{sw_Di} are the switching losses of MOSFET and power diode, p_{open_Qi} and p_{close_Qi} are the turn-on and turn-off losses of MOSFET, p_{open_Di} and p_{close_Di} are the turn-on and turn-off losses of power diode. The explanations of other parameters in Equations (14) and (15) are shown in Table 4.

The core loss of transformer p_{core} is [32]:

$$\begin{cases} p_{core} = c_m \cdot c_T \cdot f_{sw}^{\alpha} \cdot \left(\frac{L_m}{N \cdot A_e} \cdot I_{m\_pp}\right)^{\beta} \\ I_{m\_pp} = [i_1(t_{05}) - i_2(t_{05})] - [i_1(0) - i_2(0)] \approx [i_1(t_{05}) - i_2(t_{05})] \end{cases} \tag{16}$$

where c_m,c_T,α, and β are the Steinmetz coefficients provided by manufacturer, N is the number of turns of the coil, A_e is the effective cross sectional area of the magnetic core, I_{m_pp} is the peak-to-peak magnetizing current, and i_1 and i_2 are explained in Table 2.

When the switching frequency decreases, $i_1(t_{05})$ and $i_2(t_{05})$ increase. Since $i_2(t_{05})$ is proportional to $i_1(t_{05})$ and far less than it, $[i_1(t_{05}) - i_2(t_{05})]$ increases. Additionally, $\beta > \alpha$ [32], so p_{core} will increase. However, increasing N or A_e can reduce p_{core}, but they are constrained by the transformer conduction loss and volume.

Therefore, factors including the switching frequency, the type of the switching device, and the balancing power level, efficiency and the volume of the equalizer need to be fully considered in the design.

2.5. Equalizer Efficiency and Loss Analysis of DP2P Mode

In this mode, the average power of equalizer can be deduced according (7) and (8):

$$\begin{cases} P_{in} = V_{BP1} \cdot (CP1 + CP2) \cdot (V_{Cu} - V_{Cd}) \\ \quad = V_{BP1} \cdot (CP1 + CP2) \cdot \frac{(1+\alpha) \cdot [(1-\alpha) \cdot V_{BP1} + \alpha \cdot V_{BP3}]}{1 - \alpha + \alpha^2} \\ P_{out} = V_{BP3} \cdot (CP1 + CP2) \cdot (V_{Cu} - V_{Qr}) \\ \quad = V_{BP1} \cdot (CP1 + CP2) \cdot \frac{(1+\alpha) \cdot [V_{BP1} - (1-\alpha) \cdot V_{BP3}]}{1 - \alpha + \alpha^2} \end{cases} \tag{17}$$

Therefore, the equalizer efficiency is as follows:

$$\eta_{DP2P} = \frac{P_{out}}{P_{in}} = \frac{V_{BP3}}{V_{BP1}} \cdot \frac{V_{BP1} - (1-\alpha) \cdot V_{BP3}}{(1-\alpha) \cdot V_{BP1} + \alpha \cdot V_{BP3}} \tag{18}$$

From (8) and (18), it can be found that η_{DP2P} is affected by R_s and $LP1/(CP1 + CP2)$. Low R_s and high $LP1/(CP1 + CP2)$ can effectively improve η_{DP2P}.

On the other hand, the power loss of this mode mainly comes from the circuit conduction loss, the switching loss of MOSFET and power diode.

The circuit conduction loss p_{cond} is:

$$\begin{aligned} p_{cond} = \frac{1}{T_1} \Big[\int_0^{t_{11}} \Big(i_{LC} \cdot \sum_{i=7,11,12} V_{F\_Di} + i_{LC}^2 \cdot R_{eq1\_4} \Big) dt \\ + \int_{t_{11}}^{t_{12}} \Big(i_{LC} \cdot \sum_{i=2,5,9,10} V_{F\_D_i} + i_{LC}^2 \cdot R_{eq1\_5} \Big) dt + \int_{t_{12}}^{T_1} \Big(i_{LC} \cdot V_{F\_D13} + i_{LC}^2 \cdot R_{eq1\_6} \Big) dt \Big] \end{aligned} \tag{19}$$

Additionally, the switching loss p_{sw} is:

$$p_{sw} = \sum_{i=2,5,7,8,9,10,12} p_{sw\_Qi} + \sum_{i=2,5,7,9,10,11,12,13} p_{sw\_Di} \quad (20)$$

The calculation formula of p_{sw_Qi} and p_{sw_Di} is the same as (15).

3. The Bimodal Hybrid Control Strategy

A bimodal hybrid strategy as shown in Figure 6 is used to control the proposed equalizer for four 20-series $LiFePO_4$ battery packs. The voltage difference ΔV_{BPi} between a single pack's voltage and the pack group's average voltage is used as the switching condition between P2PG&AP mode and DP2P mode. If there is a pack that $\Delta V_{BPi} \geq 0.5\ V$, the P2PG&AP mode is selected. Otherwise, DP2P mode is selected. This switching condition helps to prevent the repeated equalization caused by the faster voltage drop of the donor pack in P2PG&AP mode, and achieve a tradeoff between balancing efficiency and speed. Until each $|\Delta V_{BPi}| \leq 0.1\ V$ in 5 consecutive voltage detection, the equalization is suspended. P2PG&AP mode selects the pack with the highest voltage as the donor pack for P2PG equalization, and the pack with the lowest voltage as the acceptor pack for LC2AP equalization after each voltage detection. DP2P mode selects the pack with the highest voltage as the donor pack, and the pack with the lowest voltage as the acceptor pack. A single equalization lasts for 10 s, and the equalization mode and path are updated after that.

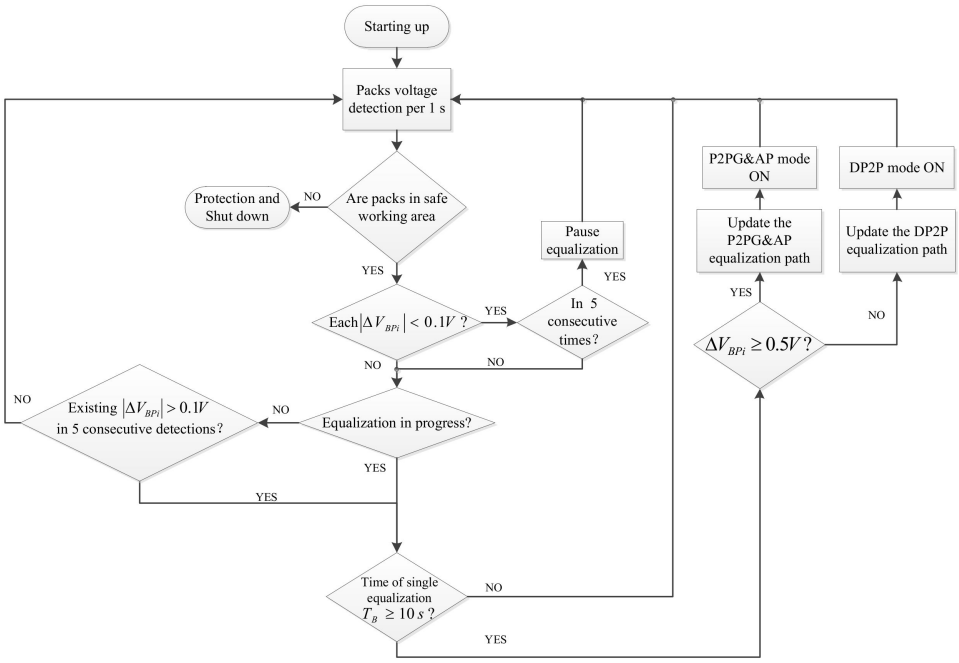

Figure 6. The bimodal hybrid control strategy of proposed pack equalizer.

4. Experiment Results

An experimental prototype was built for 4 series 66 V $LiFePO_4$ battery packs with 1100 mAh capacity, as shown in Figure 7. The peak value of equalization current was limited to 6C to minimize the impact on battery life. In order to reduce the volume and the leakage inductance of the transformer as much as possible, a planar PCB-transformer was used, and the magnetic core was EEW43.2B (Mn-Zn ferrite) of DMEGC Magnetics Co., Ltd. (Zhejiang, China). In order to cooperate with the SBC to smoothly output balancing energy to the battery pack group during the forward conduction period of the P2PG&AP mode, the transformer turns ratio was 1/4. Table 5 lists the component parameters of prototype, and it can be seen from Table 5 that the sum of the selected diodes' maximum forward

voltage drop was very small compared with the battery pack terminal voltage. Table 6 lists the relevant parameters of the transformer. It can be seen from Table 6 that SBC can reduce at least 20 turns of secondary coil while keeping the primary inductance unchanged.

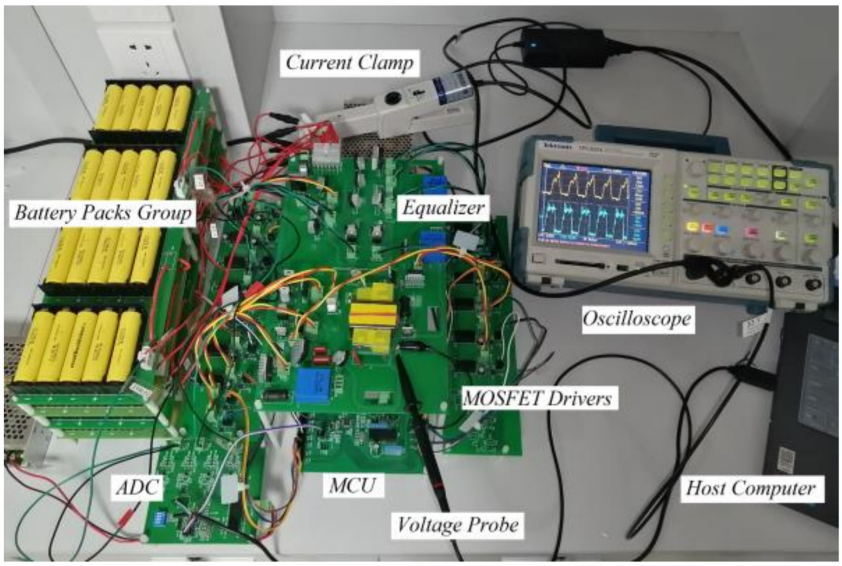

Figure 7. Photograph of the experimental prototype.

Table 5. Component parameters of prototype.

Component	Product
Q1,Q8,Q14	STW32NM50N,$R_{ds} \leq 130$ mΩ,$C_{oss} = 325\ pF$
Q2-Q7,Q12	SIHP25N40D-GE3, $R_{ds} \leq 170$ mΩ, $C_{oss} = 177\ pF$
Q9,Q10	PTW40N50, $R_{ds} \leq 85$ mΩ, $C_{oss} = 700\ pF$
Q11,Q13	IRFP4768PBF, $R_{ds} \leq 17.5$ mΩ, $C_{oss} = 830\ pF$
D1-D10	BYV29-400, $V_F \leq 1.03$ V, $t_{rr} \leq 60\ ns$
D11,D12	MBR20H150CTG, $V_F \leq 0.68$ V(Schottky diodes)
D13	PFR20V300CTF, $V_F \leq 0.89$ V(Schottky diodes)
D14, D15,D18	B1D04065K, $V_F = 1.45$ V(SiC schottky diodes)
D16,D17	ES2GB, $V_F \leq 1.25$ V, $t_{rr} \leq 35\ ns$
CP1	Film capacitor, 3.3 nF
CP2	Film capacitor, 150 nF
LP1,LP2	Inductors, 330 μH
MOSFET optocoupler driver	TLP152

Table 6. Parameters of the transformer.

Parameter	Value
N_1	10
N_2	40
L_m	346.07 μH
$L_{\sigma 1}$	1.28 μH
$L_{\sigma 2}$	0.90 μH
R_{w1}	183.81 mΩ
R_{w2}	613.64 mΩ

TPS2024 was used as the experimental measurement oscilloscope. The current clamps KEYSIGHT 1146B were used to measure the discharge current of donor pack, the STMR current was in P2PG&AP mode, and the LC quasi-resonant current was in DP2P mode. The current Hall sensors LA 25-NP/SP11 of LEM Electronics Co., Ltd. (Beijing, China) together

with a 180 Ω measuring resistor were used to measure LC reverse charging current and the SBC output current in P2PG&AP mode.

Note: N_1 and N_2 are the primary and secondary winding turns; R_{w1} and R_{w2} are the primary and secondary winding resistances.

4.1. P2PG&AP Mode

In P2PG&AP mode experiments, V_{BP2} is set to be the donor pack, V_{BP3} is set to be the acceptor pack. In Figure 8a, the negative peak voltage of primary voltage waveform is 110 V, which indicates that can the forward transformer coil voltage is effectively clamped by the STMR together with LC series quasi-resonator. The waveform of discharge current of donor pack is similar to the simulation results in Figure 3. Additionally, at the moment the forward switch is on, its negative peak is caused by the reverse voltage of primary coil which is larger than donor pack voltage. In Figure 8b, it can be seen that in t_{05}–t_{06}, the transformer provides a small part of the remanence energy to the LC quasi-resonator, and the peak value of the approximate sinusoidal charging current is converted into 0.18 A according to Equation (21), its duration is about 2.8 µs. During t_{06}–T_0, the LC quasi-resonator charges the acceptor pack, and the peak value of the first negative half wave of the reverse charging current is converted to −0.23 A, its duration is about 4.2 µs.

$$I_{measure} = \lambda \cdot (V_{Hall} / R_{measure}) \tag{21}$$

where $\lambda = 40$ is the conversion factor of LA 25-NP / SP11, and $R_{measure} = 180\ \Omega$ is the value of measuring resistor.

This shows that the LC quasi-resonator still has a small part of the energy that is not completely released after the end of a switching cycle, because Q11 cannot completely prevent the LC quasi-resonator throughput energy in 0–t_{05}. It can be seen from Figure 9b that the peak value of the ripple from sensor is 0.4 V, and the peak value of the ripple current calculated according to (21) is 0.09 A. Compared with the average discharge current of the donor pack 1.64 A in Figure 9a, it is acceptable. The reverse charging current will rise as the capacitor voltage rises to accelerate the release of LC energy, and fall back as the capacitor voltage drops.

In Figure 8c, the output current of SBC has 4 pulses in one switching cycle: the first low pulse is generated by the positive induced voltage of the secondary side at the moment the forward switch turns on; the second and third ones are SBC output current to pack group when Q14 shut down; the fourth pulse which is very close to the third one is the current produced by LP2′s residual energy after t_{05}. The STMR current has one positive pulse and one negative pulse in one switching cycle: the positive one is just the two-transistor magnetic reset current after the forward switches turn off, its peak value is 3.92 A; the negative one is the short-term reverse recovery current of D14 and D15, its peak value is −1.92 A.

Figure 9 compares the measured total efficiency of equalizer and its three parts under different f_{sw}. In Figure 9a, it can be observed that the peak value of $\eta_{P2PG\&AP}$ is about 90.49% at 40 kHz and the corresponding output power is 54.5 W. The average $\eta_{P2PG\&AP}$ reaches its maximum at 45 kHz, and drops with the decrease of f_{sw} when $f_{sw} \leq 45$ kHz. This is because with the decrease of frequency, the core loss increases and a duty cycle larger than theory needs to be used in the actual circuit to obtain the designated balancing power. Figure 9e show that the average discharge current of donor pack increases with f_{sw} decreases when balancing power is larger than 80 W.

Thereby, this fact leads to an extra increase of conduction loss. The average $\eta_{P2PG\&AP}$ at 50 kHz is a little lower because of STMR performance and larger switching loss.

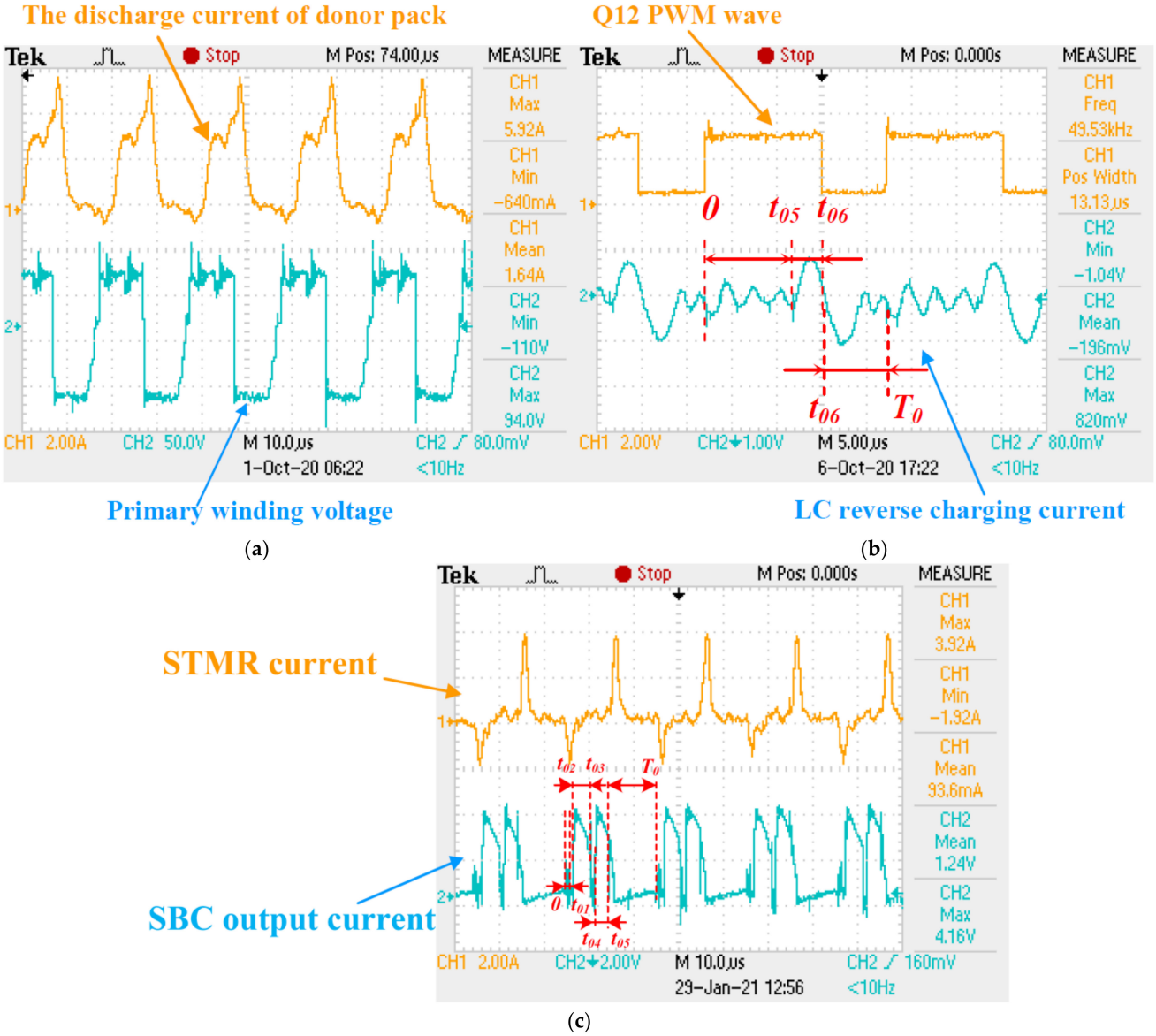

Figure 8. Experimental waveforms in 98 W, 50 kHz P2PG&AP mode when $V_{BP2} = 66.8$ V, $V_{BP3} = 65.2$ V, $\Delta V_{BPi} = 65.7$ V. (**a**) Primary current and primary winding voltage. (**b**) Q12 PWM wave and LC reverse charging current. (**c**) SBC output current and STMR current.

Figure 9b shows the trend of η_{SBC}, the average η_{SBC} decreases when f_{sw} decreases because of the core loss, and the highest average and peak η_{SBC} is both obtained at 50 kHz.

Figure 9c shows the trend of η_{STMR}, η_{STMR} increases when f_{sw} deceases because the lower f_{sw} can make the magnetic reset diodes have more time to turn off before the next cycle, and avoid the efficiency reduction caused by reverse recovery current.

Figure 9d shows the trend of η_{LC}, η_{LC} rises with f_{sw} because its energy transmission time in each switching cycle is determined by LP1 and CP1 but not f_{sw}. Additionally, with the increase of f_{sw}, the sum of transmission time per unit time becomes larger.

To summarize, it can be observed that the trends of all parts of P2PG&AP mode efficiency are consistent with the analysis above, which prove the validity of Equations (12)–(16), and the total efficiency performance at 50 kHz is better when the output power is greater than 80 W. By considering that the balancing speed is given priority in P2PG&AP mode, the design of 50 kHz 98 W with 89.66% efficiency are selected to be used in bimodal hybrid operation.

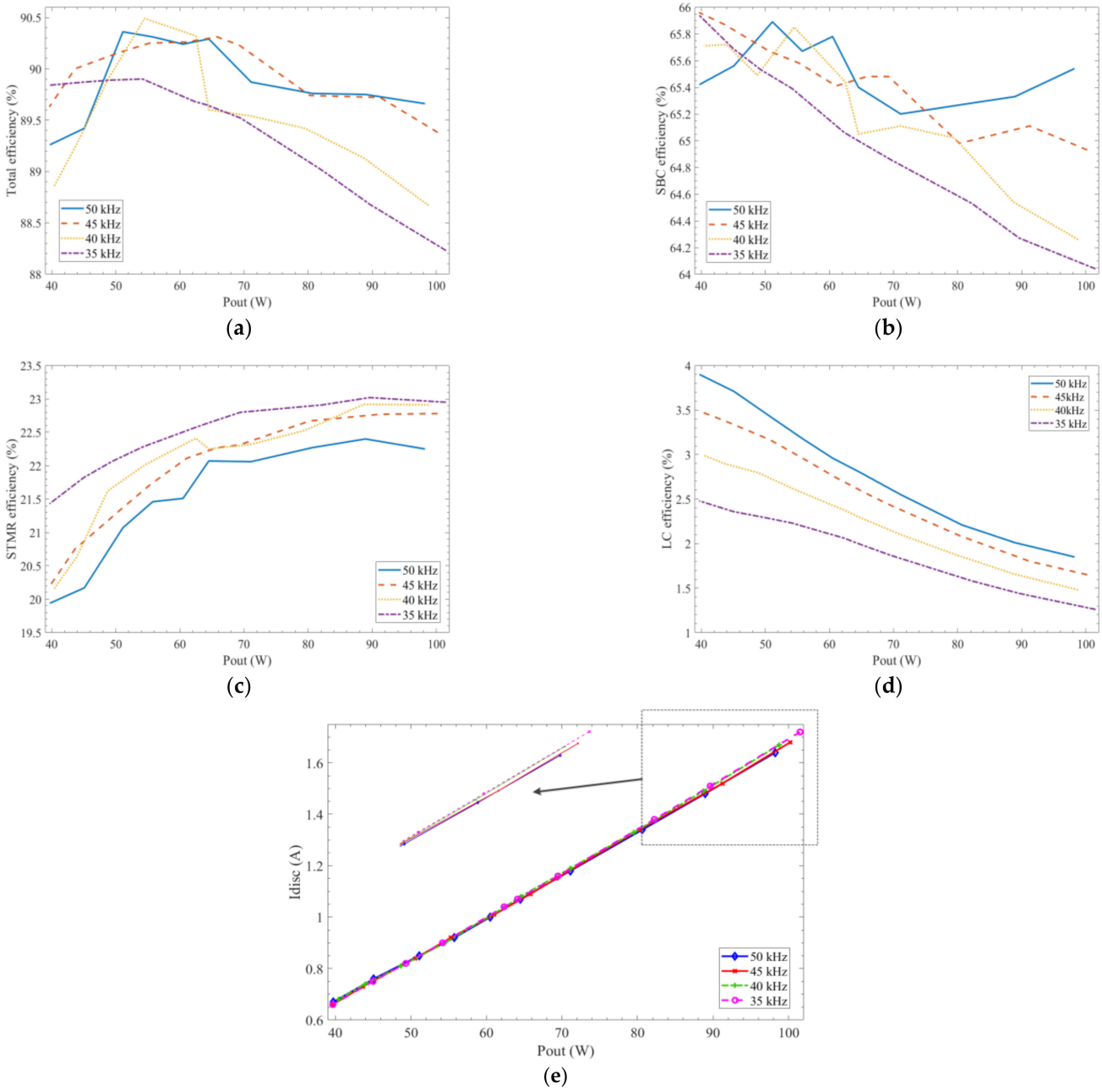

Figure 9. All parts of P2PG&AP mode efficiency and the average discharge current of donor pack at different f_{sw} with the donor pack initial voltage of 66.8 V. (**a**) The total efficiency $\eta_{P2PG\&AP}$. (**b**) The SBC part of efficiency η_{SBC}. (**c**) The STMR part of efficiency η_{STMR}. (**d**) The LC quasi-resonator part of efficiency η_{LC}. (**e**) The average discharge current of donor pack.

4.2. DP2P Mode

In DP2P mode experiments, V_{BP2} is set to be the donor pack, V_{BP3} is set to be the acceptor pack. In Figure 10, the peak value of the discharge current is 1.92 A and the duration is 22 µs. The negative peak value of the charge current is 1.84 A and the duration is 22 µs. The duration of the third resonant state is 56 µs. Since the output capacitance of Q14, the primary current waveform after Q12 turns on is affected by the secondary oscillating current, which is amplified and fed back to the primary side through the transformer. However, this does not affect the realization of equalization. As it can be found that the capacitor voltage decreases to negative value smoothly in the third resonant state.

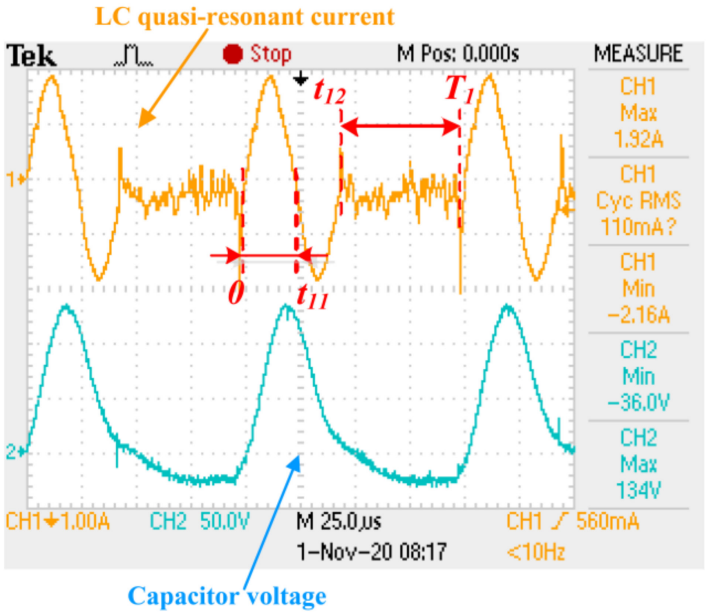

Figure 10. Experimental waveforms of LC quasi-resonant current and capacitor voltage in 13 W, 10 kHz DP2P mode when $V_{BP2} = V_{BP3} = 66.2$ V.

Figure 11 summarizes the variation trend of balancing efficiency and power with different ratio of inductor to capacitor value in 10 kHz DP2P mode, and verifies the analysis about Equation (18). Although higher efficiency can be obtained by increasing $LP1/(CP1 + CP2)$, the output power of equalizer will decrease which means reduced balancing speed. When $LP1/(CP1 + CP2)$ rises above 2000, the growth in efficiency becomes very small. In order to balance the efficiency and speed of equalizer, a reasonable value of inductor and capacitor as shown in Table 5 is selected to be used in bimodal hybrid operation, and the corresponding efficiency achieves 95.8% with 13 W balancing power.

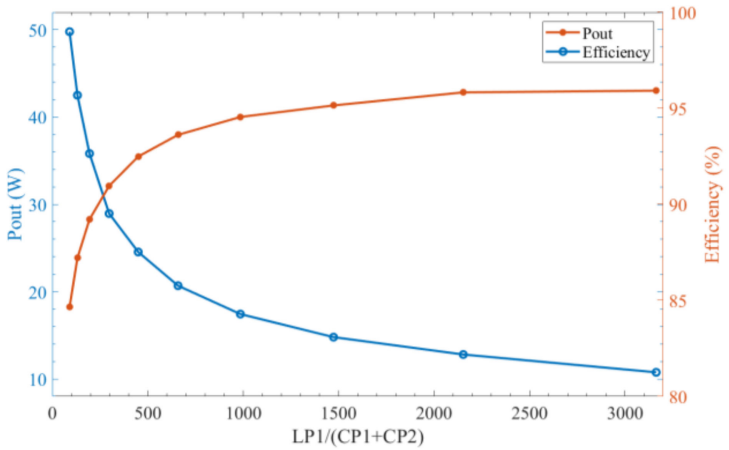

Figure 11. The efficiency and P_{out} of 10 kHz DP2P mode with different value of $LP1/(CP1 + CP2)$.

4.3. The Bimodal Hybrid Mode

The voltage evolutions in the bimodal hybrid mode are presented in Figure 12 by testing the proposed equalizer with two initial equalization states during battery pack group discharged to the load at 0.6C, as shown in Table 7. The proposed pack equalizer operates in bimodal hybrid mode with the initial pack voltage distributions of Figure 12a, and in pure DP2P mode with the initial pack voltage distributions of Figure 12b.

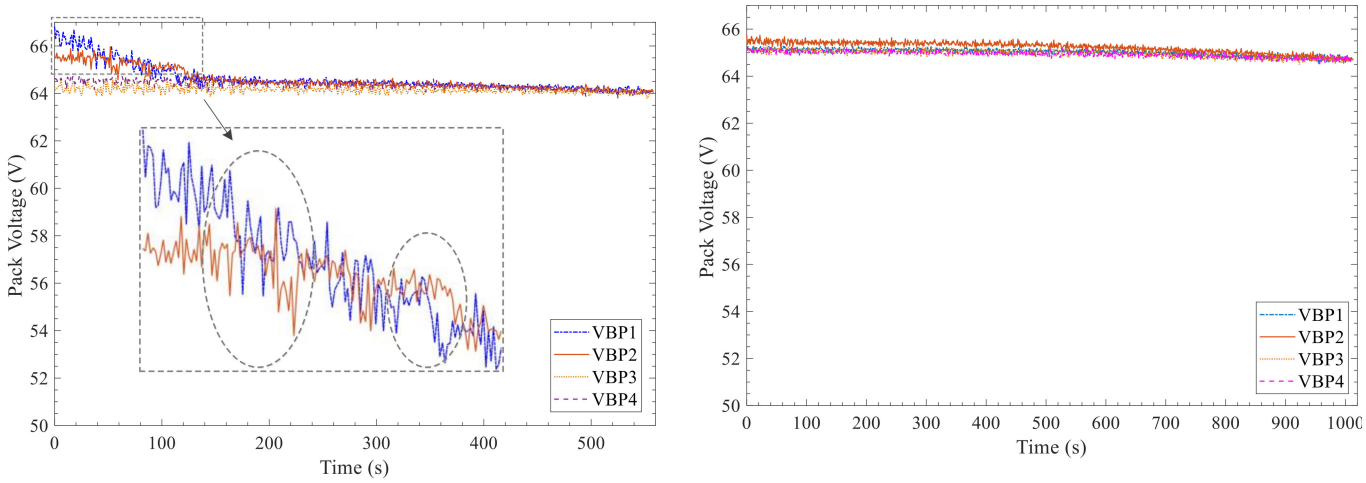

Figure 12. Comparison of the pack voltage equalization result in bimodal hybrid mode and in pure DP2P mode. (**a**) Bimodal hybrid mode. (**b**) Pure DP2P mode.

Table 7. The initial pack voltage distributions and balancing times.

Quantity	Equalization Experiments	
	Figure 12a	**Figure 12b**
V_{BP1}	66.82 V	65.19 V
V_{BP2}	65.53 V	65.76 V
V_{BP3}	64.26 V	65.12 V
V_{BP4}	64.61 V	65.09 V
ΔV_{BPi}	$\Delta V_{BP1} \geq 0.5$ V	$\Delta V_{BP1\sim4} < 0.5$ V
Balancing Time (s)	558 s	1013 s

It can be observed that all packs can be equalized simultaneously regardless of the pack voltage distributions, and this proves the robustness of the proposed equalizer to the initial imbalanced pack voltages. In Figure 12a, the equalizer worked in hybrid mode before 140 s, the donor pack voltage dropped faster in P2PG&AP mode, and then the equalizer switched to DP2P mode. The whole equalization process was completed in 558 s. In Figure 12b, the whole equalization process was completed in 1013 s. The proposed equalizer has much faster balancing speed than the conventional independent pack equalizers [28,29] with similar capacity battery objects but hour-level pack balancing time. Moreover, by comparison of Figure 12a, b, the balancing speed is found to be 45% faster in the hybrid mode than in pure DP2P mode.

5. Comparison with Conventional Pack Equalizers

Table 8 illustrates a comparison of existing battery pack equalizers in terms of power, efficiency, pack-level balancing speed and MOSFET withstand voltage. Additionally, Table 9 illustrates a comparison of these pack equalizers with their supporting cell equalizers in terms of component number, total size, and cost. It is assumed that the equalization objects include four 20-series battery packs. "AP2P" represents adjacent pack to pack topology. "PG2P" represents pack group to pack topology. "M" represents power MOSFETs, "D" represents power diodes, "W" represents the transformer windings used by equalizer, "T" represents transformers, "L" represents power inductors, and "C" represents energy storage capacitors. "SH" represents the pack equalizer sharing of the transformers with the cell equalizers in the pack. It can be seen that the proposed equalizer has clear superiority in terms of efficiency, relatively faster balancing speed, acceptable MOSFET withstand

voltage and cost. In summary, the proposed equalizer is a more suitable solution for the applications of long series battery packs.

Table 8. Comparison of the pack equalizers in terms of pack level balancing performance.

Equalizers		Power	Efficiency	Speed	MOSFET Withstand Voltage
Cooperative	Integrated equalizer based on multiwinding transformers [25]	<2.8 W (Small)	AP2P $\leq$ 91.3%	Hour level (Slow)	No MOSFET used in pack equalization
	Buck and forward converter equalizer [26]	<40 W (Medium)	PG2P $\leq$ 83.84%	Second level (Fast)	$8 \cdot \overline{V_{BP}}$
Independent	Switch capacitor direct pack equalizer [28]	No specific data	AP2P No specific data	Hour level (Extremely Slow)	$4 \cdot \overline{V_{BP}}$
	Inductor adjacent pack equalizer [29]	<0.2 W (Small)	AP2P No specific data	Hour level (Medium)	V_{BP_MAX}
	Proposed pack equalizer	$\leq$98 W (Large)	Bimodal $\geq$ 89.66%	Minute level (Fast)	$4 \cdot \overline{V_{BP}}$

Table 9. Comparison of the pack equalizers with their supporting cell equalizers in terms of component number, total size and cost.

Equalizers		Component Number											Total Size	Total Cost
		Pack Level						Cell Level						
		M	D	W	T	L	C	M	D	W	T	L		
Cooperative	Integrated equalizer based on multiwinding transformers [25]	0	0	6	SH	0	0	80	0	80	4	0	Large	High
	Buck and forward converter equalizer [26]	1	1	0	SH	1	1	4	80	84	4	0	Large	Low
Independent	Switch capacitor direct pack equalizer [28]	12	0	0	0	0	3	4	80	84	4	0	Large	Medium
	Inductor adjacent pack equalizer [29]	6	0	0	0	3	0	152	0	0	0	76	Small	High
	Proposed pack equalizer	14	18	2	1	2	2	16 five-series chip level cell equalizers					Small	Medium

6. Conclusions

This paper proposed a battery pack equalizer based on quasi-resonant, two-transistor forward converter with two equalization modes which can be freely selected according to the state of battery packs, so as to improve the balancing speed and reliability of equalizer. An experimental prototype for four 20-series battery packs was built. The theoretical analysis of the equalizer efficiency was derived and verified by experiments at different frequencies. A bimodal hybrid control strategy was designed and tested in different initial pack voltage distributions to prevent pack-level over-discharge. The simulation and experimental results indicated that the proposed equalizer topology has the following superiorities:

(1) The equalizer's P2PG&AP mode can realize FSC equalization, as shown in Figures 3 and 8. Additionally, ZVG equalization can be achieved in DP2P mode, as shown in Figures 5 and 10.

(2) An inter-pack equalization with minute level balancing time and more than 89.66% efficiency can be achieved through the bimodal hybrid control strategy, which can also effectively prevent the repeated equalization.
(3) The equalizer is robust to different switching frequencies and different initial pack voltage distributions.
(4) The proposed pack equalizer, which can cooperate with passive equalizer chips, provides a solution to simplify the structure of numerous cell equalizers in a long series battery group. This two-stage equalization scheme—which can be applied to electric vehicles, clean energy storage equipment and other fields—reduces the total number of power switches (including MOSFETs and power diodes) by at least 60%, and the total numbers of transformers and transformer coils by at least 75% and 97.5% respectively, as shown in Table 9.

Author Contributions: Conceptualization, Q.W. and M.G.; methodology, Q.W.; software, Q.W.; validation, Q.W., M.G., and H.L.; formal analysis, Q.W.; investigation, Q.W.; resources, Z.D.; data curation, Q.W.; writing—original draft preparation, Q.W.; writing—review and editing, Q.W.; visualization, Q.W.; supervision, M.G.; project administration, M.G.; funding acquisition, M.G. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the General Project of National Natural Science Foundation of China, grant number 61671194.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Informed consent was obtained from all subjects involved in the study.

Data Availability Statement: The data presented in this study are available on request from the corresponding author. The data are not publicly available due to the data use agreement.

Conflicts of Interest: The authors declare no conflict of interest.

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