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An Interleaved Phase-Shift Full-Bridge Converter with Dynamic Dead Time Control for Server Power Applications

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Abstract: A compact and high-efficiency power converter is the main business of today's power industry for server power applications. To achieve high efficiency with a low-output ripple, an interleaved phase-shift full-bridge (PSFB) converter is designed, built, and tested for server power applications in this study. In this paper, dynamic dead time control is proposed to reduce the switching loss in the light load condition. The proposed technique reduces the turn-off switching loss and allows a wide range of zero-voltage switching. Moreover, the current ripple of the output inductor can be reduced with the interleaved operation. To verify the theoretical analysis, the proposed PSFB converter is simulated, and a 3 kW prototype is constructed. The experimental results confirm that the conversion efficiency is as high as 97.2% at the rated power of 3 kW and 92.95% at the light load of 300 W. The experimental transient waveforms demonstrated that the voltage spike or drop is less than 2 V in the fast-fluctuating load conditions from 0% load to 60% load and 40% load to 100% load.

Keywords: phase-shift full-bridge converter; dynamic dead time; interleaving operation

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1. Introduction

The demand for information storage, calculation, and transmission is increasing day by day. With the rapid development of Industry 4.0 and the proliferation of data centers, we have entered an age where anyone can attempt to compose their own literary works on the Internet. Figure 1 shows the most important topics of development technology in recent years [1–3].

Figure 1. Major topics of development technology in recent years.

Running large data centers is crucial for providing services continuously and uninterruptedly. The demand for high-power power supplies continues to increase data

center cloud, industrial, and communication applications, necessitating power supplies above the kW level. Server power supplies are designed to provide a reliable and efficient front-end power source for enterprise servers, storage appliances, network computers, and other computing devices. For the server power supply unit, the most critical issue is high efficiency. Therefore, a bridge converter architecture, which has high conversion efficiency and power density, is suitable for high-power applications [4–8].

A phase-shift full-bridge (PSFB) converter is one solution to achieve zero-voltage switching (ZVS) by controlling a different phase-shift angle between the bridges [9,10]. However, under extremely light loads, the lead switch may miss the ZVS condition [11–18]. The traditional PSFB converter has some circuit defects, such as the inability of the rear arm to achieve zero voltage, circulating current loss, secondary-side conduction loss, and secondary-side ringing. In general, an additional inductor with two clamping diodes can be used to achieve the ZVS of the hysteresis switch and suppress the overshoot of the secondary rectifier. However, series inductance leads to greater loss and ringing. Another method is to extend the ZVS range by increasing the transformer inductance. The energy stored in the LC network can extend the ZVS range, but this increases the conduction losses in the primary side [18–20]. In other words, ZVS is still difficult to achieve with the hysteresis switch when the magnetic current is reduced [21]. In addition, the ZVS switching hysteresis can also be achieved using auxiliary circuits [22–25]. Under heavy loads, the ZVS condition is mainly determined by the energy stored in the leakage inductance; the auxiliary inductor does not produce a large current, and the conduction loss can be reduced. Under light loads, the current of the auxiliary inductor is used to achieve ZVS. On the contrary, the hysteresis switch ZVS condition is not limited by the transformer leakage inductance, and the leakage inductance can be minimized. If different control methods are used in accordance with the load condition, the converter can reduce the circulating current and switching losses under light load conditions, but there are still problems of conduction loss under heavy load conditions, which increases the complexity of the control circuitry [26–31].

In many applications, to reduce the current ripple and current stress, interleaved topology has been applied to achieve high power density and a low-profile package of server power applications [32,33]. By distributing the power losses and current stresses of the switch and transformer in the individual power module, the overall conversion efficiency can be improved. Moreover, the interleaved operation can reduce the current ripple or the size of the input and output filters. The appearance of the PSFB converter solves the problem of high current ringing, which occurs with conventional full-power converters. In this study, an interleaved PSFB converter with dynamic dead time control is designed, constructed, and tested for server power applications; the dynamic dead time control can reduce the switching loss in light load conditions. The technique proposed in this paper allows for the reduction of turn-off switching loss, the achievement of wide-range ZVS, and a reduction in the current ripple of the output inductor. The developed circuit configuration can be extended to any number of interleaving legs for the requirement of the power rating or current ripple. A detailed analysis of the proposed PSFB converter is presented in Section 2. Section 3 describes the design of dynamic dead time control. Section 4 presents the computer simulation and preliminary experiments that verified the performance of the proposed PSFB converter. Section 5 presents the study conclusions.

2. System Description

The switching control method of the PSFB is an extension of the traditional switching control method of the full-bridge converter. The circuit diagram of the proposed interleaved PSFB converter is shown in Figure 2. Phase 1 PSFB consists of four metal–oxide–semiconductor field-effect transistors (MOSFETs) Q_1–Q_4, Transformer T_1, a series inductor L_{k1}, a secondary rectifier with four diodes D_1–D_4, and an output choke L_o. Phase 2 PSFB consists of four MOSFETs Q_5–Q_8, Transformer T_2, a series inductor L_{k2}, and a secondary rectifier with four diodes D_5–D_8. The operation of the proposed PSFB, which is

a combination of two phases, can be generally divided into different operation modes. The key waveforms of the proposed converter are shown in Figure 3, and the assumptions on which they are based are presented as follows.

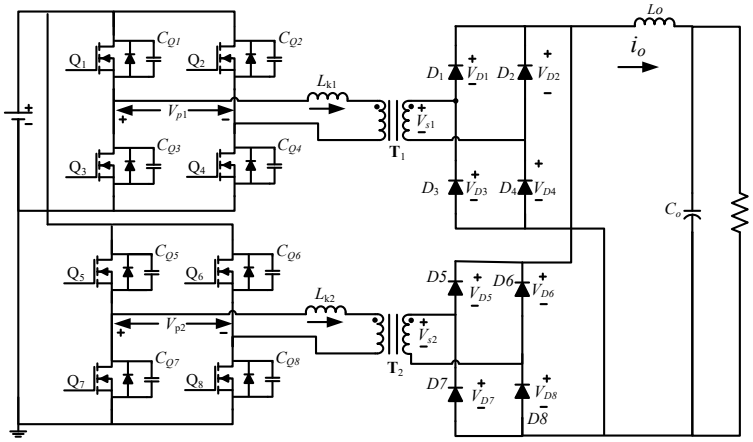


Figure 2. Circuit diagram of the proposed phase-shift full-bridge (PSFB) converter.

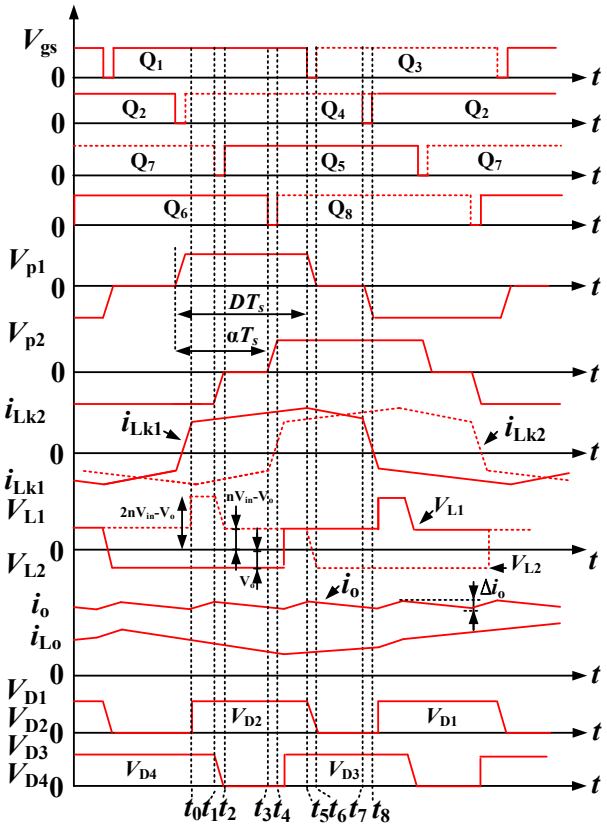
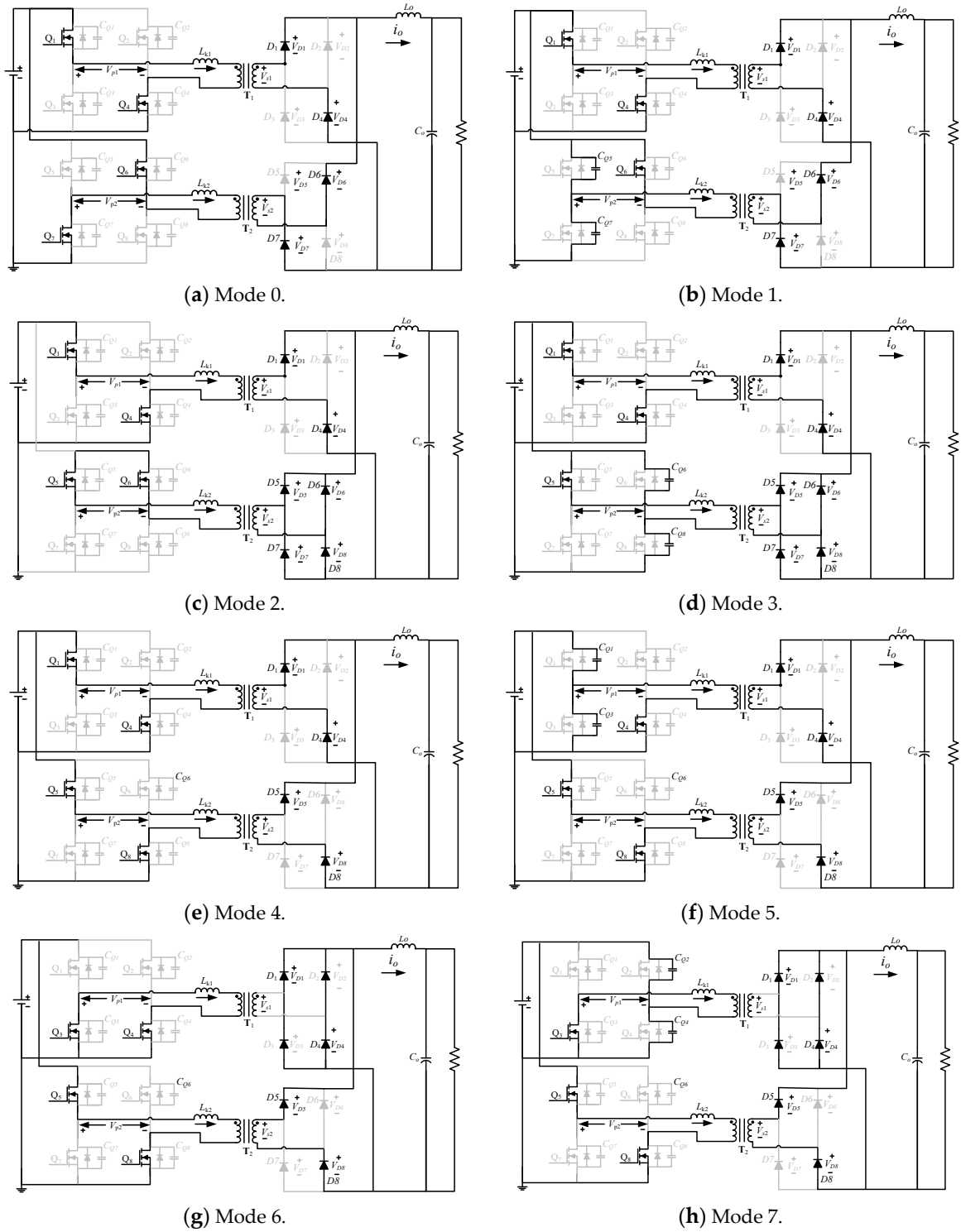


Figure 3. Key waveforms of the proposed PSFB converter.

(1) The magnetizing inductance L_m and the output inductors L_o are large enough to be considered as a constant current source during the dead time of the primary switches.
(2) Resonances by parasitic components are ignored, except for Phase 1 resonance between L_{k1} and the parasitic capacitor of Q_1–Q_4 and Phase 2 resonance L_{k2} and the parasitic capacitor of Q_5–Q_8.
(3) The turns ratio of the coupled inductor is 1:1, and it has a high coupled coefficient.

The control method is pulse-width modulation with phase-shift, which has broader controllability and an easier design compared to the control method of frequency modulation. Therefore, the operating modes are symmetrical, and a half cycle is described in this paper. The half cycle can be divided into eight modes. The equivalent circuit is shown in Figure 4. The second half of the switching cycle is symmetrical with the above description.



(**a**) Mode 0. (**b**) Mode 1.

(**c**) Mode 2. (**d**) Mode 3.

(**e**) Mode 4. (**f**) Mode 5.

(**g**) Mode 6. (**h**) Mode 7.

Figure 4. Operation modes of the proposed PSFB.

Mode 0 (t_0–t_1): In this mode, Q_1, Q_4, Q_6, and Q_7 are turned on. Energy is transferred to the secondary diodes through the transformer T_1. The secondary diodes D_1 and D_4

conduct. In this interval, i_{Lo} increases at the slope of $(nV_{in}-V_o)/L_o$. When Q_7 turns off at t_1, this mode ends.

Mode 1 (t_1–t_2): Q_7 ends at t_1, and the circulating current charges C_{Q7} and discharges C_{Q5}. The i_{Lk2} current can be regarded as a constant current source in this interval. When the Q_5 drain-to-source voltage reaches zero at t_5, this mode ends.

Mode 2 (t_2–t_3): During this time interval, current commutation is completed at t_2. The secondary diodes D_6 and D_7 conduct. When Q_6 turns off at t_3, this mode ends.

Mode 3 (t_3–t_4): Q_6 ends at t_3, and the circulating current charges C_{Q6} and discharges C_{Q8}. The i_{Lk2} current can be regarded as a constant current source in this interval. When the Q_8 drain-to-source voltage reaches zero at t_4, this mode ends.

Mode 4 (t_4–t_5): In this interval, the Q_8 drain-to-source voltage reaches zero, contributed by the i_{Lk2} current. Q_8 is turned on, and the secondary diodes D_5 and D_8 conduct. When Q_1 turns off at t_5, this mode ends.

Modes 5–7 (t_5–t_8): This interval is similar to (t_1–t_4) due to the circuit symmetry. The master phase circulates on the primary side, and the other phase transfers energy to the load.

In the proposed PSFB, the dual-loop control scheme is employed, and the control circuit is implemented using error amplifiers. It can provide the required phase margin and low-frequency gain to achieve stability with higher bandwidth. Figure 5 illustrates that a voltage divider, a current detection resistor R_{shunt}, amplifiers, and compensated network consist of a feedback controller. The output of the voltage loop error amplifier provides the current reference for the current loop error amplifier, which is used to realize the current control and current sharing of the two phases and generate the PWM signal with the phase-shift angles between the bridge legs.

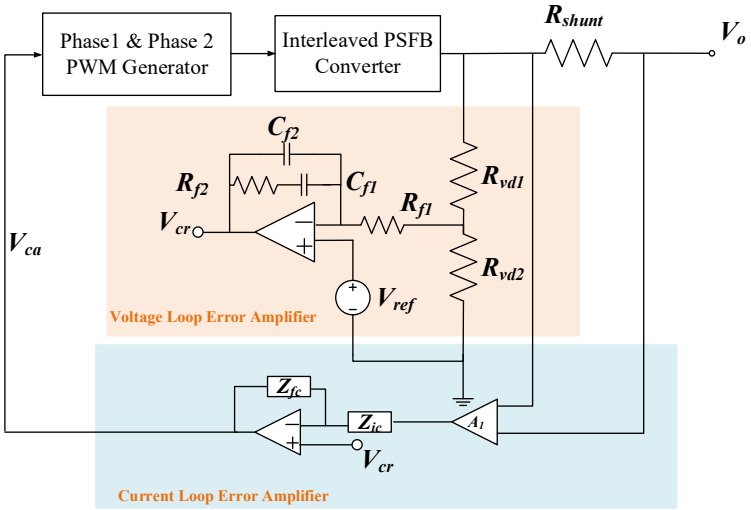


Figure 5. Dual-loop controller of the proposed PSFB.

3. Dynamic Dead Time Control

In this paper, dynamic dead time control is proposed for different output loads. In general, it is always desirable to provide an optimally minimized dead time without running into shoot-through conditions. However, achieving ZVS at light loads with a minimized dead time is challenging. Under no-load and light load conditions, ZVS may be lost if the inductive energy available in the circuit is insufficient to charge and discharge the output capacitance of the two MOSFETs in the same bridge leg. Therefore, for no/light load, a longer dead time is usually preferred, but the longer dead time leads to longer body diode conduction and a consequent loss of efficiency. Moreover, the expense of dead time will result in lower conversion efficiency, and the ZVS advantages cannot be the perfect present under heavy loads. Figure 6 shows the transformer waveform with a fixed dead time. It can be found that a voltage drop occurs with a longer fixed dead time.

Even though ZVS may be achieved under the light load condition, the overall conversion efficiency could be lower. Figure 7 illustrates the transformer waveform with dynamic dead time control.

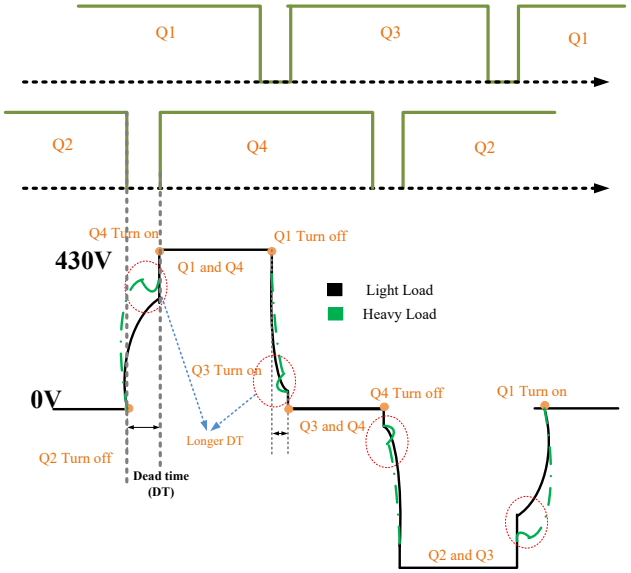


Figure 6. Theoretical transformer waveform with a fixed dead time.

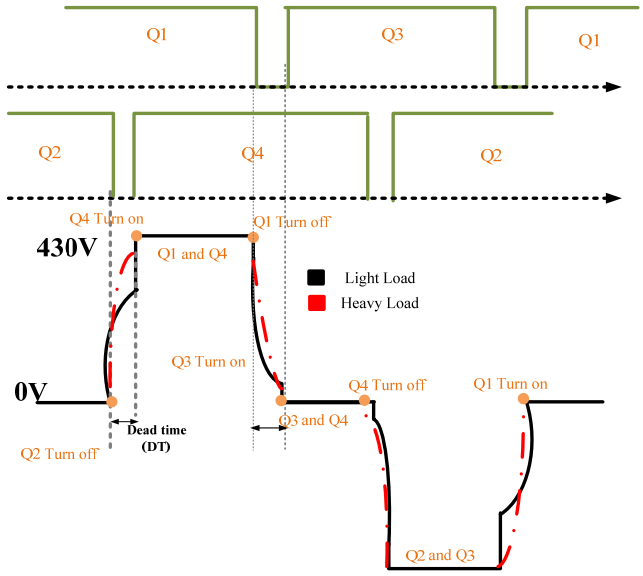


Figure 7. Theoretical transformer waveform with dynamic dead time control.

The controller can be optimized during the dead time between the low-side and high-side MOSFET depending on the load condition. ZVS can be achieved under heavy load conditions, and the switching loss can be reduced under light load conditions. Consequently, the output current can also be sensed from a current transformer, which is used for estimating the load conditions. Next, the optimal dead time can be determined.

Designing better dead time requires a detailed understanding of the transition process with different intervals. In practice, the transitions from a high level to a low level and a low level to a high level are not symmetrical. Additionally, the propagation delay through the driver stage may be added with IC-based gate drivers. To illustrate this analysis, the basic gate discharge waveform is used with a soft-switching full-bridge circuit. Figure 8 displays

three distinct stages for gate discharge. Therefore, the minimum dead time requirement can be obtained as follows:

$$T_{DT} \geq T_{GSF} + T_{GPT} + T_{LSH} + T_{DSD} \tag{1}$$

where T_{GSF} is the fall time in the first interval, T_{GPT} is the sum of the voltage fall time and the current rise time during the period closed according to driving conditions, T_{LSH} is the fall time in the last interval, and T_{DSD} is the requirement of the output capacitor discharge time. The first and last time intervals in the basic gate discharge waveform can be approximated as follows:

$$T_{GSF} = C_{GS} \times \frac{V_{GS} - V_G}{I_{Goff}} \tag{2}$$

$$T_{LSH} = C_{GS} \times \frac{V_{TH}}{I_{Goff}} \tag{3}$$

where C_{GS} is the equivalent gate-to-source capacitance, V_{GS} is the high level of the gate voltage, V_G is the Miller voltage, V_{TH} is the threshold voltage of a MOSFET, and I_{Goff} is the sink current of the driver. T_{GPT} can be approximated:

$$T_{GPT} = R_{Goff} \times \frac{Q_{sw}}{V_G} \tag{4}$$

where R_{Goff} is the equivalent turn-off resistance, and Q_{SW} is the total switching charge. The output capacitor discharge time is required for a quarter of the resonant period of the equivalent PCB trace inductance and output capacitor. T_{DSD} can be derived as follows:

$$T_{DSD} = \frac{\pi}{2} \times \sqrt{\frac{L_{PCB} \times Q_{oss}}{V_{in}}} \tag{5}$$

where L_{PCB} is the equivalent PCB trace inductance, and Q_{OSS} is the output capacitor charge. The aforementioned approach is a simple means by which to design the dead time. However, the results may not be reliable because of the uncertain output capacitance and equivalent inductance under different load conditions. To approximate the output capacitor discharge time with the output current, (5) can be further modified as follows:

$$T_{DSD} = \frac{\pi}{2} \times \sqrt{\frac{2L_m C_{oss}}{i_{CT}}} \tag{6}$$

where L_m is the magnetizing inductance, C_{OSS} is the output capacitance of the MOSFET, n is the turn ratio, and i_{CT} is the primary peak current, which is related to the output current. In addition, the capacitance across the MOSFET could be changed with the applied voltage across the transistor. The total equivalent capacitance across the transistor could be influenced by the circuit layout. Hence, it is necessary to calibrate the calculation and determine the effective capacitance after the hardware circuit is implemented.

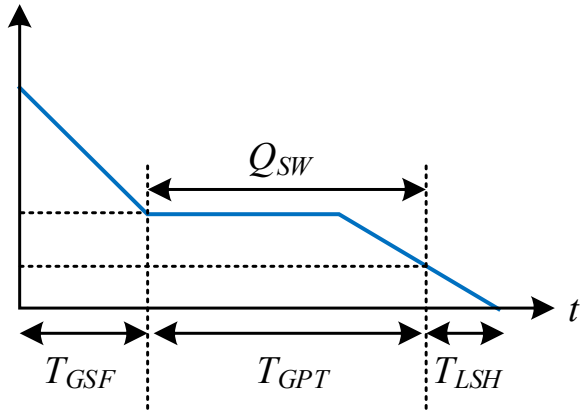


Figure 8. Gate turn-off voltage and time intervals.

In this paper, two interleaved PSFB converters are made to operate in an interleaving fashion. By shifting the duty cycles of adjacent channels at 90°, the output current ripple can be reduced. Moreover, the second converter is closed when the load condition is under 20% rated load. As the output current increases under light load conditions, the switching loss is reduced because of ZVS, thus yielding higher conversion efficiency.

4. Computer Simulations and Experimental Results

A 430 V to 240 V 3 kW interleaved PSFB converter with dynamic dead time control was designed for validation. Table 1 lists the key parameters of the proposed converter prototype. From 1 to 5, the dynamic dead time and traditional dead time can be obtained, as shown in Figure 9.

Table 1. Ratings and circuit parameters of the prototype PSFB converter.

Power rating	3 kW
Input voltage, *Vin*	390 V_{DC}−450 V_{DC}
Output voltage, *Vout*	240 V_{DC} ± 5V
Max. output current, Io_{max}	12.5 A
Min. output current, Io_{min}	0.05 A
Switching frequency, f_s	50 kHz
MOSFETs	IPP60R120C7
Secondary Rectification Diode	STPSC10H065DI
Transformer Core	PQ3230
Transformer turns radio	Np: Ns = 37:30
Magnetizing inductance, *Lm*	2.6 mH
Output inductance	392 μH
Blocking capacitor	1 μF
Diver IC	ADUM4223ARWZ-RL

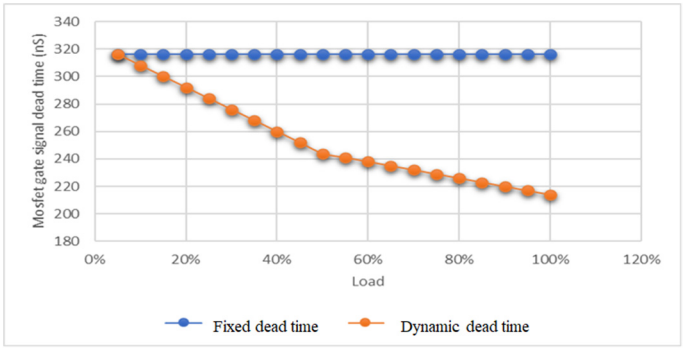


Figure 9. Fixed dead time and dynamic dead time as functions of load.

The computer simulations shown in Figure 10 are the input and output voltage waveforms of the proposed PSFB converter with dynamic dead time control. It is obvious that the output voltage ripple is reduced significantly. The voltages across the phase-shifted primary and secondary high-frequency transformers are shown in Figures 11 and 12, respectively. Another key feature of the PSFB converter is the ZVS. Figure 13 shows the simulated drain current and drain-to-source voltage waveforms of the two MOSFETs in the same bridge leg. ZVS is achieved under the rated power in the simulations.

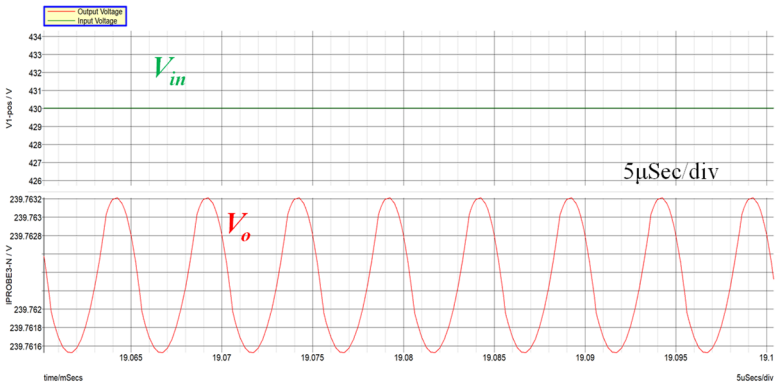


Figure 10. Simulated waveforms of the input voltage and output voltage.

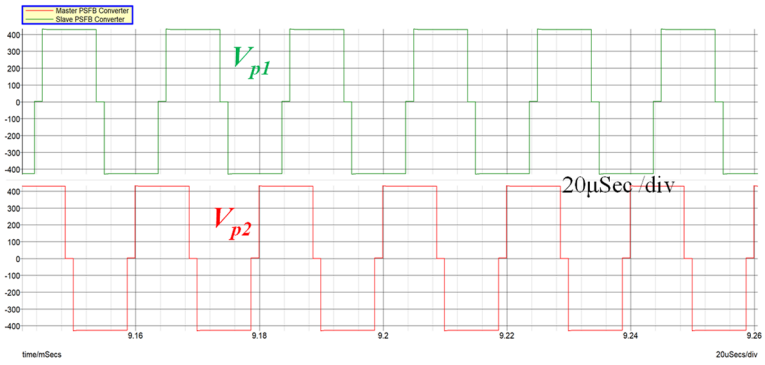


Figure 11. Simulated waveforms of the primary voltage across the transformers.

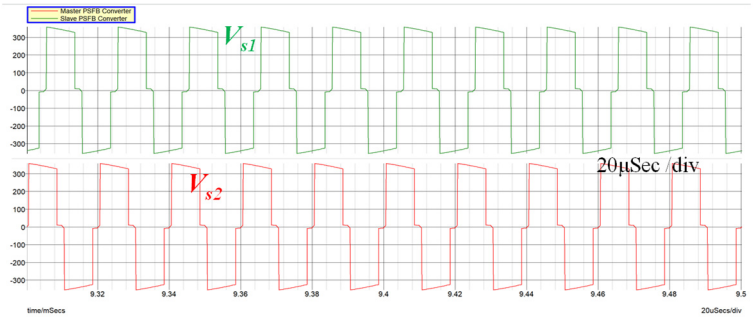


Figure 12. Simulated waveform of the secondary voltage across the transformers.

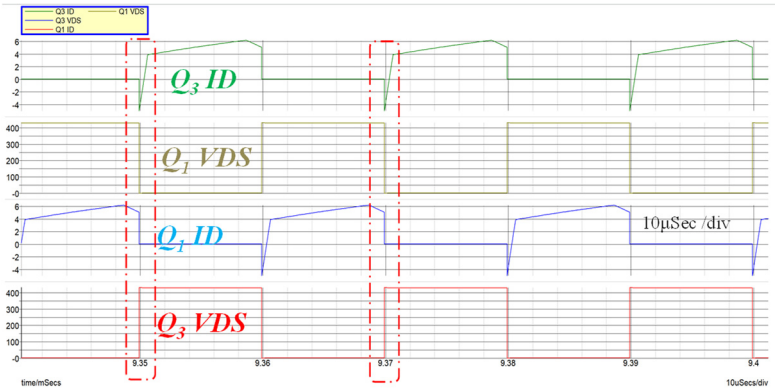


Figure 13. Simulated waveforms of the drain current and drain-to-source voltage across the MOSFETs in the same bridge leg.

The parameters in Table 1 are adopted, and a 430 V to 240 V 3 kW interleaved PSFB converter with dynamic dead time control was designed for validation. Figure 14 shows a photograph of the experimental prototype. The experimental waveforms of the proposed converter are shown in Figures 15 and 16. Figure 15 illustrates the main waveforms of the midpoint voltage of the two bridges under two operating conditions, which is consistent with the theoretical analysis. Figure 16 shows the experimental waveforms of the output voltage and output current at no load and 3-kW-rated power. The output voltage is less than 1 V. It can be found that the output inductor ripple currents can cancel each other, and the output current ripple of the output capacitor can be reduced. Therefore, a small-sized inductor is possible, thus reducing the output filter weight.

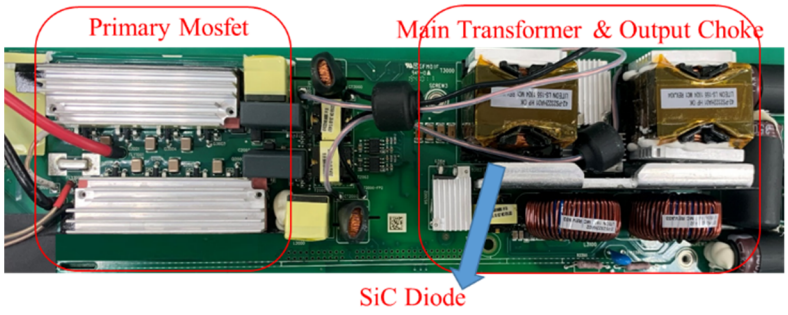
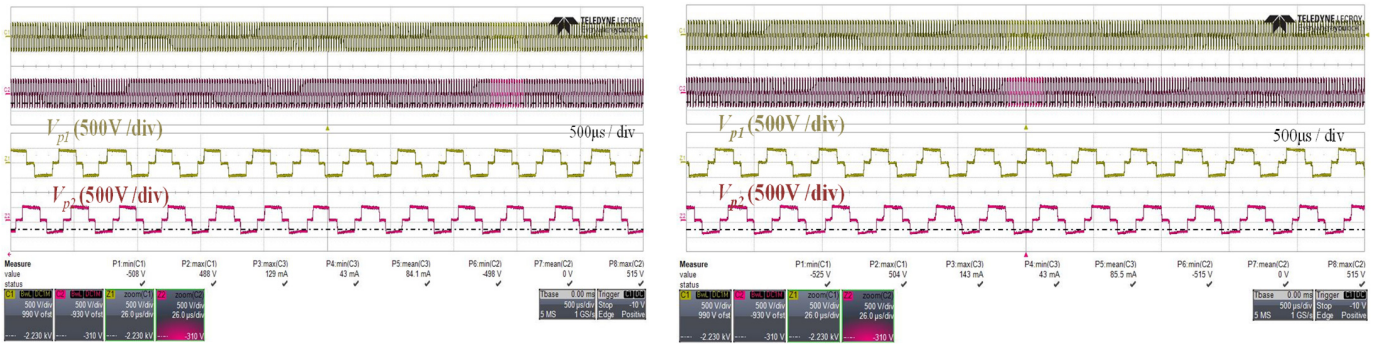
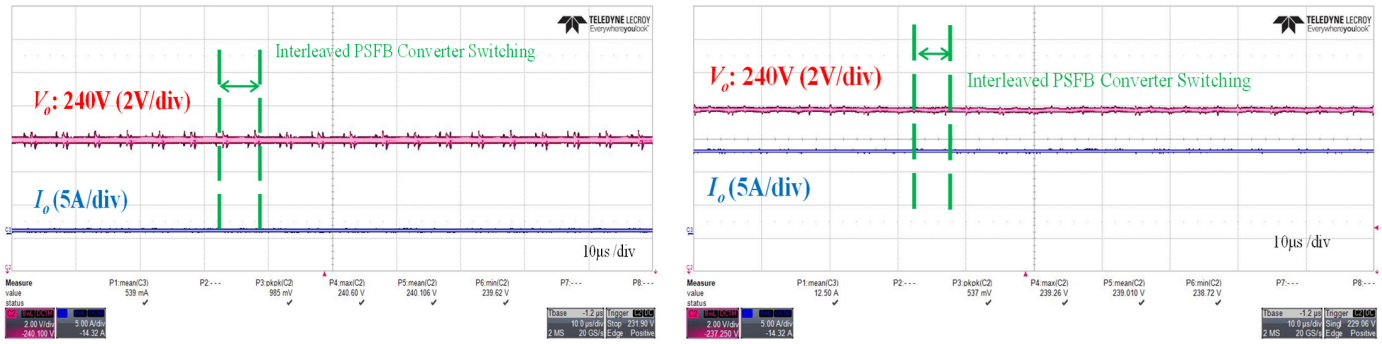


Figure 14. Prototype photograph.



(**a**) (**b**)

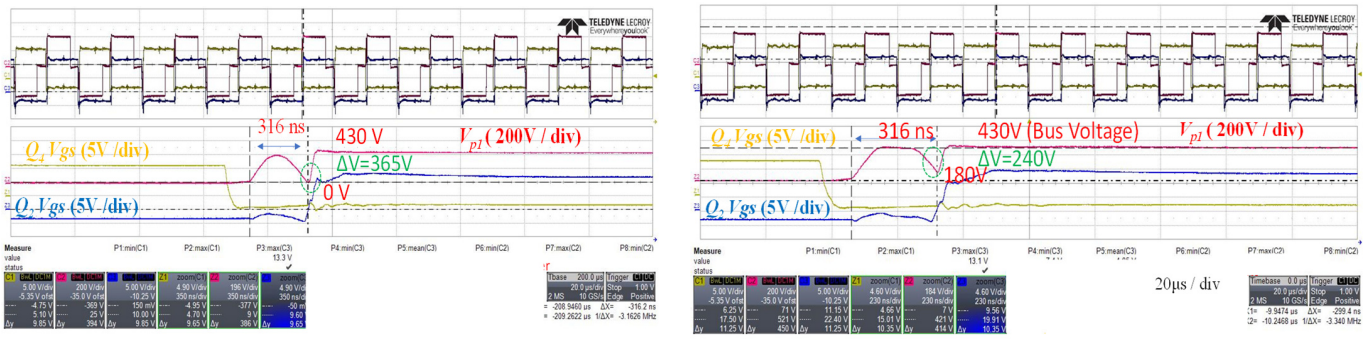
Figure 15. Experimental waveforms of the primary voltage across the transformers. (**a**) At half-rated load. (**b**) At 3-kW-rated load.



(**a**) (**b**)

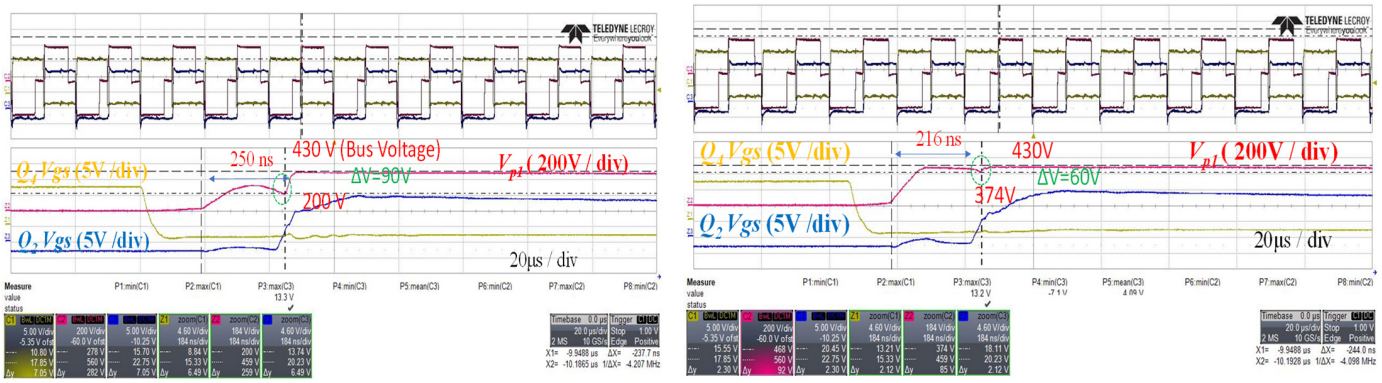
Figure 16. Experimental waveforms of the output voltage and output current. (**a**) At no load. (**b**) At 3-kW-rated load.

For server power applications, the proposed PSFB converter is designed to be optimized for the highest efficiency at 50% load and the best thermal performance at 100% load. In order to verify the dynamic dead time control design, Figures 17 and 18 are presented. Figure 17a shows the experimental waveforms with a fixed dead time at half of the rated load condition. Because the ZVS conditions of the heavy load are easier than those of light loads, we usually design a longer dead time for no light loads. Figure 17b illustrates the transformer waveforms with a fixed dead time under full load conditions. It can be observed that voltage drops of 365 V and 240 V occur at half of the rated load and full load when the Q_2 switch is turned on. Figure 18 illustrates the corresponding waveforms with dynamic dead time under different load conditions. It can be observed that voltage drops of 90 V and 60 V occur at half of the rated load and full load when the Q_2 switch is turned on. Compared with the fixed dead time control, the proposed dynamic dead time control makes an improvement of the voltage stress when the related switch is turned on. Figure 19 illustrates the experimental drain current and drain-to-source voltage waveforms of the Q_1 switch. The ZVS can be achieved under rated power in the experiments.



(**a**) (**b**)

Figure 17. Experimental transformer waveform with a fixed dead time. (**a**) At half-rated load. (**b**) At full load.



(**a**) (**b**)

Figure 18. Experimental transformer waveform with dynamic dead time. (**a**) At half-rated load. (**b**) At full load.

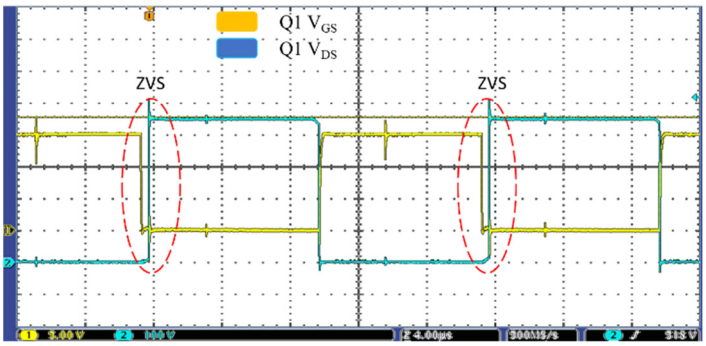


Figure 19. Zero-voltage switching (ZVS) waveforms of Q_1 at a 12.5A load.

Figure 20 illustrates the measured frequency response of the proposed PSFB converter with a voltage feedback controller in closed-loop operation. The bandwidth is observed as 2.5 kHz, and the voltage controller achieves a phase margin of 54° for stability. In practice, there is no significant difference for the stability margin between the fixed dead time control and dynamic dead time control. The prototype system may be implemented in a stable operation and equipped with low-frequency gain to improve the response speed. Figure 21a illustrates the experimental transient waveforms when the dynamic load is performed from no load to 60% load. Figure 21b illustrates the experimental transient waveforms when the dynamic load is performed from 40% load to full load. Under both conditions, the output voltage ripple is reduced significantly. The power conversion efficiency of the proposed PSFB converter under different output power is

demonstrated in Figure 22, which shows the peak efficiency of approximately 98%. In addition, the efficiency curve is compared with other PSFB converters. Reference [30] used a typical PSFB converter configuration with a modified synchronized rectifier to achieve a higher conversion efficiency. Reference [31] presented an interleaved PSFB with new coupled inductor rectifiers to reduce the primary circulating current. Compared to other works, the proposed converter has higher conversion efficiency that can achieve the 80 Plus Titanium level.

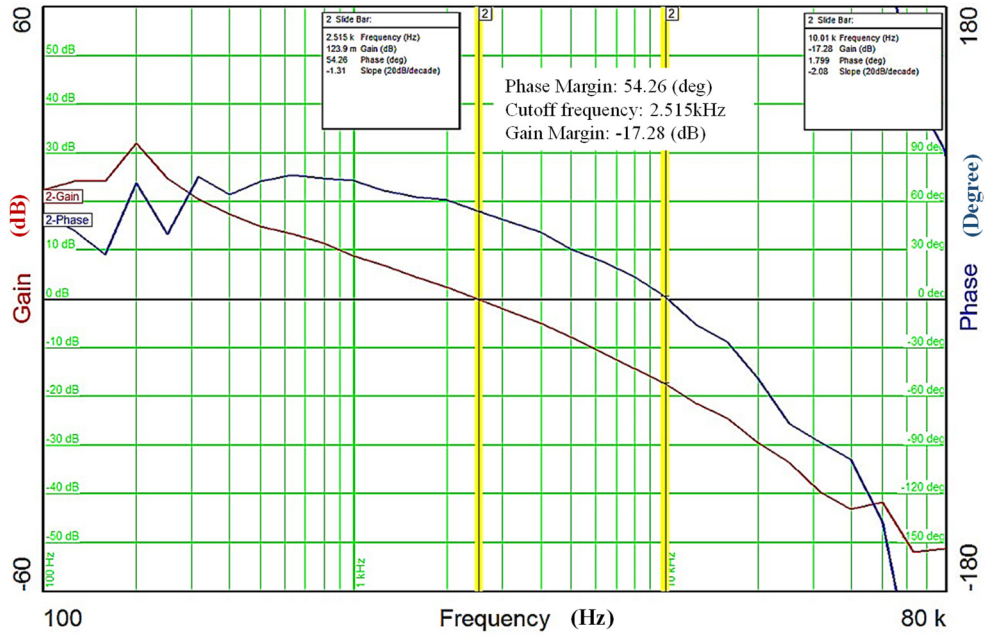
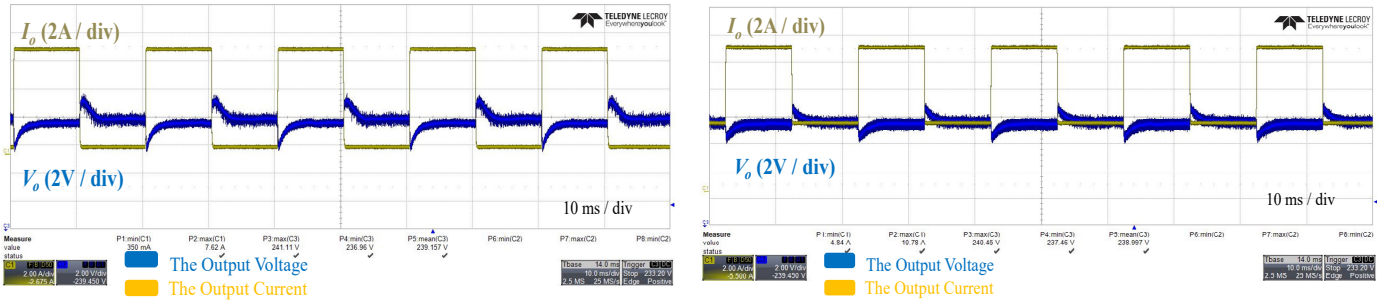


Figure 20. Frequency response of the PSFB converter.



(**a**) (**b**)

Figure 21. Experimental transient waveforms when the dynamic load is performed. (**a**) From no load to 60% load. (**b**) From 40% load to full load.

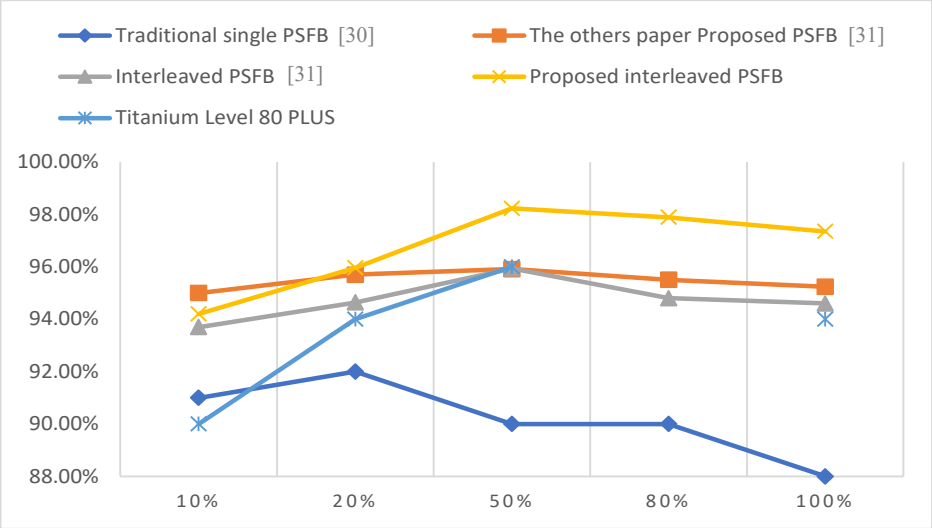


Figure 22. Measured conversion efficiency curves.

5. Conclusions

An optimized dead time for the PSFB converter is proposed in this paper. Based on the proposed dead time control, the switching characteristics and half load conditions are analyzed in detail. Further, the dead time is recommended to provide a natural burst mode operation, which results in low power consumption and excellent thermal performance under both heavy and extreme loads. All these improvements have been validated experimentally by using a 3 kW prototype. The experimental results confirmed that the conversion efficiency is as high as 97.2% at the rated power of 3 kW and 92.95% at the light load of 300 W. The experimental transient waveforms demonstrated that the voltage spike or drop is less than 2 V in the fast-fluctuating load conditions from 0% load to 60% load and 40% load to 100% load.

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