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Multiobjective Optimization Based Framework for Early Stage Design of Modular Multilevel Converter for All-Electric Ship Application

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Abstract: The Medium Voltage DC (MVDC) architecture for All Electric Ships (AES) has the potential to provide superior features compared to traditional 60-HZ AC distribution systems in terms of power density, power quality, and system stability. The MVDC system introduces extensive use of power electronics equipment into the shipboard power system (SPS) design that brings complexity to the system design. These power electronics equipment connect the power sources and load centers to the MVDC bus and play a major role in handling system faults. This paper focuses on developing a framework to determine the volume and failure rate of a Modular Multilevel Converter (MMC) for early stage ship design. Two different methodologies (Taguchi method and a genetic algorithm) were used to determine the best design from a robust set of design options. Once the design parameters have been identified, the Taguchi method forms orthogonal array to explore and evaluate designs. At the end of the design cycle, it identifies the best parameters from a large set of design parameters to achieve lower volume and failure rate. These parameters are used as input to the optimization process. This helps to narrow out the number of inputs for optimization algorithm. The Nondominated Sorting Genetic Algorithm II (NSGA-II) has been integrated with converter design tool to minimize the volume and failure rate of MMC. The results show that the optimization algorithm coupled with Taguchi Method provides the lowest volume and failure rate for MMC. One of the goals of early-stage ship design is to develop preliminary design and evaluation of trade space to narrow it down. This paper is expected to aid early-stage ship design of power electronics converter design for MVDC systems in SPS.

Keywords: AES; MMC; MVDC; NSGA-II; Taguchi design of experiments; SPS

Citation: Toshon, T.A.; Faruque, M.O. Multiobjective Optimization Based Framework for Early Stage Design of Modular Multilevel Converter for All-Electric Ship Application. *Energies* **2022**, *15*, 4418. https://doi.org/10.3390/en15124418

Academic Editor: Il-Yop Chung

Received: 26 May 2022
Accepted: 14 June 2022
Published: 17 June 2022

1. Introduction

Future AES (All-Electric Ship) designs must incorporate emerging technologies for efficient power conversion in order to enable compact ship designs with a high degree of electrification and high-energy pulsed loads. To tackle this challenge, a collaborative and concurrent design environment, called Smart Ships Systems Design (S3D), is being developed by the US Navy to provide a design space exploration across a wide range of MVDC power converter implementation [1]. The advancement towards electric propulsion and high-powered weapons make medium-voltage DC systems some of the top candidates [2]. All-electric ships are expected to require converters up to approximately 30 MW for power generation modules (PGM) and several hundreds of kW to 1 MW for power conversion modules depending on the type of loads. Integration of all these new technologies will still have to meet efficiency in volume. Hence, the requirement for a minimized volume of converters is evident. Figure 1 shows the power electronics applications for a SPS system. It can be observed from the figure that power electronics application in SPS is ubiquitous.

Several functional blocks such as Power Generation Module (PGM), Propulsion Motor Module, and Load centers use different types of power electronic converters [3].

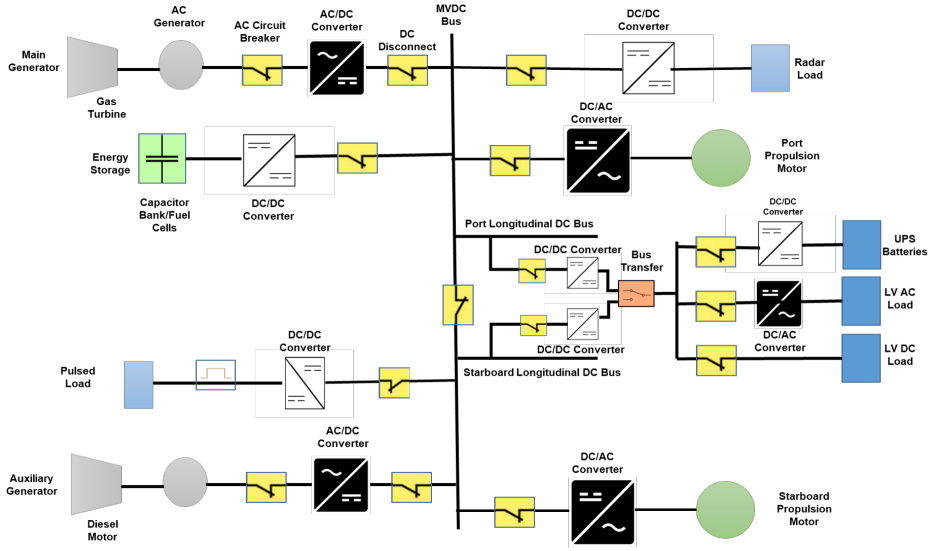

Figure 1. Simplified concept of MVDC SPS system diagram with power electronics applications [4].

The shipboard power systems require an equipment to be space efficient. Hence, it has become extremely important to evaluate the volume of power electronics in the early-stage design cycle. Figure 2 shows the trend in power density enhancement for power electronics. It can be observed that there is almost a linear increase in the power density of power electronics over the years. It is often necessary to incorporate a high power converter in a limited space inside the ship power conversion module. These systems need to be more compact than the traditional grid converter as there is little restriction regarding the space for grid applications. To address these challenges, the developed framework provides an option to restrict height, width, or length of the converter cabinet. Volume is not the only design goal for the power electronics converter, particularly targeted for application in AES. Another prime metric is failure rate. These converters are subjected to high switching frequencies for the length of the operation; hence, failure rate becomes another important metric. Switches and capacitors are subjected to high stress during the normal operation of the converter; the expected lifetime of these components must be investigated under appropriate stress levels to enable highly reliable operation.

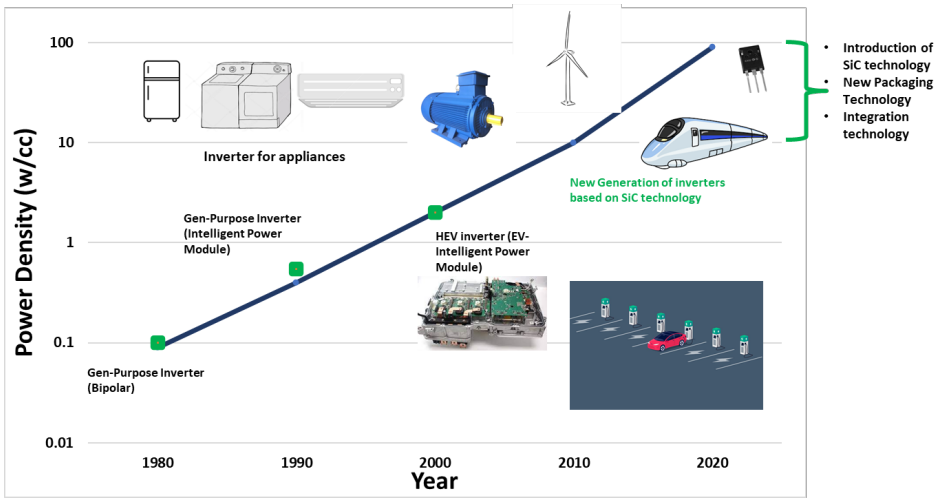

Figure 2. Power density enhancements for power electronics [2].

The US Navy has concentrated on developing Smart Ship Systems Design (S3D) to enable concurrent and multidomain design [3,5,6]. The S3D environment consists of a library of equipment components, Leading Edge Architecture for Prototyping Systems (LEAPS), to allow a rapid ship design environment (RSDE) that will eventually adhere to a set-based design approach to evaluate potential sets of ship design [4]. The LEAPS database includes equipment records with attributes such as dimension, mass, loss, electrical, mechanical, and thermal domain parameters. Application of LEAPS within S3D allows simultaneous modeling in electrical, mechanical, and thermal domain; in addition, it enables the layout aspects of the system as the design progresses. Metamodels of certain power generation and conversion modules have been developed that are scalable in nature and can be incorporated into S3D to enable RSDE studies. The Navy has also shown interest in power electronic building block (PEBB) technology for power conversion modules. Converter topologies such as the modular multilevel converter are an attractive choice to incorporate the Navy's goals for PEBB technologies for MVDC SPS.

In order to develop a design framework to design power electronics converters, all the interdependencies between the components must be properly investigated and understood so that decisions taken regarding one component do not adversely affect the others. Numerous research has been carried out for determining the design equations that dictate the power density or reliability of power converters [2,7–11].

Power density/volume is one of the most frequently utilized metrics when it comes to representing and evaluating the progress of technology [2]. Authors in [2] analyzed several key components to observe the variation in power density including thermal management, capacitors, filters, etc., but the analysis focuses only on estimating power density. Biela in [12] developed an automatic optimization algorithm to enhance the power density of two DC–DC converter topologies, but the optimization that does not use off-the-shelf components is theoretical. Lai in [13] developed a systematic approach to optimize different AC–AC converter topologies, but the simulation tool was validated neither experimentally nor in the multidomain approach. Raggl in [14] developed a single-phase power factor correction converter with the optimization of components such as boost inductor, semiconductor selection, and differential and common mode filters. Even though the work is verified experimentally, the database used is limited, hence not exploring a robust design space. Nawawi in [15] discussed an optimization process for a liquid-cooled, 50-kW, three-phase DC–AC converter, but is restricted to single domain modeling.

Recent surveys regarding the integration of power converters in industrial automation show that power converters can be vulnerable in terms of reliability [8,16]. The most commonly utilized approach for reliability evaluation is the Military Handbook 217 (MIL-HDBK-217). Apart from that, there are other resources available such as Siemens SN29500, RDF-2000, and Telcorida SR-322 [8]. These guidelines overcome the shortcomings of the Military handbook. IEC TR-62380 considers the failure mechanism for a mission profile; however, the data provided are not highly accurate [8]. IEC TR-62380 is replaced by IEC 61709, which provides mission-profile-based failure rate prediction in a more accurate manner. Several works have been reported to predict failure rate in power electronics. Authors in [17] provided a lifetime model for wear-out phase modeling that ignores different load profiles. Zhou in [18] provided an approach to predict reliability on mission-based approach but did not consider the wear-out phase. System-level planning of power electronics converters require converter availability modeling rather than just wear-out phase modeling. Thus, a complete failure rate prediction will consist of both useful life and wear-out period modeling. The power electronic reliability depends on many factors such as converter topology [19], switching schemes [20], and operating and climate conditions [9].

This paper develops a framework to design a Modular Multilevel Converter (MMC) for the MVDC shipboard power system. The application is to benefit early-stage ship design. Hence, the design constraints and parameters are considered for the preliminary stage design. The work initiates by adopting a robust design methodology (Taguchi Method) to create a versatile design space with basic design parameters and then evaluates

the designs and filters out weak design in terms of design requirements. This process eventually identifies the best parameters to achieve a design goal. The identified basic design parameters are used as an input to the multiobjective design algorithm along with other parameters and constraints. This process reduces the computation burden on the MOO greatly due to the reduced number of inputs. The multiobjective optimization (MOO) eventually explores all the designs in its space and filters them out based on constraints and objective function. This iterative process eventually provides Pareto-optimal designs and the final design is chosen from there.

2. Modular Multilevel Converter—Topology and Components

First developed by Lesnicar in [21], the modular multilevel converter (MMC) has achieved considerable attention for having scalability, excellent output performance, modularity, and comparatively lower rating switches. Figure 3 shows the basic configuration of a modular multilevel converter comprising AC and DC terminals and submodule (SM) configurations. The upper and lower arm contain an identical number of series-connected submodules with the arm inductor to suppress any high-frequency components that may exist within the arm current.

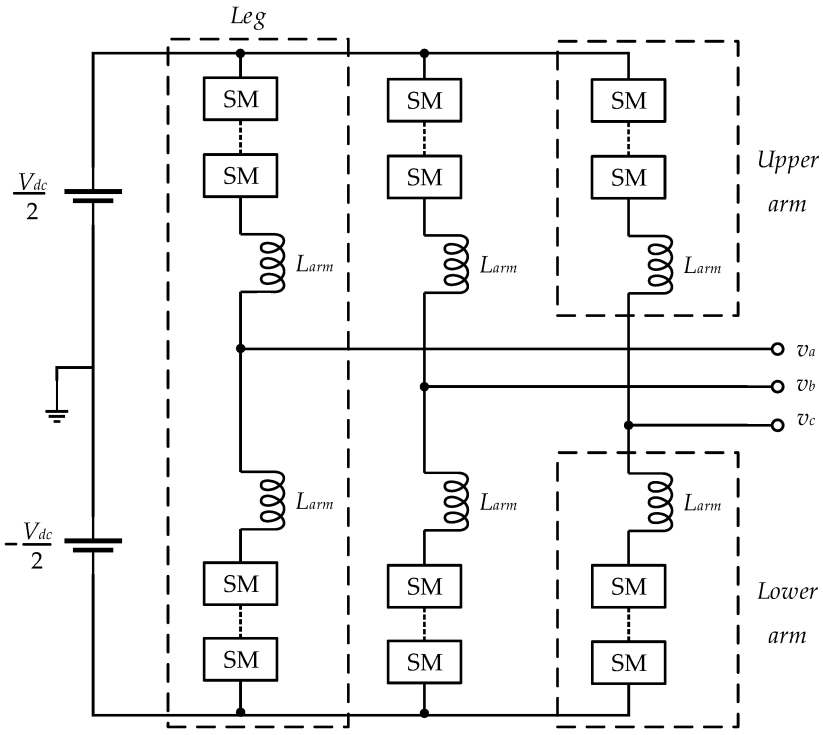

Figure 3. Basic configuration of modular multilevel converters.

The basic structure of MMC contains Si-based power IGBTs as they demonstrate superior switching characteristics. The database used by the converter design algorithm includes a variety of power IGBT modules that are available from different manufacturers. The overall number of IGBTs in a submodule depends on the submodule voltage level selection. For MMC, IGBT datasheets are populated with information on voltage drop (V_{CE}) and collector current (I_c) for at least two operating temperatures. If the current and voltage values are multiplied, the conduction power loss (P_{cond}) can be derived and can be observed with the changing I_c [22]. The benefit of deriving losses such as this is that the curves can be approximated very accurately with a second-order equation, as mentioned in Equation (1). Coefficients (a and b) for Equation (1) can be found using curve-fitting techniques.

$$P_{cond} = a \cdot I_C + b \cdot I_C^2 \quad (1)$$

The switch turn on/turn off profile of an IGBT can be found from the manufacturer datasheet and the total energy required for switching actions can be determined for a range of collector currents using second-order polynomial fitting curve; thus, the coefficients can be determined. The total energy loss due to switching can be defined as

$$E_{\mathrm{TOTAL}} = B_{IGBT}(I_C) \cdot I_C = \left(d + e \cdot I_C + f \cdot I_C^2\right) \cdot I_C \tag{2}$$

The coefficients d, e, and f can be approximated by second-order polynomial fitting curve. If the switching losses are in better approximation of linear dependency for the range of current, switching loss factor B_{IGBT} can be set as a constant.

Submodule Capacitance and Arm Inductance for MMC Submodules

The basic topology of an MMC contains capacitors in the submodules for energy balancing purposes. The selection of capacitors must take into account the compensation of the existing energy imbalance between AC and DC sides. The submodule voltage usually fluctuates with the passing current for each cycle of operation of MMC. The capacitors are required to be designed big enough to compensate for this fluctuation. Several researches have been performed to determine the required capacitance for MMC submodule [23–26]. Authors in [23] derived a relationship between the stored maximum energy and ratio between energy and power. This ratio depends on the application of the converter and typically ranges 10–50 KJ/MVA [23].

To derive the mathematical equation for required submodule capacitance, a few considerations need to be made [26]. For example, the submodule is considered as a load; hence, positive power defines the energy increment within the submodules that eventually increases the capacitor voltage. Assuming negligible stored energy in inductors and a perfect duty cycle distribution, the total energy stored in submodules can be written as follows [26]:

$$E_{converter} = N_{SM} * \frac{C_{SM}}{2} * V_{SM}^2 \tag{3}$$

Energy deviation in the converter is proportional to the nominal energy of the submodule. Following Equation (4), submodule capacitance is given by

$$C_{SM} = \frac{\Delta E_{Converter}}{2 * N_{SM} * V_{SM}^2 * \Delta V} \tag{4}$$

where N_{SM} = number of submodules, $\Delta E_{Converter}$ = change of energy in the converter (J), C_{SM} = SM capacitance (F), V_{SM} = SM voltage (V).

Analysis performed with the converter design algorithm reveals that for a fixed DC bus voltage, a higher submodule voltage level reduces the overall submodule volumes. Even though the number of switches in the module will increase with voltage increase, the capacitance requirement decreases; hence, the number of capacitors is reduced. Therefore, capacitors dictate the submodule volume. For MMC, the arm inductance limits the rise rate of fault current and minimizes distortions in the current. The circulating current magnitude among the phase legs of the MMC impact the AC side operation [23]. In order to minimize the effect of the circulating current and ripple conditions, the arm inductance can be determined by the following equation [23]:

$$\frac{L_{arm}}{2} = \frac{V_d}{4 * N * \sqrt{2} * i_{ripple} * f_{SW}} \tag{5}$$

where L_{arm} = arm inductance (H), N = submodule number, f_{sw} = switching frequency (Hz), i_{ripple} = amount of current ripple (A).

When the focus is limiting the short circuit current, the inductance can be derived as [23]

$$\frac{L_{arm}}{2} = \frac{V_d}{\alpha} \tag{6}$$

where α = rise rate of fault current (A/s).

The rise rate of the fault current can be expressed by the following equation [27]:

$$\alpha = \frac{\Delta i_{dc}}{3 * \Delta t} \tag{7}$$

where Δi_{dc} = DC current value increase during faults and Δt = delays before handling the fault.

If an oversized arm inductor becomes an issue, a filter inductor can be used to compensate for the required arm inductance. Air core reactors are used as arm inductors; the provided inductance fulfilled the requirement. Hence, filter inductors were not considered. The steady state operation of the MMC converter under direct modulation produces circulating currents consisting of even-order harmonics and DC components [23]. To avoid the circulating current resonance, the arm inductance needs to meet the following criteria:

$$L_arm < L_res2 = \frac{3 \cdot N + 2 \cdot m_a^2 \cdot N}{48 \cdot \omega^2 \cdot C_{SM}} \tag{8}$$

$$L_arm > L_res4 = \frac{15 \cdot N + 8 \cdot m_a^2 \cdot N}{960 \cdot \omega^2 \cdot C_{SM}} \tag{9}$$

where m_a is the modulation index and ω is the natural frequency. The parameters remain constant during converter operation except for the case where the converter is operating as an inverter where the modulation index and fundamental frequency are changed. Based on these two criteria, a similar analysis is made to observe the limitation of the inductance value with respect to the change in DC bus voltage. Air core reactor technology has been adopted to provide inductance for MMC; the details can be found in [5].

3. Focused Metrics and Design Methodologies

This section highlights the focused metrics for the study. The design methodologies that have been adopted to produce the desired outcomes are also discussed in detail.

3.1. Metrics of Interest

A majority of the research in the area of SPS is directed toward system-level development of power system architectures and identification of high payoff technology [28]. Different architecture evaluations demonstrate that power conversion equipment can hold up to 25–30% of the entire power system architecture and the number of conversion stages has a significant impact on the overall efficiency of the system [28]. Enhancing efficiency and selection of suitable topology can potentially reduce losses and, in turn, minimize the volume of the converter. Additionally, losses can directly be linked with the failure rate of the system. The power conversion devices are subjected to high switching, which leads to higher temperature and directly affects the operational life of the device. Hence, the focus of this work is more weighted towards volume and failure rate.

3.1.1. Converter Volume

A detailed algorithm has been developed to calculate the overall converter volume considering all the component volumes and safety measures. Figure 4 shows a simplified version of the algorithm for calculating converter volume for MMC. The steps are mentioned below:

1. Define the specification: The initialization point is the specification of the converter such as voltage, current, fundamental frequency, etc. Additionally, the component lim-

its are also specified, such as maximum allowable voltage/current ripple, maximum allowable junction temperature, etc.

2. IGBT selection and loss calculation: The IGBT is selected from the datasheet and the losses are calculated using Equations (1) and (2).
3. Capacitance selection and sizing: The capacitor requirements are calculated using Equations (4) and (5). The capacitors are chosen based on SM voltage levels from the datasheet in the library.
4. Inductance selection and sizing: Arm inductance is calculated based on Equations (5) and (6). The criteria are ensured by applying Equations (7) and (9). Air Core reactors are designed to provide necessary inductance to the converter; details of the design algorithm can be found in [5].
5. Heat Sink selection and sizing: Natural convection cooled, forced convection cooled, and liquid cooled features have been considered for the converter. Once the losses are calculated, they are used to calculate the required thermal resistance of the system. A comprehensive heat sink and liquid coldplate library are made available for the converter design tool for it to access and obtain the required component. Details of the cooling system design can be found in another publication by the authors [29].
6. Cabinet sizing: Once the components of the converter are selected, they are arranged and formed into a cabinet using creepage and clearance guidelines. Figure 5 shows the arrangement of submodules in a cabinet following dielectric standoff guidelines. Hence, the volume of the converter can be calculated from the cabinet dimensions.

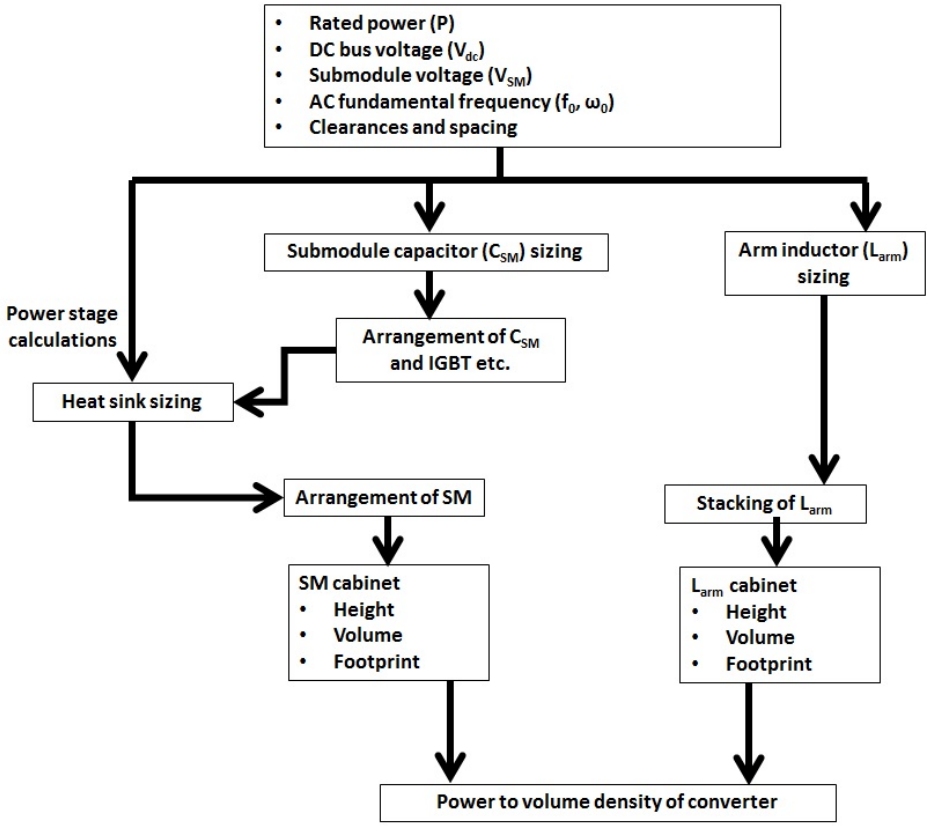

Figure 4. Simplified converter design algorithm for MMC.

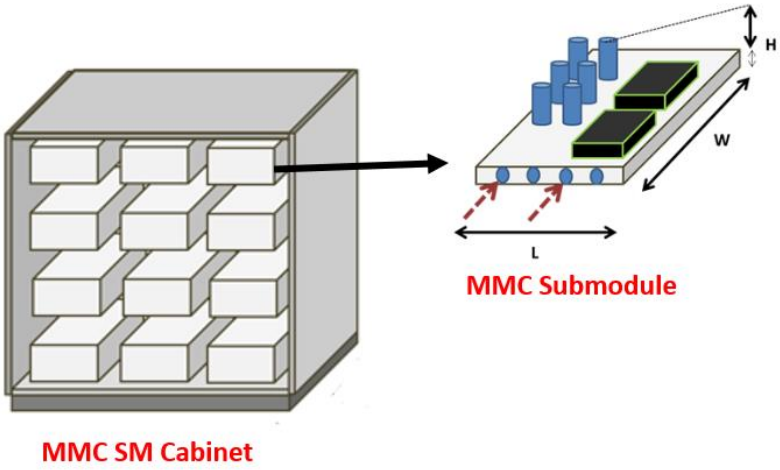

Figure 5. MMC submodule arrangement in a cabinet.

3.1.2. Converter Failure Rate

As mentioned earlier, the most utilized reliability evaluation methods rely on the Military Handbook MIL-HDBK-217. However, it becomes less effective due to newer technologies, vague failure mechanisms, and exclusion of various operating criteria [8]. Additional handbooks such as RDF-2000 and SN29500 overcome the shortcomings of the military handbook. However, an update on the MIL-HDBK-217 handbook is administered by the FIDES group that discusses the physics behind failure while deriving the failure rate [30]. Hence, FIDES' approach is the latest and most comprehensive guide to predicting the failure rate for power electronics.

The survey performed in [31] revealed that resistors and inductors are responsible for only 2% and 5% failures in power electronic converters. Among the other components, switches and capacitors are responsible for almost 50% of failures in electronics. Hence, the focus is concentrated on deriving failure in time for power semiconductor switches and capacitors only. The total converter failure rate (λ_{Conv}) can be estimated as

$$\lambda_{Conv=\sum\lambda_{Caps}+\sum\lambda_{Semi}} \tag{10}$$

$$\lambda_{Conv} = \sum\lambda_{Caps} + \sum\lambda_{Semi} \tag{11}$$

The FIDES approach [30] defines failure rate of an item as

$$\lambda = \Pi_{\mathrm{PM}}\Pi_{\mathrm{Process}}\,\lambda_{\mathrm{Phy}} \tag{12}$$

where

$$\lambda_{\mathrm{Phy}} = \sum_{i=1}^{\mathrm{Phase}} \left[\frac{t_{\mathrm{annual}}}{8760}\right]_i \Pi_i\lambda_i \tag{13}$$

$$\Pi_i = \left(\Pi_{\mathrm{Placement}}\,\Pi_{\mathrm{App}}\Pi_{\mathrm{Rugg}}\right)^{0.511\cdot\ln(C_x)} \tag{14}$$

$$\lambda_i = \sum_k \lambda_{0k}\Pi_k \tag{15}$$

Here, Π_{PM} is the quality impact and technical control over manufacturing; Π_{Process} takes into account of all the processes starting from field operation to maintenance; and Π_i defines mechanical, electrical, and thermal stresses. λ_{Phy} considers the mission profile of the application. λ_i is the failure rate corresponding to each phase of the mission profile. Π_{k} defines the physical constraints of the components within its operational lifetime. The pa-

rameters used in Equation (14) are available from [30]. The failure rate for semiconductors can be defined as

$$\lambda_{Semi} = \sum_{i=1}^{\text{Phase}} \left[\frac{t_{\text{annual}}}{8760}\right]_i \begin{pmatrix} \lambda_{0TH}\Pi_{\text{Thermal}} \\ +\lambda_{0TCy\ \text{Case}}\ \Pi_{TCy\ \text{Case}} \\ +\lambda_{0TCy\ \text{Solderjoionts}}\ \Pi_{TCy\ \text{Solderjoionts}} \\ +\lambda_{0RH}\Pi_{RH} \\ +\lambda_{0\text{Mech}}\Pi_{\text{Mech}} \end{pmatrix}_i (\Pi_{\text{Induced}})_i \tag{16}$$

The failure rate for the capacitors can be obtained by

$$\lambda_{Caps} = \lambda_{0\text{Cap}} \sum_{i=1}^{\text{Phase}} \left[\frac{t_{\text{annual}}}{8760}\right]_i \times \begin{pmatrix} \Pi_{\text{Thermo-elec}} \\ +\Pi_{TCy} \\ +\Pi_{\text{Mch}} \end{pmatrix}_i (\Pi_{\text{Induced}})_i. \tag{17}$$

The base failure $\lambda_0 X$ for capacitors and semiconductor switches are provided in [30]. Additionally, to meet the required capacitance at certain voltage levels, capacitors are connected in a series–parallel combination as mentioned before. To account for these connections, a connection-based reliability evaluation for capacitors, which was derived by the authors in [32], is also considered for the failure rate of the overall converter.

3.2. Design Methodologies

Design automation is an important consideration when it comes to power electronics converter design. For early-stage design, the focus has always been on achieving an optimal solution with reduced modeling and simulation effort without compromising accuracy. Robust design techniques are an attractive choice for power electronics design. These techniques consider a wide variety of sets and significantly reduce design process complexity. Optimal solutions are found by narrowing down the initial design space by evaluating the designs to minimize or maximize design goals. Although the technique is robust and explores a large set of design options, the process is not very effective in optimizing a particular design goal. Hence, in this work, the outcomes of the Taguchi method are employed as an input to the multiobjective algorithm. This section describes the methodologies in detail.

Taguchi Design of Experiments

Taguchi introduced a widely used methodology that can deal with the uncertainty of a design process in a systematic way [33]. This methodology is to optimize the design process, not to optimize any specific application. It employs an orthogonal design array along with the method of design of experiments [34]. This combination of methods ultimately provides the optimal design.

The Taguchi Orthogonal array (OA) is created as a first step to exploring the design space. It essentially creates a design space that constitutes a subspace of combinations created with design factors and their designated levels [34]. Some of the features are mentioned below:

- When all the factors are put in the orthogonal array table along with their associated levels, a great visual representation is achieved that helps the designer understand the trade-offs.
- Exploration and evaluation of design space will eventually enable the selection of the best parameters for design through the "Response Matrix".

Signal-to-Noise Ratio (SNR) is used as a criterion for measurement to evaluate the designs of the orthogonal array. This SNR-based evaluation identifies the dominant factors and their levels in the analysis. Commonly used SNR formulas are mentioned below [34]:

$$SNR_{LTB} = -10\, log(\frac{\sum_{i=1}^{n} \frac{1}{Y^2}}{n}) \quad (18)$$

$$SNR_{STB} = -10\, log(\frac{\sum_{i=1}^{n} Y^2}{n}) \quad (19)$$

where N = number of total measurements and Y = value obtained from measurement.

When the goal is to maximize an effect, the larger the better (LTB) should be used, and if minimization of effect is being considered, the smaller the better (STB) is used. The goal of the paper is to minimize the volume and failure rate. Hence, STB is used to achieve that goal.

The Taguchi method is helpful for preliminary stage design. However, to achieve better design accuracy, a multiobjective optimization technique is adopted.

3.3. Multiobjective Optimization

An optimization algorithm is applied to search for the local and global minimizer for a defined optimization problem. In multiobjective optimization, a single solution might not exist, but a set of equally good solutions does. One way to employ a single objective search technique to find a solution is to apply a weighing factor and perform optimization in an iterative manner until enough points are discovered to construct a Pareto front that comprises a set of Pareto-efficient solutions. Pareto efficiency can be defined as a situation where no solution can be declared better off without making at least one solution worse off. This method is beneficial but it can be challenging to designate weighing factors when dealing with multiple objectives. Another choice is to apply a random sampling technique, essentially choosing n random points in the design space; then, sample the design region uniformly to find a Pareto front [35]. As the technique is a blind search approach, this cannot accurately be described as an optimization.

In this work, a better version of the genetic algorithm entitled the Nondominated Sorting Genetic Algorithm-II (NSGA-II) has been used. This algorithm was developed by Deb [36] in 2002 and has been established as the most popular heuristic search method when a multiobjective optimization is being pursued [35].

Figure 6 shows the overall NSGA-II procedure. The algorithm starts with the generation of initial population that is created for the input of the converter design algorithm mentioned in the previous section. It creates a new population with the mixture of parent and offspring. In the next step, it searches for the nondominated population using nondominated sorting. To maintain diversity in the solutions, it calculates the crowded distance and ranks the solutions. In the last step, crossover and mutation are performed and predefined termination conditions are checked. This process is repeated until the conditions are met.

In this work, for determination of the best possible accommodation between the volume and failure rate, the design of the MMC must be presented as a mathematical mapping—$f(\overrightarrow{p}, \overrightarrow{q})$, where $\overrightarrow{p}$ stands for the design variable and $\overrightarrow{q}$ is the constants of the design—of the design space into the performance with some compatible conditions m_j and n_j (which describe converter inner functions and system requirements, respectively). In this way, a suitable combination can be picked out for a designated performance pool of designs.

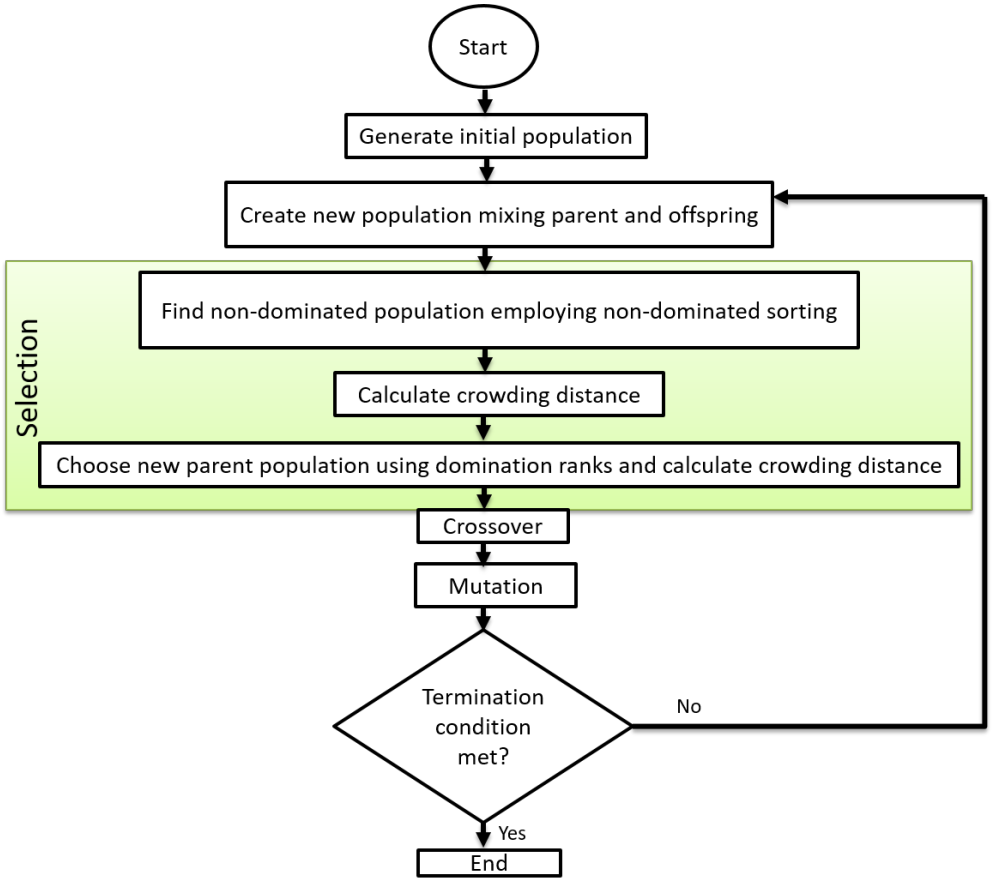

Figure 6. Steps for NSGA-II [35].

3.4. Overall Design Technique

Figure 7 shows a high-level diagram of the developed design framework. The design starts with predefined design parameters. The component library is made accessible to the tool to extract sizing information about switches, capacitors, heatsinks, etc. The steps shown in the figure are mentioned below:

1. The predefined design variables are fed to the Taguchi orthogonal array as design and noise factors. When the orthogonal array is formed, the volume and failure rate is calculated using the converter design algorithm. The calculated volume and failure rate are then explored and evaluated to create the response matrix. The response matrix reveals the best design parameters.
2. The identified design parameters are used in NSGA-II as an input along with other variables, constraints, and objectives. The initial population is formed. The converter design algorithm is executed to determine volume and failure rate. The next step is to evaluate performance space based on objectives and constraints. This process iterates over and over again until the stopping criteria are met and Pareto-optimal front is found.

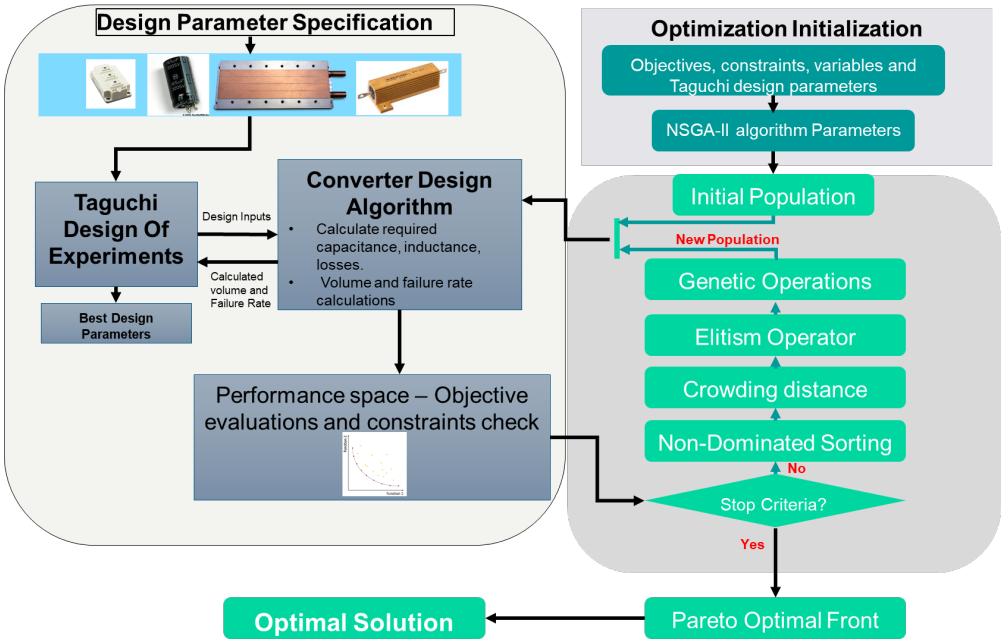

Figure 7. Framework of Design Automation for MMC.

4. Taguchi Experimentation and Optimization

The developed design methodology is utilized to perform Taguchi experimentation and multiobjective optimization on MMC. Some of the design variables are shown in Table 1.

Table 1. Converter specifications and constraints.

Specification	Value
Rated Power	1.25 MW
Fundamental Frequency	60 Hz
Modulation Index	0.9
Ambient Temperature	40 °C
Maximum output current ripple	15%
Maximum voltage ripple	5%
Power Factor	0.9

Taguchi Experiments

The design factors for MMC are selected to be submodule voltage, switching frequency, and cooling technique for the Taguchi experiment. Tables 2 and 3 show the orthogonal array for the MMC and the derived response matrix, respectively. The design factors are placed on the left side of Table 2. Voltage and current ripples are used as noise factors that are placed at the top of Table 2. This combination of design and noise factors are applied to the converter design algorithm to determine the volume and failure for each of the designs. Table 2 mentions the volume of each design. The mean and standard deviation are calculated for each row, considering all the designs within that row. Then, the STB equation is used to calculate the SNR for each row. This process enables picking out the design factors that produced less volume or failure rate.

Table 2. Taguchi orthogonal array for MMC showing volume in m^3.

			V_{Ripple}	0.05	0.05	0.05	0.02	0.02	0.02	0.01	0.01	0.01			
			I_{Ripple}	0.05	0.1	0.15	0.05	0.10	0.15	0.05	0.10	0.15			
Cooling	V_{sm}	f_{sw}	Run No.	1	2	3	4	5	9	7	8	9	μ	σ	SNR
N.C.	0.50	1		2.42	2.42	2.42	2.14	2.66	2.87	2.7	2.64	2.64	2.55	0.22	−8.14
F.C.	0.50	2		2.14	2.24	2.22	2.16	2.37	2.54	2.31	2.24	2.17	2.27	0.13	−7.11
L.C.	0.50	3		2.23	2.22	2.13	2.43	2.51	2.21	2.23	2.41	2.42	2.31	0.13	−7.28
F.C.	1.0	1		1.41	1.52	1.62	1.8	1.82	1.71	1.71	1.62	1.26	1.61	0.18	−4.17
L.C.	1.0	2		1.44	1.44	1.44	1.44	1.48	1.48	1.48	1.45	1.49	1.46	0.02	−3.28
N.C.	1.0	3		2.22	1.70	1.15	2.04	2.04	2.13	2.04	2.03	2.03	1.93	0.32	−5.82
L.C.	2.0	1		1.41	1.41	1.41	1.41	1.41	1.41	1.41	1.41	1.41	1.41	0.0	−2.98
N.C.	2.0	2		1.81	1.51	1.81	1.48	1.83	1.82	1.83	1.8	1.79	1.74	0.14	−4.84
F.C.	2.0	3		1.87	1.81	1.87	1.91	1.89	1.79	1.89	1.89	1.91	1.87	0.04	−5.43

The response matrix for Table 2 is shown in Table 3. The response matrix is created from the orthogonal array. Each row of the orthogonal array creates unique designs from the associated design factors at their respective levels. The response matrix is populated using average SNRs from each design factor at different levels. For example, the first value (−6.2) in Table 3 is obtained by taking the average SNRs of the first level of the cooling method (NC), which are −8.14, −5.82, and −4.84. When the response matrix is populated with the average SNR, the maximum value within each column will represent the best parameter to obtain the design goal. The results show that employment of liquid cooling, 2-kV submodules and 2-kHz switching frequency will provide the lowest volume. Submodule capacitance and cooling technique dominate the overall converter volume. The capacitors are sized to fulfill the minimum requirements to compensate for the energy deviation in the converter. Our studies suggest that liquid cooling employs around 10–12% of the overall SM volume whereas forced or natural convection acquires roughly 30–50% of the overall SM volume.

Table 3. Response matrix for MMC for Table 2.

Response Matrix	For $HSType$	For V_{sm}	For f_{sw}
Level 1	−6.2	−7.51	−5.09
Level 2	−5.57	−4.43	−5.08
Level 3	−4.51	−4.42	−6.18
Obtained Parameters	Liquid	2 kV	2 kHz

A similar approach has been followed to derive the failure rate for MMC employing submodule voltage and switching frequency as design factors. The noise factors are kept the same for the study. The experiments produced the response matrix found in Table 4. The results show that a lower failure rate can be obtained when SM voltage is 2 kV and switching frequency is 1 kHz. The lower switching frequency will minimize converter losses that will eventually minimize the converter failure rate.

Table 4. Response matrix for MMC to minimize failure rate.

Response Matrix	For V_{sm}	For f_{sw}
Level 1	−0.6	1.9
Level 2	0.5	1.6
Level 3	1.2	0.8
Robust level value	2 kV	1 KHz

5. Implementation of NSGA-II in MMC Design

The developed optimization algorithm constitutes a set of mutual component models; a simplified version of this can be found in Figure 8. The component models can be categorized mainly into three areas: semiconductor loss modeling and heatsink selection, capacitance and inductance calculation, and selection.

1. The semiconductor modeling calculates the loss of the switches and accordingly sizes the heatsink.
2. Optimum capacitance and inductance for the converter are determined and capacitors are selected from the manufacturer database. For inductors, a separate algorithm designs the air core reactors and determines the volume.
3. Overall converter volume and the failure in time calculation take place as mentioned in the previous section.
4. Then, the particular design is evaluated and ranked in the optimization algorithm. Eventually, iterations of the process obtain the Pareto front depicting volume and failure in time for the converter.

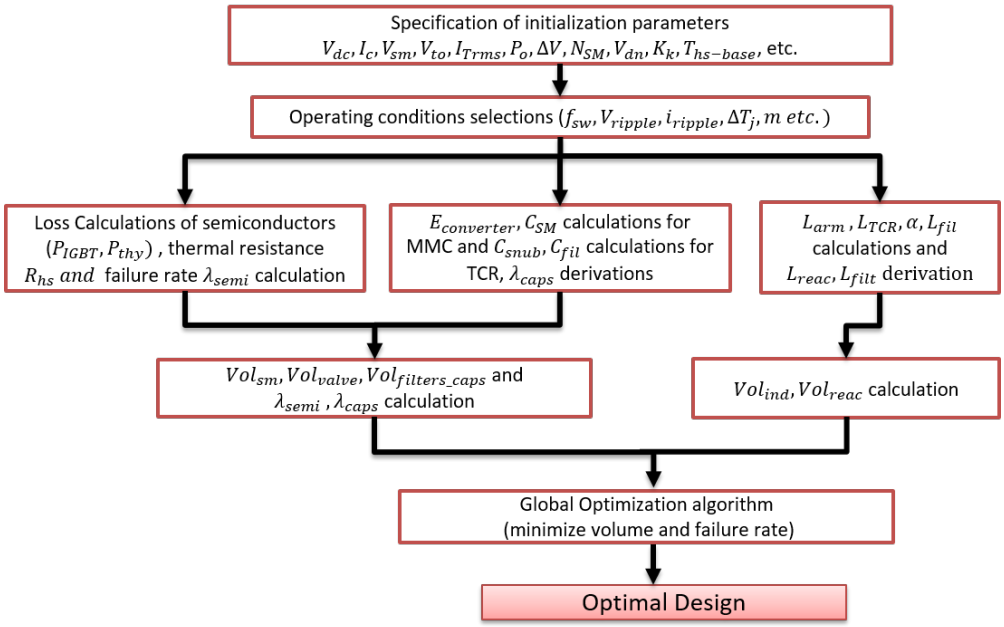

Figure 8. Simplified block diagram for the optimization procedure of the MMC.

The objective functions considered for this optimization are below:

$$\begin{aligned} Volume_{mmc} &= Vol_{sm} + Vol_{\text{inductors}} \\ Failure-rate_{mmc} &= \lambda_{\text{semi}} + \lambda_{\text{caps}} \end{aligned} \tag{20}$$

where $Volume_{mmc}$ defines the volumes of the MMC, Vol_{sm} is the total volume of all the submodules, and $Vol_{\text{inductors}}$ is the total volume of the inductors. λ_{semi} and λ_{caps} are the failure rates of semiconductors and capacitors, respectively. Hence, the optimization formulation is given as follows:

$$\begin{aligned} \text{minimize} \quad & \text{Vol}_{\text{MMC}}, F_{\text{MMC}} \\ \text{subject to} \quad & \Delta T_{j,\text{calc}} \leq \Delta T_{j,\max} \\ & V_{ripple} \leq V_{ripple,\max} \\ & i_{ripple} \leq i_{ripple,\max} \\ & C_{\text{SM,min}} \leq C_{\text{SM}} \leq C_{\text{SM, max}} \\ & L_{\text{arm,min}} \leq L_{\text{arm}} \leq L_{\text{arm, max}} \end{aligned} \tag{21}$$

MOO for MMC

The knowledge derived from the Taguchi method is applied to the MOO input. The response matrix derived from the Taguchi method helps identify the best design factors and their associated levels. These parameters were used as an input to the MOO process. A demonstration involving minimization of volume and failure rate through NSGA-II is performed in this section. The steps regarding the optimization algorithm are as follows:

1. The design algorithm starts with initial parameters such as voltage, current, frequency, SM voltage, voltage/current ripple criteria, temperature constraints, clearance and creepage distance, failure rate database of components, etc. For this case study, the power rating of the converter is selected to be 1.25 MW. The submodule voltage level is considered to be 2 kV as that is found to be the optimal choice derived from the Taguchi method. Voltage and current ripple are selected to meet the criteria of IEEE std 1709 which are 5% and 15%, respectively, at maximum. The database contains information about switches, capacitors, and resistors; these are adopted from a wide variety of manufacturers to maintain diversity in the design space. The failure rate parameters are obtained from the datasheet.
2. The initial random population of NSGA-II algorithm is generated using the initial parameters. This includes the fixed parameters such as voltage, current, and frequency. The additional variable parameters are SM voltage, voltage/current ripple, and associated databases. At this point, converter design algorithm calculates the required parameters. This process is shown in Figure 4. At this stage, initial design space is populated with the obtained population from the combination of initial parameters.
3. For MMC, the constraints are ambient temperature, voltage/current ripple, submodule capacitance, and arm inductance. The constraint values are chosen such that the voltage and current ripples are in accordance with the standard set by IEEE. The submodule capacitance is important for energy balancing of the converter along with minimizing ripples in the output. The SM capacitance is determined and the minimum and maximum are set to keep the value in the margin to avoid excessive ripple. Similarly, arm inductor constraints are designed based on fault current limiting and current ripple minimization criteria. Once the design algorithm determines the volume and failure rate, the designs are pushed out to performance space for evaluation based on objectives. The objectives are evaluated following the constraints.
4. If the stopping criteria are not met, the operations such as nondominated sorting, crowding distance calculation, and elitism selection take place to generate a new population, and the loop continues until solutions are found or the stopping criteria are met.

The submodule switching frequency (f_{sw}) is considered to be 2 kHz, as it is indicated by the Taguchi experiments to obtain a lower submodule volume. The optimization is performed for a 1.25-MW converter with a DC bus voltage of 12 kV. The Taguchi experiments show that the converter volume is minimal when liquid coldplates are used. The converter cooling is restricted to being liquid-cooled to obtain lower volume. The degrees of freedom are the number of IGBTs, area of semiconductors, HS selection, freewheeling diodes, number of turns, and layers of inductor. To account for the energy deviation in the converter, C_{SM}, min and C_{SM}, max are defined as 1900 µF and 2550 µF, respectively. Similarly, L_{arm}, min and L_{arm}, max are defined as 2.6 mH and 3.15 mH. One important thing to note is that filters are not being considered for MMC, as the submodule capacitance and arm inductance are chosen with an appropriate measure that eliminates the need for an additional DC side filter. The Pareto front is shown in Figure 9. Each individual within the front represents a complete system design. The minimum achievable volume for the system is 0.68 m^3 and a minimum 0.0000113 f/yr failure rate for a given operational period of 10 years. One important thing to note is that if the operational time and the operating temperature change, the failure rate increases drastically. The selected design has a volume of 0.95 m^3 and a failure rate of .000015 f/yr. Table 5 shows the specifics of the chosen design.

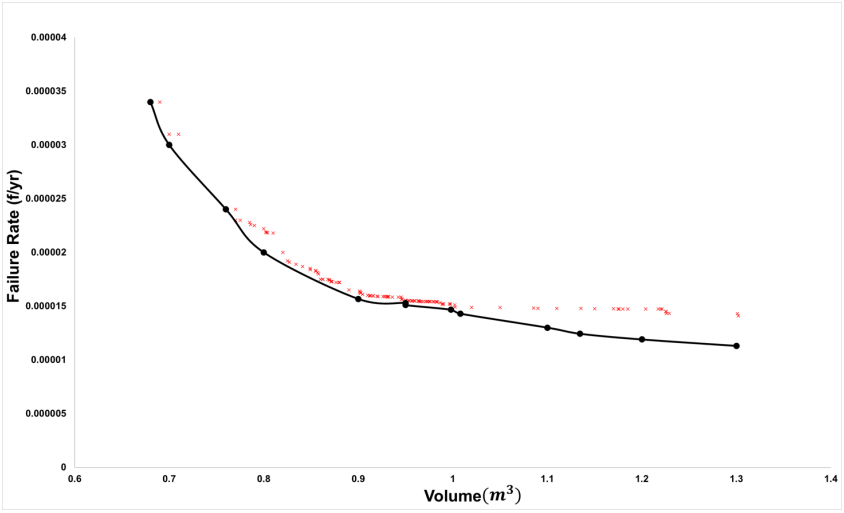

Figure 9. Calculated performance limits of volume and failure rate for MMC.

Table 5. Chosen Design Specifics for MMC.

Rated Power (MW)	1.25
System Frequency (Hz)	60
SM Switching Frequency (kHz)	2
DC Bus Voltage (kV)	12
SM Capacitance (μF)	2275
Arm Inductance (mH)	2.87
Cooling Technique	Liquid
Total Volume (m^3)	0.95
Failure rate (f/yr)	0.0000153

It is worthwhile to mention that the developed design framework can size MMC converters of any power rating. As the building block of MMC converter is the submodule, the number of submodules can be increased to meet high power requirements. The developed case study shows the design of a 1.25-MW converter as an example. For any higher-power application, the number of submodules and their arrangement can be changed to meet the voltage/current requirements. Considering different modules of the All-Electric Ship, such as power generation modules, propulsion motor modules, and load centers, the requirements for power ratings may vary, and the framework is capable of producing optimum designs for any other ratings.

6. Conclusions

This paper develops a framework for MMC design for shipboard power systems. The robust design concept is becoming increasingly popular in SPS due to emphasizing set-based design. In the early stage of the design, set-based design enables the creation of a robust design space and exploring all the design keeping some focused metrics in play. This paper employs the Taguchi method to achieve that goal. The Taguchi technique provides the feasible design parameters to achieve goals such as minimizing volume and failure rate. The NSGA-II picks up on the knowledge derived from the Taguchi method and restricts some of the input to the levels that are indicated by Taguchi method. This process, in turn, reduces the computation load and complexity of the genetic algorithm and achieves the best outcomes for the desired metrics. This process, once integrated into S3D, can aid the power electronic converter design process to establish the goal of incorporating MVDC

system for AES. The framework allows the design of MMC converters for the other ratings that may be required in other zones of the AES. Similar frameworks can also be developed for the design of any other converter topologies used in the all-electric ship. The proposed design methodology can be employed in early-stage ship design, where optimal designs can be selected from a robust design space.

Author Contributions: Conceptualization, T.A.T.; Funding acquisition, M.O.F.; Methodology, T.A.T.; Project administration, M.O.F.; Software, T.A.T.; Supervision, M.O.F.; Writing—original draft, T.A.T. All authors have read and agreed to the published version of the manuscript.

Funding: This work was partially funded by the US Office of Naval Research (ONR).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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