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DC-Link Voltage Stability Analysis of Grid-Tied Converters Using DC Impedance Models

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Abstract: With the integration of renewable energy sources into the power grid, a number of power electronic converters need to be connected together in parallel. Due to this interconnection among the power converters with a common DC bus, the equivalent impedance of the DC network, i.e., DC network impedance (DCNI) of these parallel converters, may vary and can cause oscillations in the DC link voltage (DCLV). In the literature, impedance models of grid-tied converters (GCs) based on the AC side are well reported without including these variations in DCNI. In addition, the dynamics of a phase-locked loop (PLL) play a significant role in GC system stability. To evaluate these stability issues, this paper proposes small signal impedance models viewing from the DC side of a three-phase GC operating under different control modes considering the PLL dynamics and the DCNI variations. Using the proposed DC impedance models (DCIM), DCLV stability analysis is evaluated for a GC. It is verified through bode plots that the interaction between the proposed DCIM and DCNI leads to unstable operation of the closed-loop converter near the PLL bandwidth when the phase difference between DCIM and DCNI is more than 180 degrees. Finally, the analytically developed models are validated using hardware in-the-loop (HIL) testing.

Keywords: DC network impedance (DCNI); DC impedance model (DCIM); grid-tied converter (GC); phase locked loop (PLL); stability analysis

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1. Introduction

The voltage source inverters (VSIs) are extensively used for integrating renewable energy sources with the grid. As more of these converters are integrated, there may be stability issues due to the interactions between the power converters and the utility grid [1]. These stability problems are reported in the literature for various applications, such as the integration of solar PV with grid-connected inverters, offshore wind turbines with high-voltage direct-current transmission [2,3], etc. In order to analyze the stability of grid-connected converters, small-signal stability approaches can be divided into two types, namely state-space modeling [4,5] and small signal impedance modeling [6]. As a result of the development of impedance measurement systems, impedance-based techniques are becoming increasingly important in comparison to state-space techniques. A further advantage of impedance-based models is that they do not require repeated system modeling, and they can provide the frequency domain response for the purposes of determining the stability of the system. The block diagram of a typical DC–AC interface for connecting a DC and AC network from a small signal impedance perspective is shown in Figure 1a. From Figure 1a, an impedance-based stability analysis of a grid-connected inverter can be analyzed in two ways. According to the first approach [7] which is shown in Figure 1b, if the ratio of Z_{in}/Z_{dc} satisfies the Nyquist stability criteria, then the system is stable, where Z_{dc} is the equivalent DC impedance of the total system looking across the DC link to the AC grid side as marked in Figure 1a (it also includes the impedance of the DC capacitor C_{dc}). In the other approach [8], looking from the AC side which is depicted in Figure 1c, the system remains stable if the Z_g/Z_{pcc} ratio adheres to the Nyquist stability criteria. In this

approach, the point of common coupling (PCC) impedance (Z_{pcc}) is calculated by looking from the PCC terminals or AC side to the DC side.

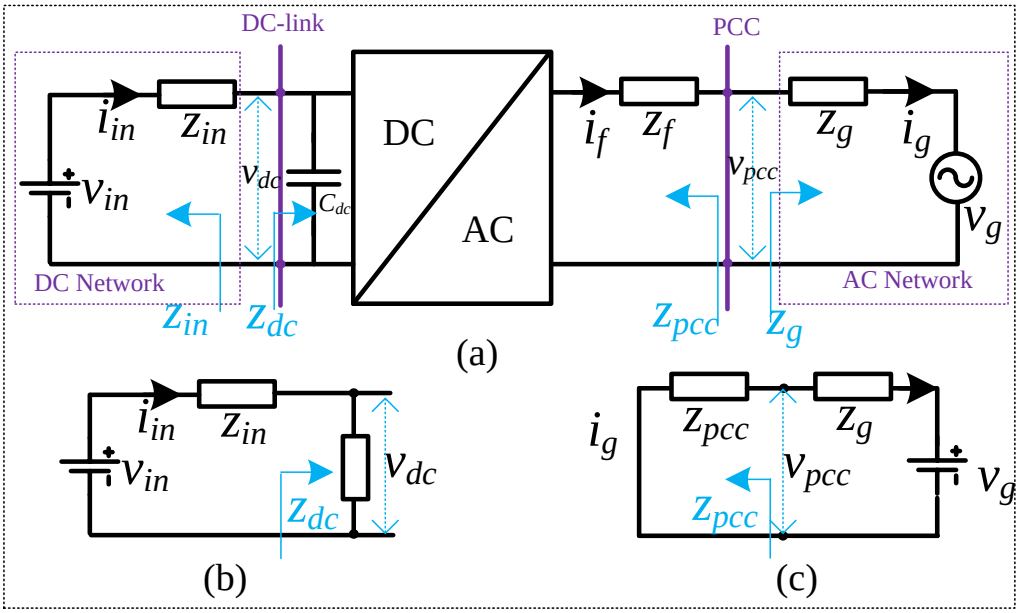

Figure 1. Block diagram of (**a**) a typical DC to AC interface for connecting an AC network and DC network from a small signal impedance perspective, (**b**,**c**) An equivalent representation of the entire system seen from the DC side and the AC side, respectively.

A synchronously rotating dq frame impedance model for three-phase grid-tied converters is developed in [9] from an AC perspective. The impedance-based stability of grid-tied voltage source converters is examined by using impedance models in [10]. Modeling the impedance of three-phase voltage source converters considering the PLL dynamics and frequency locked loops for synchronizing the converter with the grid are discussed in [11]. The research reported in [9–11] is mainly focused on developing the impedance models and investigating the influence of control parameters, system parameters, and their variations on the stability of grid-tied converters. A unified impedance model of grid-connected converter is proposed both in $\alpha\beta$ and dq reference frames [12]. The impact of PLL and weak grid conditions on GC systems is presented in [13]. In [14], the authors pointed out that PLL is acting as a bridge for propagating phase angle information from $\alpha\beta$ to dq transformation blocks. Therefore, a recent paper [15] emphasized the importance of incorporating the PLL dynamics into the dq-frame-based impedance calculation for three-phase grid-tied voltage source converters. Thus, PLL has a significant effect on GCs. Although AC side impedance models in [12–15] are used to assess the stability of the overall system, the effect of DCNI on the system stability remains unexplored in the literature.

The impedance models based on the AC side have difficulty in incorporating DCNI variations on the system stability. A few researchers have proposed the stability analysis based on DC side impedance modeling [16–23]. In [16], based on the virtual impedance method, the DCNI is estimated in the interfaced distributed generation. In [17], it is stated that when AC networks are connected with DC networks through VSCs, the stability of the VSC can be affected significantly. Therefore, it is impossible to ignore the significance of this coupling when developing impedance models. An impedance-based approach is presented to analyze the stability of HVDC systems viewed from the DC side [18]. In [18], impedance models based on the DC side have ignored the dynamics of AC networks. In [19], modeling and analysis of VSC-based HVDC systems for DC network stability studies are discussed. However, in the analysis, the effect of grid impedance and PLL dynamics is not considered for stability analysis. In [20], impedance-based DC link voltage stability analysis is presented in both $\alpha\beta$ and dq frames. DC impedance modeling of grid-

connected converters is presented in [21] considering the grid impedance. However, the DCNI between the two converters is ignored. DCIMs with L filters are proposed and DCNI effects are examined in the DCLV stability analysis of grid-tied inverters in [22]. However, the effect of DC impedance models at lower duty ratios, the dynamics of the PLL effect, and the grid impedance on system stability are not studied. In [23], grid-tied converters operating under open loop, with closed loop dq current control, and with DC link voltage control conditions are discussed based on DC side impedance models. However, stability analysis does not consider PLL dynamics. The existing models in the literature do not consider both the dynamics of PLL and DC network impedance variations in the DC link voltage stability analysis of the grid-tied converter.

Therefore, this paper presents a DC link voltage stability analysis of grid-tied converters using DC side impedance modeling considering both the dynamics of PLL and DC network impedance variations.

The main contributions of this paper are:

1. In order to assess the stability issues, this paper proposes small signal impedance models viewed from the DC side for a three-phase grid-tied converter operating under different control modes such as open loop, dq current control, and DCLV control, taking into account the dynamics of a PLL.
2. Using the proposed DC impedance models, DC-link voltage stability analysis is evaluated for a complete typical grid-tied converter, including DCNI variations.
3. From the proposed models, it is observed that the closed-loop-converter is operating under unstable mode due to the interaction of DCIM and DCNI in the frequency plot closer to the PLL bandwidth.
4. Finally, in order to validate the results obtained from the mathematical models, the grid-tied converter is simulated using controller HIL.

The rest of the paper is organized as follows: Section 2 introduces the configuration of the system. In Section 3, DC impedance models and small signal block diagrams are proposed for different control modes of the GCs. To determine the stability, Section 4 discusses the validation of the proposed models. Section 5 concludes by drawing conclusions.

2. System Configuration

Figure 2a shows the three-phase grid-tied converter with DC and AC networks. V_{in} is the DC input voltage that can be obtained from the battery, solar photo voltaic cells, fuel cells, etc. Z_{in} is the input impedance or DC network impedance. V_{dc} is the DC link voltage and C_{dc} is the DC bus capacitance. Here, AC network or AC subsystems refers to the combination of grid impedance (Z_g) and grid voltage (V_g). V_{pcc} is the common coupling point voltage, and Z_f is the filter impedance. The complete control system block diagram of the converter is shown in Figure 2b. For controlling the d-axis and q-axis currents, two PI controllers are used. The d-axis reference current is generated by an outer DC link voltage controller. PLL generates the required phase angle of the PCC voltage, which is used to synchronize the converter with the grid.

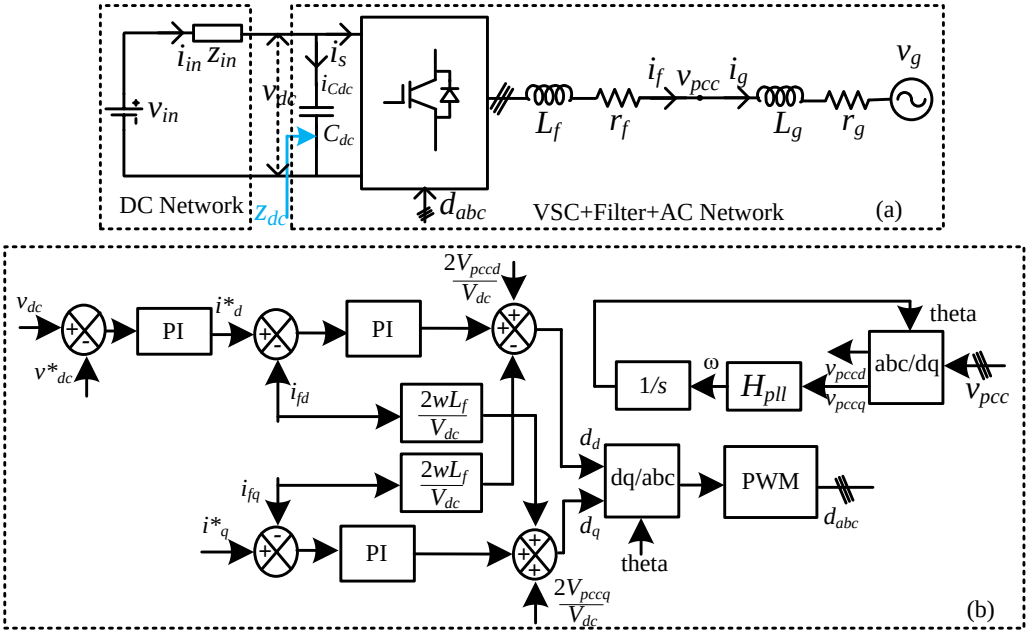

Figure 2. Block diagram of (**a**) Three phase DC–AC converter with DC and AC networks and (**b**) DC link voltage controller and PLL.

3. DC Side Impedance Modelling

Referring to Figure 1b, the DC link voltage is expressed as (1).

$$V_{dc} = \frac{1}{1 + \frac{Z_{in}}{Z_{dc}}} V_{in} \tag{1}$$

From (1), the stability of V_{dc} depends on the impedance ratio between the equivalent impedance of the DC network (Z_{in}) and the DC impedance (Z_{dc}) [22]. If this satisfies the Nyquist stability criterion, then the system is stable [6]. To analyze the DC link voltage stability, Bode analysis can also be used by analyzing the frequency responses of Z_{dc}, Z_{in}.

The intersection frequency in the magnitude plot gives the information about oscillation or resonance frequency in the DC link voltage. A phase plot gives information about stability based on the phase difference between two impedances at the intersection frequency on the magnitude plot. If the impedance ratio phase difference is less than 180 degrees, greater than 180 degrees, and close to 180 degrees, it implies that the system is stable, unstable, and marginally stable, respectively.

For different control objectives, Z_{dc} characteristics are different. Thus, in the following subsections, small signal DC impedance models are derived in open-loop, closed-loop *dq* current control, and DC link voltage control modes while considering the effect of PLL dynamics.

3.1. DC Impedance Model in an Open Loop Condition with PLL Dynamics

Small signal impedance-based model of an inverter in open-loop condition with PLL is shown in Figure 3. By using KCL from Figure 2a, the Equations (2) and (3) are expressed in the *abc* frame. Using the park transformation, abc frame quantities are converted to *dq* frame quantities, which are aligned 90 degrees behind the phase a-axis.

$$\frac{V_{dc}}{2}\begin{bmatrix} D_a \\ D_b \\ D_c \end{bmatrix} = \begin{bmatrix} sL_f + r_f & 0 & 0 \\ 0 & sL_f + r_f & 0 \\ 0 & 0 & sL_f + r_f \end{bmatrix}\begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \end{bmatrix} + \begin{bmatrix} v_{pcca} \\ v_{pccb} \\ v_{pccc} \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} v_{pcca} \\ v_{pccb} \\ v_{pccc} \end{bmatrix} = \begin{bmatrix} sL_g + r_g & 0 & 0 \\ 0 & sL_g + r_g & 0 \\ 0 & 0 & sL_g + r_g \end{bmatrix} \begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \end{bmatrix} + \begin{bmatrix} v_{pcca} \\ v_{pccb} \\ v_{pccc} \end{bmatrix} \tag{3}$$

(4) and (5) are representations of (2) and (3) in the dq frame. The small signal variables are denoted by a superscript $\wedge$ in the following equations. Here, $(y^{dq})^T = [y^d\ y^q]$, $y = I_f$, D and $(\hat{y}_{dq})^T = [\hat{y}_d\ \hat{y}_q]$, $\hat{y} = \hat{v}_{pcc}, \hat{i}_f, \hat{i}_g, \hat{d}, \hat{q}$, where $\hat{v}_{dc}, \hat{i}_{in}, \hat{i}_s$ are state variables.

$$\frac{1}{2}D^{dq}\hat{v}_{dc} + \frac{1}{2}\hat{d}_{dq}\,V_{dc} = Z_f\,\hat{i}_{fdq} + \hat{v}_{pccdq} \tag{4}$$

$$\hat{v}_{pccdq} = Z_g\,\hat{i}_{gdq} + \hat{v}_{gdq} \tag{5}$$

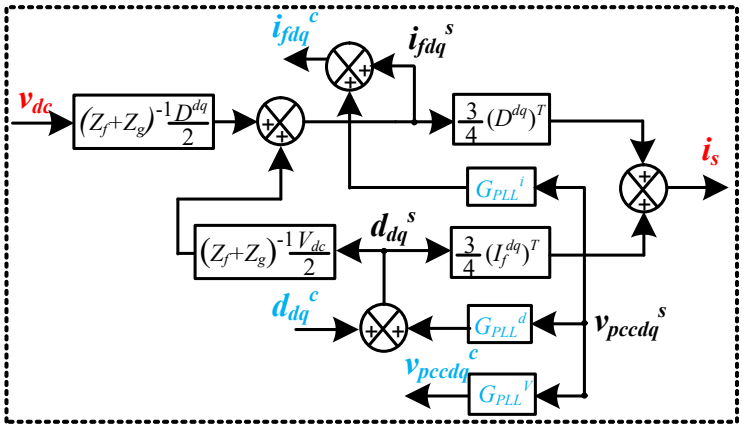

Figure 3. Small signal impedance model of GC operating in open loop with PLL dynamics.

Grid voltage is assumed to be ideal, so $\hat{v}_{gdq} = 0$. Then, (5) can be re-written as (6). The expressions for the coefficients of filter impedance and grid impedance Z_f and Z_g are given in (7) and (8).

$$\hat{v}_{pccdq} = Z_g\,\hat{i}_{gdq} \tag{6}$$

$$Z_f = \begin{bmatrix} sL_f + r_f & -\omega L_f \\ \omega L_f & sL_f + r_f \end{bmatrix} \tag{7}$$

$$Z_g = \begin{bmatrix} sL_g + r_g & -\omega L_g \\ \omega L_g & sL_g + r_g \end{bmatrix} \tag{8}$$

The inverter input current is represented as a function of duty ratio, and the inverter output current can be expressed as (9). By applying KCL on the DC capacitance node point, (10) is obtained.

$$\hat{i}_s = \frac{3}{4}\left((I_f^{dq})^T\hat{d}_{dq} + (D^{dq})^T\hat{i}_{fdq}\right) \tag{9}$$

$$C_{dc}s\hat{v}_{dc} = \hat{i}_{in} - \hat{i}_s \tag{10}$$

A PLL is used to synchronize the converter with the grid by regulating the q-axis PCC voltage. During steady state operation, the PLL angle and actual PCC voltage angle are the same. However, both angles are different when the PCC voltage fluctuates during transient operation. Due to this, the inverter has two dq-frames, namely, one is the system dq-frame and the other one is the control dq-frame [9]. The superscript 's' and 'c' in the equations represent the system and control frame, respectively. The relations for duty cycle, grid current, PCC voltage are given in (11)–(16).

$$\hat{d}_{dq}^{s} = G_{\mathrm{PLL}}^{\ d}\,\hat{v}_{pccdq}^{s} + \hat{d}_{dq}^{c} \tag{11}$$

$$\hat{i}^c_{fdq} = G_{\mathrm{PLL}}{}^i\, \hat{v}^s_{pccdq} + \hat{i}^s_{fdq} \tag{12}$$

$$\hat{v}^c_{pccdq} = G_{\mathrm{PLL}}{}^v \hat{v}^s_{pccdq} \tag{13}$$

$$G_{\mathrm{PLL}}{}^d = \begin{bmatrix} 0 & -D_q G_{PLL} \\ 0 & D_d G_{PLL} \end{bmatrix} \tag{14}$$

$$G_{\mathrm{PLL}}{}^i = \begin{bmatrix} 0 & I_q G_{PLL} \\ 0 & -I_d G_{PLL} \end{bmatrix} \tag{15}$$

$$G_{\mathrm{PLL}}{}^v = \begin{bmatrix} 1 & V_q G_{PLL} \\ 0 & 1 - V_d G_{PLL} \end{bmatrix} \tag{16}$$

In open loop condition, $\hat{d}^c_{dq} = 0$, which can be substituted in (11) and the modified equation is given in (17).

$$\hat{d}^s_{dq} = G_{\mathrm{PLL}}{}^d\, \hat{v}^s_{pccdq} \tag{17}$$

By substituting (6) in (17), the following equation is given in (18).

$$\hat{d}^s_{dq} = G_{\mathrm{PLL}}{}^d\, Z_{\mathrm{g}}\, \hat{i}_{gdq} \tag{18}$$

Using (4) and (6), (19) is obtained.

$$\frac{1}{2} D^{dq} \hat{v}_{dc} + \frac{1}{2} \hat{d}_{dq}\, V_{dc} = (Z_{\mathrm{f}} + Z_{\mathrm{g}})\, \hat{i}_{fdq} \tag{19}$$

By using (18) and (19), the modified expression is given in (20), and the equation for $\hat{i}_{fdq}$ is written in terms of $\hat{v}_{dc}$ is given in (21).

$$\frac{1}{2} D^{dq} \hat{v}_{dc} + \frac{1}{2} G_{\mathrm{PLL}}{}^d\, Z_{\mathrm{g}} \hat{i}_{fdq} V_{dc} = (Z_{\mathrm{f}} + Z_{\mathrm{g}})\, \hat{i}_{fdq} \tag{20}$$

$$\hat{i}_{fdq} = [(Z_{\mathrm{f}} + Z_{\mathrm{g}} - \frac{V_{dc}}{2} G_{\mathrm{PLL}}{}^d Z_{\mathrm{g}})^{-1} \frac{1}{2} D^{dq}] \hat{v}_{dc} \tag{21}$$

By substituting (18) and (21) in (9), $\hat{i}_{\mathrm{s}}$ is determined and given in (22).

$$\hat{i}_{\mathrm{s}} = (\frac{3}{4}[(I_f^{dq})^T G_{\mathrm{PLL}}{}^d Z_{\mathrm{g}} + (D^{dq})^T](Z_{\mathrm{g}} + Z_{\mathrm{f}} - \frac{V_{dc}}{2} G_{\mathrm{PLL}}{}^d Z_{\mathrm{g}})^{-1} \frac{1}{2} D^{dq}) \hat{v}_{dc} \tag{22}$$

Finally by using (10) and (22), the DC impedance model in an open loop condition while considering the effect of PLL dynamics is given in (23).

$$Z_{dc-ol-pll} = \frac{\hat{v}_{dc}}{\hat{i}_{in}} = \frac{1}{C_{dc} s + (\frac{3}{4}[(I_f^{dq})^T G_{\mathrm{PLL}}{}^d Z_{\mathrm{g}} + (D^{dq})^T](Z_{\mathrm{g}} + Z_{\mathrm{f}} - \frac{V_{dc}}{2} G_{\mathrm{PLL}}{}^d Z_{\mathrm{g}})^{-1} \frac{1}{2} D^{dq})} \tag{23}$$

3.2. DC Impedance Model of GCs under Closed Loop Current Control Mode Considering PLL Dynamics

An inner current controller is implemented to regulate the *d* and *q* axis currents. Based on the control block diagram shown in Figure 2b, the small signal equation is represented in the *dq* frame for a grid-tied converter operating in a closed loop *dq* current control is given by (24) and the corresponding block diagram is shown in Figure 4.

$$\hat{d}^c_{dq} = G_5\, \hat{i}^c_{fdqref} + G_6 \hat{i}^c_{fdq} + \frac{2}{V_{dc}} \hat{v}^c_{pccdq} \tag{24}$$

where the expressions for G_5, G_6, G_{i} are given by (25)

$$G_5 = \begin{bmatrix} G_i & 0 \\ 0 & G_i \end{bmatrix},\ G_6 = \begin{bmatrix} -G_i & -\omega L_i \frac{2}{V_{dc}} \\ \omega L_i \frac{2}{V_{dc}} & -G_i \end{bmatrix},$$

$$G_i = k_{pi} + \frac{K_{ii}}{s} \tag{25}$$

Using (2)–(24) expressions, the DC impedance model expression is obtained in the case of a current controller while considering the effect of PLL dynamics and it is given by (26). The expressions of M_3, $G_{\mathrm{PLL}}{}^1$, and M_4 are given in (27), (28), and (29) respectively.

$$Z_{dc-cl-pll} = \frac{\hat{v}_{dc}}{\hat{i}_{in}} = \frac{1}{C_{dc}s + \frac{3}{4}[(D^{dq})^T + (I_f^{dq})^T M_3]\,(M_4)^{-1}\frac{1}{2}D^{dq}} \tag{26}$$

$$M_3 = (G_{\mathrm{PLL}}{}^1 Z_g + G_6) \tag{27}$$

$$G_{\mathrm{PLL}}{}^1 = G_{\mathrm{PLL}}{}^d + G_6 G_{\mathrm{PLL}}{}^i + \frac{2}{V_{dc}} G_{\mathrm{PLL}}{}^v \tag{28}$$

$$M_4 = (Z_g + Z_f - \frac{V_{dc}}{2} M_3) \tag{29}$$

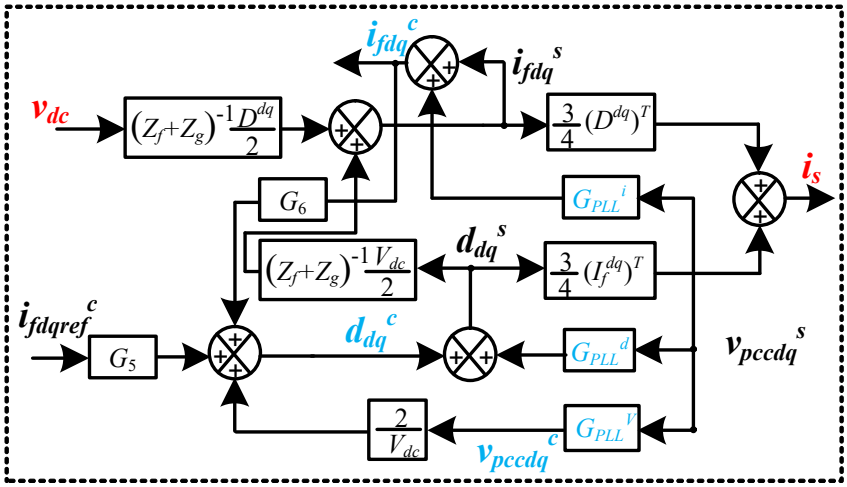

Figure 4. Small signal impedance model of GC operating in closed loop current control with consideration of PLL dynamics.

3.3. DC Impedance Model of GCs under DCLV Control Mode Considering PLL Dynamics

The small signal impedance-based block diagram for DC bus voltage control mode with PLL is represented in Figure 5. The regulation of DC link bus voltage becomes important to maintain the power balance, especially when DC loads are connected to DC bus. The expression of $\hat{i}_{fdqref}$ in terms of $\hat{v}_{dc}$ is given in (30) and where H_{v1} is given in (31).

$$\hat{i}_{fdqref} = H_{v1}\hat{v}_{dc} \tag{30}$$

$$H_{v1} = \begin{bmatrix} k_{pv} + \frac{K_{iv}}{s} \\ 0 \end{bmatrix} \tag{31}$$

$$M_5 = (\frac{1}{2}D^{dq} + \frac{1}{2}G_5 H_{v1} V_{dc}) \tag{32}$$

Finally, by using (2)–(20), (24), (30) and (31), the DC impedance model expression is obtained in the case of a DCLV controller considering the effect of PLL dynamics and is given by (33), and the expression for M_5 is given in (32).

$$Z_{dc-vl-pll} = \frac{\hat{v}_{dc}}{\hat{i}_{in}} = \frac{1}{C_{dc}s + (\frac{3}{4}\{[(D^{dq})^T + (I_f^{dq})^T M_3]\,(M_4)^{-1} M_5\} + \frac{3}{4}\{(I_f^{dq})^T G_5 H_{v1}\})} \tag{33}$$

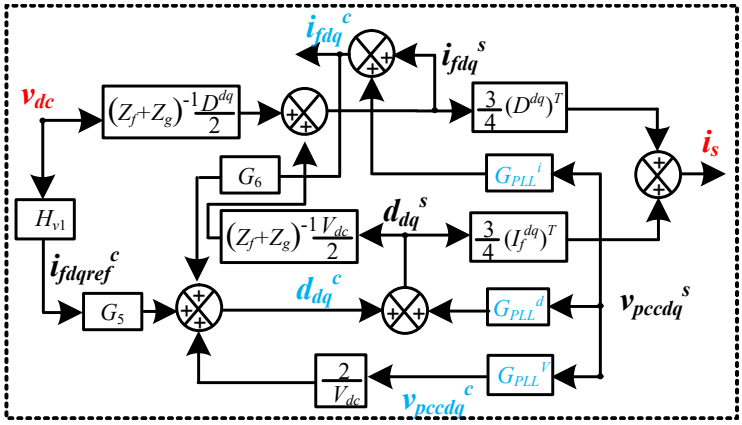

Figure 5. Small signal impedance model of GC operating in DCLV control mode with consideration of PLL dynamics.

4. Results and Discussions

Bode plot analysis is used to analyze the proposed impedance models. Table 1 shows the parameters of the system used in this study. The Typhoon controller hardware-in-the-loop is used to validate the proposed impedance models and the Typhoon HIL testbed is shown in Figure 6.

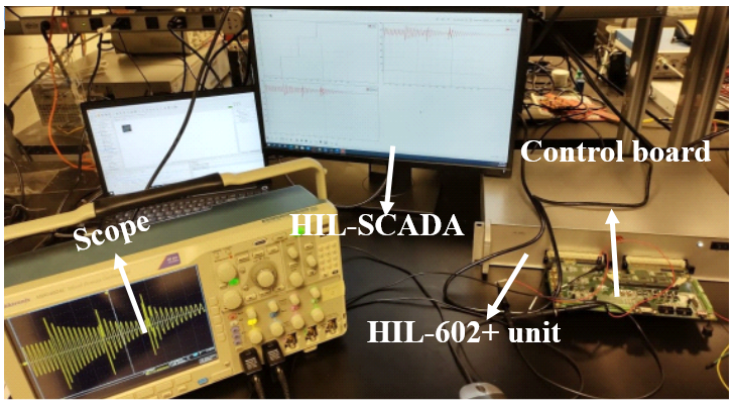

Figure 6. Typhoon HIL testbed.

Table 1. System parameter.

Symbol	Value
V_{in}, V_{grms}	750 V, 230 V
C_{dc}	1200 µF
L_f, r_f	2.6 mH, 0.77 Ω
L_g, r_g	1.3 mH, 0.38 Ω
f_{sw}, f_g	10 kHz, 60 Hz

4.1. DC Impedance-Based Stability Analysis in an Open Loop Condition with PLL Dynamics

A Bode plot for three different input impedances Z_{dcni1}, Z_{dcni2}, and Z_{dcni3}, and the derived $Z_{dc-ol-pll}$ in (22) for fixed duty ratio of $d = 0.11$ is shown in Figure 7a.

From Figure 7a, the magnitude plot shows different DC network impedances intersecting at different frequencies on the open loop DC impedance ($Z_{dc-ol-pll}$). By examining the Bode plot, it is clear that the intersection frequency of two impedances is ($Z_{dc-ol-pll}$, Z_{dcni1}) is the same as the frequency observed from the DC side, which is the resonance frequency (28.8 Hz when L_{in} = 25 mH, C_{dc} = 1200 µF) of input L_{in} and C_{dc} filter. Further, HIL tests have been conducted to validate the derived models, as shown in Figure 7b. From Figure 7b, it observed that the oscillation frequency in the DC link voltage waveform is 29.32 Hz.

Therefore, proposed impedance models are validated. In addition, when the duty ratio d = 0.8, oscillations are not due to the resonance on the DC side but due to the impedance mismatch between the DC network impedance and open loop DC impedance. Hence, it is concluded that the frequency of oscillations in the DCLV depends on the operating point of the converter in open loop conditions.

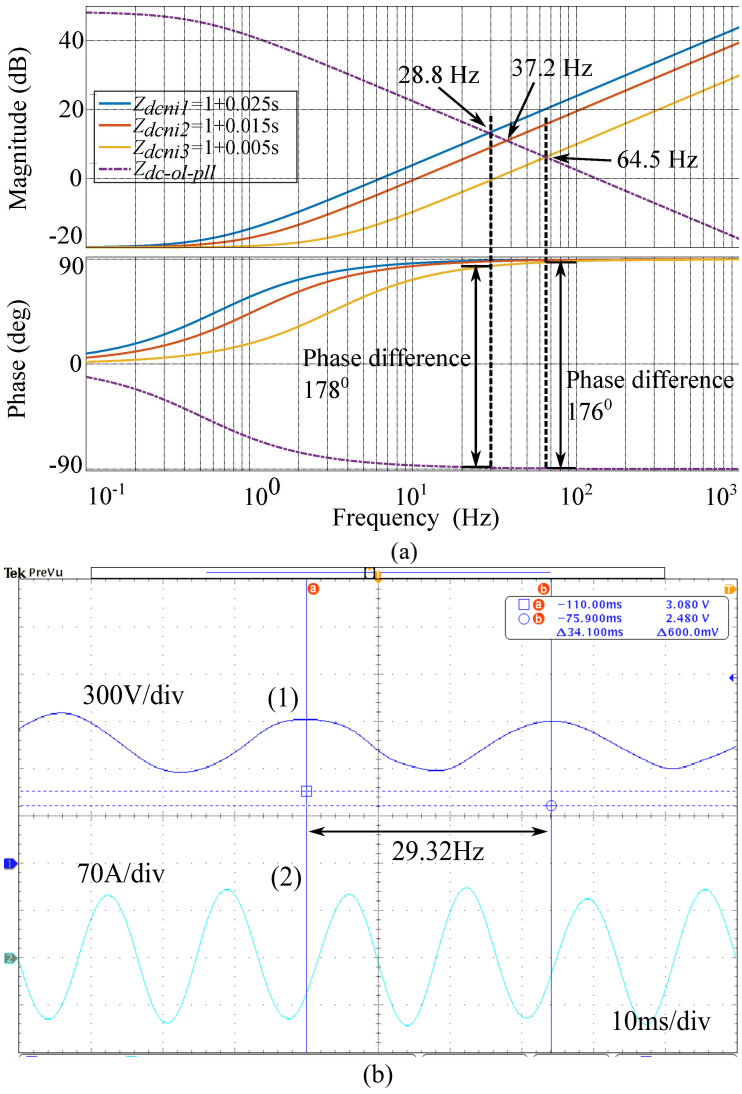

Figure 7. In open loop mode, the converter operates with d = 0.11 (**a**) A Bode plot shows the DCIM with various DCNIs, (**b**) Test result with DCNI: (1) DC link voltage, (2) Grid current

4.2. DC Impedance-Based Stability Analysis of GCs under Closed Loop Current Control Mode with PLL Dynamics

The current loop controller bandwidth and PLL bandwidth are considered as 1000 Hz and 30 Hz, respectively, in this mode of operation. Using (26), the effect of variations in I_{qref} on DC impedance model is plotted in Figure 8a. There are surges and dips around 30 Hz in both magnitude and phase plots of $Z_{dc-cl-pll}$ at I_q = 120 A in Figure 8a.

It is noticed that the phase plot is shifting down as I_{qref} is increasing, which indicates that the converter is losing stability. A phase difference of 228^0 at 36.6 Hz is observed when I_{qref} = 120 A, which results in an unstable operation of the closed loop converter under this condition. Further, the derived models are validated using the controller in the loop tests. From Figure 8a, when the current is changing from 60 A to 120 A, it was observed that I_{qref} is not tracking and reaching unstable operation. Further, very high DCLV oscillations

appeared across the dc link capacitance. The frequency of oscillations in the DC link voltage is noticed at 36.4 Hz. This indicates that derived models are accurate.

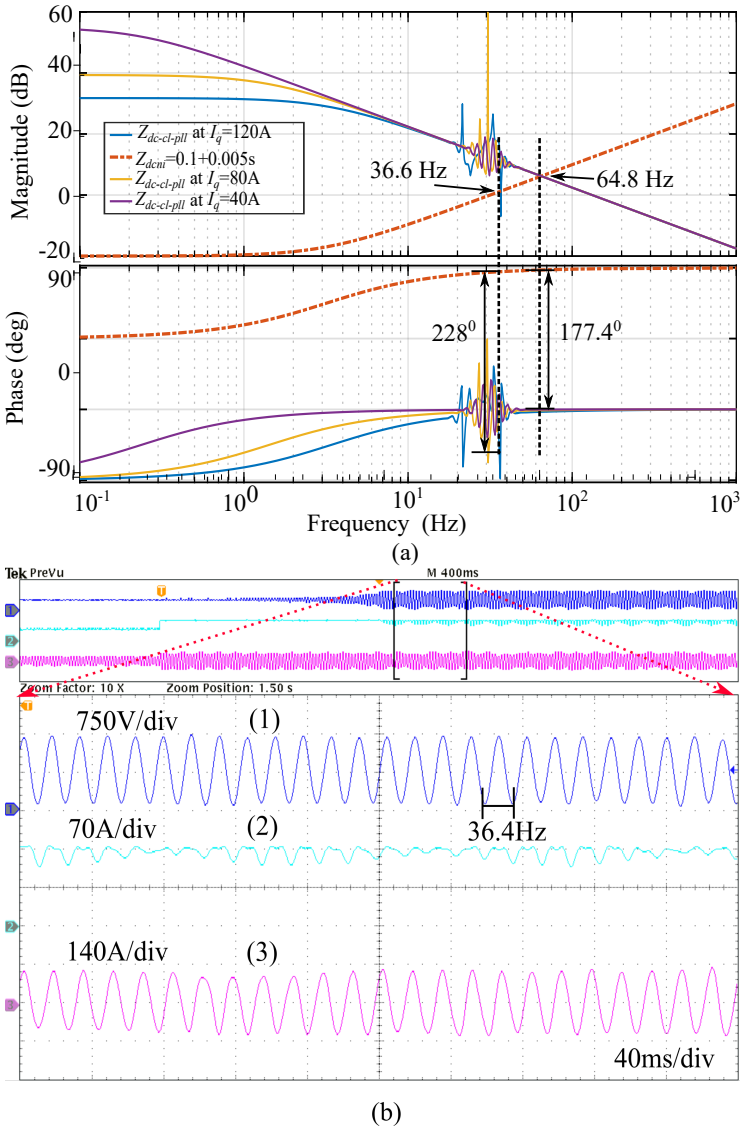

Figure 8. The converter is operating in a closed loop *dq* current control mode. (**a**) A Bode plot shows the DCIM characteristics of various *q*-axis currents with DCNI, (**b**) test result with DCNI: (1) DC link voltage, (2) *q*-axis actual current, (3) Grid current

Further, the variations in the bandwidth of PLL on DC impedance models are investigated here. The current loop controller bandwidth and PLL bandwidth are considered as 1000 Hz and 30 Hz, respectively, in this condition. Using (26), DCIM plots are drawn with two PLL bandwidths which are at $Z_{dc-cl-pll}$ (10 Hz) and $Z_{dc-cl-pll}$ (30 Hz). There are surges and dips around 30 Hz in both magnitude and phase plots of $Z_{dc-cl-pll}$ (30 Hz) in Figure 9a. Here, $Z_{dc-cl-pll}$ (30 Hz) and Z_{dcni3} intersect at 34.8 Hz. The phase difference between the two impedances is 194^0 at that crossover frequency which indicates that the gird-tied converter is operating in an unstable mode. Additionally, HIL tests have been conducted to validate the derived models, as shown in Figure 9b. In Figure 9b, before t_1, the converter was operating in a stable region with Z_{dcni1}. At t_1, Z_{dcni1} is changed to Z_{dcni3}. During this period, the DCLV gradually builds up and causes unstable operation of the converter.

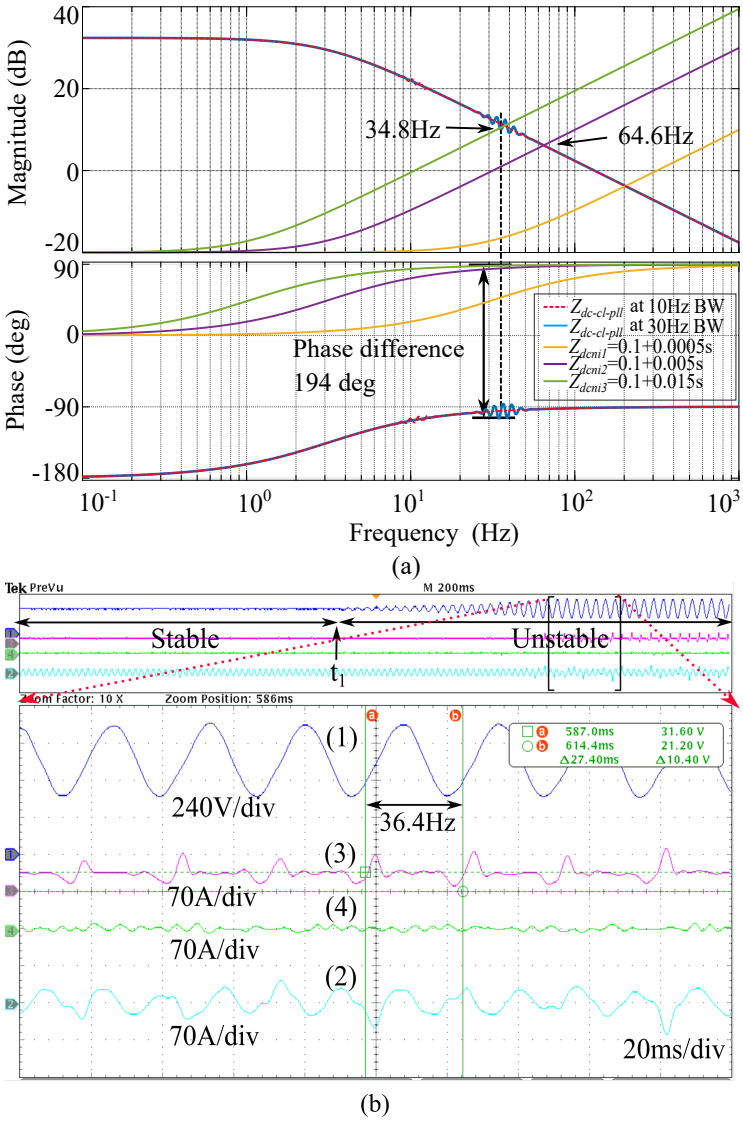

Figure 9. The converter is operating in closed loop *dq* current control mode. (**a**) A Bode plot shows the DC impedance model characteristics with different DC network impedances, (**b**) test result with DCNI: (1) DC link voltage, (2) grid current, (3) *d*-axis actual current, (4) *q*-axis actual current.

During the unstable region, the DCLV oscillations are noticed at 36.49 Hz, which is close to the intersection frequencies of both impedances in the Bode plot. It is concluded that, in *dq* current control, DCIM interacts with DCNI in and around the PLL bandwidth, which results in oscillations in the DCLV and may result in unstable operation of the converter.

4.3. DC Impedance-Based Stability Analysis of GCs under DCLV Control Mode with PLL Dynamics

By using (33), DCIM plots are drawn with two PLL bandwidths, $Z_{dc-vl-pll}$ (10 Hz) and $Z_{dc-vl-pll}$ (30 Hz) are shown in From Figure 10a. Here also in Figure 10a, there are surges and dips around 30 Hz and 10 Hz in both magnitude and phase plots of $Z_{dc-vl-pll}$ (30 Hz) and $Z_{dc-vl-pll}$ (10 Hz) respectively. From Figure 10a, $Z_{dc-vl-pll}$ (30 Hz) and Z_{dcni3} intersect at 32.1 Hz. The phase difference between the two impedances at that intersection frequency is 198^0, resulting in unstable operation. Further, HIL tests have been conducted to validate the derived models, as shown in Figure 10b. Before t_1, the converter is operating under stable conditions with Z_{dcni2}. At t_1, the impedance is changed from Z_{dcni2} to Z_{dcni3}. Then, DC link voltage is slowly building up and reaches unstable operation. During the unstable

region, the DCLV oscillations are noticed at 31.7 Hz, which is close to the intersection frequencies of both impedances. It indicates that the proposed models are accurate. It is concluded that, in the case of DCLV control, DCIM interacts with DCNI around the PLL bandwidth, which result in instability of the converter.

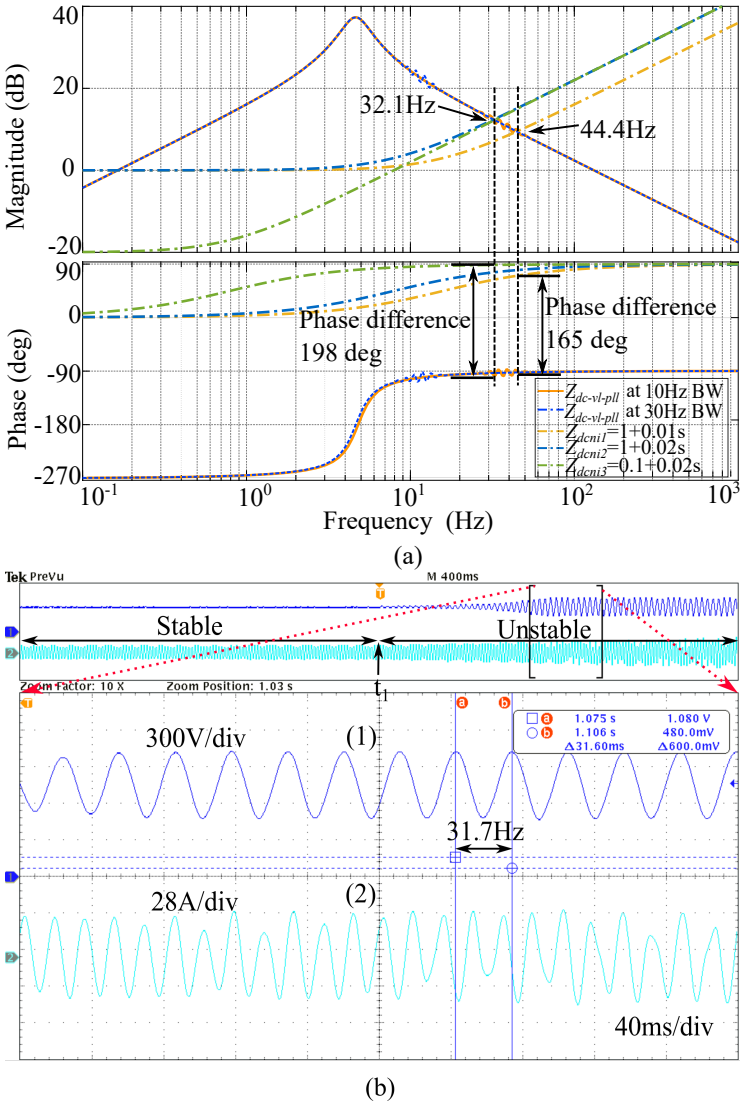

Figure 10. The converter is operating in a closed loop DC link voltage control mode (**a**) A Bode plot shows the DCIM characteristics with various DCNIs, (**b**) test result with DCNI: (1) DC link voltage, (2) grid current.

5. Conclusions

This paper proposes small signal DC impedance models for a grid-tied converter operating in an open loop, closed loop *dq* current control, and DCLV control loop with consideration of PLL dynamics. It is found that in an open loop condition, DCLV oscillation frequencies are caused by DC side LC resonance when operating with lower duty ratios. Furthermore, it is noticed that both the magnitude and phase plot of DCIMs show surges and dips around the PLL bandwidth. Because of this, when DCIMs interact with DCNIs close to the PLL bandwidth, they cause oscillations in the DCLV, which results in unstable operation when using *dq* current control mode. Moreover, in DCLV control mode, the variations in DCNI interact with the DCIM, resulting in an unstable operation. Finally, the proposed impedance models for various control modes are verified through Bode analysis and HIL testing.

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Abbreviations

The following abbreviations are used in this manuscript:

DCNI	DC network impedance
DCIM	DC impedance model
GC	grid-tied converter
PLL	phase locked loop
HIL	hardware in-the-loop
VSIs	voltage source inverters
DCLV	DC link voltage
PCC	point of common coupling
Z_g	grid impedance
Z_f	filter impedance
f_{sw}	switching frequency
f_g	grid frequency
V_g	grid voltage
V_{pcc}	voltage at the point of common coupling
i_f or i_g	grid current
D_{abc}	duty ratio to the inverter at steady state
V_{dc}	steady state DC link voltage

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