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# Reliability of Wide Band Gap Power Electronic Semiconductor and Packaging: A Review

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**Abstract:** Wide band gap (WBG) power electronic devices, such as silicon carbide metal–oxide–semiconductor field-effect transistors (SiC MOSFETs) and gallium–nitride high-electron-mobility transistors (GaN HEMTs) have been widely used in various fields and occupied a certain share of the market with rapid momentum, owing to their excellent electrical, mechanical, and thermal properties. The reliability of WBG power electronic devices is inseparable from the reliability of power electronic systems and is a significant concern for the industry and for academia. This review attempts to summarize the recent progress in the failure mechanisms of WBG power electronic semiconductor chips, the reliability of WBG power electronic packaging, and the reliability models for predicting the remaining life of WBG devices. Firstly, the typical structures and dominant failure mechanisms of SiC MOSFETs and GaN HEMTs are discussed. This is followed by a description of power electronic packaging failure mechanisms and available packaging materials for WBG power electronic devices. In addition, the reliability models based on physics-of-failure (including time-dependent dielectric breakdown models, stress–strain models, and thermal cycling models), and data-driven models are introduced. This review may provide useful references for the reliability research of WBG power devices.

**Keywords:** wideband gap semiconductor; reliability; packaging insulation; SiC; GaN



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## 1. Introduction

Over the past decade, semiconductor technology has made great progress. The present silicon (Si) technology is reaching the material's theoretical limit and is hard to meet all the requirements of the industrial applications. The third-generation semiconducting materials called wide band gap (WBG) semiconductors, such as silicon carbide (SiC), gallium nitride (GaN), and diamond, gradually become popular due to their better electrical, mechanical, and thermal properties than Si [1–4]. Presently, Si power electronic devices usually range between 85 and 97% of efficiency. WBG power electronic devices reduce losses by half or more, raising efficiencies from 95 to 99% [5]. Replacing Si with WBG semiconductors can increase the breakdown voltages, switching frequency, and operating temperatures as well as reduce switching losses [6]. Among these WBG semiconductors, SiC and GaN are the most well-developed and most mature candidates to replace Si in the future. The theoretical performances of SiC and GaN can be compared to Si in Figure 1 [7]. Compared to Si, SiC has a higher breakdown field and thermal conductivity, whereas GaN has a higher breakdown field and electron mobility [8]. These advantages make WBG power electronic devices potential candidates to be used in automotive motor drives, oil and gas drilling and extraction, geothermal drilling and extraction, avionics power supplies, space power supplies, medical equipment, and military applications [9].

Since WBG power electronic devices can withstand high temperatures, radiation, and extreme environmental conditions, it undoubtedly puts forward higher requirements for

the reliability of WBG power electronic devices. Over the past decades, much attention has been attracted to the reliability research of power electronic devices and systems. From the beginning, various metrics such as mean time to failure (MTTF) were proposed and reference books or reports such as the *Military-Handbook-217* [10] for predicting lifetime and the German Siemens' SN 29500 standard for evaluating reliability were published for Si-based power devices. During this period, many empirical-based models and databases were built to evaluate the health conditions of power electronic devices. However, empirical models, based on previous measurement results, are not able to predict the remaining life of power electronic devices in applications with different designs, operational, and environmental conditions. Then, researchers focused on the physics-of-failure model [11–13]. This kind of model is based on the failure mechanism of the device, requiring substantial knowledge of semiconductors and packaging materials. It aims to explore each root cause of device failures. The key point of power electronic reliability research is understanding the multi-physical coupling situation. It is shown in Figure 2 that the mechanical factor, thermal factor, and electrical factor are closely related to each other. The topology and structure of the power electronic device can affect the thermal resistance and stray parameters. The variation of temperature can affect the carrier (electron or hole) energy, and cause the expansion or contraction of packaging materials. Additionally, electric loss produces extra heat, and electric stress influences the mechanical structure. Therefore, understanding these relations is beneficial to explore the failure mechanisms as well as the reliability research.

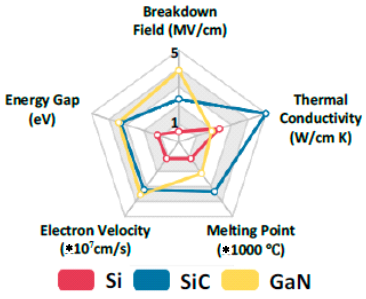



**Figure 1.** Summary of Si, SiC, and GaN relevant material properties [7].

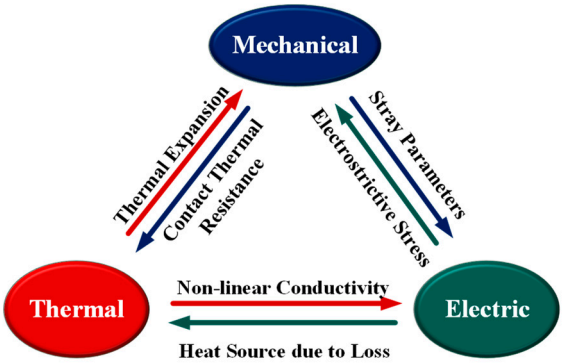



**Figure 2.** Coupling relationships among electrical, thermal, and mechanical factors in power module reliability.

For the SiC power devices: SiC diodes (Schottky diode, PiN diode, junction barrier Schottky diode), metal oxide semiconductor field effect transistors (MOSFETs), Junction Field-Effect Transistors (JFETs), and Insulated Gate Bipolar Transistors (IGBTs) have been developed for commercial use during the last two decades. High-power SiC Schottky diodes have zero reverse recovery charge and the reverse recovery current is low, which makes them popular for industrial use. The SiC PiN diode has low specific resistance but the reverse recovery current during switching and the forward voltage drop are high. The junction barrier Schottky diode combines the advantages of the Schottky and PiN diodes. The SiC MOSFETs are the main switching devices and are widely used. The SiC JFETs

are usually on devices and have advantages such as resistive forward characteristics. To overcome the increasing ON-resistance under high blocking voltage, bipolar devices such as SiC IGBTs are developed for high-power and high-voltage use. For the GaN power devices, diodes (Schottky diode, PiN diode), JFETs, and MOSFETs have similar characteristics to the SiC devices. GaN high electron mobility transistor (HEMT) is the most popular GaN device in the market. For the GaN HEMT, several modified structures have been developed to improve its performance and scope of application such as the enhancement of the GaN transistor (eGaN).

In this paper, the most widely used SiC MOSFET and GaN HEMT are chosen as representatives of WBG power electronic devices. The reliability research of WBG power electronic devices is comprehensively presented. This paper intends to display the overall situation of WBG reliability research and to suggest the direction for future reliability research. The failure mechanism of WBG power electronic chip, the reliability of WBG power electronic packaging, and the reliability models are extensively discussed below.

## 2. Failure Mechanism of WBG Power Electronic Semiconductor Chips

Due to the high breakdown field and high thermal conductivity of SiC semiconductors, they can operate at high voltages (tens kV) and high temperatures (theoretically over 500 °C) [14]. The GaN semiconductor is used in high switch speed situations due to its high electron mobility characteristic. The harsh application environment causes the inevitable degradation of WBG devices, which is critical to reliability research and should be carefully investigated. The failure mechanisms of SiC MOSFETs and GaN HEMTs are discussed in the following part.

### *2.1. Failure Mechanisms of SiC MOSFET*

With the development of SiC epitaxial growth technology, commercial SiC power devices can be widely used in situations of high temperature and power density applications [15]. It should be noted that the update of SiC switching devices is very fast, and various modified structures such as the SiC trench MOSFET (UMOSFET) are reported to achieve low channel resistance and other excellent properties. Here, we only take the SiC DMOSFET as an example, since various SiC MOSFETs have similar reliability issues. The structure of a SiC DMOSFET is shown in Figure 3. It is a vertical device with a planar gate. An inversion layer will be created when the MOSFET is driven by a voltage higher than the threshold voltage. Then, an accumulation layer is created under the gate oxide. Therefore, the electron current can flow from the source electrode to the N-region and downward toward the drain electrode [16].

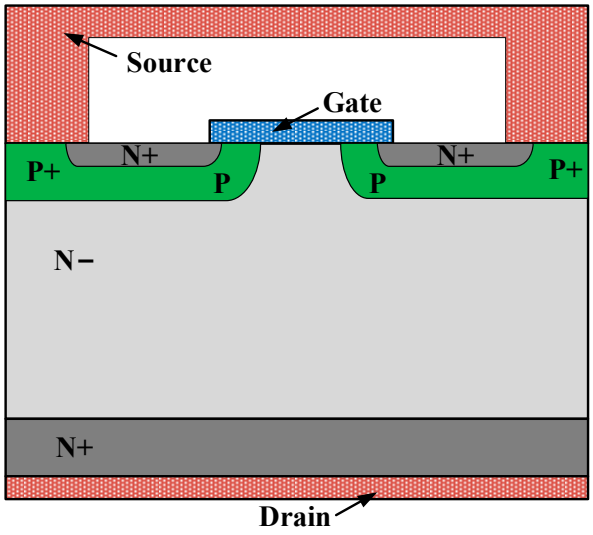



**Figure 3.** Structure of a power DMOSFET.

The gate oxide reliability of the SiC MOSFET has been a popular topic and has drawn much attention not only in academic papers but also in industrial applications over the last two decades [17]. It is found that there is a natural oxide on the surface of the SiC. The high electric field in the oxide, silicon dioxide ($SiO_2$), can cause the device to fail during the blocking mode. Many efforts have been by manufacturers made to control the number of impurities and to improve the quality of the SiC wafer [18–21]. The interface between $SiO_2$ and SiC contains traps and carrier energy states. A large number of electrons are trapped and result in high resistance in the channel. Research shows that the trap situation can be improved by post-oxidation annealing in nitric oxide (NO) [18]. Additionally, the interface between $SiO_2$ and SiC not only affects the on-state resistance but also causes threshold voltage instability [22,23]. The time-dependent dielectric breakdown (TDDB) refers to the threshold voltage instability due to the carrier transport across the interface between the SiC and the oxide [24]. Due to the lesser band offset between SiC and $SiO_2$ (2.7 eV) than between Si and $SiO_2$ (3.2 eV), the tunneling current is higher and the breakdown happens more easily, as shown in Figure 4 [25]. It is found that the variance of net charges in the interface results in the shift of threshold voltage. Positively-charged oxide traps lead to the negative shift of the threshold voltage [23]. The instability of threshold voltage affects the long-term reliability of the SiC MOSFET. Although state-of-the-art gate oxide manufacturing technology can achieve long-term reliability at high temperatures [26], gate dielectric degradation is still the main factor affecting the reliability of the SiC MOSFET [27–34].

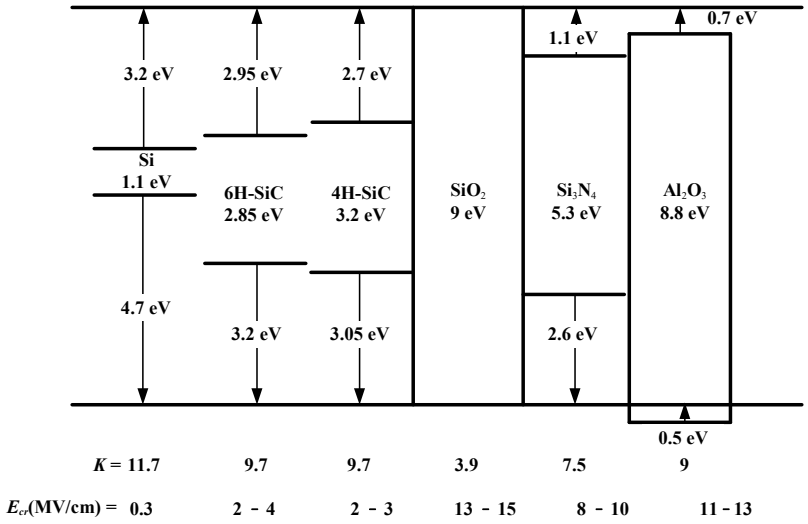



**Figure 4.** Band structures and band offsets of Si, 6H-SiC, 4H-SiC, $SiO_2$, $Si_3N_4$, and $Al_2O_3$ [25].

In addition to the degradation of the gate dielectric, the intrinsic diode degradation and avalanche occurrence are also significant threats to the reliability of the SiC MOSFET. The intrinsic diode of the SiC MOSFET is typically used as a path for fly-back energy in converter systems. It is reported that the intrinsic diode degrades under continuous forward current, resulting in increased power loss [35–37]. This can be tackled by adding an extrinsic diode, such as the SiC Schottky Barrier Diode (SBD) to prevent the degradation of the intrinsic diode [38]. The avalanche phenomenon is also one of the reasons causing SiC MOSFET failure. The root cause of the avalanche is that the device is subjected to an over-voltage with the level over the breakdown voltage. When the avalanche occurs, a high current flows through the device, causing degradation and eventually influencing the reliability of the device [39]. Even though the avalanche phenomenon does not always occur for SiC MOSFETs, it is still a factor that should be considered during reliability research.

### *2.2. Failure Mechanisms of GaN HEMT*

A GaN HEMT is a field-effect transistor containing a hetero-junction formed by two layers of GaN and AlGaN [24]. In order to meet different needs, HEMTs have been

successfully fabricated with different materials, such as Si [40], sapphire [41], SiC [42], and GaN [43] substrates. GaN epilayers that grow on Si substrates lower the fabrication cost and have commercial values [44]. Usually, a buffer layer is needed between the GaN and the substrate, which is the AlN shown in Figure 5. The high carrier mobility characteristics (1200–2000 $cm^2/Vs$) of the GaN HEMTs are due to the existence of a two-dimension electron gas (2DEG) formed in the AlGaN/GaN heterostructure. GaN HEMTs are intrinsically normally on devices, and a negative bias must be applied to the gate in order to remove the 2DEG. The unique physical structure of the GaN HEMT introduces several new failure mechanisms that should be paid attention to.

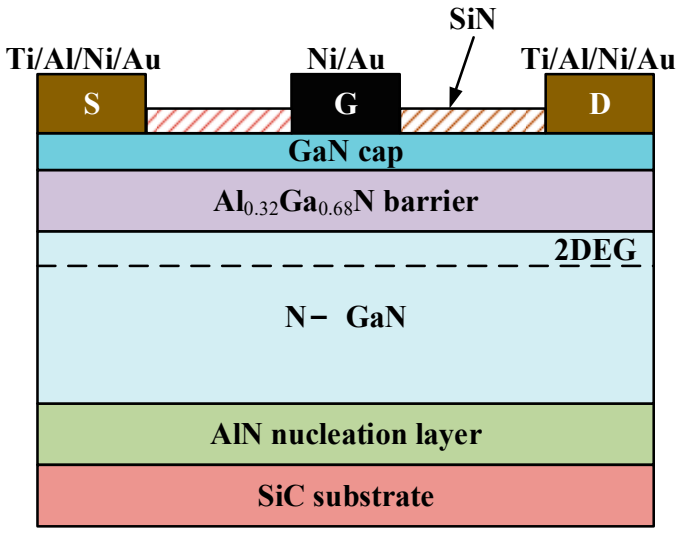



**Figure 5.** A cross-section of an advanced GaN HEMT structure [24].

The dominant factor that affects the reliability of the GaN HEMT is the gate leakage issue [45]. According to simulations, the electric field in the vicinity of the gate electrode can easily exceed 6 to 8 MV/cm, which is sufficiently high to make electrons injected into the body of AlGaN through the tunneling effect. Different field-dependent mechanisms that cause permanent device degradation are discussed in papers [46–50]. Electrons that tunnel from the gate electrode can behave in three manners. First, they can accumulate on the surface of the AlGaN, causing surface leakage. Second, once they are injected into the AlGaN, they may migrate along the surface in a hopping manner from one trap to another trap, producing a gate-to-drain leakage current. Third, they may also be injected through the AlGaN layer and into the 2DEG conducting layer, as shown in Figure 6 [51]. It can be concluded that gate leakage occurs in two regions: the surface and the bulk. It is found that surface leakage is the dominant process during practical application. Therefore, many researchers focus on surface modification, such as passivation, to weaken the effect of surface leakage [49,52–55]. In addition, a GaN cap was introduced to reduce the electric field at the gate edge and to improve surface morphology [56]. The bulk leakage is closely related to the defects generated during the epitaxial growth process. These defects provide a leakage path for electrons and effectively lower the Schottky barrier height of the gate [57]. Some researchers believe that the initial degradation is dependent only on the electric field, which means the temperature has little effect at the early stages. With the development of defects, the Arrhenius law is valid, which means the device degrades exponentially with the increase in temperature [58,59]. The hot electrons play a significant role in the degradation. They cause new traps and damages to the GaN material [60]. In general, the electrical degradation caused by the interaction between injected electrons and traps significantly affects the reliability of GaN HEMTs.

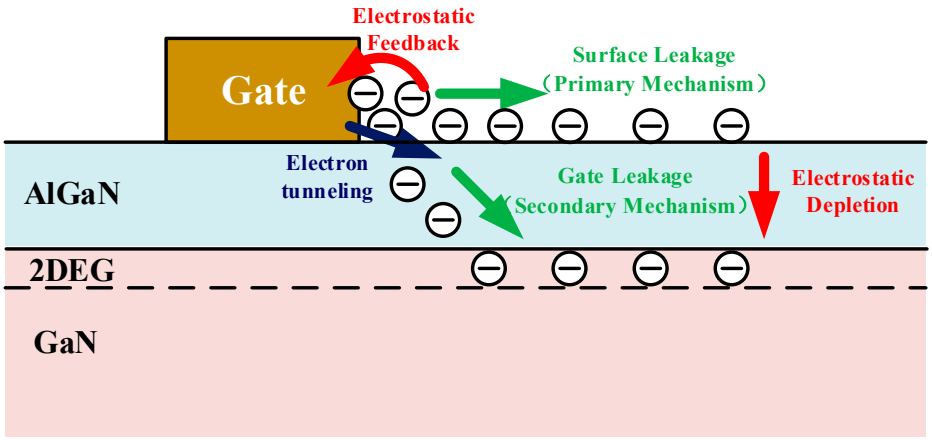



**Figure 6.** Electron tunneling leakage from the gate electrode and possible current paths [51].

In addition to the gate leakage along the surface and in the bulk, some thermally activated processes may also cause degradation. The thermally activated failure mechanisms, including feed metal, interconnect degradation, ohmic contact degradation, gate metal degradation, and delamination of passivation, which are shown in Figure 7, should also be considered [61].

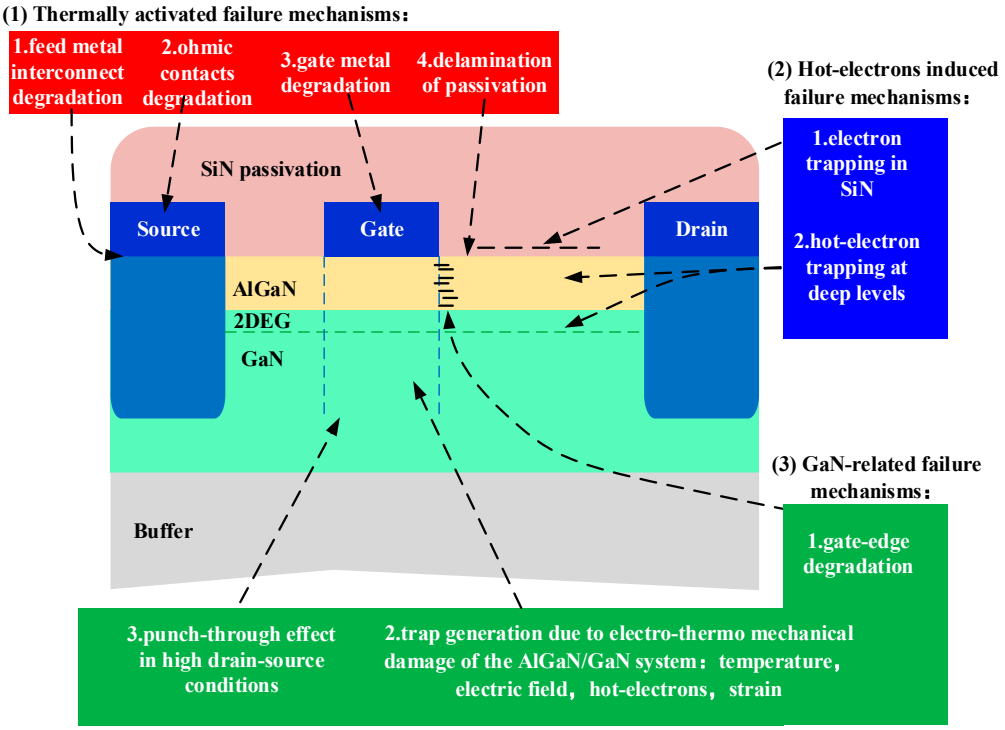



**Figure 7.** Schematic figure representing the mechanisms that can affect the reliability of High-Electron-Mobility Transistors based on GaN [61].

## 3. Reliability of WBG Power Electronic Packaging

The failure of the WBG devices contains two parts; one is the failure of WBG power electronic chips, which is discussed in Section 2. The other is the failure of WBG power electronic packaging. Since the modularization and integration of power electronics is the general developing trend, the packaging reliability of WBG power electronic devices is mainly discussed below. WBG power electronic chips can theoretically operate at a temperature over 500 °C. However, most WBG manufacturers such as Cree, Infineon, and Semikron only provide WBG power electronic products with a maximum working temperature under 175 °C,

which is the same as that of Si-based devices. The key to developing package materials which are able to endure large temperature cycles and withstand high temperatures is the innovation of the packaging structure and packaging material.

To match the operating temperature, voltage, and power of various power chips as well as the assembly structure of the application, the WBG devices are designed to have different packaging structures, such as TO package, flip-chip package, wire bonding package, and press-pack package et al. Since there are many packaging structures and some are specially designed for specific applications, this paper only takes the mostly used wire-bonding structure as an example and focuses on packaging materials. The typical packaging structure generally includes the power chip, bond wire, encapsulation, substrate, solder, base plate, and heat sink, which are shown in Figure 8. It is worth noting that the detail of the structure will vary when it comes to a specific SiC or GaN power device. It seems impossible to enumerate every advanced SiC and GaN power electronic packaging type. The reliability issues of WBG power electronic packaging mainly include the thermo-mechanical fatigue caused by power cycling and temperature cycling during on-site use, as well as the discharge degradation of the insulation material due to the high voltage applied.

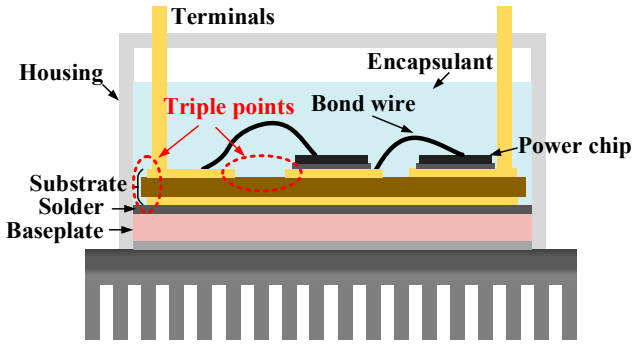



**Figure 8.** Schematic of a typical power electronic packaging.

The thermo-mechanical fatigue of packaging is usually caused by the mismatch of the coefficient of thermal expansion (CTE) between two adjacent materials during wide-range temperature cycling. Additionally, the packaging material also degrades during working time. The discharge phenomenon happens and eventually leads to device failure. Therefore, the development of materials for high-temperature and high-voltage applications is significant. The failure mechanisms of the packaging materials and possible material candidates for WBG power electronic packaging are presented.

### *3.1. Solder*

As is known to all, the solder is used to bring the power chip and the substrate, or the substrate and the base plate together. The solder fatigue is related to micro-voids and CTE mismatch between the solder and the intermetallic layer. During temperature cycling, stress concentration at the interface between the solder and the intermetallic layer will generate cracks, appearing in the intermetallic layer. Then, the heat transfer process is suppressed, which in turn worsens the situation. The cracks start in the vicinity of the solder joint and gradually spread with the shear stress [62]. It is reported that the number of temperature cycles to solder failure with a relatively small range (<100 °C) between a substrate and a base plate is weakly related to the temperature excursion [63]. The mathematical expression of the number of cycles to solder failure is always described in the form of the Coffin–Manson relationship [64]:

$$N_f = \frac{1}{2}\left(\frac{\Delta\alpha\Delta TL}{\gamma x}\right)^{c^{-1}} \quad (1)$$

where $\Delta\alpha$ is the CTE mismatch between the upper and the lower joint materials, $\Delta T$ is the temperature swing, $L$ is the lateral size of the solder joint, $\gamma$ is the ductility factor of

the solder, $x$ is the thickness of the solder joint, and $c$ is the fatigue exponent. It can be concluded from the equation that the reliability of the solder can be improved by reducing the solder joint area, increasing the solder thickness, and reducing the CTE mismatch.

The reliable packaging for WBG power electronic devices is required to withstand high temperature and wide range temperature cycling, which implies high requirements for solder materials. Researchers found some Pb-free solder materials and developed new technology to meet the requirements of the high-temperature application of WBG power electronic packaging, such as the nano-silver sintering and transient liquid phase (TLP) diffusion bonding technique.

Nano-silver sintering was proposed by some researchers [65–67], allowing for the sintering process to be performed at relatively low temperatures (normally at about 220 to 280 °C). The advantage of nano-silver sintering is that it can relieve thermo-mechanical stress due to its micro-porous structure. Some experiments presented that the nano-silver sintering can be stored at 300 °C for at least 400 h [68,69], and survive about 1000 cycles in thermal cycles between −5 and 175 °C. It seems to be a promising solder material candidate for high-temperature WBG power electronic packaging. However, the electro-migration of silver ions acts as the main threat to the reliability of nano-silver sintering. It may cause a reduction in insulation distance, and eventually lead to a short circuit.

The TLP diffusion bonding technique combines traditional liquid phase soldering with a diffusion process. The TLP diffusion bonding process involves the following steps:

- Setting up the bond;
- Heating to the specified bonding temperature to produce a liquid in the bond region;
- Holding the assembly at the bonding temperature until the liquid has isothermally solidified due to diffusion;
- Homogenizing the bond at a suitable heat-treating temperature.

The TLP diffusion bonding technique has the advantage that the resulting bond has a higher melting point than the bonding temperature. Power modules fabricated by the use of the TLP Au–Sn technique have been thermally cycled from −55 up to 200 °C without any cracks or delamination [70].

### 3.2. Bond Wire

Wire bonding is the most common interconnection method in power electronic packaging. The bond wire is used to connect different chips, and chips to metallic substrates. The widely used bond wire materials include Au, Al, and Pt. The bond wire fatigue phenomenon and the mechanism behind it are studied. The failures of the bond wire such as bond wire lift-off and bond wire heel cracking are generally caused by the mismatch between the bond wire material and the WBG semiconductor [71,72]. The bond wire experiences shear stress and temperature swing, which make it easy to generate cracks at the wire termination. The initial cracks propagate to the center and eventually cause the lift-off. It is found that the termination at the end of the chip is easier to fail than that at the end of the metallic substrate (usually copper pad) because the temperature excursion between the bond wire and the chip occurs more often than between the bond wire and the metallic substrate. Similar to the mathematical expression of solder joint fatigue, the number of cycles to fail can be expressed by the Coffin–Manson relation [64]:

$$N_f = a(\Delta T)^{-n} \tag{2}$$

where $\Delta T$ is the temperature swing, while $a$ and $n$ can be calculated by the experiment of thermal or power cycling. Studies show that this expression can precisely evaluate the life of the bond wire at a temperature lower than 120 °C [64]. The bond wire lift-off phenomenon can be observed by a microscopic method such as a scanning electron microscope (SEM), which is shown in Figure 9.

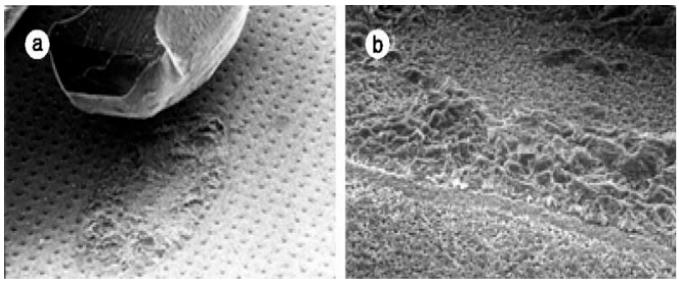


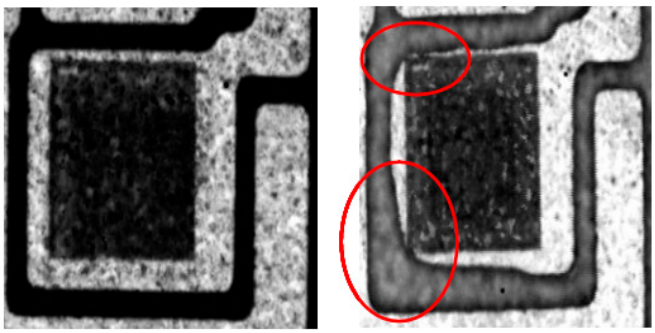

**Figure 9.** Bond wire failure [63]. (**a**) Bond wire lift-off (SEM image, 40×), (**b**) close view of the footprint of an aluminum bond wire after lift-off (SEM image, 100×).

Bond wire heel cracking is always found after long-time endurance tests. The expansion and contraction of the bond wire during temperature cycling is the main failure mechanism of heel cracking. However, experiment results show that the probability of heel cracking is much lower than bond wire lift-off. Some investigate the Cu wire and Au wire as bond wire materials [73,74]. They have higher conductivity than Al and can be used in high-temperature WBG power electronic packaging. It is reported that if the bond wire and the connected metal pad are made of the same material, the bond wire fatigue can be avoided to some extent [75].

### *3.3. Substrate*

The substrate in the WBG power electronic packaging provides insulation and mechanical support for chips and other parts. It is generally made of a ceramic layer sandwiched by two metal layers and positioned between the power chip and the base plate. Therefore, the CTE of the substrate should match those of the chip and the base plate as much as possible. The two most common substrates are called direct bond copper (DBC) and direct bond aluminum (DBA). As the names suggest, the metal layers of DBC and DBA are copper and aluminum, respectively. It is found that DBA is more reliable than DBC during thermal cycling [76]. $Al_2O_3$ is one of the most common ceramic layer materials, which is inexpensive and mature in technology. AlN is a more promising candidate for the ceramic layer for high-temperature packaging, due to its high-temperature conductivity and similar CTE to SiC [73,77]. Another competitive candidate for the high-temperature substrate is called active metal brazed (AMB) substrate, which uses $Si_3N_4$ with high tensile strength (800 MPa) as the ceramic layer [78].

The substrate failures are always presented in the form of metal layer delamination and crack on the ceramic layer, which is shown in Figure 10. The left sub-figure is the original DBC substrate and the right sub-figure is the image of the substrate after 56,780 cycles under the temperature cycle from 40 to 170 °C. The effective methods to suppress the substrate failure are to reduce the mismatch of CTE and reduce the metal area without encapsulation.



(**a**) (**b**)

**Figure 10.** DBC substrate aging, detaching of the upper Cu layer. (**a**) before aging, (**b**) after aging, red circle for detaching area [79].

### *3.4. Encapsulation*

Encapsulation is used to isolate the WBG power electronic device from the environment, preventing moisture and impurities from jeopardizing the device. Additionally, encapsulation also provides insulation for electric connections. The adhesion of the encapsulant is critical for the reliability of WBG power electronic packaging. Silicone gel is the most widely used encapsulant, even though it can only be used under 250 °C. The silicone elastomer with inorganic fillers or modified bonding can endure a higher temperature than 250 °C [80,81]. Some polymers such as polyimide (PI) and parylene are usually used as passivation on the surface of power chips to prevent a breakdown on high voltage occasions [82,83]. However, the thickness of the deposited polymers should be thick enough to withstand a certain degree of high voltage. For example, PI with a thickness of more than 14.5 μm can withstand 600 V at 300 °C [83]. The oxidation process may occur to the polymers at high temperatures, making them degrade. In addition, thermosetting materials such as epoxy resins are also used as hard encapsulants. They perform well with satisfying mechanical strength. However, there is always a trade-off between thermal stability and softness. It is found that hard encapsulants present cracks during thermal cycling [84], and soft encapsulants present thermal instability at high temperatures. It is widely acknowledged that the encapsulant material is the most important factor limiting the working temperature of WBG power devices. The need to develop proper materials that can withstand temperatures over 300 °C (about twice the maximum temperature of currently available commercial WBG power electronic devices) is rather urgent to fully utilize the high temperature and high voltage endurance of WBG power electronic devices.

### *3.5. Electric Discharge*

Since the WBG power electronic devices can operate at higher voltages and temperatures than Si-based power electronic devices, the insulation structure and insulation materials of WBG power electronic devices should be carefully designed. The electric discharge issues will be more and more prominent during the development of WBG power electronic devices [85].

The most electrical fragile position of the WBG power packaging is the triple junction of the encapsulant, the edge of the substrate metal layer, and the ceramic beneath the metal layer [86]. The electrical stress in a half-bridge MOSFET power module packaging is either constant DC stress (between the drain of the upper phase leg and the source of the lower phase leg of a half-bridge power module) or unipolar square wave stress (between drain and source of the upper and lower phase leg of a half-bridge power module). Studies have investigated the electric discharge phenomenon of the power electronic module by partial discharge (PD) measurement under DC and square wave voltages, which is shown in Figure 11. A down-mixing method is proposed to discriminate the electromagnetic interference caused by square voltages and PD signals. It is found that the partial discharge inception voltage of power module insulation under square waves is less than that under DC voltage for the same packaging structure, which is related to space charge accumulation. For the polymeric encapsulation material, it is rather easy to accumulate space charge under DC voltages. Studies have investigated the space charge characteristics at various temperatures, and it was shown that more charges are accumulated under high temperatures, which could distort the local electric field and affect the possibility for PD, as shown in Figure 12 [87]. Moreover, "streamers" are found in the silicone gel under impulse and AC high voltage with point-to-plate electrodes in order to simulate the protrusion of the metallization part in the power electronic device, which is shown in Figure 13 [88]. The results show that silicone gels are unable to recover after a series of partial discharges, presenting limited self-healing character.

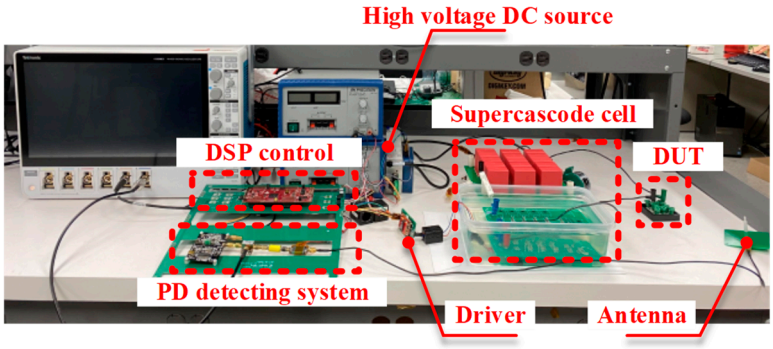



**Figure 11.** PD measurement setup under square voltages [86].

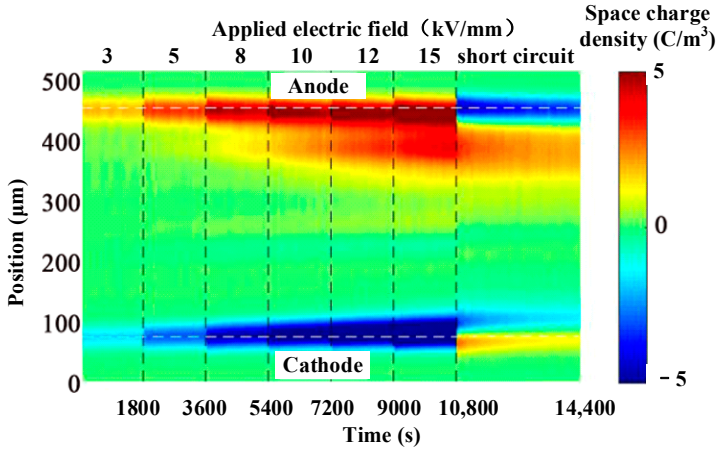



**Figure 12.** Space charge measurement results of silicone encapsulation material at 80 °C (dotted line: different stage of experiment) [87].

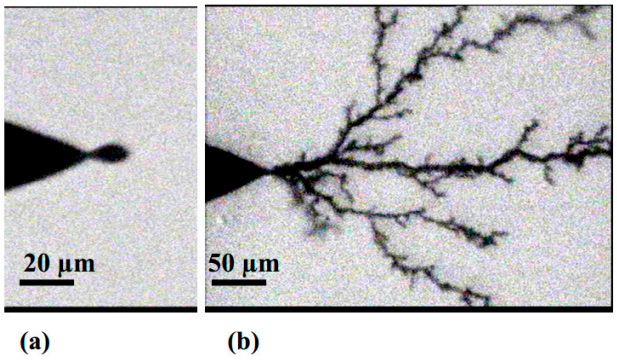



**Figure 13.** Shadow photographs of slow streamer and fast filamentary streamer [88]. (**a**) Applied voltage is 13 kV, (**b**) applied voltage is 17 kV.

Generally, two kinds of methods can reduce the possibility of electric discharge; one is increasing the quality of the packaging, such as eliminating voids, smoothing metallization, and optimizing insulation structure. The other is using a composite material to make the electric field lower than the discharge inception value. Nanoparticles are the most common fillers applied to suppress the discharge phenomenon. Experiments show the use of silicone gel with the addition of high permittivity non-linear nanoparticles, such as barium titanate, which can reduce the electric field concentration at the edge of the substrate copper and therefore increase the PD inception voltage [89].

## 4. Reliability Models

As discussed above, the physical failures of WBG power electronic devices include the failures of power electronic chips and the failures of power electronic packaging. Understanding the failure mechanisms is one of the most important methods to evaluate the condition of the power devices, hence calculating the remaining life and improving the reliability of WBG power electronic devices. Many researchers are concerned with the reliability models of power electronic devices and have proposed several models to quantitatively calculate the remaining life. Currently, the most common failure models contain time-dependent dielectric breakdown (TDDB) models [90], stress–strain models [91], and thermal cycling models [64]. These models have generally been applied to Si-based devices. Theoretically speaking, these models can be used for WBG power electronic devices as long as their failure mechanisms are the same as those of Si-based devices. However, the accuracy of these models still remains to be tested on WBG power electronic devices. Moreover, the data-driven method (or hybrid physics–statistics approach) is currently gaining popularity with the development of condition monitoring techniques and artificial intelligence (AI) tools [64]. The data-driven method may be the future development trend of power electronic prognosis.

### *4.1. Time-Dependent Dielectric Breakdown Models*

As discussed in Section 2, the critical threat to SiC MOSFET reliability is the degradation and breakdown of the gate oxide. The TDDB is caused by the long-term application of a high electric field on the oxide, forming the conducting path from the electrode to the substrate. The degradation generally results from the carrier injection process, which is affected by electric field and temperature. Therefore, the TDDB models can be divided into several types by different forms of these two parameters.

One is the thermochemical model, which is proposed by McPherson [92]. This model describes the effect of the thermal-activated trapping process on the degradation of the oxide dielectric:

$$t = A\exp(\frac{H}{kT})\exp[-\gamma(T)(E_B - E)] \tag{3}$$

where $t$ is the time-to-failure, $A$ is a constant, $H$ is the change in enthalpy required to activate the poly-filament growth at the breakdown, $k$ is the Boltzmann constant, $T$ is the temperature, $E_B$ is the breakdown strength, $E$ is the applied electric field below $E_B$, and $\gamma$ is a temperature-dependent parameter given by:

$$\gamma(T) = B + \frac{C}{T} \tag{4}$$

where $B$ and $C$ are constants. This model is also called the $E$ model because $\log(t)$ is linear to $E$. The breakdown experiment results of thin $SiO_2$ films conform to this model. Another model based on the Fowler–Nordheim tunneling effect was proposed by Chen et al. [93] and modified by Schuegraf [94] is:

$$t = \frac{A}{E^2}\exp(\frac{B}{E}) \tag{5}$$

where $t$ is the time-to-failure, $A$ and $B$ are parameters related to the dielectric, and $E$ is the applied electric field. It shows $\log(t)$ is linearly extrapolated with respect to $1/E$. This model is based on the assumption that when the injected charges reach a critical value, the breakdown occurs. It was mostly used for thin dielectrics stressed by high electric fields since the Fowler–Nordheim tunneling effect dominates the injection process. Additionally, another model based on the Poole–Frenkel effect was proposed [95]:

$$t \propto \frac{Q_{BD}}{E}\exp[\frac{q(\Phi_B - \sqrt{\frac{qE}{\pi\varepsilon_0\varepsilon_\infty}})}{kT}] \tag{6}$$

where $t$ is the time-to-failure, $Q_{BD}$ is the critical charge to breakdown, $E$ is the applied electric field, $q$ is the elementary charge, $\Phi_B$ is the trap depth, $\varepsilon_0$ is the vacuum permittivity, and $\varepsilon_\infty$ is the dielectric constant in the optical limit. The time-to-failure is proportional to the square root of the electric field. Therefore, it is also called $\sqrt{E}$ model. However, sometimes it is hard to determine the exact mechanism since TDDB experimental results can be analyzed by all the three models above, and the analysis results, shown in Figure 14, may be similar.

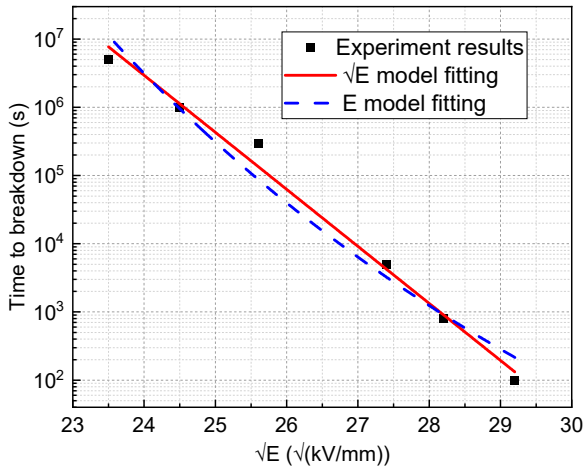



**Figure 14.** TDDB results and two different fitting models [95].

### *4.2. Stress–Strain Models*

It is discussed in Section 3 that solder fatigue, bond wire lift-off, bond wire heel cracking, and substrate delamination are mainly caused by thermal–mechanical fatigue. Stress–strain models are mainly used to describe the fatigue mechanism and evaluate the condition of power electronic devices. Specifically, stress–strain models can be classified as stress-based, plastic strain-based, creep strain-based, energy-based, and damage-based models. The number of cycles to failure is the output of the model. One of the plastic-strain models, the Engelmaier fatigue model, is expressed as [96]:

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma_t}{2\varepsilon_f}\right)^{1/c} \tag{7}$$

where $N_f$ is the number of cycles to failure, $\Delta\gamma_t$ is the total shear strain, $\varepsilon_f$ is the fatigue ductility coefficient, and $c$ is related to temperature and frequency of the cycle. This fatigue model improves the Coffin–Manson relationship by including cyclic frequency effects, temperature effects, and elastic-plastic strains. In all stress–strain models, energy-based models are the largest group of models based on a hysteresis energy term or a type of volume-weighted average stress–strain history [91]. They describe the relationship between the fatigue energy and the stress–strain hysteresis loop. Akay [97] proposed a model based on the total strain energy:

$$N_f = \left(\frac{\Delta W_{total}}{W_0}\right)^{1/k} \tag{8}$$

where $N_f$ is the mean cycles to failure, $\Delta W_{total}$ is the total strain energy, and $W_0$ and $k$ are fatigue coefficients. Liang et al. [98] reported a model concerning the life of solder joints based on elastic and creep analyses:

$$N_f = C(W_{ss})^{-m} \tag{9}$$

where $W_{ss}$ is the stress–strain hysteresis energy density. $C$ and $m$ are temperature-dependent material constants derived from low-cycle fatigue tests. Several papers apply this model to predict solder fatigue and fit the parameters of $C$ and $m$ through experiments [99]. These

models require information with respect to the geometry of the solder or the bond wire, which makes these models more accurate than some empirical models. However, these models neglect the microstructure effect, which may cause a deviation from the practical situation [64].

### 4.3. Thermal Cycling Models

Thermal cycling is one of the main causes of WBG power electronic chip failure and packaging fatigue. Most of the thermal cycling models are based on the Coffin–Manson relationship or its modified form. The Coffin–Manson model is expressed as [64]:

$$N_f = \frac{\delta}{(\Delta T)^{\alpha}} \tag{10}$$

where $N_f$ is the number of cycles to fail, $\Delta T$ is the temperature swing of the cycle, while $\delta$ and $\alpha$ are the parameters related to the material and test setup, respectively. A modified Coffin–Manson model has been successfully applied to the prediction of solder fatigue and other failures [100]:

$$N_f = Af^{-a}\Delta T^{-b}G_{T\max} \tag{11}$$

where $N_f$ is the number of cycles to fail, $\Delta T$ is the temperature swing of the cycle, $f$ is the cycling frequency, $A$ is a coefficient, $a$ and $b$ are cycling frequency exponent and temperature exponent, respectively, and $G_{T\max}$ is an Arrhenius term evaluated at the maximum temperature reached in each cycle.

### 4.4. Data-Driven Approach

The physics-of-failure models discussed above use material properties, packaging geometry, and cycling tests to estimate the life of power devices. Unlike physics-of-failure models, the data-driven approach is based on the condition monitoring technique and data processing technology; therefore, the data-driven approach is easy for engineers to use. The purpose of this approach is to use the variation of parameters, features, or changes in possibilities of the system state to estimate the time-to-failure. Due to the development of the condition monitoring technique, the relation between device failure and monitored parameters has been vastly investigated. Several condition monitoring methods such as the on-state collector-emitter voltage-based method, the gate emitter threshold voltage-based method, the switch time-based techniques, and the temperature-based techniques are reported and applied in practical situations [101].

To use the data-driven approach, researchers need to pay enough attention to two key steps: the variable reduction step and the failure threshold defining step. In terms of the condition monitoring method, it monitors many parameters, and the amount of data continues to grow over time. In such an important data collection, it is necessary to find several critical parameters which are related to the health condition and which may be used to predict the remaining life of power electronic devices.

In order to reduce redundancies of data, several variable reduction methods are proposed. Some are the principal component analysis (PCA) and the minimum redundancy maximum relevance (mRMR) method. The PCA method is one of the most widely used data dimensionality reduction algorithm. The main idea of PCA is to map n-dimensional features to k-dimensions. This k-dimension is a brand-new orthogonal feature, also known as principal component, which is a k-dimensional feature reconstructed on the basis of the original n-dimensional feature. Only the dimension features containing most of the variance are retained, and the feature dimensions containing almost no variance are ignored to achieve a dimensionality reduction processing for data features [102].

The mRMR method is proposed by Peng et al. [103]. The principle is very simple, that is, to find a set of features with the largest correlation with the final output result (max-relevance) in the original feature set, but the least correlation between the features (min-redundancy). It first calculates the mutual information of every two variables, then calculates the relevance between variables and class variables, as well as the redundancy of

all variables. Lastly, the mRMR criterion is the combination of relevance and redundancy, typically using subtraction. The detailed expression is described in [103].

After the reduction in redundant variables, it is necessary to discriminate the data indicating failure or the trend towards failure from the whole important data set. The Mahalanobis distance (MD) is one of the most commonly used methods to define the failure threshold. The MD is a measure of the distance between a point $X$ and a set of points $D$, introduced by P. C. Mahalanobis in 1936 [104]. The Mahalanobis distance of a point $X = (x_1, x_2, \ldots, x_n)^{\mathrm{T}}$ from a set of points $D$ with mean $U = (\mu_1, \mu_2, \ldots, \mu_n)^{\mathrm{T}}$ and covariance matrix $S$ is defined as:

$$D_M(X) = \sqrt{(X-U)^T S^{-1}(X-U)} \tag{12}$$

The MD is used in anomaly detection, pattern recognition, and process control [105]. It has been used to detect anomalies in notebook computers [106] and multilayer ceramic capacitors [107]. To see more of MD, refer to [104].

Apart from the MD, several cluster analysis algorithms are well developed to determine which class (usually two groups: healthy and faulty) a new data element belongs to. The k-nearest neighbors (KNNs) algorithm is one of the cluster analysis algorithms and is used for classification and regression [108]. In KNNs classification, the output is a class membership. The algorithm generally contains two steps: the training step and the classification step. During the training step, vectors (data) with a class label are the training examples in a multidimensional space. Then, the vectors and class labels of the training samples are stored. During the classification step, an unlabeled vector (a data point) is classified by assigning the label which is the most frequent among the k training samples nearest to that data point. The KNNs algorithm is among the simplest of all machine learning algorithms but has been applied to evaluate the conditions of a lot of power equipment [109].

In recent decades, AI tools, such as expert system, fuzzy logic, neural network, and genetic algorithm have advanced significantly and are expected to be powerful solutions for evaluating the reliability of power electronic devices and systems [110,111]. The input of these tools is the monitored data, and the output of these tools are the health conditions of the power electronic systems.

The artificial neural network (ANN) is one of the most frequently used AI tools in machine learning, image recognition, medical diagnosis, and power equipment prognosis. In common ANN implementations, ANN is divided into three layers: the input layer, several hidden layers, and the output layer. The input data transfer between artificial neurons and the output of each artificial neuron is calculated through the non-linear function of the sum of its inputs. Similarly to the KNN algorithm, the ANN should be trained with labeled samples and the training process can be intermittent and restarted with human supervision. The resemblance between a biological neuron and an artificial neuron is shown in Figure 15. Recently, an ANN method called recurrent neural network (RNN) presents powerful ability in handwriting recognition [112] and speech recognition [113,114]. The RNN passes the state through its own network, so it can accept a wider range of time sequence inputs. Therefore, this characteristic makes it perfect to handle time sequence data and can predict future performance based on past data. The long short-term memory (LSTM) structure is one of the most widely used RNN structures. It modifies the RNN structure by adding "cell" to judge whether the data is useful or not, as seen in Figure 16. Researchers have applied RNN to trace the electric vehicle battery states, using measurable data (current and voltage) from an electric vehicle where the batteries are charged and discharged according to its driving profiles [115].

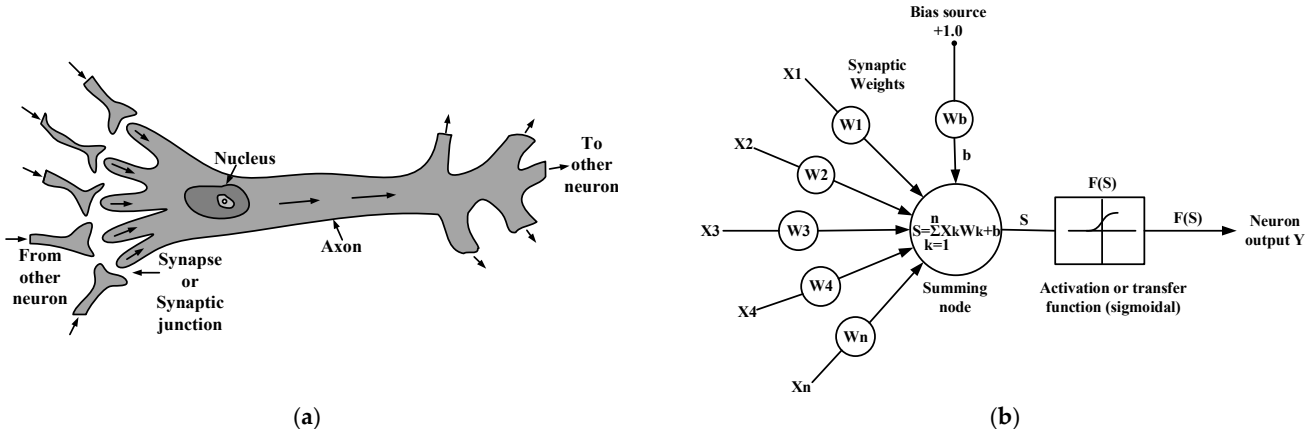



**Figure 15.** Resemblance between a biological neuron and an artificial neuron [106]. (**a**) Biological neuron, (**b**) artificial neuron.

Since the ANN has gained much popularity in many applications, the ANN algorithm has also attracted much attention in the prognosis of power electronic devices. H Ma et al. [116] use an ANN for the fault diagnosis of a three-phase silicon-controlled rectifier (SCR) circuit with an inductive load. The relations between faults and waveforms of a power electronic circuit are kept in a neural network. They set the waveform data of the SCR as the input and the condition of the SCR as the output. The key issue of the application of the neural network is the training process of the network. The network prediction ability relies on the completeness of the training samples, which means the reliability of the network is based on the accuracy of the trained samples.

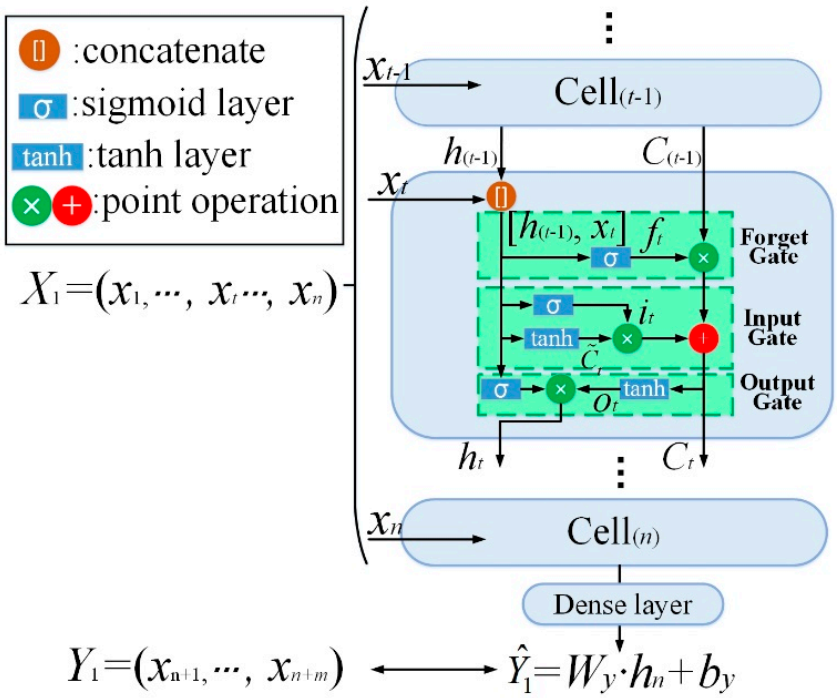



**Figure 16.** Structure of long short-term memory (LSTM) unit [117].

## 5. Discussion

### *5.1. Major Threats to WBG Power Electronic Chips*

In this paper, the two most widely used, most maturely developed, and most promising WBG power electronic devices, SiC MOSFET and GaN HEMT, are selected as representatives of WBG power electronic devices. The critical failure mechanism of SiC MOSFET is the fatigue

of the gate dielectric. The conduction band offset between SiC and $SiO_2$ is smaller than that between Si and $SiO_2$, which causes severe gate dielectric reliability issues such as tunneling injection (Fowler–Nordheim effect), instability of threshold voltage, and time-dependent dielectric breakdown. The interface between the gate dielectric and SiC is the critical factor affecting the performance and the reliability of SiC MOSFET through the interaction between injected carriers and traps (local states). The high operating temperature of the SiC device affects the carrier injection, transport, trapping, detrapping, and recombination process, which makes the reliability issues more prominent. Although the development of SiC manufacturing makes it possible to generate SiC wafers with fewer defects, the reliability of the gate dielectric is still an issue to be adequately handled. With the development of SiC semiconductor manufacturing technology, the defects in SiC power chips will hopefully be controlled at such a low level that the cost of production may highly decrease.

GaN HEMT is always designed to be a horizontal structure. The special 2DEG with high carrier mobility characteristics makes GaN HEMT operate in the high-frequency application. However, the gate leakage issue is the dominant threat to device reliability. The hot electrons penetrate into the bulk of the AlGaN layer and even to the interface between AlGaN and GaN. In addition, the leakage along the surface also degrades the surface passivation layer and eventually causes surface flashover. Much effort has been paid to increase the reliability of the GaN HEMT, such as increasing the quality of the passivation layer by using highly reliable materials and decreasing the number of defects in the heterojunction. Compared to SiC MOSFET, GaN HEMT is less developed and the improvement of its reliability needs to be further explored.

### *5.2. Challenges to WBG Power Electronic Packaging*

The most critical threat to the reliability of WBG power electronic packaging is the fatigue appearing at high temperatures. The thermo-mechanical fatigue of packaging is usually caused by the CTE mismatch and happens to the solder, bond wire, and substrate. However, with the increase in working temperatures and voltages, the thermo-mechanical fatigue issue becomes more and more troublesome, and the electric discharge issue gradually appears. The reliability issue of high-temperature packaging is the main cause of WBG power electronic devices being unable to reach the theoretical working temperature limit. The requirement of high-temperature packaging makes researchers explore new materials, which can increase the reliability of WBG power electronic devices.

The common thermo-mechanical fatigue such as solder fatigue, bond wire lift-off, bond wire heel cracking, and substrate delamination have attracted enough attention and have been extensively researched. However, the degradation caused by electric discharge has not been entirely investigated. The most fragile position of the WBG device is the triple junction of the encapsulant, the edge of the substrate metal layer, and the ceramic beneath the metal layer. The partial discharge phenomenon always occurs at this position. Since the WBG power electronic devices are meant to be used in high-voltage and high-temperature situations, the electric discharge issue will be more and more prominent when the designed voltage and temperature for WBG power electronic devices are increased. Future research on electric discharge in WBG power electronic devices may focus on the online partial discharge monitoring method, using nanocomposites to increase the inception voltage of discharge, as well as the electrical degradation mechanism of packaging materials.

### *5.3. Developing Trends in Reliability Models*

After the proposal of physics-of-failure models, much research has been conducted to find accurate models predicting the remaining life of power electronic devices. TDDB models focus on the degradation of the gate dielectric, while the stress–strain models and the thermal cycling models focus on the fatigue of packaging. These models are based on failure mechanisms and require the engineers have a broad knowledge of material properties and the specific geometric information of the packaging. In recent years, data-driven approaches based on the condition monitoring technique and data processing

technology have gained much popularity. They do not require broad physical knowledge but identify the health condition by analysis of the measured data (parameters or variables). Moreover, with the development of AI techniques, such as artificial neural networks, genetic algorithms, and deep learning algorithms, these methods offer vast options for evaluating WBG power electronic device reliability. Data-driven methods have the advantage of correlating the monitored data with the health conditions of the power electronic devices, without the pre-knowledge of failure mechanisms. Therefore, it can be inferred that the data-driven methods will attract more attention.

## 6. Conclusions

With the popularity and application of WBG power electronic devices in high-voltage and high-temperature fields, the reliability issue of WBG devices will become more and more prominent. This paper presents a review of WBG reliability research, including the failure mechanisms of WBG power electronic chips, the reliability of WBG power electronic packaging, and the reliability models. Some key points are summarized as follows:

(1) SiC MOSFET and GaN HEMT are the most mature and widely used WBG power electronic devices. The gate dielectric degradation and gate leakage are dominant factors that affect the reliability of SiC MOSFET and GaN HEMT, respectively. With the future development of WBG semiconductor manufacturing technology, the quality of WBG power chips will hopefully be improved, resulting in a considerable decrease in the production cost.

(2) The main challenge for WBG power electronic device packaging is the high temperature and high voltage reliability. The thermo-mechanical fatigue and electric discharge are the common degradation mechanisms. The packaging materials should withstand high temperatures and wide-range temperature cycling. The coordination of mechanical, electrical, and thermal characteristics of packaging materials should be carefully considered and extensively investigated during the design process of WBG power electronic devices. Commercial WBG power electronic devices are limited to operate within 175 °C, which is far less than enough to exert the full potential of WBG power chips. The new development of materials and techniques for the bond wire, solder, substrate, and encapsulant makes it possible to produce reliable WBG power electronic packaging in the laboratory, but it is still a relatively long way to large-scale commercial use.

(3) The classic reliability models based on the physics-of-failure concentrate on the condition of the gate dielectric, thermo-mechanical effect, and stress–strain relation, whereas the data-driven methods based on the analysis of monitored data have gained much popularity because they do not need the pre-knowledge of failure mechanisms. With the development of condition monitoring methods and AI technology, new diagnostic methods, such as principal component analysis, k-nearest neighbor algorithm, and artificial neural network, will receive more attention and become the future research trend for WBG power electronic device reliability.

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