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Non-Isolated Interleaved Hybrid Boost Converter for Renewable Energy Applications

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Abstract: DC-DC boost converters are necessary to extract power from solar panels. The output voltage from these panels is far lower than the utility voltage levels. One of the main functions of the boost converter is to provide a considerable step-up gain to interface the panel to the utility lines. There are several techniques used to boost the low panel voltage. Some of the issues faced by these topologies are a high duty ratio operation, complex design with multiple active switches and discontinuous input current that affects the power drawn from the panel. This paper presents a boost converter topology that combines the advantages of an interleaved structure, a voltage lift capacitor and a passive voltage multiplier network. A mathematical analysis of the proposed converter during its various modes of operation is presented. A 100 W prototype of the proposed converter is designed and tested. The prototype is controlled by a PIC16F18455 microcontroller. The converter is capable of achieving a gain of 10 without operating at extremely high duty ratios. The voltage stress of the switch is far lower than the maximum output voltage.

Keywords: high gain; interleaved; DC-DC converter; renewable energy; voltage lift capacitor

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1. Introduction

There is a shift in energy consumption and generation trends globally. Many countries are moving away from fossil-fuel-based energy sources to renewable energy sources [1,2]. Of the various types of renewable energy sources available, solar energy is the solution of choice for the electrification of rural areas or remote areas with little access to grid power. That said, the deployment of solar photovoltaic (PV) systems is not without issues. The utility voltage levels are significantly higher than the raw output voltage of solar panels. Solar panels are further affected by the ambient temperature, level of solar irradiation and partial shading [3–7]. Therefore, a power electronic interface is mandatory to extract power from the PV panels.

Many converter technologies provide a solution to achieving a high gain. The most basic converter topology, the classic boost converter, provides an output voltage greater than its input voltage as a function of its duty cycle [8–10]. The output voltage of the classic boost converter is solely dependent on the duty cycle of operation, and the voltage stress on the switch is equal to the output voltage. The gain of the classic boost converter is given by $\frac{1}{1-D}$, where D is the duty cycle of the converter. If a gain of 10 is required, the converter needs to operate at a duty of 90%. This operation at an extreme duty ratio may lead to commutation issues at high frequencies. Therefore, there are practical limits on the gain that can be achieved through the classic boost converter. These limits make the classic boost converter not viable for operation at a high gain.

Transformer-based converters, also known as isolated converters, are discussed in [11–13]. The turns ratio of the transformer provides one more degree of design freedom in addition to the duty cycle. The leakage inductances result in additional undesired stored energy, which results in voltage spikes and requires snubbing circuits. In addition, transformer-based circuits are larger and heavier. In cases where isolation is not necessary, tapped-inductors, switched-inductors and switched-capacitor topologies can be used [14–22]. These topologies offer a higher gain by utilizing the energy stored in the switched element. However, similar to isolated topologies, these topologies have leakage inductance issues and current spike issues. Due to the limitations of large leakage inductances and parasitic capacitances, voltage multiplier-based topologies offer a viable alternative. Voltage multiplier-based topologies can offer the output gain in stages [23–25]. However, this increases input current fluctuation, increasing the size and losses as the number of multiplier stages increases. Cascaded converters, also known as quadratic converters, combine and utilize several converters in succession in order to obtain a high gain [26–28].

Converters that draw a continuous input current are beneficial for photovoltaic applications [29,30]. Interleaved boost converters (IBC) have multiple inputs that are phase displaced. This reduces the fluctuations in the current drawn from the source. Though a classic interleaved converter has the advantage of a continuous input current, the gain is identical to that of a classic boost converter [31–34].

Interleaved hybrid converters use an interleaved input structure in addition to another gain stage. This stage is usually a coupled inductor/switched capacitor network. Ref. [35] presents a type of interleaved converter that uses coupled input inductors. This converter provides a gain of $\frac{1}{1-(D_1+D_2)}$, where D_1 and D_2 are the duty cycles of each phase. Though this converter has an excellent current-sharing property, it does not address the issue of a high gain. Ref. [36] presents an interleaved hybrid boost converter with an asymmetric structure. This topology ensures reduced input current and output voltage ripples while providing a gain of $1 + \frac{1}{1-D}$, where D is the duty cycle of the operation. Ref. [37] uses a zero-voltage-switched (ZVS) network with an active clamping circuit. This converter has a gain of $\frac{2N+2}{1-D}$, where N is the turns ratio of coupling and D is the duty cycle of the converter. This converter offers an additional degree of design freedom in the form of an adjustable turns ratio. Ideally, the gain of the converter is 10 at a duty cycle of 60% when $N = 1$. However, the gain drops with an increase in the leakage inductance. Furthermore, this topology is complex because of the presence of the clamping switch, and increases in size as N increases.

This paper presents a non-isolated interleaved hybrid boost converter using the voltage-lift technique and a passive multiplier network. The input of the converter consists of a two-phase IBC. The output of both phases is combined by using a voltage lift capacitor. This is fed to a passive voltage multiplier cell consisting of two diodes and two capacitors. The output is filtered through an output diode and capacitor before being fed to the load. This converter offers a high gain at relatively low duty cycles, continuous input current and low peak overshoot. The details of the converter topology, its various modes of operation, an analysis of the proposed converter and the results of testing the prototype are discussed in the following sections.

1.1. Proposed Converter

Figure 1 shows the proposed interleaved hybrid boost converter. The converter can be viewed in two parts: the interleaved input stage and the passive voltage multiplier cell. L1 and L2 are the input inductors; together with switches Q1 and Q2, they form the two-phase interleaved input. The voltage lift capacitor C_{lift} clamps the output of one phase to the other through diode D1. The output of the interleaved input stage is fed to the passive voltage multiplier cell. Diodes D2 and D3 with capacitors C1 and C2 form the passive voltage multiplier network. Diode D_{out} and capacitor C_{out} deliver the output to the load.

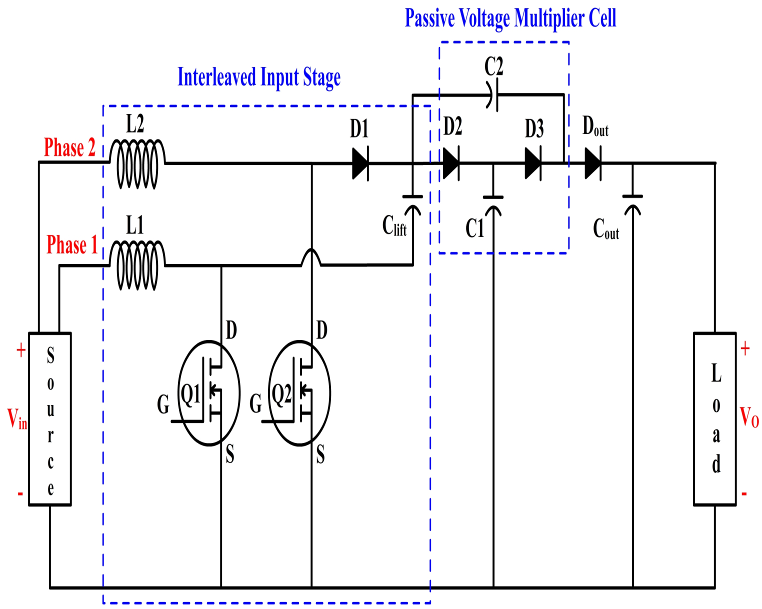

Figure 1. Proposed non-isolated interleaved hybrid boost converter.

1.2. Modes of Operation

The converter can be considered as two distinct stages working together to deliver a high gain. The interleaved input stage consists of the active elements that are controlled to vary the output voltage and the passive voltage multiplier cell that adds to the gain of the interleaved stage. Since there are two switches in the active stage, there are two possible scenarios during operation. The modes of operation during each of these scenarios are classified as: (i) Group 1: When duty is >50 %, an overlap occurs during which both switches are ON, and (ii) Group 2: When duty is <50 %, there is a duration during which both switches are OFF.

The operation of the interleaved stage without considering the passive voltage multiplier cell is explained as follows. Q1:G and Q2:G are the gate pulses given to switches Q1 and Q2. V_{in} is the input voltage. I_{L1} and I_{L2} are the currents through inductors L1 and L2. $V_{C_{lift}}$ is the voltage across C_{lift}. V_O is the output voltage. T is the period of one switching cycle. The characteristic waveforms of various elements are shown in Figure 2.

1.2.1. Group 1: Duty > 50%

Mode 1 (0 < t < t1): Switches Q1 and Q2 are ON. Diode D1 is OFF. Inductors L1 and L2 are charging, i.e., the currents I_{L1} and I_{L2} rise. Capacitor C_{lift} holds the voltage from the previous mode. The capacitor C_{out} supplies the load. The output voltage V_O reduces.

Mode 2 (t1 < t < t2): Switch Q1 is ON and Q2 is OFF. Diode D1 turns ON. Inductor L1 continues to charge, i.e., the current I_{L1} continues to rise. The input voltage and the energy stored in inductor L2 charge C_{lift} through D1. Current I_{L2} falls. Voltage $V_{C_{lift}}$ increases. Capacitor C_{out} continues to feed the load. The output voltage V_O continues to reduce.

Mode 3 (t2 < t < t3): Switch Q1 and Q2 are ON. Diode D1 is OFF. Similar to Mode 1, inductors L1 and L2 charge. The voltage lift capacitor C_{lift} holds the voltage from the previous mode. The capacitor C_{out} continues to feed the load. The output voltage V_O continues to reduce.

Mode 4 (t3 < t < T): Switch Q1 is OFF and Q2 is ON. This is the power delivery stage. The input voltage V_{in}, the energy stored in inductor L1 and the voltage across the voltage lift capacitor $V_{C_{lift}}$ discharge into the output capacitor C_{out}. Inductor L2 charges. The voltage across C_{lift} decreases. The output voltage V_O increases.

1.2.2. Group 2: Duty < 50%

Mode 1 (0 < t < t1): Switch Q1 is ON and Q2 is OFF. Diode D1 is ON. Inductor L1 charges, i.e., current I_{L1} increases. During this time, the inductor L2 and capacitor C_{lift} charge through the switch Q1. The capacitor C_{out} supplies the load. The output voltage V_O reduces.

Mode 2 (t1 < t < t2): Switch Q1 and Q2 are both OFF. Diode D1 is ON. Inductors L1 and L2 begin discharging. The voltage lift capacitor C_{lift} discharges. The output voltage V_O increases.

Mode 3 (t2 < t < t3): Switch Q1 is OFF and Q2 is ON. Diode D1 is OFF. Inductor L1 and the voltage lift capacitor C_{lift} continue to discharge. Inductor L2 charges. The output voltage V_O reduces.

Mode 4 (t3 < t < T): Switch Q1 and Q2 are OFF. Diode D1 is ON. Inductor L1 continues to discharge. Inductor L2 starts to discharge. The voltage lift capacitor C_{lift} discharges. The output voltage V_O increases.

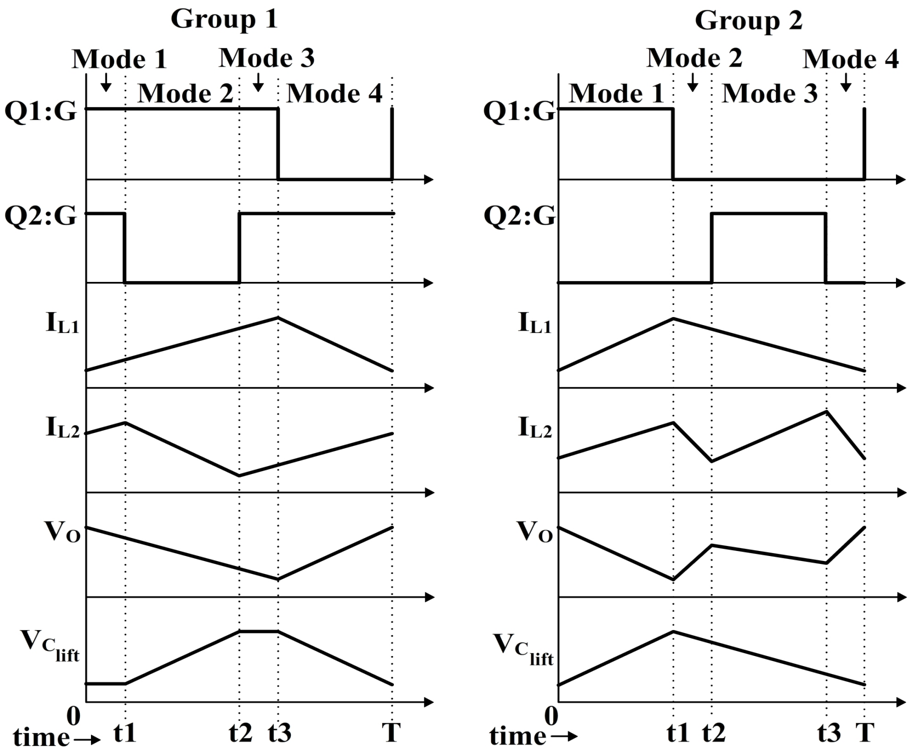

Figure 2. Characteristic waveforms during operation.

2. Analysis

The analysis is carried out on the various operating modes explained in the previous section. The average energy stored in the capacitor or inductor over one switching operation is zero. The expression for the average energy stored in an inductor is $\frac{1}{T}\int_0^T V_L(t)dt$ and $\frac{1}{C}\int_0^T i_C(t)dt$. By applying this to the energy storage elements in the circuit, we can derive the relation for the gain of the converter. The voltage lift capacitor serves the function of adding the voltage output of the interleaved input in series [25]. The voltage lift capacitor is charged by the operation of Q2; therefore, the average voltage across C_{lift} is

$$V_{C_{lift}} = \frac{V_{in}}{1-D} \tag{1}$$

where D is the duty ratio given by $D = \frac{T_{ON}}{T}$.

2.1. Analysis of Group 1 Operation

Consider inductor L1. The total duration for which switch Q1 is ON is T_{ON} and the duration for which it is OFF is T_{OFF}.

When Q1 is ON:

$$V_{L1} = V_{in} \tag{2}$$

When Q1 is OFF:

$$V_{L1} = -(V_O - V_{in} - V_{C_{lift}}) \tag{3}$$

Applying volt-second balance to inductor L1,

$$V_{in} \times T_{\text{ON}} - (V_O - V_{in} - V_{C_{lift}}) \times T_{\text{OFF}} = 0 \tag{4}$$

Simplifying and substituting for D,

$$V_{in} \times D - (V_O - V_{in} - V_{C_{lift}}) \times (1 - D) = 0 \tag{5}$$

$$V_{in} \times D - (V_O - V_{in} - V_{C_{lift}} - V_O \times D + V_{in} \times D + V_{C_{lift}} \times D = 0 \tag{6}$$

$$-V_O + V_{in} + V_{C_{lift}} + V_O \times D - V_{C_{lift}} \times D = 0 \tag{7}$$

$$V_O - V_O \times D = V_{in} + V_{C_{lift}} - V_{C_{lift}} \times D \tag{8}$$

$$V_O \times (1 - D) = V_{in} + V_{C_{lift}} \times (1 - D) \tag{9}$$

$$\frac{V_O}{V_{in}} = \frac{1}{1 - D} + \frac{V_{C_{lift}}}{V_{in}} \tag{10}$$

Substituting Equation (1),

$$\frac{V_O}{V_{in}} = \frac{2}{1 - D} \tag{11}$$

2.2. Analysis of Group 2 Operation

Consider the voltage lift capacitor (current direction from top to bottom is considered positive). I_O is the output current.

From time *t* = *0* to *t1*:

$$I_{C_{lift}} = I_{L2} \tag{12}$$

From time *t* = *t1* to *t2*:

$$I_{C_{lift}} + I_{L2} = I_O + I_{C_{out}} \tag{13}$$

$$I_{C_{lift}} = -I_{L1} \tag{14}$$

From time *t* = *t2* to *t3*:

$$I_{C_{lift}} = -I_{L1} \tag{15}$$

$$I_{C_{lift}} = I_O + I_{C_{out}} \tag{16}$$

From time *t* = *t3* to *T*:

$$I_{C_{lift}} + I_{L2} = I_O + I_{C_{out}} \tag{17}$$

$$I_{C_{lift}} = -I_{L1} \tag{18}$$

Averaging the current through C_{lift}:

$$\frac{1}{C_{lift}}[(I_{L2})_0^{t1} - (I_{L1})_{t1}^{t2} - (I_{L1})_{t2}^{t3} - (I_{L1})_{t3}^{T}] = 0 \tag{19}$$

$$\frac{1}{C_{lift}}[(I_{L2})(t1 - 0) - (I_{L1})(t2 - t1) - (I_{L1})(t3 - t2) - (I_{L1})(T - t3)] = 0 \tag{20}$$

$$I_{L2} \times t1 - I_{L1}[(t2 - t1) + (t3 - t2) + (T - t3)] = 0 \tag{21}$$

$$I_{L2} \times t1 - I_{L1}(T - t1) = 0 \tag{22}$$

Simplifying and expressing $\frac{t1}{T}$ as D,

$$I_{L2} \times D = I_{L1}(1 - D) \tag{23}$$

Similarly, averaging the current through C_{out},

$$\frac{1}{C_{lift}}[(-I_O)_0^{t1} + (I_{L1} + I_{L2} - I_O)_{t1}^{t2} + (I_{L1} - I_O)_{t2}^{t3} + (I_{L1} + I_{L2} - I_O)_{t3}^{T}] = 0 \tag{24}$$

$$-I_O \times t1 + (I_{L1} + I_{L2} - I_O)(t2 - t1 + T - t3) + (I_{L1} - I_O)(t3 - t2) = 0 \tag{25}$$

Simplifying,

$$I_{L1}(T - t1) + I_{L2}(T - t1 + t2 - t3) - I_O T = 0 \tag{26}$$

$$I_{L1}(T - t1) + I_{L2}(T - t1 - (t3 - t2)) - I_O T = 0 \tag{27}$$

Since the gate pulses to each switch are identical, the duration *t1* is equal to the duration ($t3 - t2$). Applying this to the above equation and simplifying,

$$I_{L1}(1 - D) + I_{L2}(1 - D - D) - I_O = 0 \tag{28}$$

$$I_{L1}(1 - D) + I_{L2}(1 - 2D) - I_O = 0 \tag{29}$$

From Equation (23),

$$I_{L1} = \frac{I_{L2} \times D}{1 - D} \tag{30}$$

$$I_{L2}D + I_{L2} - 2D \times I_{L2} - I_O = 0 \tag{31}$$

$$I_{L2} - I_{L2} \times D - I_O = 0 \tag{32}$$

$$I_{L2}(1 - D) = I_O \tag{33}$$

$$I_{L2} = \frac{I_O}{(1 - D)} \tag{34}$$

The input current to the converter can be expressed as

$$I_{in} = I_{L1} + I_{L2} \tag{35}$$

$$I_{in} = \frac{I_{L2} \times D}{(1 - D)} + I_{L2} \tag{36}$$

$$I_{in} = \frac{I_O \times D}{(1 - D)^2} + \frac{I_O}{(1 - D)} \tag{37}$$

$$\frac{I_{in}}{I_O} = \frac{D}{(1 - D)^2} + \frac{1}{(1 - D)} \tag{38}$$

The input–output voltage ratios of the current and voltage are related as

$$\frac{V_O}{V_{in}} = \frac{I_{in}}{I_O} \tag{39}$$

The group 2 gain is given by

$$\frac{V_O}{V_{in}} = \frac{D}{(1 - D)^2} + \frac{1}{(1 - D)} \tag{40}$$

Adding the effect of the voltage multiplier cell increases the gain additionally by $\frac{N}{1-D}$, where N is the number of voltage multiplier cells [23]. Applying this to Equations (11) and (40), we obtain the overall gain during group 1 operation,

$$\frac{V_O}{V_{in}} = \frac{2}{1-D} + \frac{N}{1-D} \tag{41}$$

and overall gain during group 2 operation,

$$\frac{V_O}{V_{in}} = \frac{D}{(1-D)^2} + \frac{1}{1-D} + \frac{N}{1-D} \tag{42}$$

The plot of Equations (41) and (42) is shown in Figure 3.

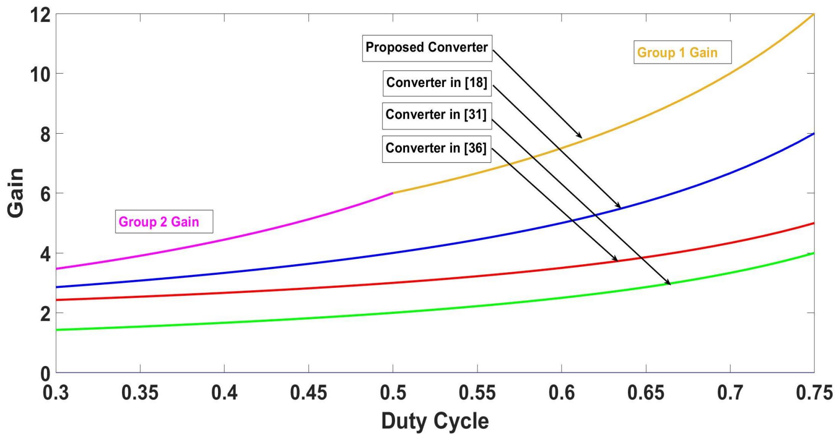

Figure 3. A comparison of gain vs. duty cycle.

3. Converter Design

To prove the validity of the converter, a 280 V/100 W hardware model was built and tested. The prototype uses one passive voltage multiplier cell. This number may be increased as per the requirement of the gain. A closed-loop PI control is implemented using a Microchip PIC16F18455. The controller maintains the set value of the output voltage. The output of the converter is sensed using a LEM LV25-P voltage transducer. The prototype of the converter is shown in Figure 4. The flowchart of the algorithm used to control the prototype is shown in Figure 5. The details of the various elements of the prototype are shown in Table 1.

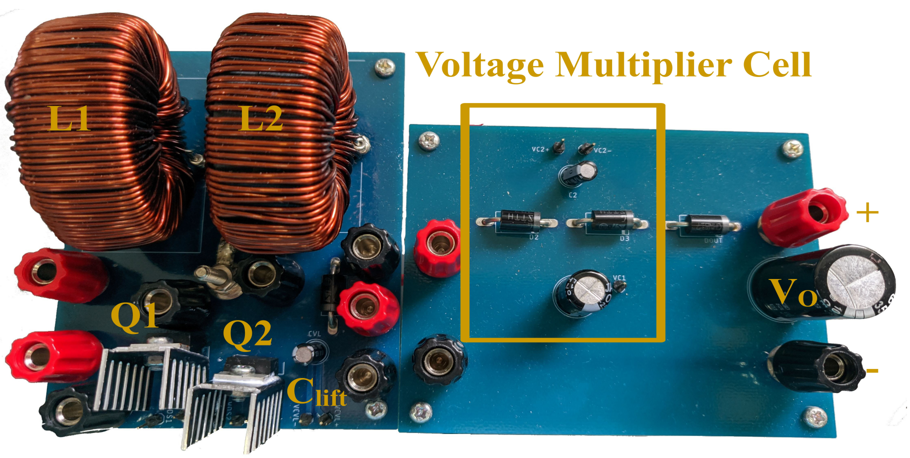

Figure 4. Hardware prototype of the proposed converter.

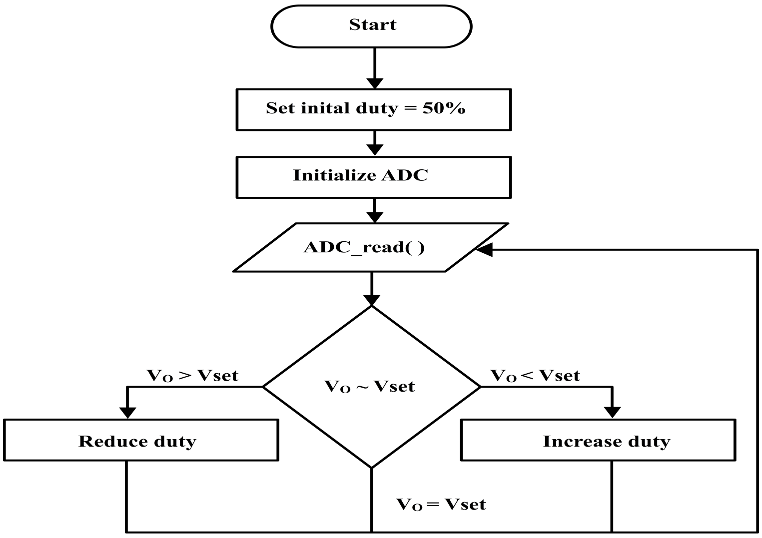

Figure 5. Flowchart of the closed-loop PI control scheme.

Table 1. Prototype details.

Parameter	Value/Description
$L1$	500 µH
$L2$	500 µH
C_{lift}	10 µF/100 V
C1	10 µF/100 V
C2	10 µF/200 V
C_{out}	68 µF/350 V
Switches $Q1$ and $Q2$	FDP2552
Diodes	STTH302
Voltage Sensor	LV25-P
Controller	Microchip PIC16F18455
MOSFET Drivers	TLP250
Switching Frequency	20 kHz

4. Results

The proposed converter was simulated in PSIM and the 280 V/100 W prototype was tested. It can be seen that the simulated results closely match the results shown by the prototype. Figures 6 and 7 show the output voltage of the converter at start-up. It is seen that the prototype reaches its steady-state output within 400 ms. The peak overshoot is less than 10 V greater than the steady-state voltage of 280 V. Figures 8 and 9 show the input and output voltage waveforms. It is seen that the input varies between 28 V and 44 V, whereas the output maintains a steady voltage of 280 V. This proves the voltage gain capability of the converter, as explained in Equations (41) and (42). Figures 10 and 11 show the input voltage, output voltage and output current of the prototype. It is seen that the converter delivers 103.42 W at 280.5 V. Figures 12 and 13 show the input voltage, input current and output voltage of the proposed converter. It can be seen that the input current is continuous and that the prototype draws 114.64 W of power. The efficiency is calculated to be 90.21% without soft-switching. Figures 14 and 15 show the gate pulse and switch stresses of switch Q1. Figures 16 and 17 show the gate pulse and switch stresses of switch Q2. The duty cycle of the converter is approximately 62%. Switch Q1 has a drain-source voltage of 131.5 V peak and 100 V average during its off-state, whereas switch Q2 has a drain-source voltage of 174 V peak and 100 V average during its off-state. These values are far less than the output voltage of 280 V. It is seen that the proposed converter achieves the above results without using bulky magnetic components or operating at an extreme duty ratio.

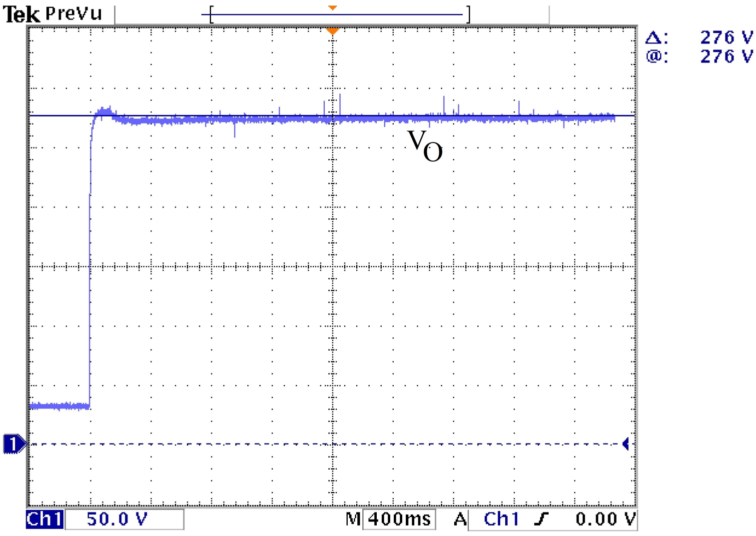

Figure 6. Output voltage vs. time.

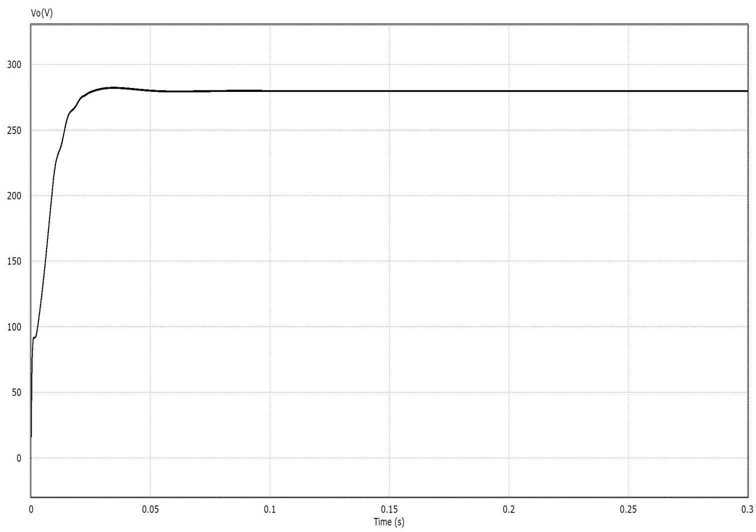

Figure 7. PSIM simulation of output voltage vs. time.

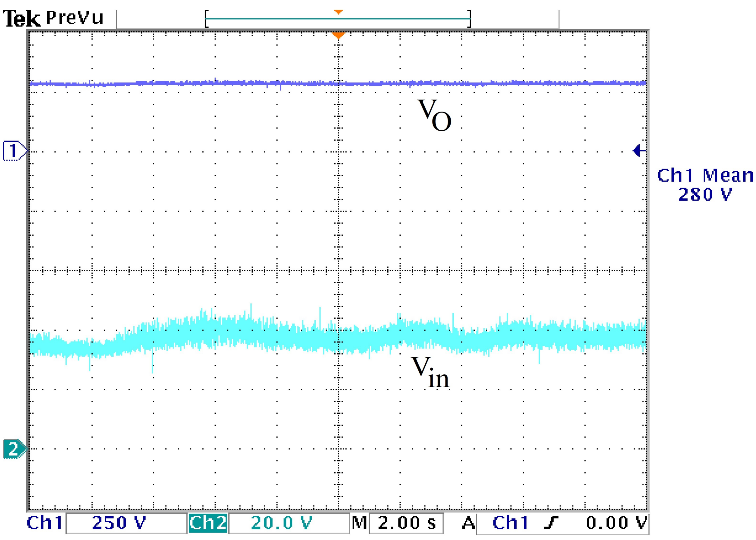

Figure 8. Input voltage and output voltage.

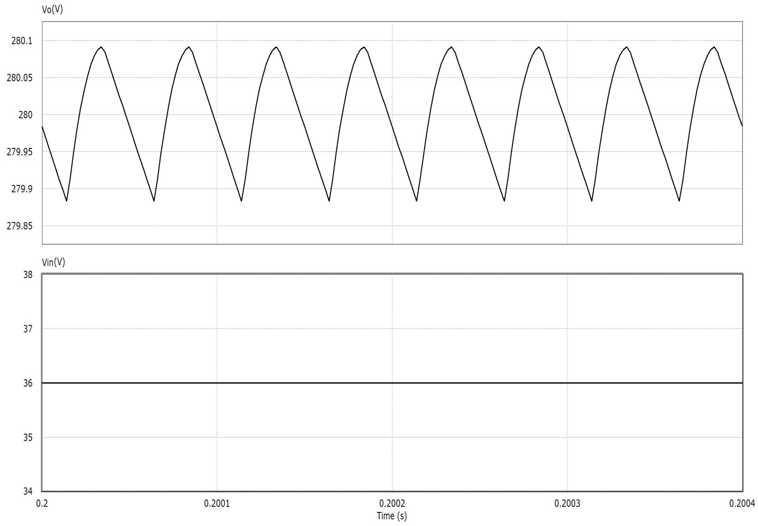

Figure 9. PSIM simulation of input and output voltages.

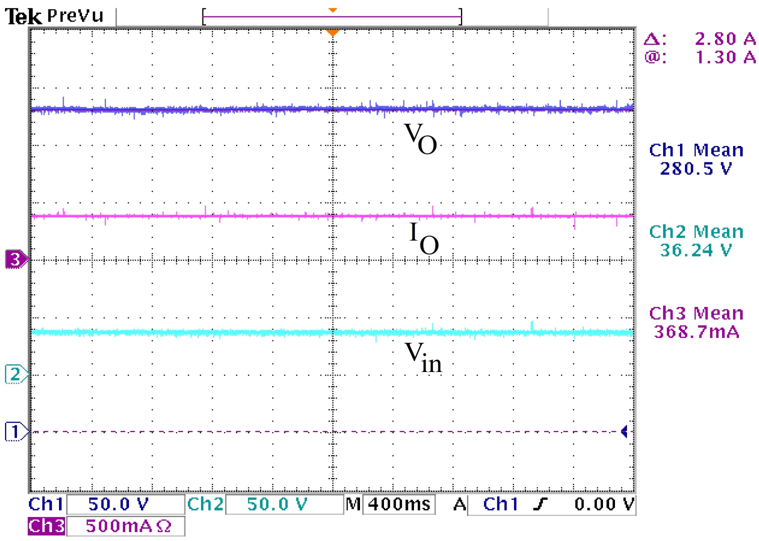

Figure 10. Input voltage, output voltage and output current.

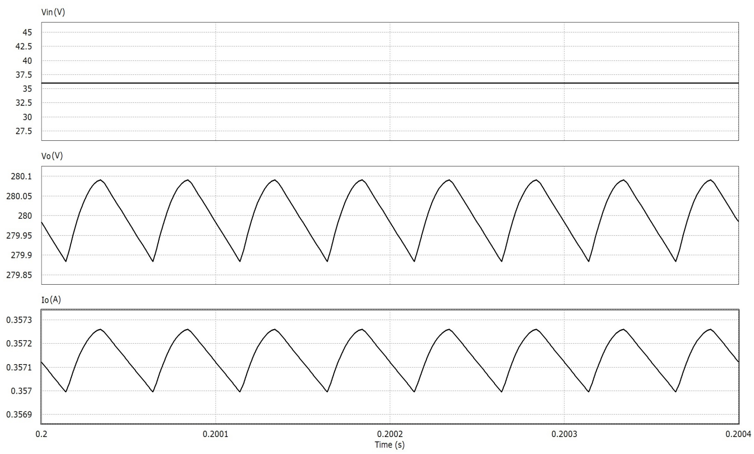

Figure 11. PSIM simulation of input voltage, output voltage and output current.

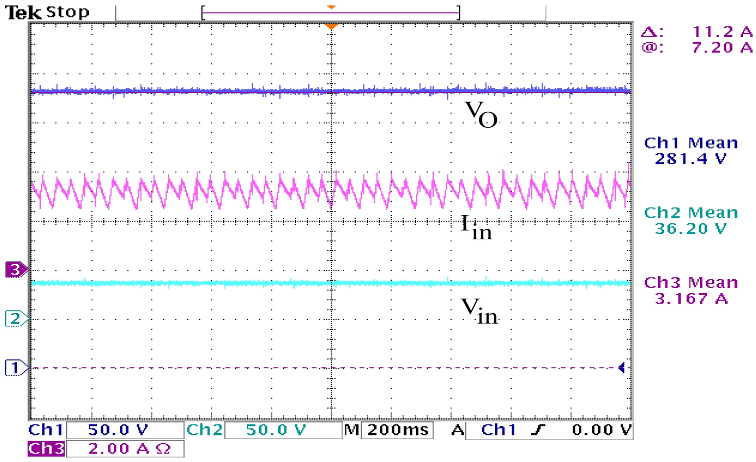

Figure 12. Input voltage, input current and output voltage.

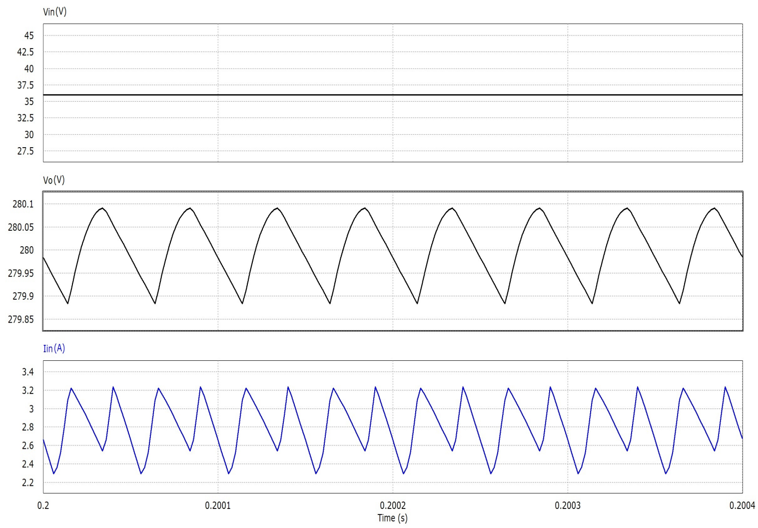

Figure 13. PSIM simulation of input voltage, input current and output voltage.

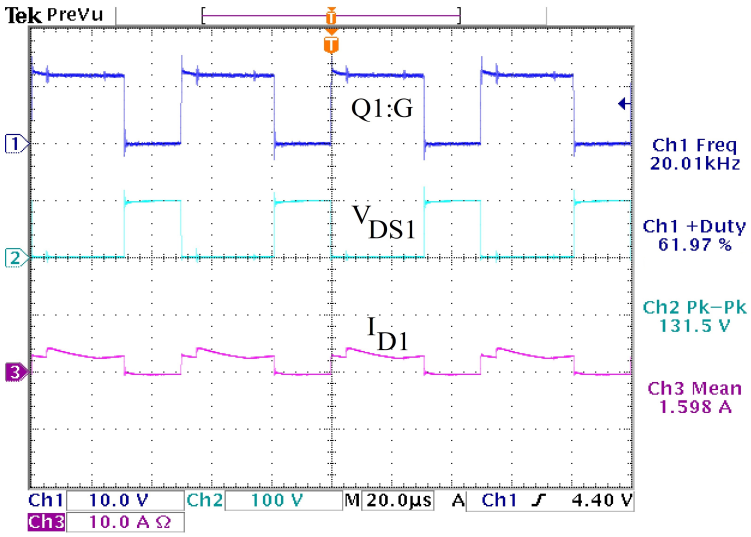

Figure 14. Switch stresses of Q1.

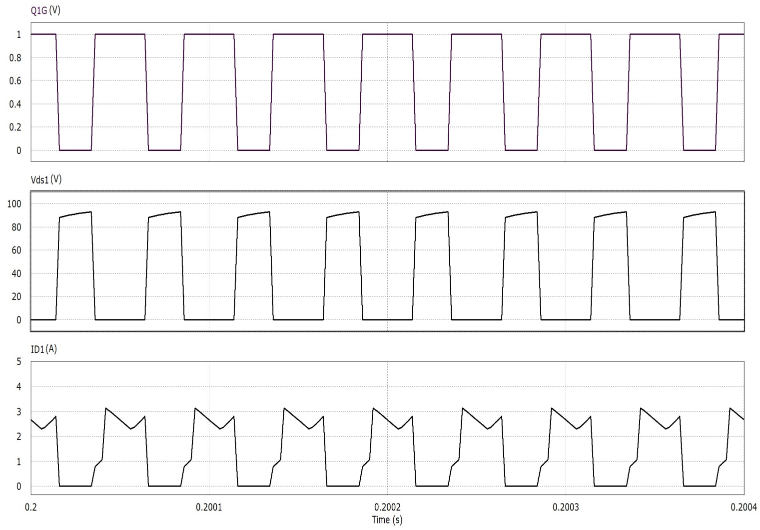

Figure 15. PSIM simulation of switch stresses of Q1.

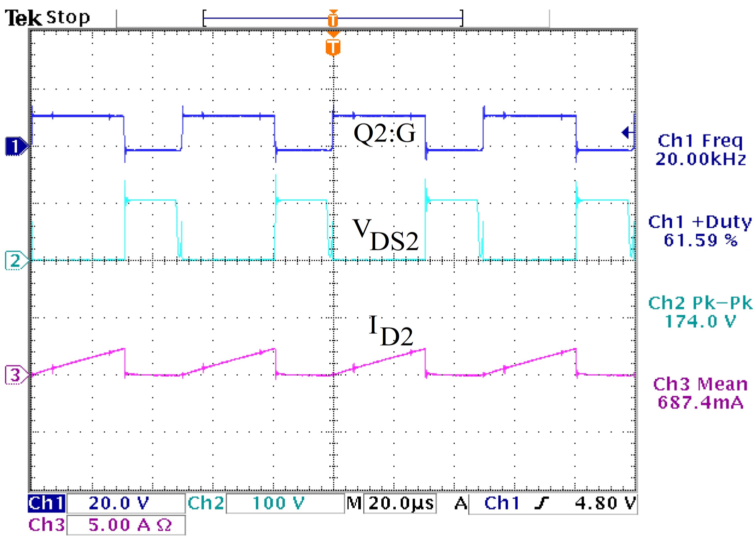

Figure 16. Switch stresses of Q2.

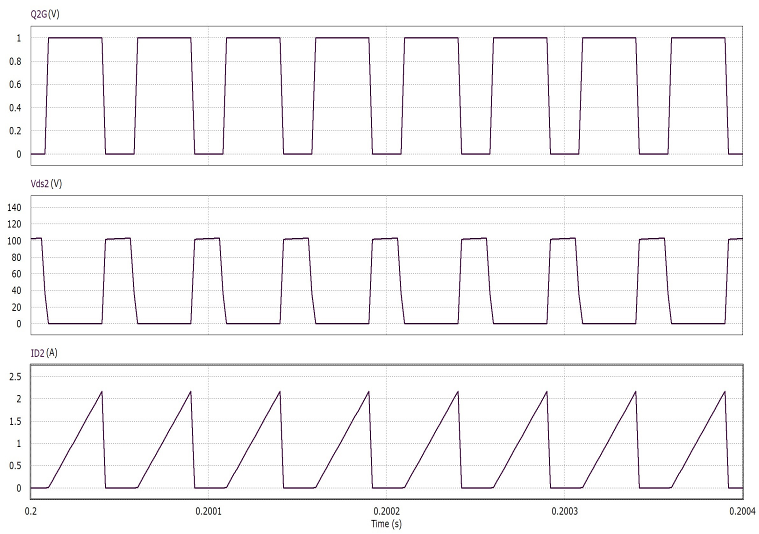

Figure 17. PSIM simulation of switch stresses of Q2.

5. Conclusions

A non-isolated interleaved hybrid boost converter for renewable energy applications is presented. The presented topology uses a two-phase interleaved input stage with a voltage lift capacitor connected to a passive voltage multiplier network. An extensive analysis of the various states of the converter operation is presented and verified. A 280 V/100 W prototype of the proposed converter is built and tested. The gain of the converter is compared to other topologies presented in the references, and it can be seen that the presented converter has a higher gain. For a varying input, the proposed converter provides a steady gain of 10 at the designed power of 100 W, with an efficiency of 90.21% without soft-switching. The advantages of the converter are a high gain without using additional magnetic elements and a continuous input current.

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