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A Transformerless AC-AC Converter with Improved Power Quality Employed to Step-Down Power Frequency at Output

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Abstract: Variable voltage and frequency are required to govern the torque-speed characteristics of many industrial drive systems. Traditionally, this is achieved with a power converting system implemented with multistage converters. This technology is based on rectifying AC power into DC and then DC into AC with an inverter circuit. The power quality concerns of both conversion stages are tackled by selecting high switching frequency PWM control and harmonics mitigation filters. Also, using a bulky DC-link capacitor is one of the big sources of low system reliability, so this approach increases the conversion losses, circuit, and control complications. The frequency step-down conversion is very attractive with direct AC-AC converters as it has a simple control and circuit structure, but these converters face poor power quality challenges once the output frequency is decreased with respect to an input. In these converters, the total harmonic distortion (THD) of the output voltage becomes very poor once the output frequency is reduced. The problem of high THD of the output is addressed in the power converting circuits implemented with line frequency multi-winding transformers. The required number of output winding and switching devices (diodes and thyristors) increases once the value of the output frequency is decreased. This will increase the overall volume, cost, and losses. The use of a bulky and costly line frequency transformer may be eliminated if AC voltage controllers have non-inverted and inverted voltage buck capabilities, such existing topologies either have complex control schemes or require a large number of operating devices. Therefore, in this research article, a new transformerless frequency step-down converter employing fewer devices is proposed. This approach is realized with a high-frequency controlled rectifier for the required voltage stabilization and a low-frequency inverter bridge for frequency control. Its validation is supported by the results attained from Simulink and practical-based prototypes.

Keywords: DC-link capacitor; diodes and thyristors; multistage converters; multi-winding transformer; total harmonic distortion; variable voltage and frequency

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1. Introduction

The electric power supplied by the utility grid to an end-user has a constant voltage (rms value) and frequency. This power characteristic cannot be directly employed for specific loads such as electric traction systems, induction heating processes, and variable speed industrial drive systems [1–4]. In these applications, controlling the voltage and frequency is a compulsory requirement. The conventional way for achieving this is an indirect conversion of electrical power based on rectification of AC into DC by employing voltage-controlled or uncontrolled approaches and inverters to obtain regulated AC from

DC power [5–7]. With an uncontrolled rectification scheme, the voltage of the DC-link capacitor may be made controllable by employing DC-to-DC voltage regulating systems [8]. This approach has however several limitations, including high circuit volume, losses, and cost. These issues may be resolved with the other approach for regulating a DC-link capacitor that includes a controlled rectifier circuit, but this scheme is the main source of the harmonics injection in the input supply system. Complicated filtering schemes must be implemented to eliminate the dominant harmonics [9]. A high-frequency inverter with various control schemes provides the high-quality controllable AC voltage and frequency required by the loads. The power quality of this stage is also maintained at an acceptable range with the help of harmonic suppression filters. This power conversion method is complicated and is not favorable as its implantation requires a multilevel conversion process [10–12].

The control of voltage and frequency in a single-level conversion approach is attractive as it is simple to implement with a small size and reduces the cost. Here the control of output voltage is achieved by adjusting the input voltage with the proper on and off operation of the semiconductor devices. Most of the traditional commercially developed AC-AC frequency regulators used in electric traction systems [13], rolling and grinding processes [14] are based on the thyristors or Triac switching operation. The turn-off process of these devices is obtained through the line commutation approach. Although these power converters have high power capabilities, in this process, dominant generated harmonics are low-frequency, as reported in [15]. The conversion losses of thyristors-based operating topologies are high as they have high internal resistance and voltage. These schemes are mostly employed to reduce the input or grid frequency at the output.

The stabilization of the frequency at the output may also be attained with the high-frequency operation of the semiconductor devices. This target is achieved using PWM control that may invert or non-invert the input with voltage regulation features. Such schemes have two categories, in which one requires the use of the z-source configuration, and the other one is employed without this structure. The first approach is very inefficient and undesirable as its implementation needs a large number of devices and components [16]. This makes it challenging to control the dynamic behavior as this sort of system has high order. High cost and large size are the other aspects of this system. Non-z-source power converting approaches are gaining more attention nowadays as they have no such issues [17–19]. These techniques are further classified as frequency regulation with and without voltage regulation features [20–22]. The frequency stabilization schemes stated in [19] have voltage regulation features, but their control strategies are non-identical to obtain the non-inverted and inverted forms of the input voltage at the output. The control schemes stated in [23] introduce a new circuit to ensure the symmetric nature of the control process, but their employment needs the use of a high number of switching devices. In the second approach, a power converter that only facilitates frequency stabilization (high or low) has easy and simple control approaches. Also, their implementation needs fewer electronic devices and components, but their output power quality is low, especially once the output frequency is almost one-third or one-fourth of the input frequency [24]. The total harmonic distortion (THD) of such output voltage waveforms becomes more worsen than a square waveform of the output voltage that is approximately 48%. A new approach is developed in [25] shown in Figure 1 to address and tackle such issues. This circuit facilitates to attain the output pulses with the peak of $\pm V_m/2$ and $\pm V_m$ but this solution requires the use of a line frequency multi-winding transformer to change the instantaneous values of the selected output pulses. In any operating interval, one thyristor and one diode turn on to obtain the required form of the output. Their low-frequency on and off behavior is the main source of high conduction losses. The level in the output voltage is proportional to the number of winding and semiconductor devices. The application of a line frequency transformer with multi-winding is the main source of high volume, losses, and cost. The number of operating devices and their gate controller increases as the output voltage level is required to be increased.

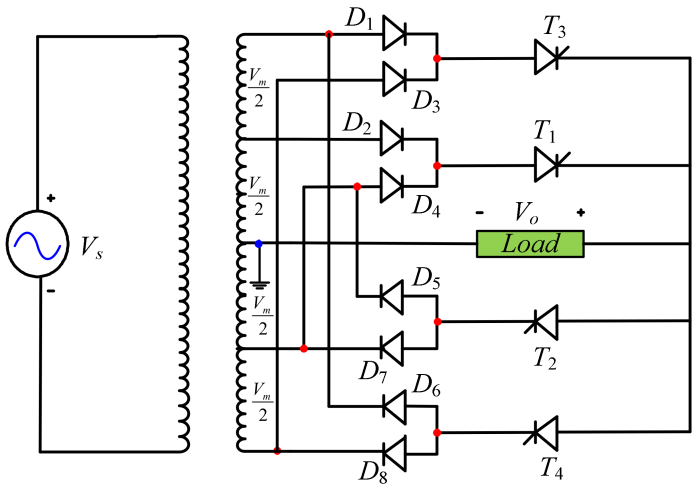


Figure 1. Frequency converter established in [25].

This research article introduces a new direct frequency regulator by eliminating the use of the line frequency transformer with a fixed number of semiconductor devices. The various levels in the output pulses are ensured with the help of the voltage control process obtained from the PWM control of operating transistors. The required voltage level is based on the analysis of the generated harmonics. This solution reduces the overall circuit's volume, losses, and cost.

This research article is organized by introducing the developed configuration and its operation in Section 2. Section 3 explores the power quality analysis of the various forms of the output voltage. Its performances are investigated and compared in Section 4. The experimental and simulation results are described in Section 5. Section 6 addresses the conclusions of the work.

2. Developed Circuit and Operation

The created circuit capable of governing the output frequency and voltage is shown in Figure 2. This circuit is obtained by adding two more high switching transistors to the converter we developed in [22].

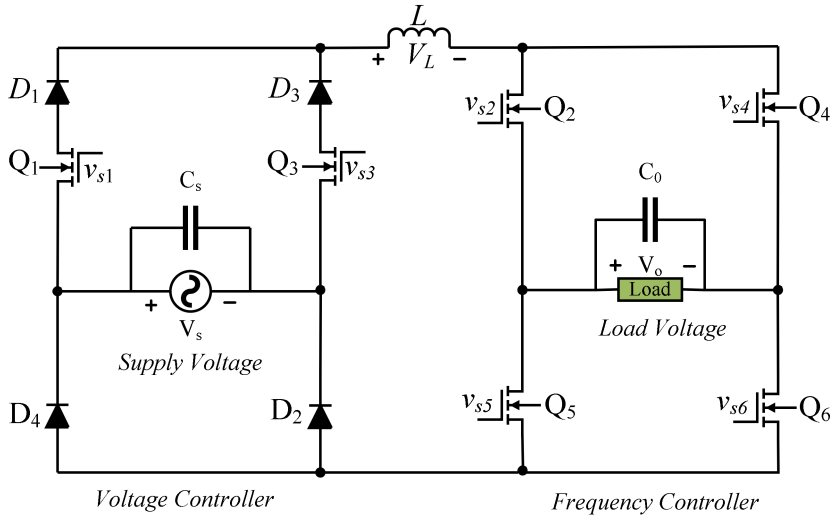


Figure 2. Created circuit's arrangement.

Six transistors and four diodes are used as switching devices along with one filtering inductor and two capacitors in its construction. This circuit can regulate the load voltage and frequency in a separate control. The voltage control circuit is responsible for governing the instantaneous or peak value of the selected output pulses by employing PWM control. The power quality criterion of output is maintained at the required level by selecting the appropriate switching frequency once the voltage regulation is needed. Otherwise, all the semiconductor elements operate at low grid frequency.

The voltage controller circuit (constructed with transistors Q_1, Q_3 and diodes D_1 to D_4) regulates the selected pulses. It converts the regulated and non-regulated voltage pulses into their absolute form. For this purpose, the transistors Q_1 and Q_3 operate with PWM control once voltage regulation is desirable otherwise their role is to operate at low grid frequency for positive and negative input, respectively. The expected values of the output of the voltage controller (input of the frequency controller) for the use in which the load frequency is one-third the frequency of the input voltage are described in Figure 3a. This is plotted by ignoring its ripple content as it has to be filtered out by the output capacitor C_o. According to PWM control signals (v_{s1}, v_{s3}) of Figure 4a, the transistor Q_1 turns on and off at high-frequency and transistor Q_3 retains its on-state for the first half period of the output voltage. The transistor Q_1 cannot transfer power for negative input as with this polarity of the source voltage, the operating state of the diode D_1 is non-conducting. The turning-on state of transistor Q_3 facilitates the continuous flow of the inductor current and power transfer as diode D_3 starts conduction once the diode D_1 becomes reverse bias or transistor Q_1 turns off. Similarly, for the period in which output voltage has a negative value, the role of transistor Q_1 and Q_3 is reversed. Now the high-frequency switching of the transistor Q_3 is responsible for storing the power to the inductor during its turn-on interval and is transferred to load in its turn-off period as diode D_1 becomes forward biased. The diode D_3 is switched to its off state once the input voltage is positive or the transistor Q_3 turns off.

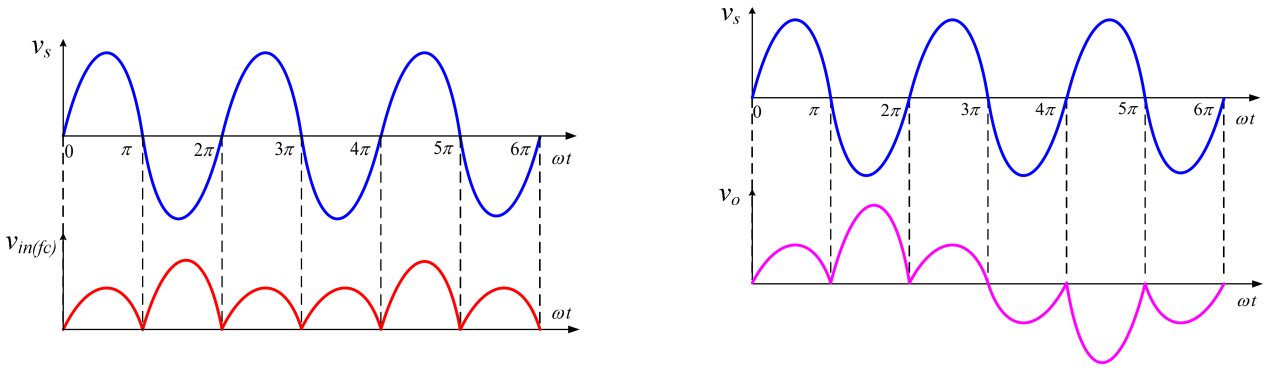


Figure 3. Expected outputs of (**a**) absolute value voltage controller and (**b**) frequency controller.

The role of the frequency control circuit (constructed with transistors Q_2, Q_4, Q_5, and Q_6) is to arrange the absolute value pulses generated by the voltage controller into its non-inverted and inverted form according to the desired output frequency. As an example in which the required output frequency is three times lower than the constant grid frequency, the frequency controller organizes the three pulses in non-inverted form and the next three pulses in inverted form as described in Figure 3b. This action increases the output voltage period three times with respect to the grid's voltage period. The power quality index of the output voltage is improved by regulating the magnitude of the first and third pulses from the positive pulses and fourth and sixth pulses from the negative pulses of output voltage. A similar approach may be tested for other output frequency requirements.

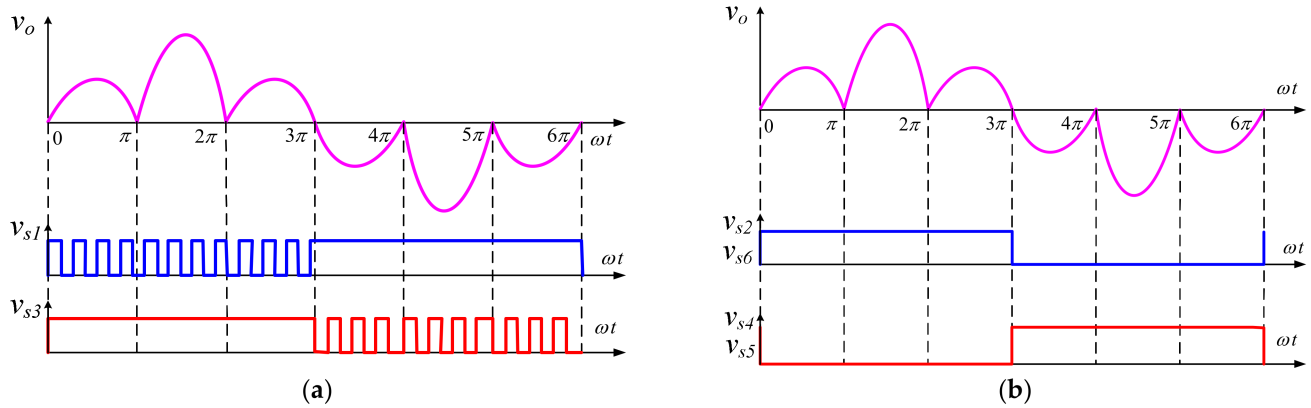


Figure 4. Control inputs applied to switching transistors of (**a**) absolute value voltage controller circuit and (**b**) frequency controller circuit.

The operation of the developed circuit is supported with the generated control outputs of Figure 4a,b illustrating how voltage and frequency control is achieved.

The plotted control signals of Figure 4a highlight the voltage control achieved by employing the PWM strategy. This control facilitates the governing of the maximum value of the selected output pulse from zero to the maximum input voltage level. The PWM behavior of the transistor Q_1 and Q_3 is responsible for governing the desired instantaneous voltage during the positive and negative half cycles of the load voltage. The frequency converter is responsible for output frequency control; this task is attained by arranging the voltage pulses obtained from the voltage controller as viewed from Figure 3a into their non-inverted and inverted forms. The instantaneous load voltage is in-phase with the instantaneous voltage pulses at its input terminal once the transistor Q_2 and Q_6 operate in conducting states. The turning on the transistors Q_4 and Q_5 transform positive pulse into negative pulses. The control inputs of Figure 4b are employed to obtain the required output of Figure 3b. The further detail of how the controllable output can be produced is described and highlighted from the power flow loops of Figures 5 and 6.

2.1. Operation as an Absolute Value Voltage Controller

It has already been stated that output frequency conversion is linked with the operation of transistors Q_2, Q_6 and Q_4, Q_5 to non-invert and invert the voltage available at the input terminals of the frequency controller bridge. The regulated and non-regulated voltage operations depend on the high-frequency switching of the transistors Q_1 and Q_3. They can regulate the voltage once their operation is controlled in a PWM manner; otherwise, their conduction facilitates the power transfer path from input to output.

The transistor Q_1 always operates in voltage control mode or non-voltage control mode only if the input is positive, as it is shown in part 'a' of Figures 5 and 6. In voltage control mode, it turns on and turns off at high-frequency to store and transfer the power in the inductor as described in Figure 5a,b and Figure 6a,b. In part 'a' of these figures, the power is stored in the inductor (L), and in (b), the stored power is released to load. In this operating mode, the operation of the transistors Q_1 and Q_3 is complementary, and the role of transistor Q_3 is to establish the power transfer path once the transistor Q_1 changes it state from on to off. In non-regulated voltage modes, the transistor Q_1 only conducts during the positive half cycle of the input voltage as described in power transferring loops in part 'a' of Figures 5 and 6.

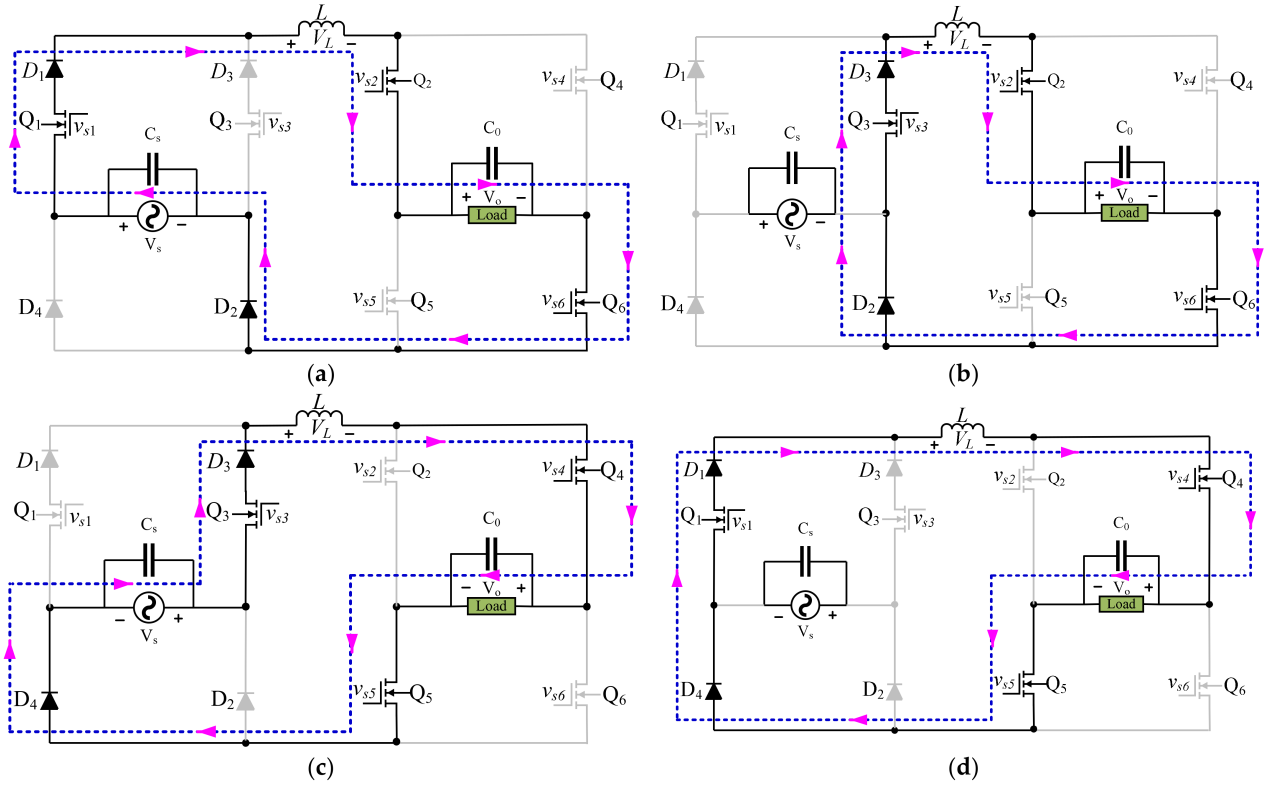


Figure 5. Power transferring loops to obtain the non-inverted form at the output with (**a**,**b**) positive input value; (**c**,**d**) negative input value.

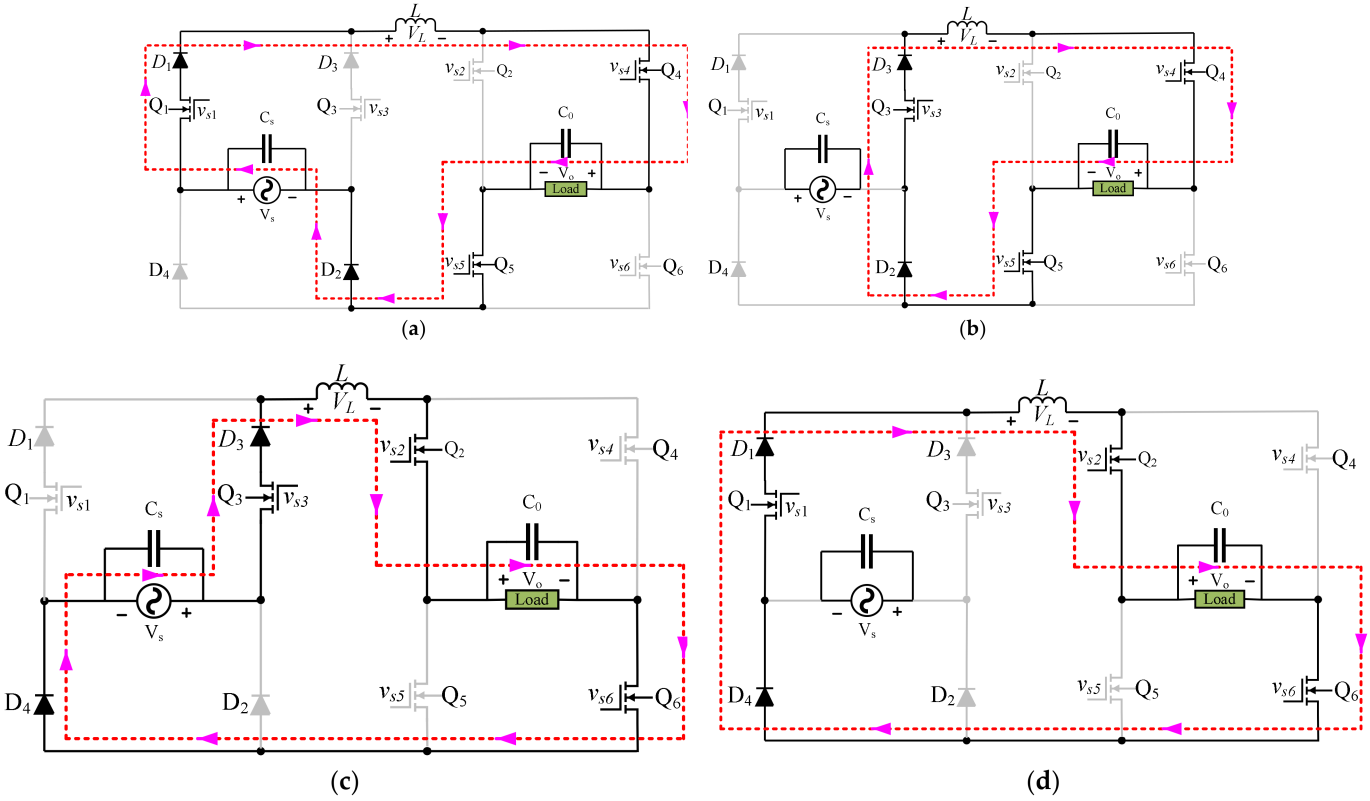


Figure 6. Power transferring loops to obtain the inverted form at the output for (**a**,**b**) positive input value; (**c**,**d**) negative input value.

During the negative half of the line voltage, the voltage regulated and non-regulated capabilities are governed through the operation of transistor Q_3. It operates at a high frequency to ensure the voltage control facility by storing the power in the inductor and here the conduction of transistor Q_1 helps to release that stored power as described in part 'c' and 'd' of Figures 5 and 6. In non-regulated voltage mode, as there is no need to store the power in the inductor, only the low-frequency operation of transistor Q_3 completes this task, and it can be viewed from the power transferring loops as described in part 'c' of Figures 5 and 6.

2.2. Operation as a Frequency Controller

The non-inverted and inverted forms of the output voltage are obtained with the switching of the transistors employed in the frequency controller circuit. There is no change in the operating behavior of the operating transistors employed in the absolute value voltage controller circuit as their role is only to convert the voltage regulated and non-regulated pulses of the input into their absolute form. The control inputs v_{s2} and v_{s6} generate the positive output as viewed by highlighted loops of Figure 5a–d for positive and negative input, respectively. Inverted behavior of the output is governed by changing the role of control signal v_{s2}–v_{s6} with v_{s4}–v_{s5}. The power transferring paths of Figure 6a,c illustrate how the voltage at the output is inverted. The turning on of the transistors Q_4 and Q_5 produce the negative output from positive input while the on-state operation of the transistors Q_2 and Q_6 during negative input convert it to a positive value. The voltage regulation capability of the output is attained by storing and releasing the power in the inductor as may be seen in the power flow loops of Figure 6a–d for a period in which the input is positive and negative respectively. The instantaneous value of the non-inverted output voltage in a voltage-regulated and non-regulated mode is mathematically computed in Equations (1) and (2):

$$v_o(\omega t) = DV_m\text{Sin}(\omega t) \tag{1}$$

$$v_o(\omega t) = V_m\text{Sin}(\omega t) \tag{2}$$

The instantaneous inverted form of the output voltage during the voltage regulated and non-regulated modes is mathematically formulated in Equations (3) and (4):

$$v_o(\omega t) = DV_m\text{Sin}(\omega t - \pi) \tag{3}$$

$$v_o(\omega t) = V_m\text{Sin}(\omega t - \pi) \tag{4}$$

Here 'D' is the duty cycle of the voltage control circuit, and its value may be governed from 0% to 100% range and 'V_m' is the peak value of the input voltage.

3. Power Quality Analysis of Output Voltage

For this purpose, the decomposition of the output voltage represented in Figure 3b is decomposed into its parent sinusoidal forms in Figure 7. Here the instantaneous value of the output pulse No. 1, 3, 4, and 6 are controllable but the second and fifth pulses have non-regulated voltage capabilities. The instantaneous form of this sort of output voltage waveform or pulses is mathematically described in Equations (5)–(9).

$$v_o(\omega t) = DV_m\text{Sin}(\omega t) \qquad 0 \le \omega t \le \pi \tag{5}$$

$$v_o(\omega t) = -V_m\text{Sin}(\omega t) \qquad \pi \le \omega t \le 2\pi \tag{6}$$

$$v_o(\omega t) = DV_m\text{Sin}(\omega t) \qquad 2\pi \le \omega t \le 4\pi \tag{7}$$

$$v_o(\omega t) = -V_m\text{Sin}(\omega t) \qquad 4\pi \le \omega t \le 5\pi \tag{8}$$

$$v_o(\omega t) = DV_m\text{Sin}(\omega t) \qquad 5\pi \le \omega t \le 6\pi \tag{9}$$

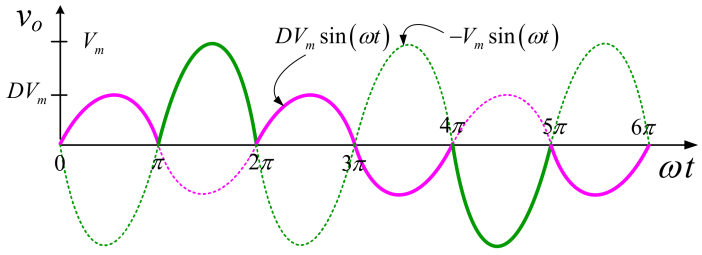


Figure 7. Decomposition of the output voltage into its parent sinusoidal pulses.

The pulse selective or half-cycle mathematical approach reported in [15] is applied to compute the rms voltage and Fourier coefficients of Equation (10) for the output voltage waveform of Figure 7.

$$v_o(\omega t) = a_o + \sum_{n=1}^{\infty} a_n \cos\left(\frac{n\omega t}{3}\right) + b_n \sin\left(\frac{n\omega t}{3}\right) \tag{10}$$

$$V_{o(rms)} = \sqrt{\frac{1}{2\pi}\left[\begin{array}{l}\int_0^{\pi} D^2V_m^2 \sin^2(\omega t)d(\omega t) - \int_{\pi}^{2\pi} V_m^2 \sin^2(\omega t)d(\omega t) + \int_{2\pi}^{3\pi} D^2V_m^2 \sin^2(\omega t)d(\omega t) \\ + \int_{3\pi}^{4\pi} D^2V_m^2 \sin^2(\omega t)d(\omega t) - \int_{4\pi}^{5\pi} V_m^2 \sin^2(\omega t)d(\omega t) + \int_{5\pi}^{6\pi} D^2V_m^2 \sin^2(\omega t)d(\omega t)\end{array}\right]} \tag{11}$$

$$V_{o(rms)} = V_m\sqrt{\frac{(2D^2+1)}{6}} \tag{12}$$

$$a_o = \frac{1}{2\pi}\left[\begin{array}{l}\int_0^{\pi} DV_m \sin(\omega t)d(\omega t) - \int_{\pi}^{2\pi} V_m \sin(\omega t)d(\omega t) + \int_{2\pi}^{3\pi} DV_m \sin(\omega t)d(\omega t) \\ + \int_{3\pi}^{4\pi} DV_m \sin(\omega t)d(\omega t) - \int_{4\pi}^{5\pi} V_m \sin(\omega t)d(\omega t) + \int_{5\pi}^{6\pi} DV_m \sin(\omega t)d(\omega t)\end{array}\right] = 0 \tag{13}$$

$$a_n = \frac{2}{2\pi}\left[\begin{array}{l}\int_0^{\pi} DV_m \sin(\omega t)\cos\left(\frac{n\omega t}{3}\right)d(\omega t) - \int_{\pi}^{2\pi} V_m \sin(\omega t)\cos\left(\frac{n\omega t}{3}\right)d(\omega t) \\ + \int_{2\pi}^{3\pi} DV_m \sin(\omega t)\cos\left(\frac{n\omega t}{3}\right)d(\omega t) + \int_{3\pi}^{4\pi} DV_m \sin(\omega t)\cos\left(\frac{n\omega t}{3}\right)d(\omega t) \\ - \int_{4\pi}^{5\pi} V_m \sin(\omega t)\cos\left(\frac{n\omega t}{3}\right)d(\omega t) + \int_{5\pi}^{6\pi} DV_m \sin(\omega t)\cos\left(\frac{n\omega t}{3}\right)d(\omega t)\end{array}\right] = 0 \tag{14}$$

$$b_n = \frac{2}{2\pi}\left[\begin{array}{l}\int_0^{\pi} DV_m \sin(\omega t)\sin\left(\frac{n\omega t}{3}\right)d(\omega t) - \int_{\pi}^{2\pi} V_m \sin(\omega t)\sin\left(\frac{n\omega t}{3}\right)d(\omega t) \\ + \int_{2\pi}^{3\pi} DV_m \sin(\omega t)\sin\left(\frac{n\omega t}{3}\right)d(\omega t) + \int_{3\pi}^{4\pi} DV_m \sin(\omega t)\sin\left(\frac{n\omega t}{3}\right)d(\omega t) \\ - \int_{4\pi}^{5\pi} V_m \sin(\omega t)\sin\left(\frac{n\omega t}{3}\right)d(\omega t) + \int_{5\pi}^{6\pi} DV_m \sin(\omega t)\sin\left(\frac{n\omega t}{3}\right)d(\omega t)\end{array}\right] \tag{15}$$

$$b_n = \begin{cases} 0 & for\ n = 2,4,6,\ldots \\ \dfrac{-12V_m(1+D)}{\pi(n^2-9)}\sin\left(\dfrac{n\pi}{3}\right) & for\ n = 1,3,5,7\ldots \end{cases} \tag{16}$$

For fundamental components (n = 3)

$$a_n(n=3) = \frac{2}{2\pi}\left[\begin{array}{l}\int_0^{\pi} DV_m \sin(\omega t)\cos(\omega t)d(\omega t) - \int_{\pi}^{2\pi} V_m \sin(\omega t)\cos(\omega t)d(\omega t) \\ +\int_{2\pi}^{3\pi} DV_m \sin(\omega t)\cos(\omega t)d(\omega t) + \int_{3\pi}^{4\pi} DV_m \sin(\omega t)\cos(\omega t)d(\omega t) \\ -\int_{4\pi}^{5\pi} V_m \sin(\omega t)\cos(\omega t)d(\omega t) + \int_{5\pi}^{6\pi} DV_m \sin(\omega t)\cos(\omega t)d(\omega t)\end{array}\right] = 0 \quad (17)$$

$$b_n(n=3) = \frac{2}{2\pi}\left[\begin{array}{l}\int_0^{\pi} DV_m \sin(\omega t)\sin(\omega t)d(\omega t) - \int_{\pi}^{2\pi} V_m \sin(\omega t)\sin(\omega t)d(\omega t) \\ +\int_{2\pi}^{3\pi} DV_m \sin(\omega t)\sin(\omega t)d(\omega t) + \int_{3\pi}^{4\pi} DV_m \sin(\omega t)\sin(\omega t)d(\omega t) \\ -\int_{4\pi}^{5\pi} V_m \sin(\omega t)\sin(\omega t)d(\omega t) + \int_{5\pi}^{6\pi} DV_m \sin(\omega t)\sin(\omega t)d(\omega t)\end{array}\right] \quad (18)$$

$$b_n(n=3) = \frac{(2D-1)V_m}{3} \quad (19)$$

The Fourier expression of the output voltage of Equation (10) can be represented in Equation (20) by putting the value of the computed harmonic coefficients a_o, a_n, and b_n:

$$v_o(\omega t) = \frac{(2D-1)V_m}{3}\sin(\omega t) + \sum_{n=1,3,5,7,\ldots}^{\infty} \frac{-12(1+D)V_m}{\pi(n^2-9)}\sin\left(\frac{n\pi}{3}\right)\sin\left(\frac{n\omega t}{3}\right) \quad (20)$$

The fundamental component of the output voltage waveform is obtained by putting the value of n = 1 in Equation (20):

$$v_{o1}(\omega t) = \frac{3\sqrt{3}(1+D)V_m}{4\pi}\sin\left(\frac{\omega t}{3}\right) \quad (21)$$

The rms value of this voltage component is obtained as:

$$v_{o1}(\omega t) = \frac{3\sqrt{3}(1+D)V_m}{4\sqrt{2}\pi} \quad (22)$$

If the duty cycle of the voltage-regulated pulses is set to '1' then the magnitude of all voltage-regulated pulses becomes equal to the magnitude of the non-regulated voltage pulses. The output voltage waveform with this duty cycle is described in Figure 8.

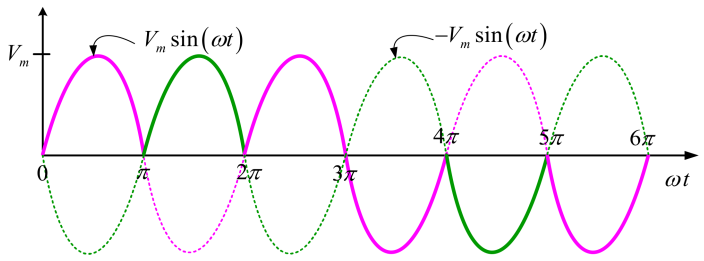


Figure 8. Output voltage waveform with D = 1.

The instantaneous value of the output voltage and voltage fundamental component, total rms voltage may compute by putting the value of duty cycle $D = 1$ in Equation (20), Equation (21), and Equation (12) respectively:

$$v_o(\omega t) = \frac{V_m}{3}\sin(\omega t) + \sum_{n=1,5,7,11,\ldots}^{\infty} \frac{-24V_m}{\pi(n^2-9)}\sin\left(\frac{n\pi}{3}\right)\sin\left(\frac{n\omega t}{3}\right) \tag{23}$$

$$v_{o1}(\omega t) = \frac{3\sqrt{3}V_m}{2\pi}\sin\left(\frac{\omega t}{3}\right) \tag{24}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = 0.707V_m \tag{25}$$

Its rms value, the rms value of the total harmonic components, and THD of the output voltage of Figure 8 may be found as:

$$V_{o1(rms)} = \frac{3\sqrt{3}V_m}{2\sqrt{2}\pi} = 0.5847V_m \tag{26}$$

$$V_{oh(rms)} = \sqrt{V_{o(rms)}^2 - V_{o1(rms)}^2} = 0.3976V_m \tag{27}$$

$$T.H.D = \sqrt{\frac{V_{rms}^2 - V_{01(rms)}^2}{V_{01(rms)}^2}} \approx 68\% \tag{28}$$

The low power quality of the output voltage needs investigation as it has a high value. It is observed from Equation (20) that output harmonic at source voltage frequency can be eliminated by setting the value of the duty ratio or duty cycle to 0.5. The output voltage wave with this duty cycle control may be viewed from Figure 9.

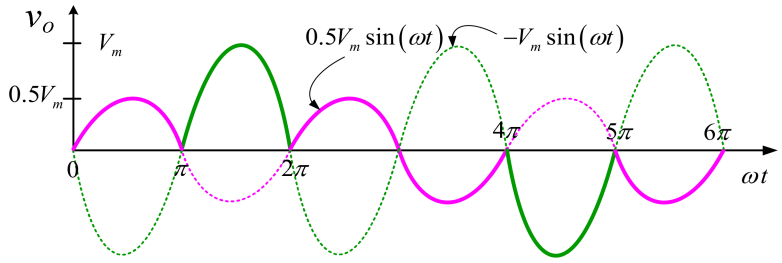


Figure 9. Output voltage waveform with $D = 0.5$.

The instantaneous value of the output voltage and voltage fundamental component, total rms voltage may compute by putting the value of duty cycle $D = 0.5$ in Equation (20), Equation (21), and Equation (12), respectively.

$$v_o(\omega t) = \sum_{n=1,5,7,11,\ldots}^{\infty} \frac{-18V_m}{\pi(n^2-9)}\sin\left(\frac{n\pi}{3}\right)\sin\left(\frac{n\omega t}{3}\right) \tag{29}$$

$$v_{o1}(\omega t) = \frac{9\sqrt{3}V_m}{8\pi}\sin\left(\frac{\omega t}{3}\right) \tag{30}$$

$$V_{o(rms)} = \frac{V_m}{2} = 0.5V_m \tag{31}$$

Similarly, the rms value, the rms value of the total harmonic components, and THD of the output voltage of Figure 9 may be found as:

$$V_{o1(rms)} = \frac{9\sqrt{3}V_m}{8\sqrt{2}\pi} = 0.43V_m \tag{32}$$

$$V_{oh(rms)} = \sqrt{V_{o(rms)}^2 - V_{o1(rms)}^2} = 0.43V_m \tag{33}$$

$$T.H.D = \sqrt{\frac{V_{o(rms)}^2 - V_{o1(rms)}^2}{V_{o1(rms)}^2}} \approx 55\% \tag{34}$$

With this approach, the THD or harmonic factor is lowered from 68% to almost 55%.

4. Comparison with Similar Topologies

The requirement of the output voltage that includes the frequency and voltage regulation is achieved by developing a transformer-less AC-AC converter. This approach has the ability to vary the magnitude of the selected output pulse via the PWM control. The range for the output voltage control lies from 0% to 100% value of the input peak or rms voltage. Such variation in the output pulses governs the required output rms voltage and power quality. The voltage control of the selected pulses via the use of multiple transformer winding requires more space, and this is a costly solution or approach. The application of the low-frequency transformer is the main source of power losses and low conversion efficiency. Although the converter reported in [25] has the ability to achieve the required output with the conduction of one diode and one thyristor during any instant of its operation, but its voltage control capability requires a multiple windings transformer operated at line frequency. The voltage of these windings is connected to the load through the number of diodes and thyristors. The number of voltage levels is proportional to the number of the transformer's windings. Increasing the number of winding increases the required number of diodes and thyristors as one thyristor and two diodes are associated with each winding.

The AC voltage controllers that have the ability to govern the voltage regulation with PWM control for both the non-inverted and inverted forms of the input voltage at the output may also be employed to achieve such outputs without involving bulky line frequency transformers [26,27]. The proposed circuit is developed with this principle and its implementation uses a fixed number of semiconductor devices. The required voltage level in the output may be obtained just by regulating the duty cycle control of the PWM control. The elimination of the low line frequency transformer saves the required space and cost significantly. The control input signal of the proposed circuit and power converting circuits described in [23,26,27] are drawn in Figure 10. The gate control inputs of the converter reported in [26] are demonstrated in Figure 10b. The peak amplitude of the second and fifth output pulses is equal to the peak of the input and they are the inverted forms of the input voltage. The amplitude of remaining output pulses is one-half of the input peak and their characteristics are non-inverted with respect to the input voltage. Therefore, the required voltage gain is '-1' for the second and fifth output pulses while it is '0.5' for the rest of the pulses. This circuit has the ability to convert the input voltage to a non-inverted voltage buck form with a voltage gain of '0.5'. But its output cannot be directly connected with the input source to obtain its inverted form with the voltage gain of '-1'. Its voltage inverting form can only be obtained from its buck-boost operation. Therefore, its non-inverted and inverted control is non-identical. This non-symmetrical form of the gate control signals becomes complex for output voltage regulation. The voltage buck-boost operation always increases the peak-to-peak inductor ripple current, and voltage and current rating of the devices. The duty cycle value (k) to obtain the output for voltage buck and buck-boost operation is '0.5'. The value of the peak-to-peak ripple (ΔI_L) inductor current, average inductor current (I_L), and maximum breakover voltage ($V_{bo(m)}$) is computed as:

$$\Delta I_L = \frac{0.5V_{s(p)}}{L} T_s \tag{35}$$

$$I_L = \frac{I_o}{1-k} = 2I_o \tag{36}$$

$$V_{bo(m)} = V_{s(m)} + V_{o(m)} = 2V_{s(m)} \tag{37}$$

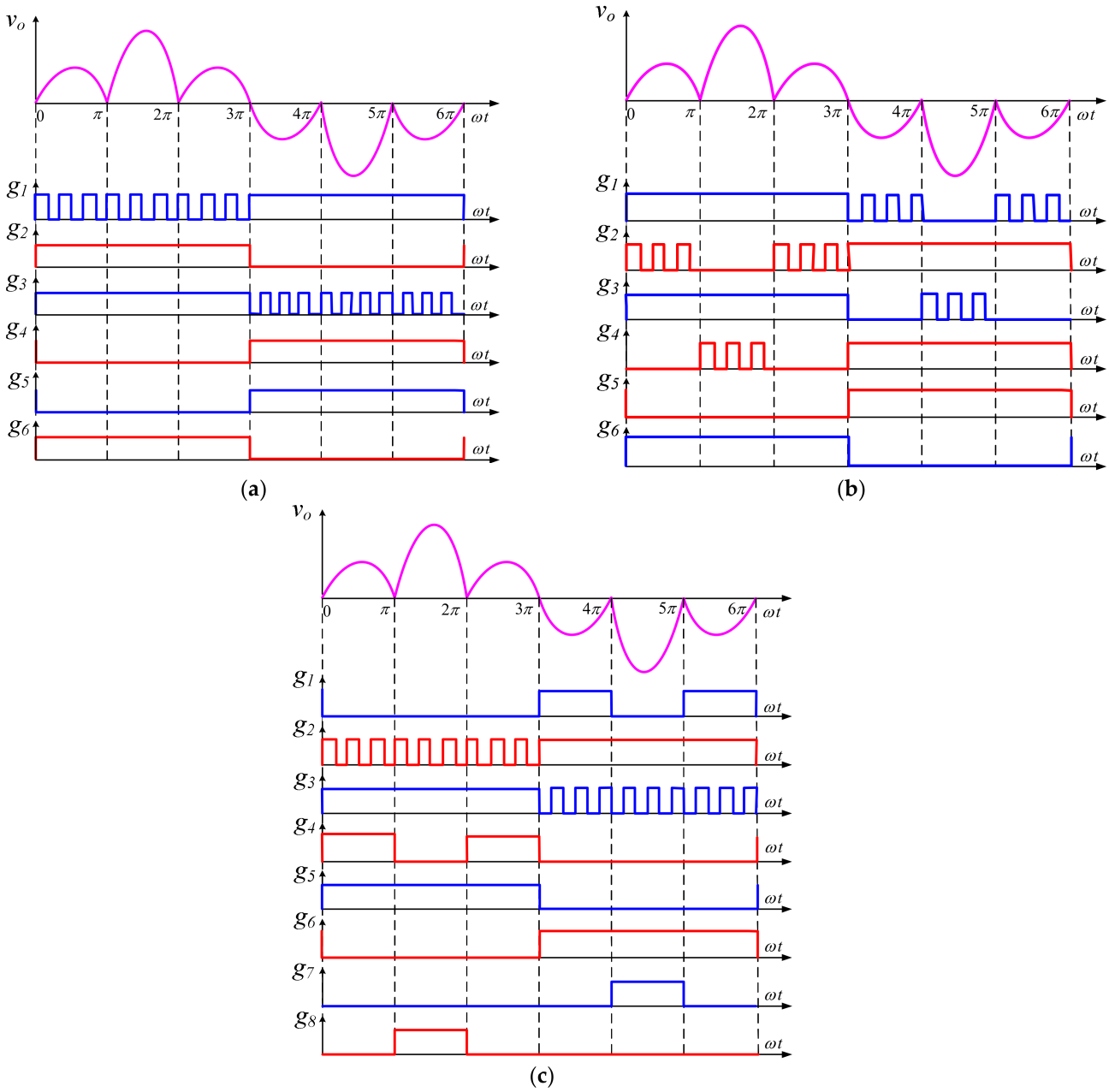


Figure 10. Generation of control signals: (**a**) proposed circuit; (**b**) circuit in [26]; (**c**) circuit in [23].

In these equations, the 'T_s' is the PWM switching period, 'I_o' is output current, '$V_{o(m)}$' and '$V_{s(m)}$' are the maximum output and input voltage, respectively. The preceding issues are addressed in the circuit arrangement reported in [23] by ensuring the identical control scheme that is effectively used to obtain the output in non-inverted and inverted form. Its value of maximum breakover voltage, inductor ripple, and average current can be represented as in Equations (38)–(40). These values are low with respect to the circuit described in [26]. Also, the voltage control schemes of this topology as described in Figure 10c are relatively simple than that of the circuit reported in [26]. The major issue in this existing topology is the use of more devices and gate control circuits that are the

main sources for the high volume and cost. These issues are addressed in the proposed circuit by reducing the number of switching devices and gate control circuits. Also, its gate control algorithm as depicted in the plot of Figure 10a is much simpler with the same value of maximum breakover voltage, inductor ripple, and average current than that of [26]. This achievement reduces the circuit's overall volume:

$$\Delta I_L = \frac{0.25V_{s(p)}}{L} T_s \tag{38}$$

$$I_L = I_o \tag{39}$$

$$V_{bo(m)} = V_{s(m)} \tag{40}$$

The power conversion losses are the other index used to compare the performance of the various circuit topologies. They include the losses caused by the filtering components, switching and conduction losses of the semiconductor devices, and core losses of the line frequency input transformer. The contribution of the losses caused by the filtering com is ignorable as they have a low value of their internal resistance [26]. The switching losses of high switching frequency (f_s) operating transistors depend on their rise (t_r) and fall time (t_f), and for diodes, they are related to their reverse recovery charge (Q_{rr}). These losses also depend on the value of current and voltage at which the switching devices are going to change their operating states 'on' to 'off' and vice versa. The instantaneous values of the voltage and current may regard constant as their variation can be ignored at high switching frequencies. The value of switching losses for the existing circuits of [23,25,26] and the proposed topology in Equations (41)–(44) respectively may be realized with the procedure as detailed in [28,29].

$$P_{sw} \simeq \frac{1}{6} f_s V_s I_o \left(t_r + t_f\right) + f_s V_s Q_{rr} \tag{41}$$

$$P_{sw} = 0 \tag{42}$$

$$P_{sw} \simeq \frac{1}{3} f_s V_s I_o \left(t_r + t_f\right) + \frac{4}{3} f_s V_s Q_{rr} \tag{43}$$

$$P_{sw} \simeq \frac{1}{6} f_s V_s I_o \left(t_r + t_f\right) + f_s V_s Q_{rr} \tag{44}$$

The value of rise, fall, and reverse recovery times lie in the nanosecond range so, for modern fast switching devices, these losses can be ignored.

The main source of the conversion losses consists of conduction losses (especially for diode and thyristors) and line frequency input transformer. The conduction losses in the topologies reported in [23,25,26] and the developed circuit are calculated from Equations (45)–(48) respectively by following the procedure adopted in [29]. In these equations, the notation V_f is used to represent the value of the forward voltage of a diode or a thyristor. In the same way, the notations R_s and R_f represent the internal resistances of a transistor and a diode or a thyristor, respectively.

$$P_{cond} = 3I_o \left[V_f + I_o \left(R_s + R_f\right)\right] \tag{45}$$

$$P_{cond} = 2I_o \left[V_f + I_o R_f\right] \tag{46}$$

$$P_{cond} = 4I_o \left[V_f + I_o \left(R_s + R_f\right)\right] \tag{47}$$

$$P_{cond} = 3I_o^2 R_s + 2I_o \left[V_f + I_o R_f\right] \tag{48}$$

The conduction of the developed circuit is less than the topologies in [23,26] and slightly greater than the circuit in [25].

In summary, the comparison Table 1 highlights the significance of the developed circuit topology for one-third of the output frequency.

Table 1. Comparison for the output frequency of one-third (3:1) with the respective input frequency.

Parameters	Suggested Converter	Converter in [25]	Converter in [23]	Converter in [26]
Number of transformer windings	0	4	0	0
Number of diodes	4	8	8	6
Number of controlled devices	6	4	8	6
Number of gate supporting circuit	6	4	8	6
Inductor ripple current	$\frac{0.25V_{s(p)}}{L}T_s$	0	$\frac{0.25V_{s(p)}}{L}T_s$	$\frac{0.5V_{s(p)}}{L}T_s$
Inductor average current	I_o	I_o	I_o	$2I_o$
Maximum breakover voltage	$V_{s(m)}$	$V_{s(m)}$	$V_{s(m)}$	$2V_{s(m)}$
Maximum switching voltage across high-frequency devices	$2V_{o(m)}$	0	$2V_{o(m)}$	$3V_{o(m)}$
%*THD* of the output voltage	55	55	55	55
Conduction losses	$3I_o^2R_s + 2I_o\left[V_f + I_oR_f\right]$	$2I_o\left[V_f + I_oR_f\right]$	$3I_o\left[V_f + I_o\left(R_s + R_f\right)\right]$	$4I_o\left[V_f + I_o\left(R_s + R_f\right)\right]$
Switching losses	$\frac{1}{6}f_sV_sI_o\left(t_r + t_f\right) + f_sV_sQ_{rr}$	0	$\frac{1}{6}f_sV_sI_o\left(t_r + t_f\right) + f_sV_sQ_{rr}$	$\frac{1}{3}f_sV_sI_o\left(t_r + t_f\right) + \frac{4}{3}f_sV_sQ_{rr}$

The proposed circuit is an attractive topology as it has low conversion losses, low value of maximum breakover voltage, low inductor ripple, and average current that lower the voltage and current rating of the operating devices. The proposed circuit also needs a fewer number of semiconductor components without the requirement of the bulky line frequency transformer.

5. Results and Discussion

The computerized and real results are used to prove or validate the strength of the recommended circuit.

5.1. Simulation Results

The Simulink-based system is one of the big sources of modern tools available in the market to analyze the performance of switching converters, so this tool was considered for analysis and verification of the mathematically computed values of the harmonic section. The modeling of the operating devices is carried by considering the parameters of their datasheets. These parameters include the value of internal resistance and voltage drops for their conducting states. The internal on-state resistance of a transistor and diode is set to 100 mΩ and 600 Ω, respectively. The forward drops of the diodes are set to 1 V. A value of load resistance 50 Ω ensures the safe circuit operation to limit the output current to a low value for 65 V input peak. An appropriate value of the required switching frequency of 25 kHz is used to reduce the current and voltage ripple to an acceptable level. The computerized results of Figure 11 describe the frequency control of the output voltage for the ratio of 3 to 1 means output frequency is one-third of the grid frequency. This regulation is achieved without voltage control capability. Hence the peak values of the output positive and negative pulses are equal to input voltage's peaks (see Figure 11a,b) for the confirmation of these values. The output voltage has a constant rms value that is the same as the input voltage. The FFT plot of Figure 11c confirms the computed value of the output voltage's THD of Equation (28). Her line frequency harmonic (50 Hz) has significant magnitude, and it is a major cause of the high THD of the output voltage.

The plot of Figure 12b is obtained through Simulink simulation by setting the optimal value of the duty cycle of '0.5' that is investigated in the mathematical results. This duty cycle control sets the peak of the first, third, fourth, and sixth pulse to 50% of the input voltage's peak. It also leaves the peak value of the output voltage's second and fifth pulse unchanged. This profile of the peak values of the output voltage's pulses improves its power quality, and the computed value of the THD of the output voltage in Equation (34) is validated by the plot of Figure 12c.

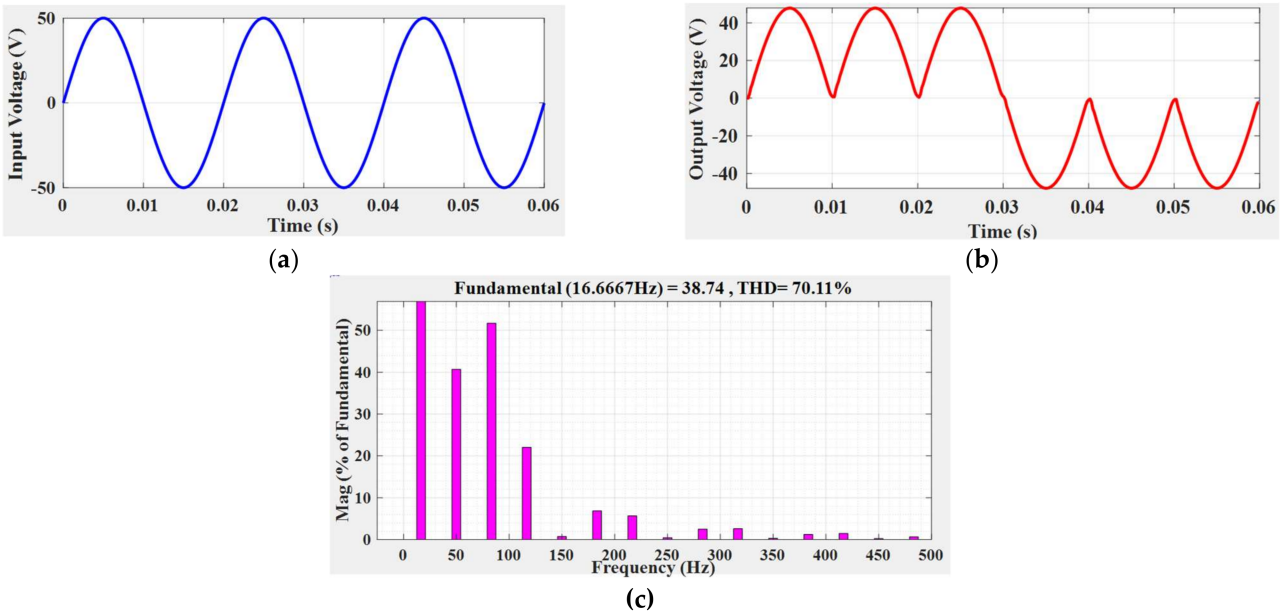


Figure 11. Simulated results of frequency controller without voltage regulation: (**a**) input voltage; (**b**) output voltage; (**c**) FFT of the output voltage.

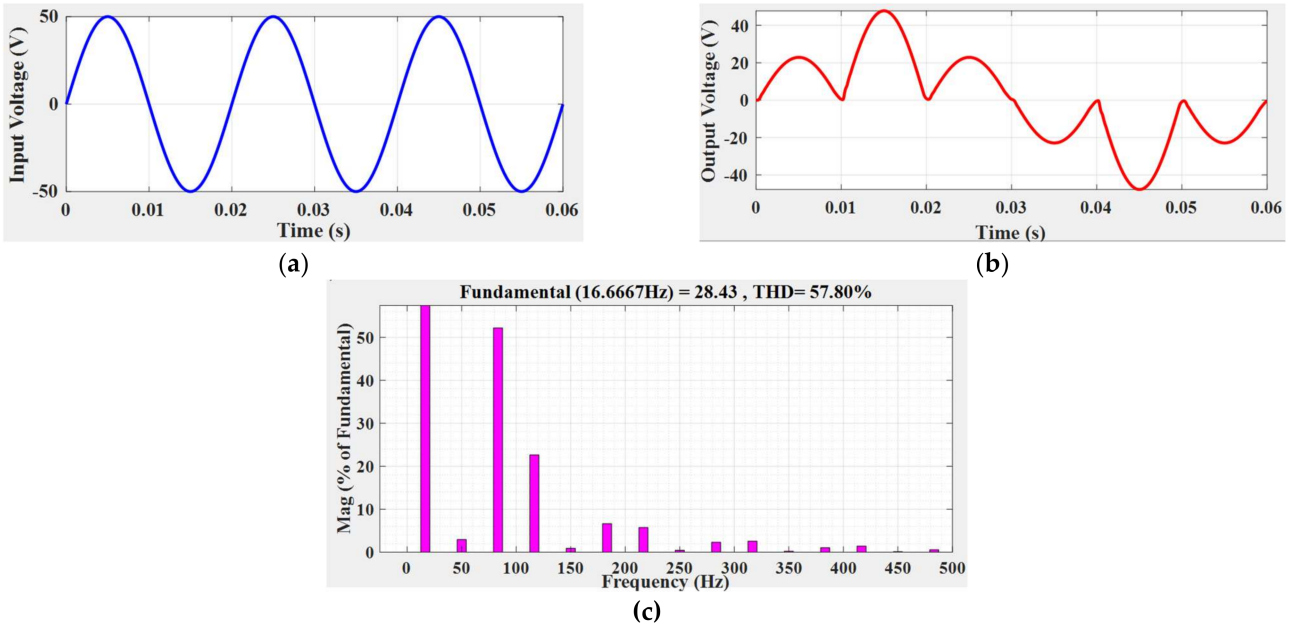


Figure 12. Simulated results of frequency controller with voltage regulation: (**a**) Input voltage; (**b**) output voltage; (**c**) FFT of the output voltage.

The FFT plot of Figure 12c demonstrates the significant reduction in the magnitude of the generated at line frequency. This reduction result in low THD of the output voltage.

5.2. Experimental Results

The proposed circuit is practically tested with the development of a lab prototype. The photograph of this practical setup is shown in Figure 13.

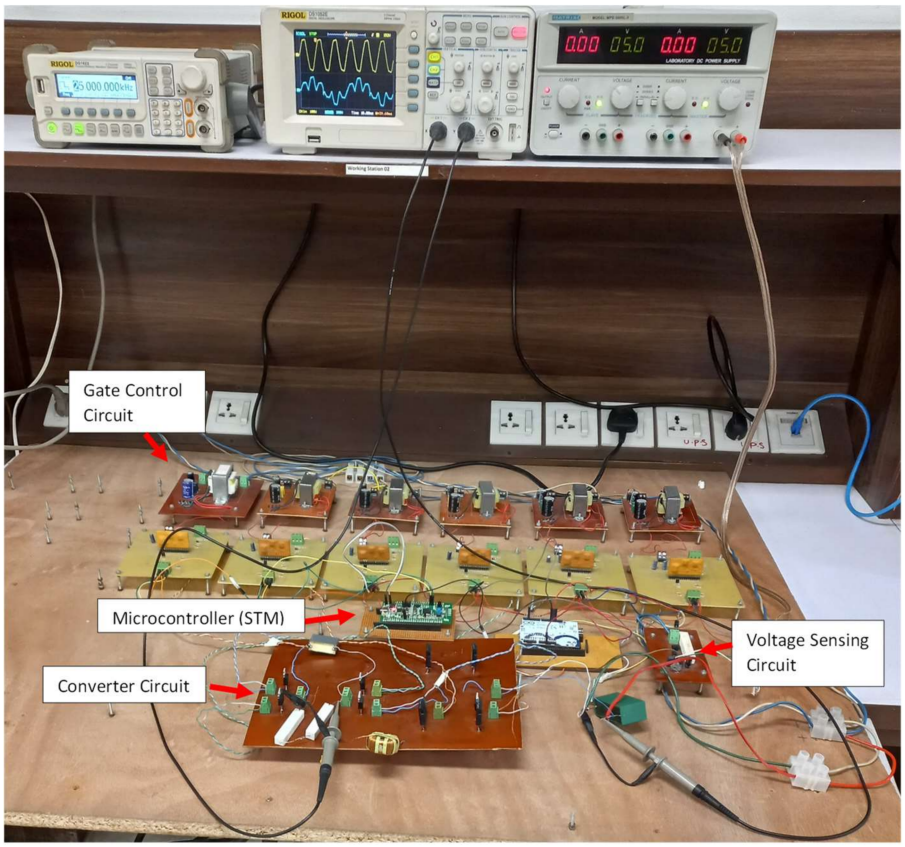


Figure 13. Photograph of practical setup.

It consists of six gate control circuits that are implemented with six hybrid EXB 840 chips and six isolated DC sources that ensure the electrical isolation of the generated control signals. All these control signals are to be aligned with the input AC voltage and for this purpose, one voltage detecting circuit is connected to the input source. The output of this circuit with respect to input AC voltage is shown in Figure 14.

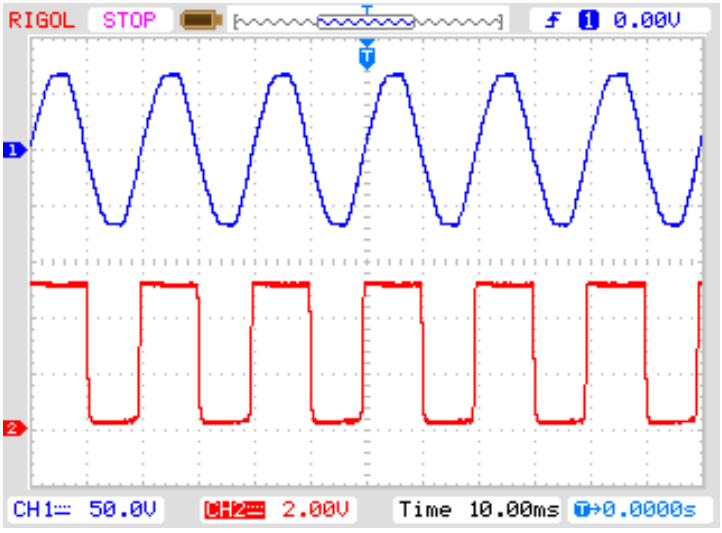


Figure 14. Output (red) of voltage sensing circuit with respect to input AC voltage (blue).

The output of this circuit is approximately 5 V and 0 V during the positive and negative half cycles of the input AC voltage. The output of the voltage sensing circuit is applied to the microcontroller (STM) to generate two high-frequency and four low-frequency gating signals. These six signals are connected to the inputs of the six gate control circuits. The outputs of these gate control circuits as shown in Figure 15 are connected to the input of the six transistors (IRF 840). The plot of Figure 15a shows the generation of one low-frequency signal (red) with respect to input AC voltage (blue). Here it may be observed that the control input used by the output frequency controller is approximately 10 V and 0 V for the first and second half periods of the output voltage, while the plot of Figure 15b depicts the plot of low frequency (blue) and high frequency (red) control signals. The high-frequency signal uses pulse width modulation for a one-half period of the output voltage and it remains logic high (10 V) for the other half period of the output voltage. In the same way, the plots of Figure 15c,d show the control inputs connected to voltage and frequency controller circuits, respectively.

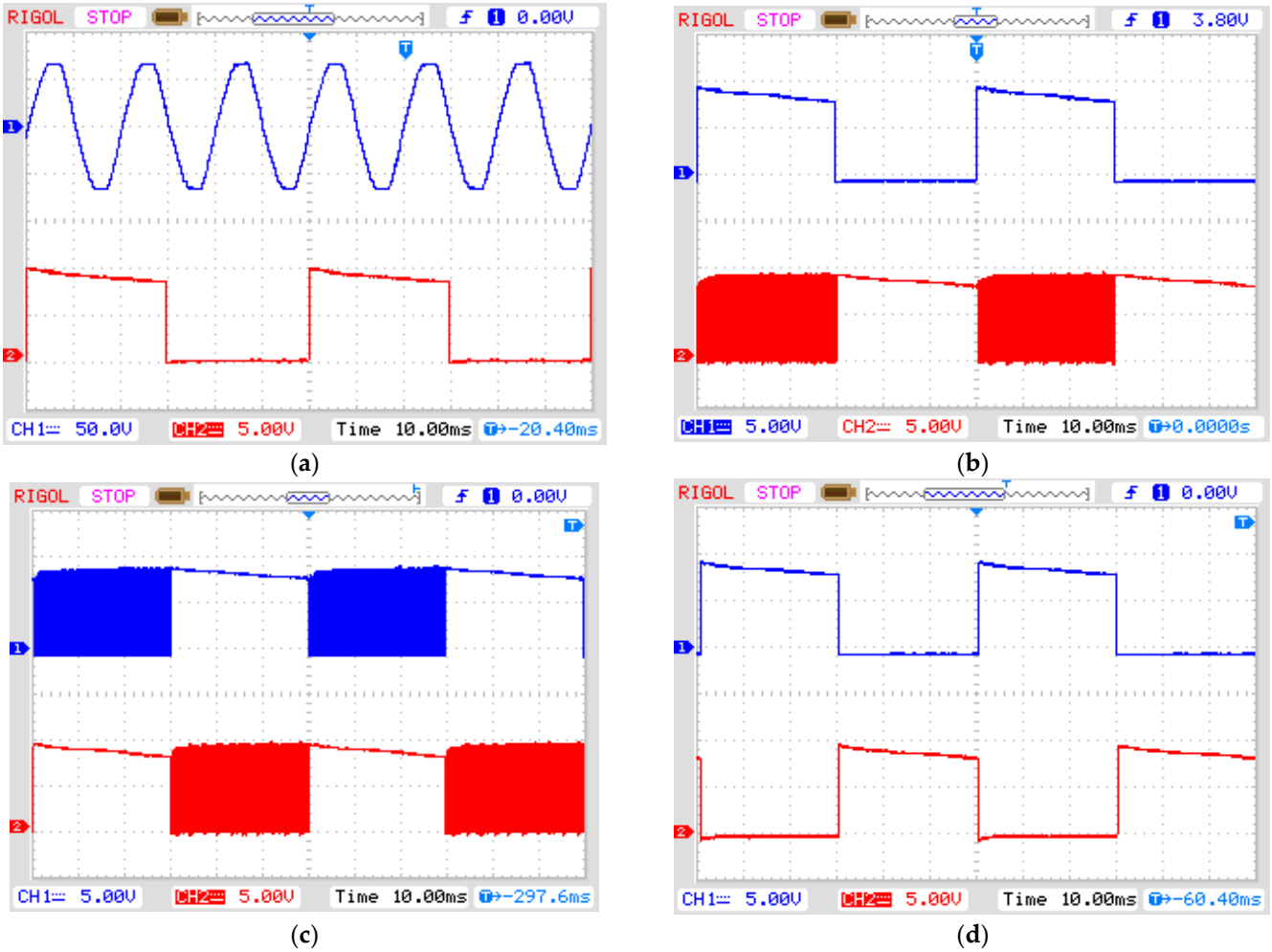
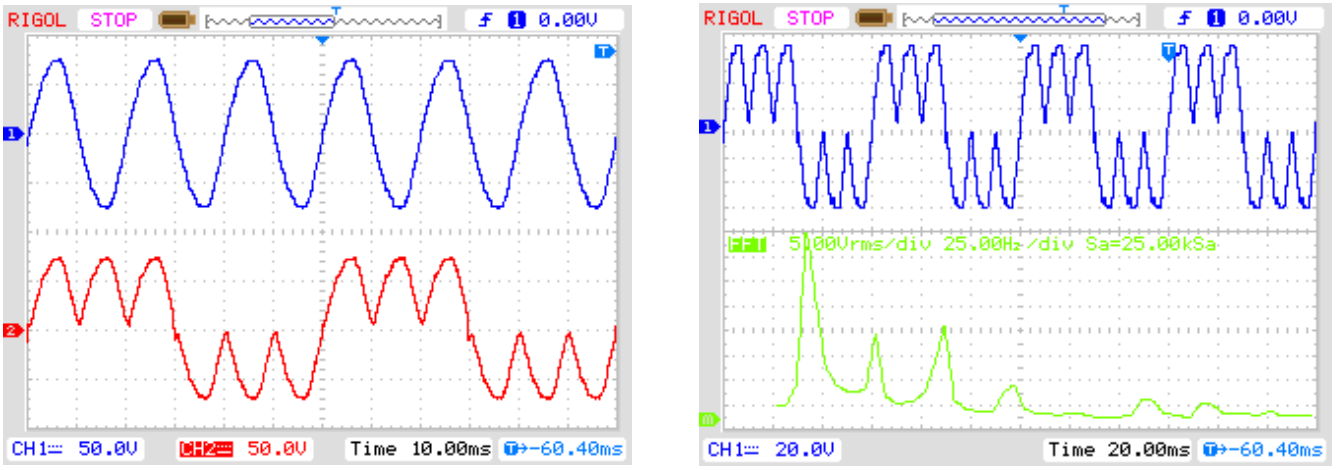


Figure 15. Generation of the control signals: (**a**) low-frequency signal (red) with respect to input AC voltage (blue); (**b**) high-frequency PWM signal (red) with respect to low frequency signal (blue); (**c**) high-frequency PWM signals; (**d**) low- frequency signals.

Four abrupt recovery diodes (MUR3040) having high voltage and current ratings are also used to construct the test circuit bench. The voltage and frequency control circuits are separately constructed in the test circuit, and an intermediate inductor with the value of 1 mH facilitates their connection. The inductor not only helps to tackle the shoot-through problem caused by a complementary operated transistor but also acts as an energy-storing

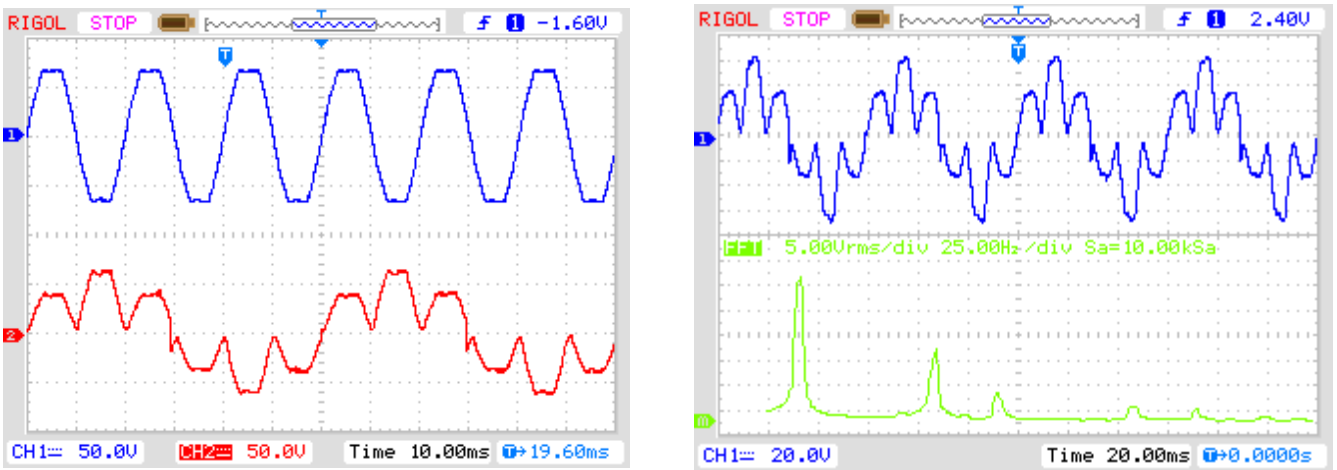
element and harmonic filterer. The input and the output capacitor with a value of 4.7 μF are responsible for improving the power quality of both sides of the circuit that is input and output. Input AC voltage with its peak value of 70 V and frequency of 50 Hz is used to test the output without and with the regulation of the output pulses. The output frequency in both cases is 16.667 Hz that is almost one-third of the input frequency. Figure 16a shows the output voltage waveform with respect to the input voltage for the non-regulated output form. The practically obtained FFT of this output is demonstrated in Figure 16b, validating the harmonic profile of the simulated output of Figure 11c.



(**a**) (**b**)

Figure 16. Real value results of frequency controller without voltage regulation capability: (**a**) Input (blue) and output (red) voltage; (**b**) FFT of output voltage pulses.

For the regulated form of the output pulses, the peak value of the output's first, third, fourth, and sixth pulse is 35 V, while the peak of the second and fifth pulse is 70 V as may be seen from Figure 17a. These amplitudes of the output pulses have optimal values that are addressed in the power quality evaluation section to have a low-value harmonic factor of the output voltage. The plot of Figure 17b depicts that harmonic of 50 Hz frequency in the output is eliminated from the frequency spectrum of the output voltage. This reduction improves the harmonic profile of the output voltage, and as a result, the THD of the output voltage is reduced.



(**a**) (**b**)

Figure 17. Real value results of frequency controller with voltage regulation capability: (**a**) input (blue) and output (red) voltage; (**b**) FFT of output voltage pulses.

6. Conclusions

This study was focused on the development of an improved direct AC-AC frequency controller having a low value of the THD of the output voltage. Improvement in the power quality is obtained by regulating the peak value of the selected output pulses with the required voltage gain. The optimal value of the voltage gain for the voltage regulating pulses is obtained through the analysis of the power quality. The variation in the output pulses that is based on the use of low-frequency multiple winding transformers is directly linked with the number of windings. Each winding is associated with the requirement of two diodes and one thyristor for the required operation. The number of required semiconductor components increases if the required voltage level of the output pulses is increased. The application of a massive low-frequency transformer with a large number of semiconductor devices is the main source of large size, cost, and overall conversion losses. The adjustment in the output pulses in the proposed circuit topology is achieved by employing the PWM control to the switching devices that eliminate the need for the multiple winding transformer for voltage control. This characteristic fixes the use of a number of the semiconductor devices in the proposed circuit that help to lower the overall volume, conversion losses, and cost. The power quality index of the output voltage is computed with a mathematical approach to confirm the analysis that is based on simulation and practical results.

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