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An Improved Charge-Based Method Extended to Estimating Appropriate Dead Time for Zero-Voltage-Switching Analysis in Dual-Active-Bridge Converter

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Abstract: This paper presents a comprehensive analysis of zero-voltage-switching (ZVS) realization with an improved charge-based method by considering both voltage dependency parasitic capacitance and dead time in dual-active-bridge (DAB) converters, when the voltage ratio between the primary and secondary sides does not match the turn ratio of the transformer. For this purpose, a unified equivalent circuit is proposed to represent the switching motions at all possible switching instances under the condition of one-leg manipulation. The combinations of switching cases can be presented in a table to build the corresponding equivalent circuit for ZVS analysis. Combined with the improved charge-based method, the common solutions of the minimum required switching current and the appropriate dead-time range for each equivalent circuit to realize ZVS are deduced. The allowable range of the dead time for ZVS as a function of the switching current is analyzed to determine the appropriate dead time. Once the switching current and dead-time range are derived, the model-based lowest switching current control method can be used to achieve ZVS by using the appropriate amount of both factors. Experiments using a 4 kW DAB prototype were conducted to verify the theoretical analyses.

Keywords: dual-active-bridge converter; zero-voltage switching; extended-phase shift

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1. Introduction

Over recent years, the dual-active-bridge (DAB) converter has been widely studied as an interface converter for various applications that require galvanic isolation, a high-voltage step-up/-down ratio, and bidirectional power flow control [1–3], for example, in vehicle-to-grid (V2G)-capable electric vehicle (EV) chargers, solid-state transformers (SSTs), and supercapacitor-based energy storage systems. By applying the conventional modulation method, the single-phase-shift (SPS) method, the DAB converter can easily achieve zero-voltage switching (ZVS) when the voltage ratio is fixed at its designated value without additional circuitry [4]. ZVS realization can effectively reduce the switching losses and electro-magnetic interference (EMI) emissions, especially for the areas where high-switching frequency converters are widely applied [5]. Moreover, ZVS operation can also reduce the risk of malfunction and the breakdown of power devices [6]. As another method of soft switching, zero-current switching (ZCS) is also an important technique in the research of bidirectional converters [7]. However, certain switching losses are still generated during the turning-on process compared with ZVS in a DAB converter. Thus, the research on ZVS in DAB converters has received much attention.

In some applications, such as energy storage using batteries and supercapacitors, and power conversions for an active power decoupling [8], a varying input voltage can be applied. However, once the input voltage deviates from the desired value, ZVS operation can be lost in some parts of the operation range. To address the above problem, many studies have been conducted over the past decade. A switched auxiliary inductor to change the equivalent magnetizing inductance has been proposed for extending the ZVS range in [9].

One of the drawbacks of this method is that additional components are needed; therefore, the power density can be reduced. Another major approach is using the so-called burst mode [10–12]. However, the switching transients present at the exchanging of the active and inactive periods cannot realize ZVS. In similar approaches, some modulations using a variable switching frequency have been proposed in [13–15]. Increasing the switching frequency can extend the range of ZVS in low-power operations. However this extension cannot be infinitely increased and the other losses related to the frequency can be increased. In addition to the above methods, ZVS-range extensions based on some advanced modulation strategies, such as an extended-phase shift (EPS), a dual-phase shift (DPS) and a triple-phase shift (TPS), by introducing a higher degree of freedom, have been introduced in [16–20].

Most research [12–14,16–20] discusses the switching condition to judge the ZVS under a current-based method, in which the current direction at the switching instant is simply used to judge whether the switching is ZVS or not. A charge-based method is much more precise method than the current-based method [21,22]. It judges ZVS considering if the charge stored in the parasitic capacitance of switches has totally been released before the switches turn on. With this method, the actual switching current needed to complete the ZVS can be obtained. Based on this approach, some works have proposed controlling the critical switching current for ZVS with optimized operations from certain aspects [21,23]. Moreover, an improved charge-based method, which considers the non-linearity of the parasitic capacitance of semiconductor devices, has been introduced. In [24], the ZVS judgement, in particular, the operating conditions of the EPS, is analyzed with the improved charge-based method. This can provide a much more accurate estimation of the required switching current to ensure the ZVS.

However, the switching current is not the sole required condition to achieve ZVS. An appropriate dead time is also needed. The charge-based method with considering the non-linear parasitic capacitance can estimate the process during the dead time accurately; however, it has not been applied to discuss the appropriate dead time in terms of ZVS realization. A strategy to determine the dead time, including the margin for possible error and a method to realize ZVS in actual converters, is a beneficial topic that will be discussed later on in this paper.

This paper applies the improved charge-based method, which considers the voltage dependency of the parasitic capacitance of devices, to discuss the appropriate dead-time period. For this purpose, a unified equivalent circuit used to consider all the possible switching conditions and any phase-shift modulations is proposed for the first time. Based on the equivalent circuit, the equation of the minimum required switching current to ensure ZVS is deduced. Then, a comprehensive analysis on characteristics of dead time is performed and the acceptable dead-time range as a function of the switching current is discussed so that strategies to determine the dead time can be discussed.

A 4 kW laboratory prototype of the DAB converter was used to verify the above theoretical research. The model-based lowest switching current control proposed in [23] for EPS was taken as an example to verify the appropriate dead-time period with enough of a margin of the switching current for ZVS.

2. Unified Equivalent Circuit for Switching Instant in DAB Converters

2.1. Model of Dual-Active-Bridge Converter

The configuration of the DAB converter is shown in Figure 1. The DAB converter consists of two H-bridges and a medium-frequency transformer (MFT) with a turn ratio of $N:1$. V_1 and V_2 are the DC terminal voltages of the input and output. L is the primary-side referred equivalent inductance of the transformer. The voltage ratio is defined as $k = V_1/(NV_2)$. The power devices are operating under the switching frequency of f_{sw}.

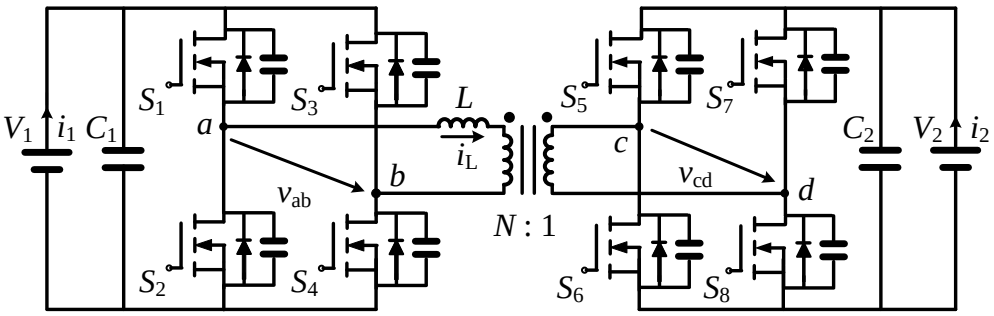


Figure 1. Configuration of the dual-active-bridge (DAB) converter.

Phase-shift modulations are the most widely used modulation techniques in DAB converters. Schematic waveforms of three typical methods, SPS, EPS and TPS, are shown in Figure 2. $S_1 \sim S_8$ are the gate signals for the corresponding switches in Figure 1. In all the modulations, switches are controlled by 50% duty ratio signals and the phase-angle differences between them are controlled. Using different phase-shift relationships of gate signals, two- or three-level square voltages are generated in the port voltages of two full bridges, v_{ab} and v_{cd}. All the possible patterns to achieve cyclic and symmetric port voltages can be classified into three modulation schemes.

The schematic waveforms with SPS, which have a two-level port voltage on both sides, are shown in Figure 2a. The phase-shift difference between the two-level port voltage is expressed by its per-unit value as D_δ and it is the sole control freedom in SPS for controlling power. In EPS, a three-level voltage is involved on one side, as shown in Figure 2b. Thus, another phase-shift ratio expressed as D_f is introduced to this side. TPS is the most general modulation, which has a three-level voltage on both sides. The inherent phase-shift ratios in the primary and secondary sides are expressed as D_fp and D_fs, respectively. Thus, SPS and EPS are unique cases of TPS.

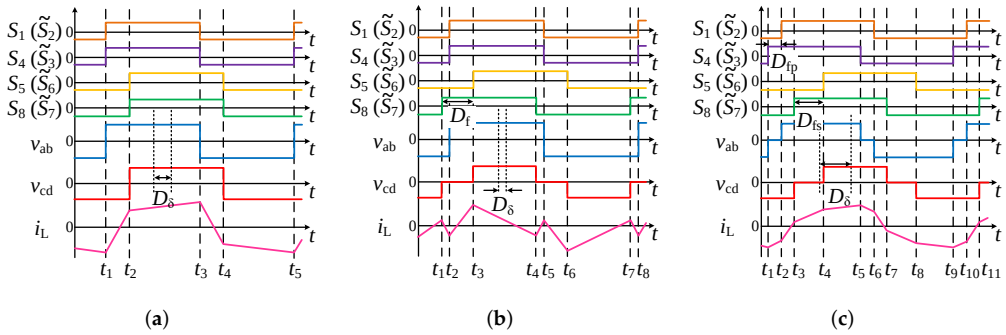


Figure 2. Schematic waveforms of the DAB converter with the (**a**) SPS modulation, (**b**) EPS modulation, and (**c**) TPS modulation.

2.2. Unified Equivalent Circuit

To analyze ZVS realization, all the switching instants that cause changes in the port voltages should be analyzed. In any switching instances, only one or two legs are manipulated, while the others are kept as they are. The conditions where two legs are manipulated at the same time only happen in SPS and EPS.

A unified equivalent circuit, as shown in Figure 3, can be used to analyze all the possible switchings in the above modulations. The considered leg is composed by upper and lower devices, S_U and S_L, respectively. V_DC is the DC terminal voltage of the operating side. V_eq is the equivalent voltage source that represents the port voltage of the other side bridge converted to the operating side, V_port'. It should be mentioned that V_port' is equal to Nv_cd, which can be $+NV_2$, $-NV_2$ and zero, for considering the primary-side bridge, and v_ab/N, which can be $+V_1/N$, $-V_1/N$ and zero, for considering the secondary-side

bridge. Then V_{eq} is determined in accordance with the status of the other leg in the same bridge, and can be $+V_{port}{}'$ or $-V_{port}{}'$. L_{eq} is the equivalent series inductance converted to the operating side.

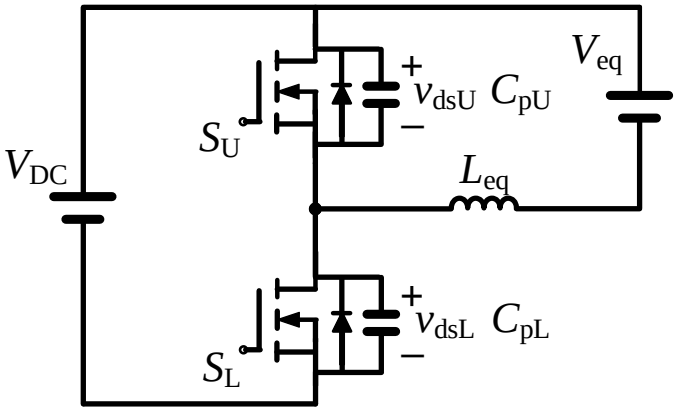


Figure 3. Unified equivalent circuit of the DAB converter, in which all the possible switching instances can be analyzed.

The leg which connects to the positive pole of the port voltage is defined as the left leg, and the leg which connects to the negative pole of the port voltage is defined as the right leg.

All the possible combinations of the switching leg, switching motion, and other conditions are listed in Table 1, resulting in V_{eq} in the unified equivalent circuit. The # in the left column represents the number of conditions. All the cases are divided into left-leg switchings and right-leg switchings; the switching motion, status of the adjacent leg and $V_{port}{}'$ are three decisive factors. By using these three factors, V_{eq} in the unified equivalent circuit can be picked from the table. The connection of the equivalent circuit shown in Figure 3 corresponds to the conditions in which the upper switch in the adjacent leg of the considered bridge is kept on; therefore, V_{eq} in these conditions can be directly obtained by the decisive factors and is shown in Table 1.

On the other hand, the cases in which the lower device in the adjacent leg is kept on cannot directly be explained by the circuit shown in Figure 3; however, the switching process of all these can be explained by any one of the cases with the upper switch on in the adjacent leg owing to the symmetry of the circuit. The counterparts of these cases are described in Table 1. The counterpart case has the complete opposite conditions of the three decisive factors in the same switching leg of the considered case. It should be mentioned that the corresponding direction of the inductor current is also the opposite in this case. It can be said that the opposite switching motion with the opposite current direction achieves the same switching process with the considered case, but the roles of upper and lower devices are changed. Consequently, all the possible switching instances that can happen in DAB converters can be explained by the unified equivalent circuit shown in Figure 3, picking V_{eq} from Table 1 for the decisive factors.

For instance, at the t_1 instant of TPS in Figure 2c, the lower device S_4 turns on and the upper device S_3 turns off in the right leg. In the adjacent leg, the lower device S_2 is kept on. Meanwhile, the port voltage on the opposite side, $V_{port}{}'$, is negative. Thus, the switching at t_1 corresponds to case #23. As shown in the table, the counterpart case of #23 is #13, in which the upper device turns on in the right leg, the upper device in the adjacent leg is kept on and $V_{port}{}'$ is positive. Since the upper device in the adjacent leg is kept off in #23, the t_1 instant cannot be explained by the given circuit directly. However, the switching process of #23 can be completely explained by its counterpart case, #13. Thus, the switching transient that happens at t_1 can be explained by the unified equivalent circuit with conditions described for case #13, that is, $V_{eq} = +V_{port}{}' = NV_2$.

Table 1. List of all possible combinations of switching cases and the corresponding results of V_{eq} in phase-shift modulations.

#	Switching Leg	Switching Motion	Device in Adjacent Leg	V_{port}'	V_{eq}
1	left	S_U turns on, S_L turns off	upper on	+	$-V_{port}'$
2				−	$+V_{port}'$
3				0	0
4			lower on	+	refer to #8
5				−	refer to #7
6				0	refer to #9
7		S_U turns off, S_L turns on	upper on	+	$-V_{port}'$
8				−	$+V_{port}'$
9				0	0
10			lower on	+	refer to #2
11				−	refer to #1
12				0	refer to #3
13	right	S_U turns on, S_L turns off	upper on	+	$+V_{port}'$
14				−	$-V_{port}'$
15				0	0
16			lower on	+	refer to #20
17				−	refer to #19
18				0	refer to #21
19		S_U turns off, S_L turns on	upper on	+	$+V_{port}'$
20				−	$-V_{port}'$
21				0	0
22			lower on	+	refer to #14
23				−	refer to #13
24				0	refer to #15

It should be mentioned that the above discussion only involves the condition where one leg has switching motion. In SPS and EPS modulations, the conditions where two legs are manipulated simultaneously also existed; for instance, the switching at t_1 in SPS shown in Figure 2a and the switching at t_2 in EPS shown in Figure 2b. However, these conditions in EPS are usually not the critical switchings for ZVS. When these conditions become the critical switchings in SPS, other advanced modulations are usually used to take the place of SPS. Therefore, the conditions with one leg being manipulated are focused on in most of studies for ZVS in DAB converters and this paper does not pay much attention to the analysis of the conditions with two legs being manipulated.

3. Improved Charge-Based Method and Dead-Time Estimation

3.1. Concept of Minimal Switching Current

The most fundamental condition for realizing ZVS by the current-based method is the current direction at turn-on switching being negative (source to drain). Thus, the corresponding direction of the inductor current at the switching instant can be a sole judgement factor for ZVS. However, in practical converters, the parasitic capacitance and snubber capacitors connected to the devices in parallel need to be discharged by the end of

the dead time to achieve ZVS. Therefore, the time for discharging and the dead time should be considered to judge the ZVS. This paper introduces a method considering both aspects. The improved charge-based method is extended to estimate the appropriate dead time.

With the knowledge introduced in the last section, all the switching instances under the condition of one leg being manipulated in DAB converters can be explained by the unified equivalent circuit in Figure 3. Furthermore, all of these switching instants can be classified into two cases in equivalent circuits where the upper device, S_U, is turning on or the lower device, S_L, is turning on. The circuits of these two cases are shown in Figure 4. The correct current direction to achieve ZVS based on the current-based method is assumed at the beginning of the dead time, and the current paths for the charging and discharging of the parasitic capacitance are drawn as dashed lines in the circuit diagrams with the direction.

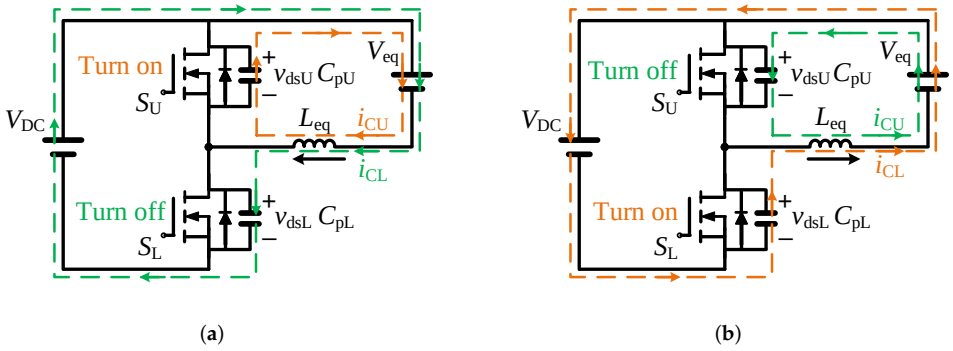


Figure 4. Equivalent circuits for analyzing ZVS: (**a**) for S_U turning on and (**b**) for S_L turning on. The required initial directions of currents to achieve ZVS are also shown in the circuits.

The voltages across S_U and S_L are defined as v_{dsU} and v_{dsL}, respectively. In the action shown in Figure 4a, for instance, C_{pU} is charged at the dc-side voltage; therefore, $v_{dsU} = V_{DC}$, and $v_{dsL} = 0$ at the beginning of the process. Then, v_{dsL} is increased by charging C_{pL} and v_{dsU} is decreased by discharging C_{pU} when the direction of the inductor current is the right direction. After a certain period, the charging and discharging are completed. To achieve a zero-voltage turning-on of S_U, it should be turned on after v_{dsU} becomes zero. After v_{dsU} becomes zero, the remaining current flowing through the inductor conducts through the free-wheeling diode of S_U for a while. To achieve ZVS, S_U should be turned on during this period, where v_{dsU} is kept at zero. A similar derivation can be obtained for the case where S_L is turned on with the current direction shown in Figure 4b. To ensure the remaining current flows through the body diode after the charging and discharging, a certain amount of the initial current in the inductor is indispensable.

This paper involves a concept of minimal switching current, I_m, that is the minimum required current flowing through the inductor at the beginning of the dead time to complete the charging and discharging. With this current at the beginning of the dead time, the inductor current becomes exactly zero when the charging and discharging process is completed. With this condition, the end of the dead time can only be set at the instant when the inductor current reaches zero. Both longer and shorter dead times than this result in losing ZVS.

3.2. Derivation of Minimal Switching Current

Here, the case shown in Figure 4a with S_U turning on is taken as a representative case in the following analysis. Considering the energy conservation in the equivalent circuit, the initial energy stored in the parasitic capacitance of the devices and the inductor should be equal to the sum of the final energy stored in them and the energy transferred to dc voltage sources. By assuming that the same type of devices are used for both the upper and lower arms, the electrostatic energy stored in C_{pU} at the beginning of the instant is totally equal to that in C_{pL} at the end; therefore, these parts can be canceled. If the initial inductor

current is equal to the minimal switching current I_m, the magnetic energy stored in the inductor becomes zero at the end of the transient; therefore, the initial magnetic energy in the inductor is equal to the energy transferred to the voltage sources as

$$\frac{1}{2}L_{eq}{I_m}^2 = E_{dc}, \tag{1}$$

where E_{dc} is the energy transferred to two dc voltage sources during the charging and discharging process.

The equivalent circuit shown in Figure 4a represents the case of upper device, S_U, turning on. E_{dc} in this condition, $E_{dc(S_{U\_on})}$, can be derived as

$$E_{dc(S_{U\_on})} = \int_{t_a}^{t_b} \left(- V_{DC} i_{CL}(t) + V_{eq} i_L(t) \right) dt, \tag{2}$$

where i_{CL} and i_L are the currents flowing through the dc voltage sources V_{DC} and V_{eq}, respectively. t_a and t_b are the time of the beginning and the end of the charging and discharging, respectively. In the equivalent circuits, the direction of V_{eq} represents the polarity when the equivalent port voltage on the other side bridge takes positive. i_L can be derived as

$$i_L(t) = i_{CU}(t) + i_{CL}(t), \tag{3}$$

where i_{CU} is the discharging current of C_{pU} and i_{CL} is also the charging current of C_{pL}. i_{CL} and i_{CU} can be expressed as

$$\begin{cases} i_{CL} = C_{pL}(v_{dsL}) \dfrac{d}{dt} v_{dsL} = C_p(v_{dsL}) \dfrac{d}{dt} v_{dsL}, \\ i_{CU} = -C_{pU}(v_{dsU}) \dfrac{d}{dt} v_{dsU} = C_p(V_{DC} - v_{dsL}) \dfrac{d}{dt} v_{dsL}, \end{cases} \tag{4}$$

where C_p is a universal expression for parasitic capacitance; therefore, S_U and S_L can be represented by the same function of C_p. C_p is usually a function of its drain–source voltage. As a result, the inductor current can be expressed as

$$i_L = \left[C_p(v_{dsL}) + C_p(V_{DC} - v_{dsL}) \right] \frac{d}{dt} v_{dsL}. \tag{5}$$

The total transferred charge by i_{CL} and i_L are defined as ΔQ_{CL} and ΔQ_L, respectively, and can be calculated as

$$\begin{cases} \Delta Q_{CL} = \displaystyle\int_{t_a}^{t_b} i_{CL}(t) dt = \int_0^{V_{DC}} C_p(v) dv, \\ \Delta Q_L = \displaystyle\int_{t_a}^{t_b} i_L(t) dt = \int_0^{V_{DC}} \left[C_p(v) + C_p(V_{DC} - v) \right] dv. \end{cases} \tag{6}$$

In general, the transferred charge through a device with the voltage charging from 0 to V can be expressed as

$$Q(V) = \int_0^V C_p(v) dv, \tag{7}$$

and its value can usually be obtained from device data-sheets. By using (7), ΔQ_{CL} and ΔQ_L in (6) can be expressed as

$$\begin{cases} \Delta Q_{CL} = \displaystyle\int_0^{V_{DC}} C_p(v) dv = Q(V_{DC}), \\ \Delta Q_L = \displaystyle\int_0^{V_{DC}} 2C_p(v) dv = 2Q(V_{DC}), \end{cases} \tag{8}$$

By using (6) and (8), (2) can be rewritten as

$$E_{\mathrm{dc}(S_{\mathrm{U\_on}})} = \int_0^{V_{\mathrm{DC}}} \left[-V_{\mathrm{DC}} C_{\mathrm{p}}(v) + 2V_{\mathrm{eq}} C_{\mathrm{p}}(v) \right] dv = (-V_{\mathrm{DC}} + 2V_{\mathrm{eq}}) Q(V_{\mathrm{DC}}). \quad (9)$$

I_{m} for the case of the upper device turning on, $I_{\mathrm{m}(S_{\mathrm{U\_on}})}$, can be derived as

$$I_{\mathrm{m}(S_{\mathrm{U\_on}})} = \sqrt{\frac{2E_{\mathrm{dc}(S_{\mathrm{U\_on}})}}{L_{\mathrm{eq}}}} = \sqrt{\frac{2(2V_{\mathrm{eq}} - V_{\mathrm{DC}}) Q(V_{\mathrm{DC}})}{L_{\mathrm{eq}}}}. \quad (10)$$

When the practical voltage ratio of $0.5 < k < 2$ and $V_{\mathrm{eq}} = +{V_{\mathrm{port}}}'$, which gives $2V_{\mathrm{eq}} - V_{\mathrm{DC}} > 0$, is assumed, $E_{\mathrm{dc}(S_{\mathrm{U\_on}})} > 0$ is achieved. For example, case #13 in Table 1 can be a representative of this condition. On the contrary, when $V_{\mathrm{eq}} = -{V_{\mathrm{port}}}'$, as is the case of #14, $E_{\mathrm{dc}(S_{\mathrm{U\_on}})} < 0$ is achieved. It is obvious that, when $E_{\mathrm{dc}(S_{\mathrm{U\_on}})} < 0$, a valid $I_{\mathrm{m}(S_{\mathrm{U\_on}})}$ is not available.

The same derivation can be performed in the equivalent circuit shown in Figure 4b with S_{L} turning on. The energy transferred to the voltage sources of the equivalent circuit for the case of the lower device turning on, $E_{\mathrm{dc}(S_{\mathrm{L\_on}})}$, and the minimal switching current in this condition, $I_{\mathrm{m}(S_{\mathrm{L\_on}})}$, can be derived as

$$E_{\mathrm{dc}(S_{\mathrm{L\_on}})} = \int_0^{V_{\mathrm{DC}}} \left[V_{\mathrm{DC}} C_{\mathrm{p}}(v) - 2V_{\mathrm{eq}} C_{\mathrm{p}}(v) \right] dv = (V_{\mathrm{DC}} - 2V_{\mathrm{eq}}) Q(V_{\mathrm{DC}}), \quad (11)$$

and

$$I_{\mathrm{m}(S_{\mathrm{L\_on}})} = \sqrt{\frac{2E_{\mathrm{dc}(S_{\mathrm{L\_on}})}}{L_{\mathrm{eq}}}} = \sqrt{\frac{2(V_{\mathrm{DC}} - 2V_{\mathrm{eq}}) Q(V_{\mathrm{DC}})}{L_{\mathrm{eq}}}}. \quad (12)$$

When the practical voltage ratio of $0.5 < k < 2$ and $V_{\mathrm{eq}} = +{V_{\mathrm{port}}}'$, as is the case of #1, for instance, which gives $V_{\mathrm{DC}} - 2V_{\mathrm{eq}} < 0$, $E_{\mathrm{dc}(S_{\mathrm{L\_on}})} < 0$ is achieved. On the contrary, when $V_{\mathrm{eq}} = -{V_{\mathrm{port}}}'$, as is the case of #20, $E_{\mathrm{dc}(S_{\mathrm{L\_on}})} > 0$ is achieved. Additionally, when $E_{\mathrm{dc}(S_{\mathrm{L\_on}})} < 0$, a valid $I_{\mathrm{m}(S_{\mathrm{L\_on}})}$ is not available.

In conclusion, all of the possible switching instances with one-leg manipulation can be classified into two categories: $E_{\mathrm{dc}} > 0$ and $E_{\mathrm{dc}} < 0$. The schematic and example waveforms of the drain–source voltages and the inductor current with a long enough dead time for these two categories are shown in Figure 5. $E_{\mathrm{dc}} > 0$ means that the dc voltage sources receive energy from the inductor; therefore, the current at the end of the charging and discharging process becomes closer to zero than that at the beginning, as shown in Figure 5a. This clearly indicates that a certain positive value of I_{m} is needed to complete the charging and discharging with this current, where the positive value for I_{m} means the correct direction for ZVS based on the current-based method. On the other hand, $E_{\mathrm{dc}} < 0$ means that the dc voltage sources give out energy to the inductor; therefore, the current at the end of the charging and discharging process becomes farther from zero than that of the beginning as shown in Figure 5b. Hence, even zero initial current can realize ZVS and any correction for ZVS in practical condition is not needed. That is the reason why I_{m} does not have an available solution in the case of $E_{\mathrm{dc}} < 0$.

3.3. Lowest Switching Current Control

Once I_{m} at a specific switching instant is deduced, a strategy called lowest switching current control, which is proposed in [23], can be used to control the current at this instant to be equal to a given reference, which is defined as ${I_{\mathrm{m}}}^*$. This is a modification of the conventional modulations that manipulates the current at some switching instances slightly based on the model of the circuit with known parameters. This method is only available for the modulations which have two or more degrees of control freedom, such as EPS and TPS, since the switching current must be modified without changing the transferred power. At the very least, ${I_{\mathrm{m}}}^* > I_{\mathrm{m}}$ is needed. In addition, it should be mentioned that an appropriate

margin should be included into $I_m{}^*$ to ensure ZVS for both the possible control error of the lowest switching current and the variations in circuit parameters and operating conditions.

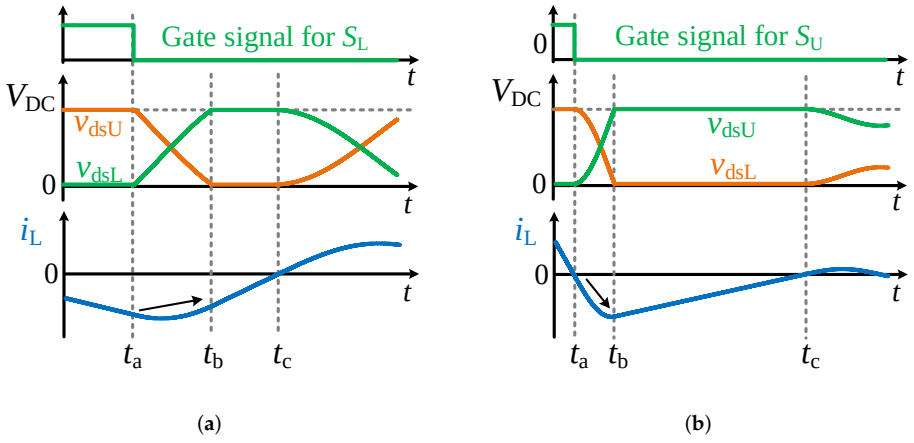


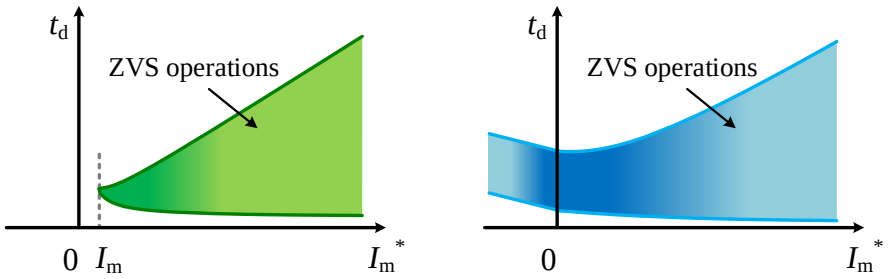
Figure 5. Schematic waveforms of the drain–source voltages and the inductor current with a long enough dead-time period of critical switchings, (**a**) for the condition of $E_{dc} > 0$, and (**b**) for the condition of $E_{dc} < 0$.

3.4. Range of Dead-Time Duration for ZVS

All the above analyses focus on the initial current value at the beginning of the dead time, t_a. It is also important to discuss the end instant of the dead time. Here, we also took the two categories of $E_{dc} > 0$ and $E_{dc} < 0$ as different cases to analyze. It can be seen from the schematic waveforms shown in Figure 5 that the current conducts the free-wheeling diode of S_U (or S_L) after the charging and discharging process is completed at t_b. The switch voltages are clamped until i_L reaches zero at t_c. Consequently, the dead time should be ended between t_b and t_c, and the dead-time duration, t_d, should be longer than $t_b - t_a$ and shorter than $t_c - t_a$.

The allowable range of the dead time for ZVS depends on the initial current. This paper assumes that the initial current is successfully controlled to be equal to $I_m{}^*$. The range of the dead time can be a function of $I_m{}^*$. It is difficult to solve the charge and discharge duration algebraically; however, it is enough to analyze it by a numerical approach for the purpose of suggesting the appropriate dead time, since it only depends on the almost fixed circuit parameters, including dc source voltages and the characteristics of the parasitic capacitance.

Figure 6 shows the schematic view of the range of the dead-time duration, t_d, for ZVS as function of $I_m{}^*$. There is a lower limit, which corresponds to $t_b - t_a$, and an upper limit, which corresponds to $t_c - t_a$. As discussed in Section 3.2, there is a certain positive value of minimal switching current, I_m, under the condition of $E_{dc} > 0$. With this minimal switching current condition, the charging and discharging process is ended when the current reaches zero; therefore, the lower and upper limits become equal, as shown in Figure 6a. Consequently, there is no ZVS area below this initial current under $E_{dc} > 0$. On the other hand, there is no limitation related to the initial switching current under $E_{dc} < 0$, as shown in Figure 6b; therefore, the ZVS range still exists around zero initial current and even in the negative initial current range in principle. With the negative initial current, an extra time period before t_a, in which the charging and discharging of the parasitic capacitance are not started, is included in the dead time. Therefore, both the lower and upper limits of the dead time linearly increased for as long as the increase in $|I_m{}^*|$, as shown in Figure 6.



(**a**) (**b**)

Figure 6. Schematic view of the range of dead-time durations, t_d, as function of $I_m{}^*$ in the conditions of (**a**) $E_{dc} > 0$ and (**b**) $E_{dc} < 0$.

The results shown in Figure 6 suggest that a wider range of dead-time durations to achieve ZVS can be available by setting a high value for $I_m{}^*$. Therefore, a large margin of $I_m{}^*$ is good for ZVS realization in both aspects—enough of an initial switching current and appropriate dead-time value.

Furthermore, it can be found that the allowable range of t_d for ZVS under the condition of $E_{dc} > 0$ is narrower than that under $E_{dc} < 0$ in general. This is due to the fact that $|i_L|$ decreases under $E_{dc} > 0$, while it increases under $E_{dc} < 0$, as can be seen from Figure 5. The narrower range of t_d makes it more difficult for the switching under $E_{dc} > 0$ to achieve ZVS than that under $E_{dc} < 0$.

4. Experimental Verification of ZVS Realization

4.1. Experimental Setup

To verify that the evaluation of ZVS by improved charge-based method and dead-time estimation is effective, a laboratory prototype of the DAB converter with the power rating of 4 kW was fabricated as shown in Figure 7. Table 2 shows the specifications of the fabricated DAB converter.

Table 2. Specifications of 4 kW Prototype of DAB Converter.

Rated power	P	4 kW
Switching frequency	f_{sw}	20 kHz
Input voltage	V_1	270 V ($k = 0.67$) 400 V ($k = 1.5$)
Output voltage	V_2	400 V ($k = 0.67$) 270 V ($k = 1.5$)
Leakage inductance	L	61 µH
Transformer winding ratio	$1 : n$	1 : 1
Type of devices		C3M0025065D

The DAB converter can be operated, for instance, in EPS modulation. It should be mentioned that, in other modulations, operations with one-leg manipulations will achieve the same results. The switching instant at t_4 of EPS, as shown in Figure 2b, is the critical switching. The critical switchings in the condition of $k < 0$ and $k > 0$ exactly correspond to cases #13 and #8 in Table 1. Two different settings of the voltage ratio, $k = 0.67$ and $k = 1.5$ with the power flow from the primary to secondary side, which represent the condition $E_{dc} > 0$ and $E_{dc} < 0$, respectively, are taken as examples.

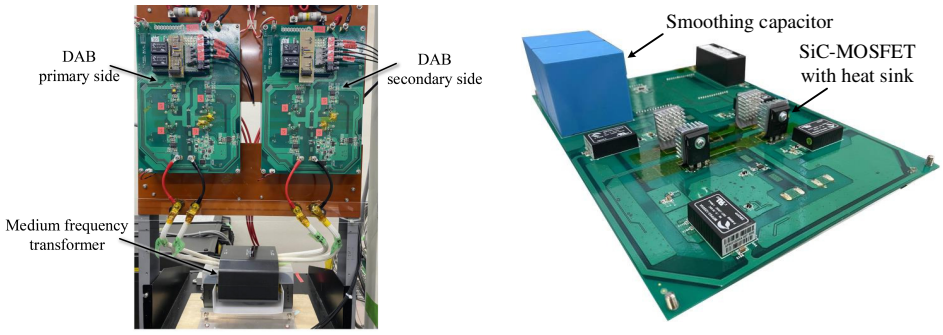


Figure 7. Overview of (**a**) fabricated 4 kW experimental setup and (**b**) back side of the single DAB board.

4.2. Estimation of Minimal Switching Current and Dead-Time Range for ZVS

To verify the feasibility of the proposed method for ZVS realization in the practical condition, the lowest switching current control was tested in the fabricated converter. Prior to the experiments, the minimal switching current, I_m, and the dead-time range for ZVS with the parameters of the fabricated converter were estimated in both settings. As discussed in Section 3.2, the constraint of the minimum switching current exists in the condition of $E_{dc} > 0$, with $V_{DC} = 400$ V, and $Q(V_{DC})$ can be calculated as 137 nC by using (7) and the C–V characteristics of the device. Thus, the theoretical minimal switching current, I_m, for $k = 0.67$ is calculated as 0.8 A by using (10). Due to the dc voltage giving out energy to the inductor in the condition of $E_{dc} < 0$ with $V_{DC} = 400$ V, $I_m = 0$ A is assumed in this paper without any correction for ZVS in the practical condition.

The lower and upper limits of the dead-time duration, t_d, as a function of the initial switching current were also estimated. The estimation was performed numerically since the algebraic derivation of the duration is complicated. The numerical analysis was in the time domain and based on the given initial circuit parameters at the beginning of the dead time. It also considered the voltage-dependent parasitic capacitance, which is represented by the C–V characteristics of the device.

The estimation results of the dead-time range for both $k = 0.67$ and $k = 1.5$ are shown in Figure 8 as solid lines. Figure 8a also confirmed that the upper and lower limits meet at I_m = 0.8 A.

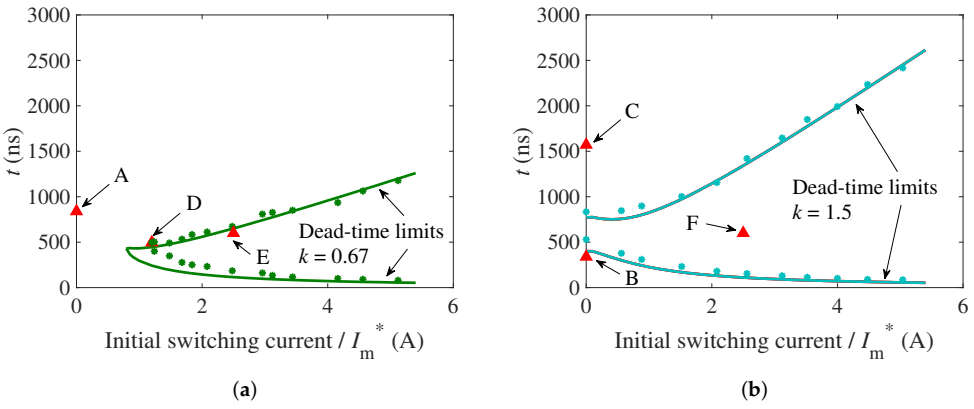


Figure 8. Lower and upper limits of the dead-time duration for ZVS shown as solid lines, and experimentally measured boundary operating points shown as star marks in the conditions of (**a**) $k = 0.67$ ($E_{dc} > 0$), and (**b**) $k = 1.5$ ($E_{dc} < 0$). Some example operating points discussed in this section are marked as A, B, C, and D, and resulting settings for operations are marked as E and F.

4.3. Verification of ZVS Realization with Lowest Switching Current Control

4.3.1. operations without Lowest Switching Current Control

To verify that the ZVS cannot be achieved without considering the parasitic capacitance and dead-time period, some operations with the initial switching current controlled to be zero were tested. These operating points are indicated in Figure 8 as A, B, and C. To observe the critical switching transients, the reference power was set at 2000 W for all the operations of A, B, and C.

The experimentally measured zoomed waveforms during the dead time of the critical switching transients are shown in Figure 9. These include the drain–source voltage of the device to be turned on, v_{dsU} in Figure 9a, v_{dsL} in Figure 9b,c, the transformer current, i_L, and the gate signals for S_U and S_L instead of the gate–source voltages. It can be seen that the converter did not achieve zero voltage turn-on at those switching transients. In operation A, in which the initial switching current is equal to zero under $E_{dc} > 0$, the discharging of v_{dsU} was not completed by the time that i_L becomes zero; therefore, there was no chance of achieving ZVS, even by controlling t_d. In operation B, in which t_d is lower than the lower limit under $E_{dc} < 0$, the discharging was slowly continuing with increasing i_L; however, there was not enough dead time to complete the discharging. In operation C, in which t_d was higher than the upper limit, the dead time was too long so that the recharging of v_{dsL} was observed.

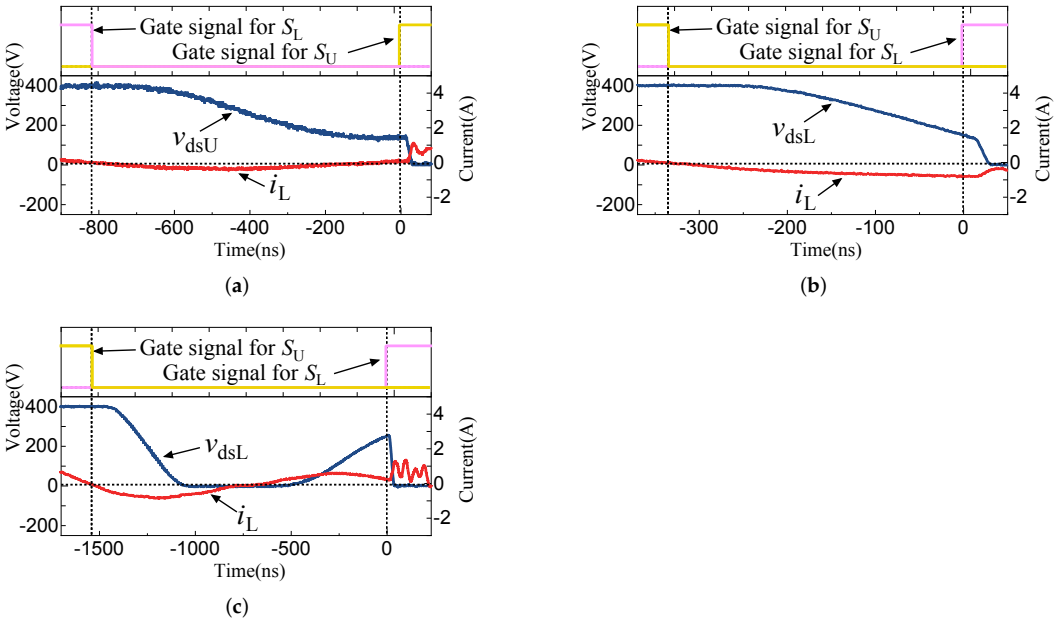


Figure 9. Zoomed waveforms around critical switching transients with the operating points outside of dead-time range for ZVS as example points, (**a**) marked as A, (**b**) marked as B, and (**c**) marked as C in Figure 8.

4.3.2. Verification of Dead-Time Range for ZVS

To verify the theoretical calculation of the limits, the boundary operations of the ZVS were searched experimentally. Specifically, the lower and upper limits of t_d were identified by observing the waveforms when changing the initial switching current. During the experiments, the reference powers were set at 2000 W for both $k = 0.67$ and $k = 1.5$. The experimentally observed lower and upper limits of t_d for $k = 0.67$ and $k = 1.5$ are shown in Figure 8 as marks. The trend of experimental results agreed with the calculated boundaries. Both the calculated and experimental results verify that the dead-time range in $E_{dc} > 0$ is narrower than that under $E_{dc} < 0$. It is much easier to achieve ZVS with a wide dead-time range under the condition of $E_{dc} > 0$.

The operating point with the experimental minimal switching current in $E_{dc} > 0$ was found at the point of $I_m = 1.2$ A and $t_d = 500$ ns, and is marked as D in Figure 8a. The zoomed waveforms during the dead time of one critical switching transient with this operation are shown in Figure 10. It can be observed from the waveforms that the discharging of v_{dsU} was completed just at the moment when i_L reached 0 A.

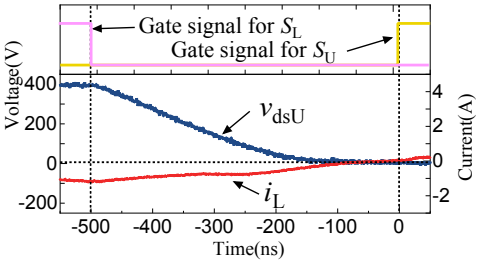


Figure 10. Zoomed waveforms around critical switching transient with the operating point at the experimental minimal switching current indicated as point D in Figure 8a.

4.3.3. Operations with Lowest Switching Current Control and Designed Dead Time

To verify that the ZVS can always be achieved in the operations with a designed initial switching current and the dead time discussed in Section 4.2, two operating points under the lowest switching current control were tested. $I_m{}^*$ were set as 2.5 A for both $k = 0.67$ and $k = 1.5$ considering margins for possible errors. On the other hand, a constant dead time, $t_d = 600$ ns, was set for this setup to ensure that the switching condition is far enough from both limits for any initial switching current. Corresponding settings of $I_m{}^*$ and t_d are marked as E and F in Figure 8.

The zoomed waveforms of the critical switching transients of the operations with the power reference of 2000 W for both $k = 0.67$ and $k = 1.5$ are shown in Figure 11. It can be clearly seen that the drain–source voltage of the device to be turned on discharged completely and the polarity of i_L did not change during the dead-time in both operations. Thus, it is confirmed that ZVS was successfully realized with enough of a margin for this setting.

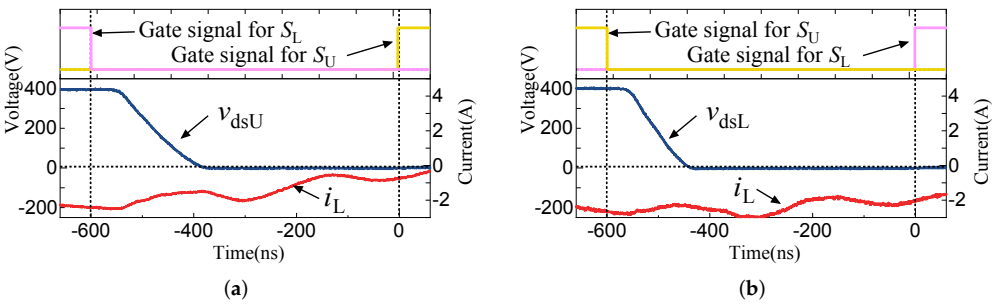


Figure 11. Zoomed waveforms around critical switching transients with enough margin of initial switching current and dead-time as example points (**a**) marked as E, (**b**) marked as F in Figure 8.

5. Conclusions

This paper proposes a unified equivalent circuit to consider all the possible switching instants under the condition of a one-leg manipulation in DAB converters. By using the unified equivalent circuit, an improved charge-based method with dead-time estimation is studied to identify the ZVS realization considering the effect of both the voltage-dependent parasitic capacitance and dead-time period. All equivalent circuits can be divided into two cases, the upper or lower device turning on, and the corresponding equations of the specific initial current, which is defined as the minimal switching current, are deduced. With the different parameters of the circuit, all of the switching instants can be further classified into two categories according to the sign of the energy transferred to dc voltage sources. Based on the classification, the function of the acceptable dead-time range with a switching

current is analyzed and different difficulties for realizing ZVS operations are found in these two categories. A laboratory 4 kW DAB prototype was fabricated to verify that the estimation of ZVS realization by an improved charge-based method is effective. The lowest switching current control when considering enough of a margin of the switching current and dead time can successfully achieve ZVS at critical switching instants. It is much easier to realize ZVS operation with a wider dead-time range by using the category of $E_{dc} < 0$. Thus, during the designing and operating of DAB converters, besides the margin of the switching current and dead time being considered, operations that satisfied $E_{dc} < 0$ are welcomed for easier ZVS realization.

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