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A Step-Up Converter with Large Voltage Gain and Low Voltage Rating on Capacitors

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Abstract: Step-up converters are widely used in many applications, such as renewable energy generation with photovoltaic panels and fuel cell stacks. In many cases, the required voltage gain is larger for those applications than a traditional boost converter can achieve. Several large-voltage gain converters have been recently studied. This paper introduces a converter topology in which the voltage gain is larger than a traditional boost converter. The main advantages of the proposed topology are: *(i)* it provides a large voltage gain without the use of an extreme duty cycle; *(ii)* its capacitors require a smaller voltage to be sustained compared with other, similar state-of-the-art converters; *(iii)* the voltage among the ground input and output is not pulsating; and *(iv)* it can be synthesized with commercial, off-the-shelf half-bridge packed transistors. The proposed converter can be employed in different applications, such as distributed generation and microgrids. This paper presents the steady-state analysis of the proposed converter in the continuous conduction mode, a short comparison with similar topologies, and their voltage on capacitors. Computer-based simulation results are provided to verify the principle of the proposed converter in different operating conditions.

Keywords: DC–DC converter; PWM power conversion; voltage rating; continuous conduction mode (CCM); step-up converter

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1. Introduction

Several applications require a large voltage-gain DC–DC converter; one of the emerging applications is the generation of electricity from renewable energy sources, such as photovoltaic (PV) panels and fuel cell (FC) stacks. Power electronic converters are used to customize the electrical energy from those sources to the characteristics required to feed electrical appliances or inject power into the utility grid [1–5].

In some applications, particularly in renewable energy generation with PV panels and FC stacks, a power converter requires a relatively large voltage gain, those sources provide a DC voltage in low amplitude, and a larger amplitude (well-regulated) is usually required to feed an inverter, the last converter of which can feed appliances or inject power into the grid. A DC–DC step-up converter is usually required, and in some cases, the required voltage gain of the DC–DC converter is usually larger than what a traditional boost converter can achieve [5–8].

A traditional boost converter meets limitations when the voltage gain is larger than five due to parasitic components in power semiconductors and passive components [6–8]; this is why, in some cases, the integrated circuit (IC) controllers of power converters have a maximum duty cycle of 0.8 [8].

Several large-voltage gain converters have been recently studied; this article focuses on converters without magnetic coupling (without transformers or coupled inductors). Transformer-less converters can be used as a base to develop transformer-based converters. Figure 1 shows a recent contribution, a converter introduced in [9] with two equal inductors that are charged in parallel and discharged in series, splitting the power into two paths with a low parasitic resistance. Due to its advantages, its structure has been used as a base to develop other topologies [9–13].

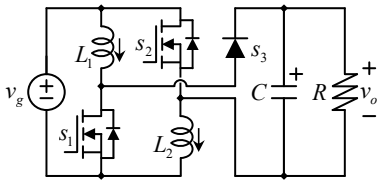

Figure 1. One of the boost-type topologies in [9].

This paper introduces a two-transistor-based, transformer-less DC–DC converter topology whose main advantages are: *(i)* it provides a large-voltage gain without the use of an extreme duty cycle; *(ii)* its capacitors require a smaller voltage to be sustained compared with other similar, state-of-the-art converters; *(iii)* the voltage among the ground input and output is not pulsating; and *(iv)* it can be synthesized with commercial, off-the-shelf half-bridge packed transistors if synchronous rectification is preferred.

Two capacitors provide the output voltage in additive series with the input power source, which results in the voltage sustained by capacitors being smaller than the output voltage, which allows for the use of smaller capacitors for the same power rating since the physical size of capacitors depends on the stored electrical energy, which depends on the square of their voltage [14–16]. The steady-state analysis of the proposed converter in the continuous conduction mode is presented here. This paper also presents a design procedure that includes the selection of capacitors and inductors, as well as their maximum voltage and current values for an application example. The converter is compared to other converters in the literature. Finally, computer-based simulation results are provided to verify the operation principle of the proposed converter.

2. Proposed Converter Topology

Figure 2a shows the proposed topology. Their step-up unidirectional version contains two inductors (L_1 and L_2), two capacitors (C_1 and C_2), two transistors (s_1 and s_2), and two diodes (s_{n1} and s_{n2}). As in other DC–DC converter topologies, the basic topology (Figure 2a) has a unidirectional power flow since diodes can drain current in one direction. However, with the addition of antiparallel transistors with diodes, what we call synchronous rectification provides bidirectional power flow (along with a possibly better efficiency). The bidirectional version of the converter is shown in Figure 2b.

The connection of the topology allows for operation with two capacitors whose voltage is smaller than the output voltage, as further explained in the paper. Furthermore, the voltage from the input reference to the output reference is floating, as in other state-of-the-art topologies (see Figure 1), but in this case, the voltage is non-pulsating, which reduces the noise and common mode current. Another advantage of the proposed topology is that their bidirectional power-flow configuration can be made with two half-bridges, which are commercial, off-the-shelf products.

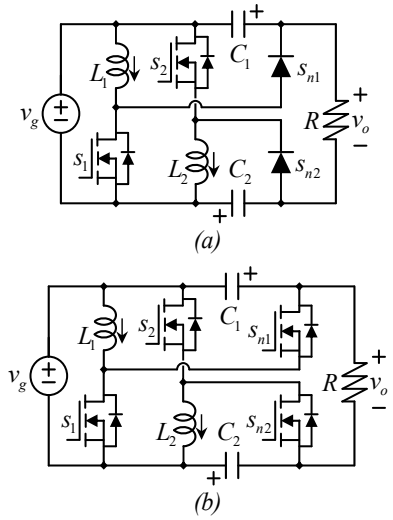

Figure 2. Proposed circuit: (**a**) unidirectional power flow and (**b**) bidirectional power flow.

By applying Kirchhoff's voltage law in the external loop of the circuit in Figure 2 and considering the polarities defined for voltage in capacitors, the output voltage can be expressed as (1).

$$v_o = v_g + v_{C1} + v_{C2} \tag{1}$$

An important note about the circuit (see Figure 2 and Equation (1)), as further explained later, is that no capacitor sustains the output voltage.

In this case, the output voltage is provided by the summation of the input voltage source and two series-connected capacitors. In other topologies available in the literature (see Figure 1), a capacitor is rated to the output voltage. This capacitor may store a significant amount of energy, which is related to the size of the capacitor.

Transistors of the proposed converter have the same switching functions. In the continuous conduction mode (CCM), this operation leads to two possible equivalent circuits according to the switching state; see Figure 3. The current direction and voltage polarities follow the passive components' sign convention.

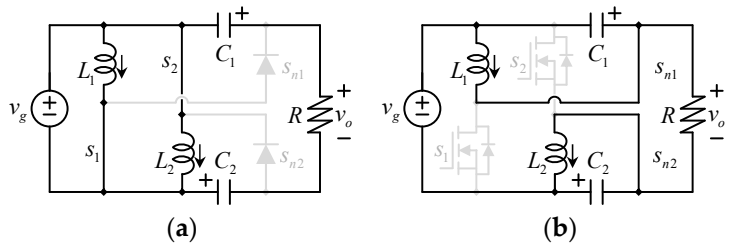

Figure 3. Equivalent circuits, according to the switching state, (**a**) when transistors are closed and (**b**) when transistors are open.

2.1. Theoretical Waveforms

Figure 4 shows the theoretical waveforms for inductors from top to bottom, respectively: the inductors' currents (i_{Lx}, x = 1, 2.), the inductors' voltages (v_{Lx}, x = 1, 2.), and the firing signals (s_x, x = 1, 2.); both inductors have similar waveforms. The firing signal is a digital signal that switches from high to low, thus closing and opening switches.

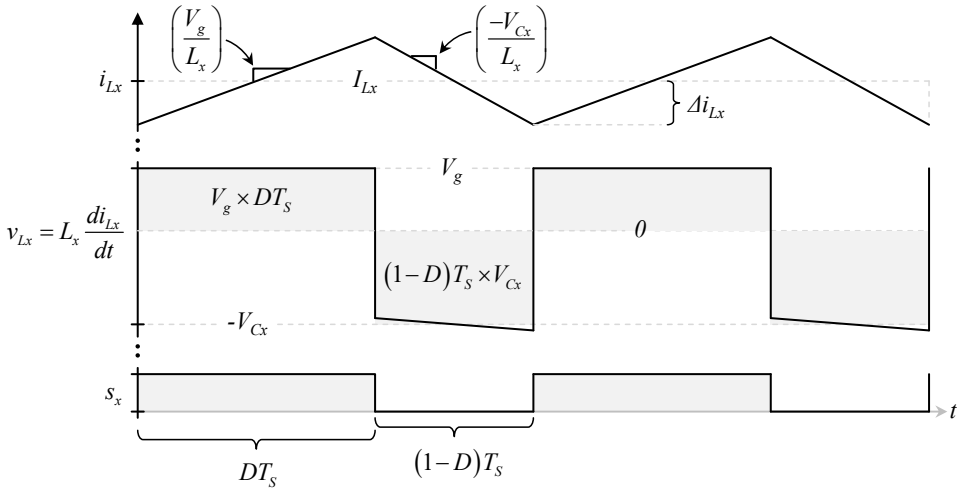

Figure 4. Important waveforms related to the inductor from top to bottom, respectively: inductor current, inductor voltage, and switching function.

The inductor voltage is a DC signal whose average value is I_L, and it has a triangular switching ripple that can be explained in the following manner: when switches are closed, the converter behaves as in Figure 3a. Inductors are connected to the input voltage V_g, and the current through inductors rises with a slope of (V_g/L_x). When switches are open, the converter behaves as in Figure 3b. Inductors are connected to their respective capacitors (C_x, x = 1, 2.), and the current through inductors decreases with a slope of $(-V_{Cx}/L_x)$.

The voltage through inductors looks like a rectangular waveform. The steady state is reached when the area under the curve during the first semi-cycle ($V_g DT_S$) equals the area under the curve during the second semi-cycle ($(1 - D)T_S(V_{Cx})$).

It is considered that the input voltage is a DC signal, so the rising slope of the current is almost constant. Something similar happens to the falling slope. During this time, the capacitor is charging and the negative voltage across the inductor is decreasing (becoming more negative). As can be seen, we could choose to have a very small voltage ripple (for example, 1%) the capacitor, which would make the signal look rectangular.

Figure 5 shows the theoretical waveforms corresponding to capacitors from top to bottom, respectively: the voltages of the capacitors (v_{Cx}, x = 1, 2.), the capacitors' currents (i_{Cx}, x = 1, 2.), and the firing signals (s_x, x = 1, 2.); both capacitors have similar waveforms. The firing signal for transistors is the same as in Figure 4 and is included to give an idea of the synchronization.

When switches are closed, the converter behaves as in Figure 3a. Capacitors are discharged with the output current I_o, and the voltage across capacitors decreases with a slope of $(-I_o/C_x)$. When switches are open, the converter behaves as in Figure 3b. Capacitors are charged with the inductor currents, and the voltage is increasing with a slope of $((I_L - I_o)/C_x)$. The current through capacitors looks like a rectangular waveform. The steady state is reached when the area under the curve during the first semi-cycle ($I_o DT_S$) equals the area under the curve during the second semi-cycle $(1 - D)T_S(I_{Lx} - I_o)$.

Since the current ripple in inductors is usually larger than the voltage ripple in capacitors, the current charging the capacitor has a ripple that seems more significant and the rising slope of the capacitor voltage seems slightly curved.

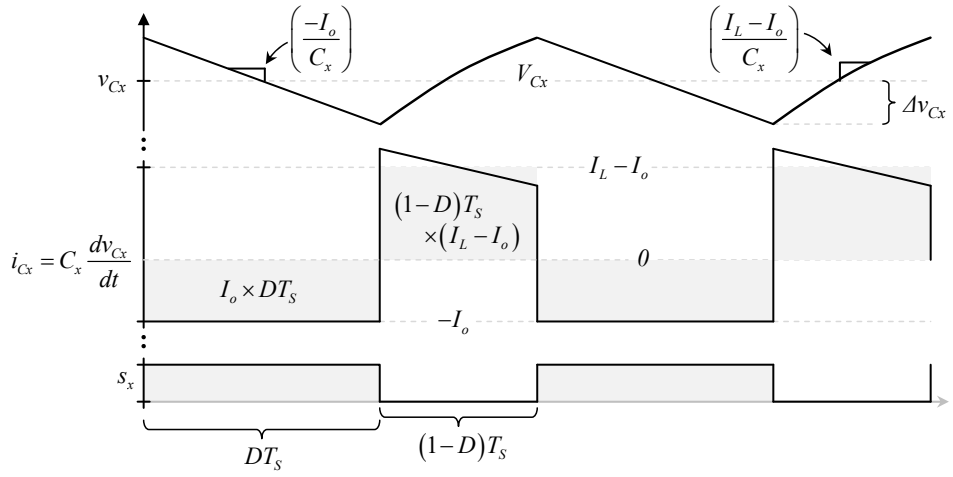

Figure 5. Important waveforms related to the capacitors from top to bottom, respectively: capacitor voltage, current, and switching function.

2.2. Converter's Mathematical Model

Let us now discuss the mathematical model of the converter. With the description of the circuit and the equivalent circuits shown in Figure 2, the standard averaging technique can be used to write the mathematical model of the converter [1–3].

The average voltage across inductors L_1 and L_2 during one switching cycle can be expressed as (2) and (3), respectively.

$$L_1 \frac{di_{L1}}{dt} = d(v_g) + (1-d)(-v_{C1}) \tag{2}$$

$$L_2 \frac{di_{L2}}{dt} = d(v_g) + (1-d)(-v_{C2}) \tag{3}$$

The first term of the right side of Equation (2), dv_g, represents the voltage across L_1 when the transistor is closed (v_g) multiplied by the average time in which the transistor is closed (d). The second term of Equation (2), $(1-d)(-v_{C1})$, represents the voltage across L_1 when the transistor is open ($-v_{C1}$) times the average time in which the transistor is open $(1-d)$.

Similarly, the averaging technique can be applied to the current through capacitors. The average current through capacitors C_1 and C_2 can be expressed as (4) and (5), respectively.

$$C_1 \frac{dv_{C1}}{dt} = d\left(-\frac{v_o}{R}\right) + (1-d)\left(i_{L1} - \frac{v_o}{R}\right) \tag{4}$$

$$C_2 \frac{dv_{C2}}{dt} = d\left(-\frac{v_o}{R}\right) + (1-d)\left(i_{L2} - \frac{v_o}{R}\right) \tag{5}$$

where the first term $d(-v_o/R)$ represents the current through C_1 when transistors are closed $(-v_o/R)$ multiplied by the average time transistors are closed d. The second term in equation (4) represents the current through capacitor C_1 when transistors are open $(i_{L1} - v_o/R)$ multiplied by the average time in which transistors are closed $(1-d)$.

The set of Equations (2) to (5) is the average dynamic model of the converter. Before analyzing the model, Equations (2) to (5) can be simplified by algebraic manipulation and rewritten as Equations (6) to (9).

$$L_1 \frac{di_{L1}}{dt} = dv_g - (1-d)v_{C1} \tag{6}$$

$$L_2 \frac{di_{L2}}{dt} = dv_g - (1-d)v_{C2} \tag{7}$$

$$C_1 \frac{dv_{C1}}{dt} = (1-d)i_{L1} - i_o \tag{8}$$

$$C_2 \frac{dv_{C2}}{dt} = (1-d)i_{L2} - i_o \tag{9}$$

The output current i_o is present in the system and can be expressed in terms of the output voltage (1) and the output resistance R. This model considers CCM operation.

As can be seen from the dynamic model (6)–(9), the average model is non-linear. This also happens to other topologies, such as that of a traditional boost converter; there are several ways to deal with this, such as small AC signal linearization, in which signals are represented by the sum of their DC component plus an AC component, the DC component is usually the equilibrium or steady-state condition (which is introduced in Section 2.3), and the AC component is the component that contains deviations from the equilibrium, such as transient oscillations; this technique was used in [1].

2.3. DC Components of State Equations or Equilibrium Operation Point

From the dynamic Equations (6) to (9), the equilibrium operation point can be calculated considering the small ripple approximation [1], which can be summarized as variables in (6) to (9) appearing in the lower case, indicating that they are not constant values. The small ripple approximation considers that changes on the state variables are negligibly small (during a single switching cycle), which can be accomplished via the good selection of the switching frequency, capacitance in capacitors, and inductance in inductors. In the steady state, the derivative of state variables is zero. Then, after making (6) equal to zero and considering the small ripple approximation, the voltage in C_1 can be expressed as (10).

$$V_{C1} = \frac{D}{1-D} V_g \tag{10}$$

DC values obtained with the small ripple approximation are indicated in capital letters. With the same procedure, from (7), the voltage across C_2 can be expressed as:

$$V_{C2} = \frac{D}{1-D} V_g \tag{11}$$

Then, from (1), (10) and (11), the output voltage can be expressed in the steady state as (12).

$$V_o = V_g \frac{1+D}{1-D} \tag{12}$$

The current through inductors L_2 and L_1 can also be expressed from (9) and (10), respectively, as (13) and (14) from the same procedure that leads to (10) and (11).

$$I_{L2} = \frac{1}{(1-D)} \frac{V_o}{R} \tag{13}$$

$$I_{L1} = \frac{1}{(1-D)} \frac{V_o}{R} \tag{14}$$

We can make some remarks about the obtained result. The voltage gain expressed in (12) is the same as that for the previous converter (the one in Figure 1). Both converters offer a larger voltage gain compared with a traditional boost converter for the same duty cycle. However, an advantage is that capacitors sustain a lower voltage in the proposed converter. Figure 6 shows two graphs: (i) In blue, the voltage gains of the converter as a function of the duty cycle—which is basically (12) divided over the input voltage V_g for the former topology—is the same as the voltage in the output capacitor since the output capacitor sustains the output voltage; (ii) in red, the function of the voltage across capacitors of the proposed converter—basically (10) or (11) divided over the input voltage V_g—is shown to be substantially smaller than the blue graph.

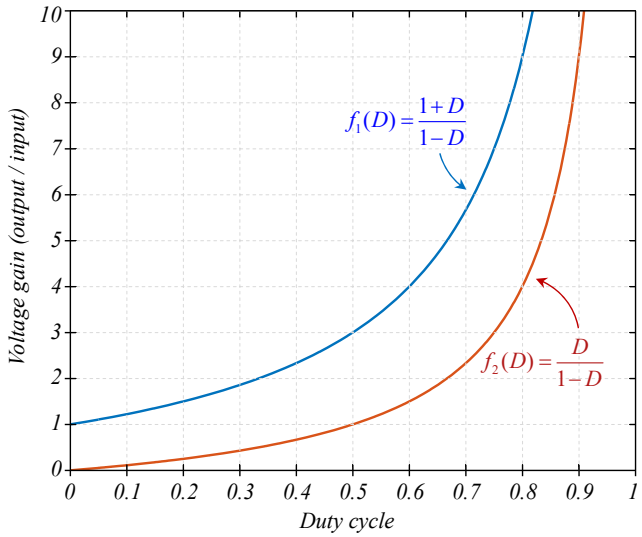

Figure 6. Voltage gains as a function of the duty cycle for the proposed and traditional boost converters.

For example, let us consider a converter that operates with an input voltage of 100 V and an output voltage of 300 V. The former topology would require a capacitor to sustain 300 V, while the proposed topology would require two capacitors of 100 V. We must also consider that the input-to-output reference has a continuous (non-pulsating) voltage.

The stored energy in a capacitor is a function of its voltage and capacitance, according to (15).

$$E_C = \frac{CV_C^2}{2} \tag{15}$$

We can observe the stored energy in a capacitor is proportional to the square of its voltage, for which a reduction in the voltage of a capacitor would result in a reduction in stored energy. Furthermore, the volume of a capacitor is linearly dependent on its stored energy [14–16].

2.4. Selection of Inductors and Capacitors

This section discusses the selection of reactive components based on the maximum ripple allowed for the state variables.

Inductors L_1 and L_2: Both inductors have the classical waveform of inductor current in switched-mode power supplies; this is a DC component plus an AC triangular variation. The DC component depends on the voltage gain (or duty cycle) and the load; see (13) and (14). The variation is usually called ripple, and it depends on more parameters, such as the switching frequency F_S (or their inverse, the switching period T_S), the duty cycle, and the inductance. The inductance is then selected according to the desired ripple as follows.

From Figure 3, it can be seen that when transistor s_1 is on, its terminal voltage is equal to V_g, and then its current rises with a slope equal to V_g/L_1. This situation holds for a time equal to DT_S. In the field of power electronics, the current ripple used to be defined as half of the total current change (half the peak-to-peak ripple). In other words, we consider the ripple as the deviation from the average value of a signal. For the current through an inductor, this can be expressed as (16), and the inductance can be calculated as (17).

$$2\Delta i_{L1} = \frac{V_g}{L_1} DT_S \tag{16}$$

$$L_1 = \frac{V_g}{2\Delta i_{L1}} DT_S \tag{17}$$

Note that the small ripple approximation is considered in (17), and in all reactive elements sizing equations, (17) allows for the selection of L_1 for a desired current ripple in

L_1. Since both switching stages have the same duty cycle, (17) can be used to calculate L_2; in other words, we can make $L_1 = L_2$.

Capacitors C_1 and C_2: Capacitors can be calculated with a similar procedure to that of inductors, but the state variable is instead the voltage; the voltage in capacitors is a DC component plus an AC variation, and the DC component depends on the voltage gain (or duty cycle) and the input voltage. The AC variation depends on other parameters, including the current, switching frequency, and capacitance. The capacitance is then selected according to the desired ripple as follows.

When transistor s_1 is open, the current through capacitor C_1 is equal to the output current. A negative sign may be considered to indicate that the voltage is falling since the capacitor is being discharged, and then its voltage is being reduced with a slope equal to $-I_{out}/C_1$. This situation holds during the time $(1 - D)T_s$, and during this period, the voltage drop can be expressed as Equation (18).

$$-2\Delta v_{C1} = \frac{-I_{out}}{C_1}(1 - D)T_s \tag{18}$$

Negative signs indicate a voltage drop. From (18), the capacitor C_1 can be selected to comply with the desired voltage ripple Δv_{C1} in C_1 by following (19).

$$C_1 = \frac{I_{out}}{2\Delta v_{C1}}(1 - D)T_S \tag{19}$$

Equation (19) allows for the selection of C_1 for the desired voltage ripple in C_1. Since both switching stages have the same duty cycle, (19) can be used to calculate C_2. In other words, we can make $C_1 = C_2$.

2.5. Selection of Semiconductors

The main data needed to choose semiconductors are the voltage they need to block when they are open and the current they drain when they are closed. It can be observed from Figure 3b that both transistors (as well as both diodes) are rated to the same voltage, which is the input voltage plus the voltage in a capacitor; this can be expressed as (20).

$$V_{switch} = V_g + V_C = V_g + \frac{D}{1 - D}V_g = \frac{1}{1 - D}V_g \tag{20}$$

The voltage rating of the switch is expressed with the same function as the voltage rating in a boost converter. Still, due to the different voltage gain functions, the proposed converter requires transistors rated to a smaller voltage, as is shown in Section 5.

Figure 3a shows that the current through transistors when they are closed is equal to the current through inductors. Then, the average current through transistors can be expressed as (21).

$$I_{Switch} = DI_L = \frac{D}{(1 - D)}I_o \tag{21}$$

Again, the current through switches seems equal to that in a traditional boost, but the proposed converter would require a smaller duty cycle to achieve an equivalent voltage gain for which the current rating of transistors is again smaller; see Section 5.

If switches are synthesized with IGBTs, the average current is enough to calculate their conduction losses, but if MOSFETs are used instead, the RMS current is required. The RMS current through transistors can be expressed as:

$$I_{RMS-Switch} = I_L\sqrt{D}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2} \tag{22}$$

Consider here that Δi_L is as defined in (16) and I_L is as defined in (13) and (14).

The average current of diodes can also be determined by considering Figure 3a and using the averaging technique. When closed, the current through diodes is equal to the current through inductors, and the average current through diodes can be expressed as (23).

$$I_{Switch} = (1 - D)I_L = I_o \tag{23}$$

If synchronous rectification is required, the *RMS* current needs to be calculated to evaluate conduction losses. The *RMS* current can be expressed as:

$$I_{RMS-Diode} = I_L\sqrt{(1 - D)}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2} \tag{24}$$

Consider here that Δi_L is as defined in (16) and I_L is as defined in (13) and (14).

3. Gain Considering Losses and Efficiency Calculations

This section analyzes two important aspects of the converter related to power losses. First is the gain considering losses; the real gain may differ from Equation (12) and Figure 6 due to some power losses. Second, the loss calculation in each element of the converter is shown.

3.1. Real Voltage Gain Considering Losses

Figure 7 shows a circuit equivalent to the proposed topology in which ideal elements are drawn with their Equivalent Series Resistance (ESR) to indicate their conduction losses. In this section, the considered elements are inductors and switches since they have dominant effects on the real voltage gain. In the efficiency section, capacitor losses are also calculated. R_{L1} and R_{L2} are the ESR of inductors L_1 and L_2, respectively. R_{S1}, R_{S2}, R_{S1n}, and R_{S2n} are the on-resistance of switches. This model considers the converter to have synchronous rectification; see Figure 2b.

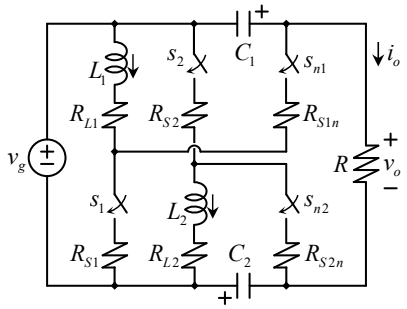

Figure 7. Proposed circuit with series losses through inductors and transistors.

Figure 8 shows the equivalent circuits of the converter according to the switching state; Figure 8a shows the state in which transistors s_1 and s_2 are closed while s_{1n} and s_{2n} are open, and Figure 8b shows the state in which transistors s_{1n} and s_{2n} are closed while s_1 and s_2 are open.

According to those equivalent circuits (see Figure 8), the dynamic equations for inductors (in other words, the average voltage across inductors L_1 and L_2 during one switching cycle) can be expressed as (25) and (26), respectively.

$$L_1\frac{di_{L1}}{dt} = d\left(v_g - i_{L1}R_{L1} - i_{L1}R_{S1}\right) + (1 - d)\left(-v_{C1} - i_{L1}R_{L1} - i_{L1}R_{S1n}\right) \tag{25}$$

$$L_2\frac{di_{L2}}{dt} = d\left(v_g - i_{L2}R_{L2} - i_{L2}R_{S2}\right) + (1 - d)\left(-v_{C2} - i_{L2}R_{L2} - i_{L2}R_{S2n}\right) \tag{26}$$

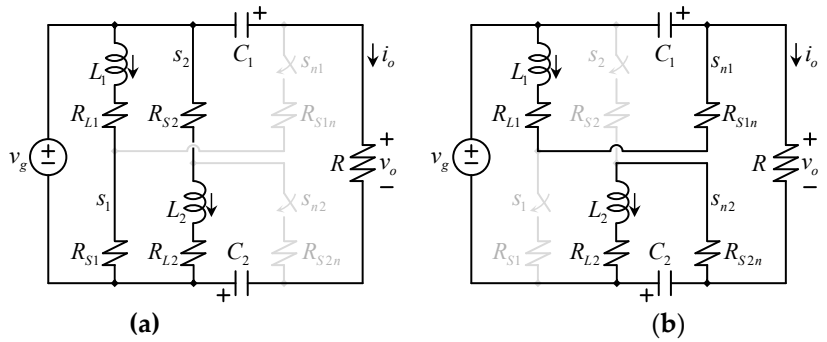

Figure 8. Equivalent circuits according to the switching state. Proposed circuit with series losses through inductors and transistors (**a**) when transistors are closed (**b**) when transistors are open.

Equations (25) and (26) contain the voltage drops in ESR of elements in series with inductors when they are charging and discharging. Similarly, the averaging technique can be applied to the current through capacitors. The average current through capacitors C_1 and C_2 can be expressed as (27) and (28), respectively.

$$C_1 \frac{dv_{C1}}{dt} = d\left(-\frac{v_o}{R}\right) + (1-d)\left(i_{L1} - \frac{v_o}{R}\right) \tag{27}$$

$$C_2 \frac{dv_{C2}}{dt} = d\left(-\frac{v_o}{R}\right) + (1-d)\left(i_{L2} - \frac{v_o}{R}\right) \tag{28}$$

Note that in this case, (27) and (28) are equal to (4) and (5) since there is not a current drop effect. The set of Equations (22) to (28) is the average dynamic model of the converter considering conduction losses. If we consider that all transistors are of the same type, their ESR must be similar. We can call R_S the ESR of all transistors; this allows us to simplify Equations (25) to (28) and rewrite them as Equations (29) to (32).

$$L_1 \frac{di_{L1}}{dt} = dv_g - (1-d)v_{C1} - (R_{L1} + R_S)i_{L1} \tag{29}$$

$$L_2 \frac{di_{L2}}{dt} = dv_g - (1-d)v_{C2} - (R_{L2} + R_S)i_{L2} \tag{30}$$

$$C_1 \frac{dv_{C1}}{dt} = (1-d)i_{L1} - i_o \tag{31}$$

$$C_2 \frac{dv_{C2}}{dt} = (1-d)i_{L2} - i_o \tag{32}$$

In this case, the equilibrium equations cannot be directly obtained, as we did it with (10) and (11) since the current is present in (29) and (30). However, as explained in [1], the current relationships are in the steady state in (31) and (32) and are then substituted to obtain the voltages in equilibrium. Considering the equilibrium operation from (29) and (30), the following expressions can be written.

$$DV_g = (1-D)V_{C1} + (R_{L1} + R_S)I_{L1} \tag{33}$$

$$DV_g = (1-D)V_{C2} + (R_{L2} + R_S)I_{L2} \tag{34}$$

From (31) and (32), the current relationship in the equilibrium can be expressed as (35) and (36).

$$I_{L1} = \frac{1}{(1-D)} I_o \tag{35}$$

$$I_{L2} = \frac{1}{(1-D)} I_o \tag{36}$$

Due to the symmetry of the circuit and Equations (33)–(36), the current through inductors are equal; see (35) and (36). Then, both capacitors have the same voltage; see (33) and (34). We can simplify these to (37).

$$V_C = V_{C1} = V_{C2} \tag{37}$$

By applying the KVL in Figure 7 and considering (37), the output voltage can be expressed as (38).

$$V_o = V_g + V_{C1} + V_{C2} = V_g + 2V_C \tag{38}$$

The output current can also be expressed as (39).

$$I_o = \frac{V_g + V_{C1} + V_{C2}}{R} = \frac{V_g + 2V_C}{R} \tag{39}$$

By substituting (37) with (33), we can obtain:

$$DV_g = (1-D)V_{C1} + (R_{L1} + R_S)\frac{1}{(1-D)}I_o \tag{40}$$

$$DV_g = (1-D)V_{C1} + \left(\frac{R_{L1} + R_S}{1-D}\right)\left(\frac{V_g + 2V_{C1}}{R}\right) \tag{41}$$

$$DV_g = (1-D)V_{C1} + \frac{(R_{L1} + R_S)V_g}{(1-D)R} + \frac{(R_{L1} + R_S)2V_{C1}}{(1-D)R} \tag{42}$$

$$DV_g - \frac{(R_{L1} + R_S)V_g}{(1-D)R} = (1-D)V_{C1} + \frac{(R_{L1} + R_S)2V_{C1}}{(1-D)R} \tag{43}$$

$$V_g\left(D - \frac{(R_{L1} + R_S)}{(1-D)R}\right) = \left((1-D) + \frac{(R_{L1} + R_S)2}{(1-D)R}\right)V_{C1} \tag{44}$$

$$V_{C1} = V_{C2} = V_C = V_g\frac{\left(D - \frac{(R_{L1}+R_S)}{(1-D)R}\right)}{\left((1-D) + \frac{(R_{L1}+R_S)2}{(1-D)R}\right)} \tag{45}$$

Equation (45) provides us with the voltage in each capacitor considering the losses. The real gain depends on the percentage of R_{L1} and R_S concerning the output resistance R. Note that if that parasitic resistance is equal to zero, (45) becomes (10) and (11).

Let us consider that parasitic resistors R_{L1} and R_S are lumped in a single parasitic resistance R_P.

$$R_P = R_L + R_S \tag{46}$$

Figure 9 shows the gain of the converter considering conduction losses as a relation of R_P/R_L, as in Figure 3.9 in [1] for a traditional boost converter.

The relations among R_P/R_L in Figure 9 are relatively high for practical application, but we used the same relations as shown in Figure 3.9 in [1] for reference or a point of comparison. A traditional boost converter achieves a maximum gain of five when $R_P/R_L = 0.01$, while the proposed converter achieves a maximum gain of nine for the same relation.

A traditional boost converter achieves a maximum gain of around 3.5 when $R_P/R_L = 0.02$, while the proposed converter achieves a maximum gain of six for the same relation.

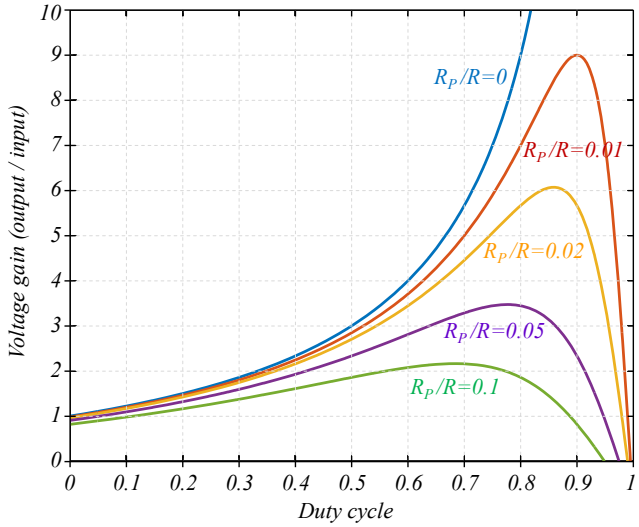

Figure 9. Voltage gains as a function of the duty cycle considering conduction losses in the parasitic resistance of elements.

3.2. Efficiency Analysis

After calculating the new steady state (considering conduction losses), the voltage across capacitors V_{C1} and V_{C2} can be expressed with (45), and the current through inductors I_{L1} and I_{L2} as determined in (35) and (36), the current ripple in inductors Δi_{L1} and Δi_{L2} as expressed in (16), and the voltage ripple in capacitors Δv_{C1} and Δv_{C2} as expressed in (18) can be used to express the losses in each element.

The losses in inductors can be expressed as the RMS current square times their ESR, and the RMS current through inductors L_1 and L_2 can be expressed as (47) and (48).

$$I_{RMS-L1} = I_{L1}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L1}}{I_{L1}}\right)^2} \tag{47}$$

$$I_{RMS-L2} = I_{L2}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L2}}{I_{L2}}\right)^2} \tag{48}$$

The losses in capacitors are usually very small, but they can also be calculated as their RMS current times their ESR. As shown in Figure 5, the current through capacitors has a trapezoidal and rectangular segment. To express the RMS current through the trapezoidal segment, it is convenient to define the maximum current (of the trapezoid) termed I_{Aux1} and the minimum current (of the trapezoid) termed I_{Aux2}, as defined in (49) and (50), respectively.

$$I_{Aux1} = I_{L1} - I_o + \Delta i_{L1} \tag{49}$$

$$I_{Aux2} = I_{L1} - I_o - \Delta i_{L1} \tag{50}$$

The RMS current through capacitor C1 can be expressed as (51).

$$I_{RMS-C1} = \sqrt{D\frac{1}{3}({I_{Aux1}}^2 + I_{Aux1}I_{Aux2} + {I_{Aux2}}^2) + (1-D)I_o} \tag{51}$$

Similarly, to express the RMS current through C_2, it is convenient to define the maximum current (of the trapezoid) termed I_{Aux3} and the minimum current termed I_{Aux4}, as defined in (52) and (53), respectively.

$$I_{Aux3} = I_{L2} - I_o + \Delta i_{L2} \tag{52}$$

$$I_{Aux4} = I_{L2} - I_o - \Delta i_{L2} \tag{53}$$

The RMS current through the capacitor can be expressed as (54).

$$I_{RMS-C2} = \sqrt{D\frac{1}{3}({I_{Aux3}}^2 + I_{Aux3}I_{Aux4} + {I_{Aux4}}^2) + (1-D)I_o} \tag{54}$$

The conduction losses of switches can also be calculated with their RMS current (square) times their on-resistance. When switches are closed, they drain the current through inductors, and their RMS current can be calculated as (55)–(58).

$$I_{RMS-S1} = I_{L1}\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L1}}{I_{L1}}\right)^2} \tag{55}$$

$$I_{RMS-S2} = I_{L2}\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L2}}{I_{L2}}\right)^2} \tag{56}$$

$$I_{RMS-S1n} = I_{L1}\sqrt{1-D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L1}}{I_{L1}}\right)^2} \tag{57}$$

$$I_{RMS-S2} = I_{L2}\sqrt{1-D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L2}}{I_{L2}}\right)^2} \tag{58}$$

Switches s_1 and s_2 also have switching losses in both the turn-on and the turn-off transitions; their switching losses can be estimated with the triangular approximation.

$$\begin{aligned} s_{1-swLoss} &= 0.5\Delta t_{off}(I_{L1}+\Delta i_{L1})(V_{C1}-\Delta v_{C1})f_S \ldots \\ &+0.5\Delta t_{on}(I_{L1}-\Delta i_{L1})(V_{C1}+\Delta v_{C1})f_S \end{aligned} \tag{59}$$

$$\begin{aligned} s_{2-swLoss} &= 0.5\Delta t_{off}(I_{L2}+\Delta i_{L2})(V_{C2}-\Delta v_{C2})f_S \ldots \\ &+0.5\Delta t_{on}(I_{L2}-\Delta i_{L2})(V_{C2}+\Delta v_{C2})f_S \end{aligned} \tag{60}$$

where f_S is the transistor switching frequency. Those calculations are useful to determine the power losses in each element, as well as the efficiency of the converter.

The loss calculations were performed and are included in Section 6, along with the efficiency measured from the experimental prototype. The losses used for the calculated efficiency are shown in Table 1.

Table 1. Parameters.

The Inductance of Inductors L_1 and L_1	L_1 = L_2 = 250 µH
Inductors' ESR	50 mΩ
Capacitor C_1 and C_2	C_1 = C_2 = 10 µF
Capacitors' ESR	5 mΩ
Switching Frequency F_S	F_S = 50 kHz
Transistors' On-Resistance	85 mΩ
Transistors' On an Off time	100 nS
Input Voltage V_g	V_g = 20 V
Duty Cycle D	0.66
Output Power	0 to 300 W

4. Comparative Evaluation

This section compares a particular design with two converters: (i) the converter proposed in [9] and shown in Figure 1 and (ii) the proposed converter. This is useful for understanding the advantages of the proposed converter. For the comparison, a particular design with some specifications is solved with both converters, and the result is compared; the advantage of the proposed topology is that it requires less stored energy in the capacitors. The presented comparison can be validated with a computer simulation via commercial software such as Synopsys Saber, PLECS, and PSIM.

Converters have different numbers of capacitors, but we can establish equivalencies based on the stored energy. The proposed converter's main advantage is the capacitor's voltage rating, which reduces the stored energy. The energy stored in capacitors strongly depends on their size [14–16].

4.1. Specifications

The objective of this study was to design a converter fed with 20 V, which required stepping it up to 100 V. The switching frequency was set to 50 kHz. The peak-to-peak output voltage ripple specification was set to 3 V (1.5 volts peak), representing 3% of the output voltage. The specification was given as maximum values. Evidently, one may choose smaller capacitors, but they may not comply with the spec. The spec was tested at 100 W of output power (I_o = 1 A).

4.2. Solution to the Design

Figure 10 shows the solution to the design with the converter in [9]; this converter required a 4.44 µF capacitor to comply with the specified peak-to-peak ripple of 3 V; we chose a commercial value of 5 µF, which resulted in a peak-to-peak ripple of 2.6 V (1.3 V peak) and the storage of 25.7 mJ of energy. Figure 11 shows the solution to the design with the proposed converter. This converter required an 8.88 µF capacitor to comply with the specified peak-to-peak ripple of 3 V. We chose a commercial value of 10 µF, resulting in a peak-to-peak ripple of 2.6 V (1.3 V peak). This matched both designs to the same output voltage ripple. The design with the proposed converter could store 16.9 mJ of energy. The stored energy in the capacitors led to a significant reduction. The proposed converter required only 65% of the stored energy in capacitors compared with the first solution.

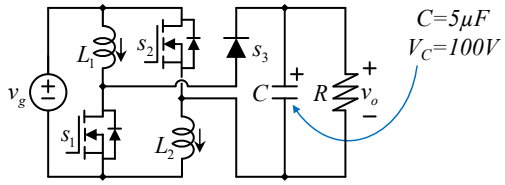

Figure 10. Solution with the topology in [9].

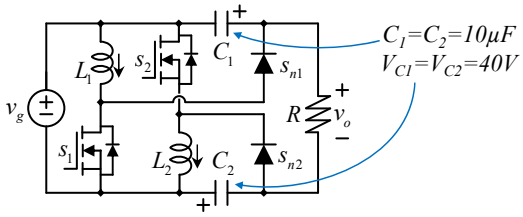

Figure 11. Solution with the proposed topology.

5. Simulation Results

To corroborate the operation of the proposed converter, the converter was simulated in the software Synopsys Saber in a computer with an Intel i7 processor (11th Gen i7-1165G7 at 2.80 GHz), 32 GB of RAM, and Windows 11 Pro (64 bits). Figure 12 shows the simulation schematics of the bidirectional (or synchronous rectified) version.

Table 2 shows the parameters of the simulation. According to equilibrium Equations (10)–(14), the output voltage was expected to be 100 V and the voltage across capacitors was equal to 40 V. In most step-up converters, there is an output capacitor rated to the output voltage (100 V in this case) since the volume of capacitors is proportional to their stored energy, and the stored energy is proportional to the square of their voltage rating. A reduction in the voltage rating is an advantage.

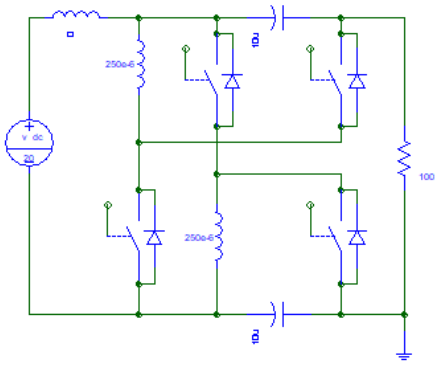

Figure 12. Schematic of the simulated converter.

Table 2. Parameters.

Inductor L_1 and L_1	L_1 = 250 µH, L_2 = 250 µH
Capacitor C_1 and C_2	C_1 = 10 µF, C_2 = 10 µF
Switching Frequency F_S	F_S = 50 kHz
Input Voltage V_g	V_g = 20 V
Output Load Resistance R	R = 100 Ω

Figure 13 shows a comparison of the output voltage, around 100 V in this case, and the voltage across capacitors, around 40 V in this case.

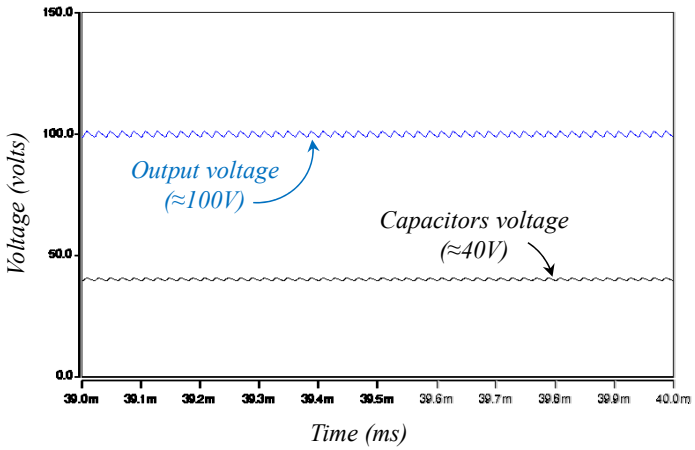

Figure 13. Output voltage and the voltage across capacitors.

Figure 14 shows a zoom into the output voltage. Two waveforms are shown in Figure 14 because, in this case, we included the version without synchronous rectification (only diodes for s_{1n} and s_{2n}) (see Figure 2a) and the version with synchronous rectification (see Figure 2b). The real voltage was slightly smaller than 200 V due to the losses in devices (the simulation was performed considering non-ideal elements). Still, the synchronous rectification had a slightly lower voltage since the on-voltage on diodes was larger than the voltage drops in MOSFETS.

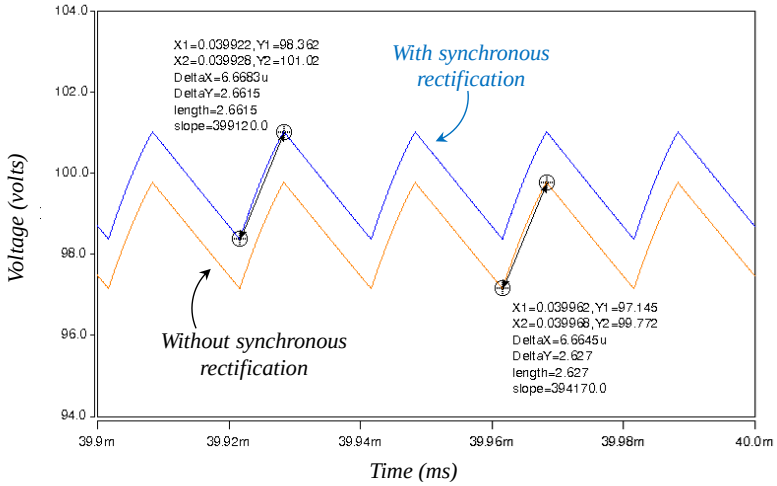

Figure 14. Zoom in the output voltage.

6. Experimental Results

A small prototype was built to demonstrate the principle of the proposed topology. The prototype was based on the Transphorm brand TDHB-65H070L-DC half-bridge (the Digi-Key part number is TDHB-65H070L-DC-ND), which is made of TP65H070L series GaN FETs. Figure 15 shows a diagram of the prototype, as well as the used capacitor and inductor types. The capacitors were the 10 µF EXH2E106HRPT from the Nichicon brand (their Digi-Key part number is 493-13827-ND), and the inductors were the 250 µH ATCA-08-251M-V from the Abracon LLC brand (their Digi-Key part number is 535-13513-ND).

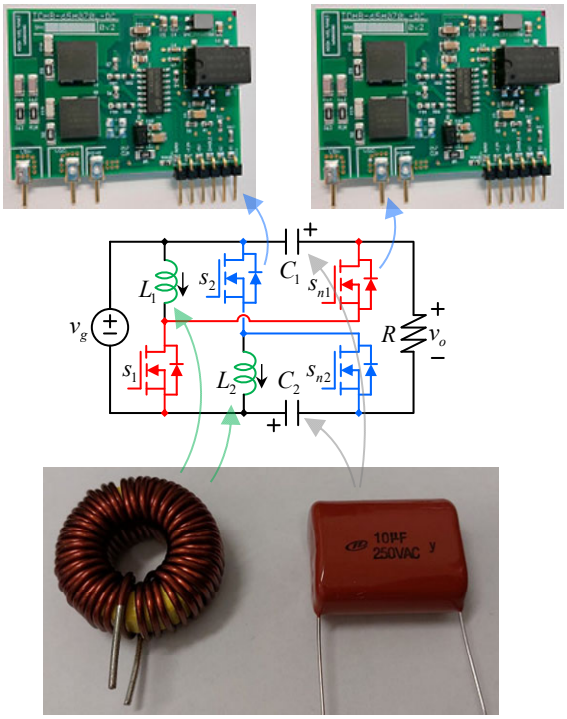

Figure 15. Experimental prototype diagram and main part photos.

To connect the GaN FETs boards, a Transphorm brand TDHBG1200DC100-KIT motherboard was used. Figure 16 shows a photo of the prototype connected to the test bench.

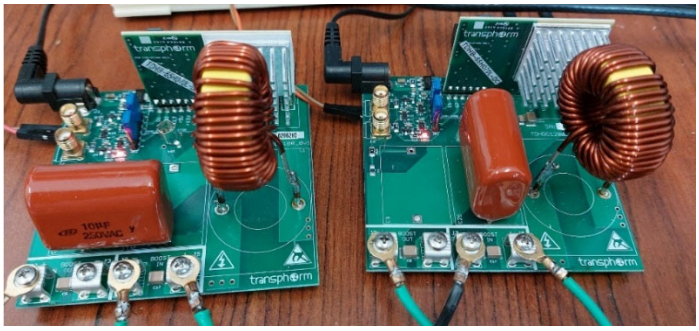

Figure 16. Experimental prototype photo.

Figure 17 shows the waveforms related to L_1, as in Figure 4, for a particular operating point in which the duty cycle D = 0.66, the input voltage was around 20 V, the output voltage was around 100 V, and the output power was around 100 W.

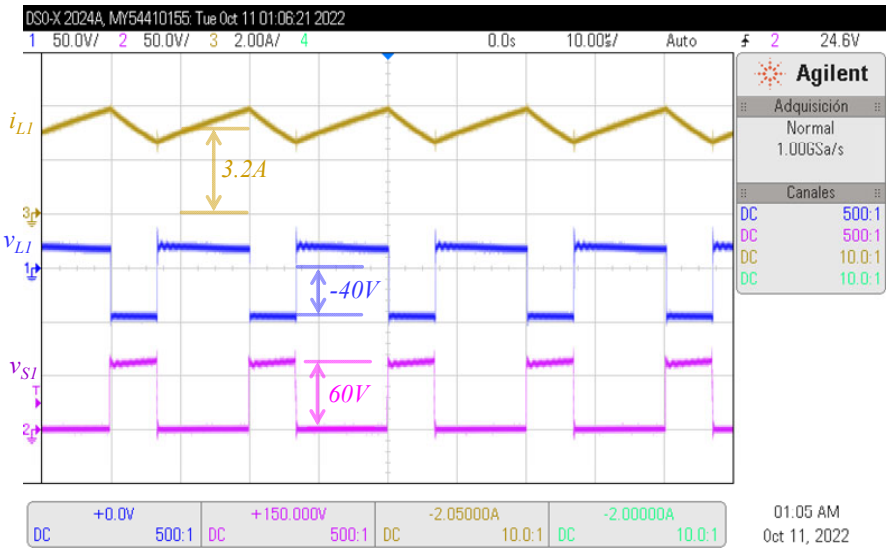

Figure 17. Current and voltage in L_1, as well as the voltage across switch s_1.

Figure 18 was captured at the same operating conditions, but it shows the current through the two inductors (they had the same amplitude and shape). Figure 18 also shows the output voltage.

The top signal in Figure 17 is the current through an inductor (L_1), and it looks like a DC plus a triangular waveform; it is shown at 2 A/div, and the triangular increased to slightly more than 1 A during the time in which its transistor (s_1) was closed. The time lasted for D/f_S (D = 0.66 and f_S = 50 kHz), which was the time in which transistors were closed, and it turned out to be around 13.2 µS. The oscillogram was captured at 10 µS/Div.

The voltage across the inductor is shown below the inductor current in Figure 17; when the switch was closed (which coincided with the positive slope in the inductor), the voltage across the inductor was the input voltage (20 V); the inductor voltage was captured with a Tektronix P5200A voltage prove at 50 V/div. When the transistor was open, the voltage across the inductor was negative (which coincided with the negative slope in the inductor current). The inductor had the same voltage across the capacitor (but negative), which was around −40 V under these operating conditions.

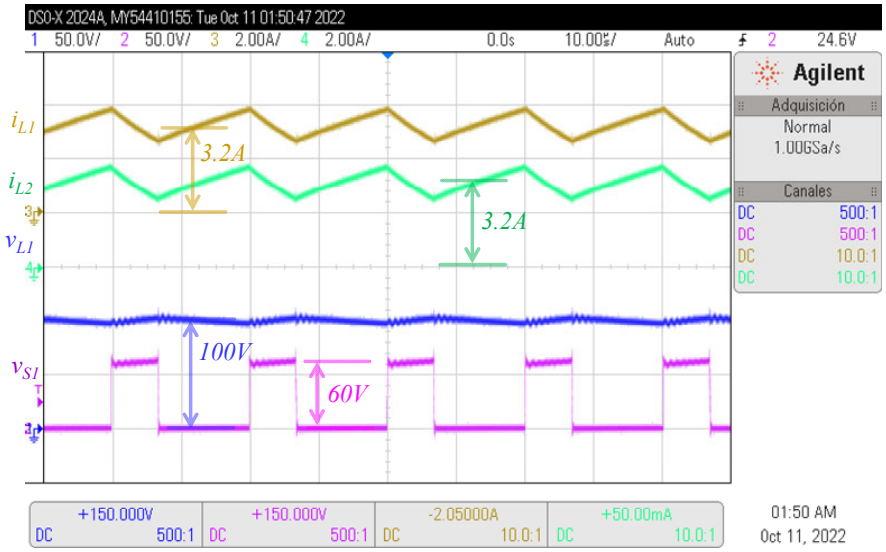

Figure 18. Current through inductors, output voltage, and the voltage across s_1.

Finally, the voltage across the switch s1 at the bottom of Figure 17 in pink; it was almost zero when the switch was closed and $V_g + V_{C1}$ when the switch was open; in these operating conditions, its value turned out to be around 60 V.

Figure 19 shows the efficiency measured for different operating conditions. The line in Figure 19 shows the calculated efficiency according to the procedure in Section 3. Points are measurements of the efficiency in particular operating conditions.

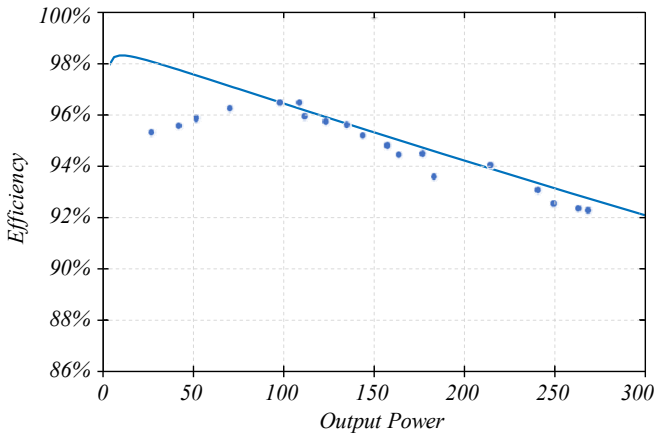

Figure 19. Calculated efficiency (line) and measured (points).

7. Conclusions

This paper introduces a transformer-less DC–DC converter topology that provides a high voltage gain without an extreme duty cycle. The main advantage of the proposed topology compared with other similar circuits is that capacitors are rated to a reduced voltage. Furthermore, the voltage among the ground input and output is not pulsating, and their synchronous rectified version can be synthesized with commercial, off-the-shelf transistors in half-bridge packages. Reducing the voltage rating in capacitors is advantageous since the physical size of capacitors depends on the stored electrical energy, which depends on the square of their voltage. The steady-state analysis of the proposed converter in the continuous conduction mode is presented along with their large-signal and linearized small-signal models. Future work will be dedicated to the study of their dynamics and control. The paper also presents a design procedure that includes the selection of capacitors and inductors and their maximum voltage and current values for an application example. For this particular design with specifications, the proposed converter required only 65% of

the stored energy in capacitors compared with a similar converter in the literature. Finally, the results from a computer-based simulation and from an experimental test bench verified the principle of the operation of the proposed converter. The experimental prototype was able to achieve a peak efficiency of over 96%.

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