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Analytical Estimation of Power Losses in a Dual Active Bridge Converter Controlled with a Single-Phase Shift Switching Scheme

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Abstract: Micro-grid solutions around the world rely on the operation of DC/DC power conversion systems. The most commonly used solution for these topologies is the use of a dual active bridge (DAB) converter. Increasing the efficiency and reliability of this system contributes to the improvement in the stability of the entire microgrid. This paper discussed an analytical method of energy efficiency and power loss estimation in a single phase dual active bridge (DAB) converter controlled with a single-phase shift (SPS) modulation scheme for microgrid system stability. The presented approach uses conduction and commutation losses of semiconductors and high frequency transformer. All parameters required for the calculation may be obtained from the manufacturers' datasheets or can be based on a simple measurement. The approach was validated by the comparison of the estimated energy efficiency characteristics with the measured ones for a prototype of a 5 kW single phase DAB converter equipped with silicon carbide metal-oxide semiconductor field-effect transistors (SiC MOSFET).

Keywords: dual active bridge; bidirectional isolated DAB; efficiency; estimation; power loss; analytical calculations; DC/DC converter; SiC MOSFET

Citation: Turzyński, M.; Bachman, S.; Jasiński, M.; Piasecki, S.; Ryłko, M.; Chiu, H.-J.; Kuo, S.-H.; Chang, Y.-C. Analytical Estimation of Power Losses in a Dual Active Bridge Converter Controlled with a Single-Phase Shift Switching Scheme. *Energies* **2022**, *15*, 8262. https://doi.org/10.3390/en15218262

Academic Editor: Nicu Bizon

Received: 11 October 2022
Accepted: 2 November 2022
Published: 4 November 2022

1. Introduction

Dual active bridge (DAB) topology is among the most popular DC/DC converters used in electronic power systems. This topology is widely used in DC/DC microgrids as well as mixed networks and owes its popularity to many advanced features such as bidirectional power flow, galvanic isolation, control simplicity, wide range of voltage regulation, and soft switching of semiconductor devices. DAB topology has been applied to solid-state transformers, electromobility, energy storage systems, and DC voltage distribution networks [1,2]. Nowadays, the development of DAB converters is mainly focused on the increase in energy efficiency by using modern power semiconductors (SiC, GaN), where the adaptation of new control strategies enables a reduction in the current stress and the limitation of current RMS values, and a diminishing of DAB transformer power losses [1–6]. Crucially, the application of modern power semiconductor devices enables an increase in the switching frequency up to 1 MHz [7], which results in a higher power density, a reduction in passive components dimensions, and a reduction in the overall converter dimensions.

The problem of energy efficiency evaluation is one of the main aspects of the beginning stage of the design process of a future converter. Importantly, a proper evaluation of power losses allows for a selection of cooling methods and radiator features, which reduce the overall converter dimensions and the total cost. At the early stages of the design process, energy efficiency may be estimated using a simulation tool or via an analytical analysis. Many simulators (e.g., PLECS) offer comprehensive tools for the evaluation of power losses and a thermal analysis using electro-thermal models [8]. This method is easy to use and delivers results with a satisfactory accuracy for the design purpose. However, it requires access to precise models of semiconductors, which not all suppliers offer, because such models are usually shared by manufacturers only for selected types of semiconductors, or the developed models are dedicated to one specific simulator. Crucially, many models of semiconductors presented in the literature cannot be parameterized using the manufacturer's datasheet, hence additional laboratory measurements are required to obtain the model parameters, which is usually time-consuming and increases the total cost [9,10].

Notably, the measurement of some quantities in the DAB converter (e.g., the power loss of a transformer) may be problematic, hence using analytical methods may be a suitable approach to obtaining a power loss distribution.

Another approach uses an analytical analysis based on a set-up of mathematical equations describing the function of the considered converter. It is worth mentioning that the presence of high-frequency currents in a DAB converter AC circuit, or the determination of the switching process mechanism of semiconductors (under soft or hard conditions) in dependence on the converter AC side currents values results in limited usefulness of the analytical methods, which have been derived for classic H-bridge topologies. These approaches are usually described for sinusoidal modulation with a low fundamental current frequency at the inverter AC side [11–13]. Moreover, in some systems, the transistor turn-on losses are neglected [14], or it is assumed that both the turn-on and turn-off processes perform only under hard switching conditions [12]. In available application notes, switching losses under hard conditions are usually calculated using simplified formulas with constant values of time parameters describing the switching processes [4]. Moreover, to simplify the considerations, the impact of transistor gate resistance is often omitted [12,14,15].

In the literature, analytical methods of power loss estimation dedicated to DAB converters have also been proposed.

For example, in [16], an analysis of a power transfer in a single-phase DAB converter was provided. The presented analyses were performed for different cases of input-to-output voltage relations including the influence of the dead time and conduction losses of semiconductor devices. However, the presented analysis was incomplete as it omitted the discussion of the impact of semiconductor switching losses and transformer losses. An interesting approach was presented in [17], where a theoretical analysis of power losses was given, which was used for the optimal design methodology of a single-phase DAB converter. A valuable part of this work is a presentation of an estimation method of capacitors and transformer losses. The obtained results were compared with the results of the simulation and experimental measurements to prove the correctness of the adopted methodology, however, an analysis of the semiconductor switching losses was not included—the authors assumed that all switches were switched under soft conditions. Another solution was presented in [18], where an analysis of the conducted differential mode current harmonic magnitudes and the power factor in a DAB converter was discussed. Importantly, that solution was based on a Fourier series theory, hence its adaptation is more complex and time consuming. This approach may be used for the overall prediction of the DAB operational performance and to optimize and identify the current and voltage ranges. Commutation losses were not considered here either; hence based on the methodology presented in [18], the DAB converter efficiency may only be evaluated in a generic way.

The approach presented in [19] was dedicated to the estimation of semiconductor losses including the impact of dead-time and turn-off process for SiC MOSFET and Si IGBT transistors operating in DAB converters. All of the required parameters may be easily extracted using the manufacturer's datasheet. The used mathematical expressions are not complicated, and method adaptation is not time-consuming. It should be noted that the presented considerations did not take into account the transformer losses, which is a significant disadvantage of the method.

A more advanced approach was described in [20], where the estimation method of semiconductors and transformer losses was proposed. The obtained results were used to improve the overall energy efficiency by modifying and optimizing the DAB converter control strategy. The limitations of the primary approach are the omission of the diodes' reverse recovery process and neglect of the impact of transistor gate resistance on the switching process dynamics.

A comprehensive estimation method of the DAB converter efficiency was proposed in [21]. The transformer losses were predicted using the Steinmetz equation and the semiconductors' conduction and switching losses were also calculated. Additional analyses were performed for hard and soft switching conditions in dependency on the current values in the AC circuit of the DAB converter. The high accuracy of the obtained results and the usefulness of the proposed approach were confirmed by a comparison with the experimental measurement results. However, two different polynomial functions—one for hard switching and one for soft switching—must be used to calculate the semiconductor switching losses. Parameters of these functions were fitted by using least means squares approximation. As a result, the method is complicated and time-consuming.

Based on the presented analysis, it appears that a different approach is necessary. In this paper, a calculation method of power loss and energy efficiency of a one-phase DAB converter composed with SiC-MOSFETs and controlled with single phase shift was proposed. The proposed set of equations, whose coefficients may be easily obtained from the manufacturer's datasheets, describes the commutation and conduction losses of diodes and transistors and the transformer losses were also considered. The correctness of theoretical considerations was verified by comparing the analytical results with the experimental ones, performed on a 5 kW DAB converter prototype.

2. Dual Active Bridge DC/DC Converter

The basic topology of the dual active bridge (DAB) DC/DC converter with a one-phase high frequency transformer is presented in Figure 1a. It consists of two H-bridges coupled by an AC-link formed by a transformer with a turn's ratio $n = N_2/N_1$ and an additional inductor L_d. The DAB converter may be driven using various control methods. Due to its simplicity of implementation, small inertia, and satisfactory dynamic performance, the single phase shift (SPS) switching scheme, where all transistors are switched with a 50% duty cycle ratio and the phase-shift ϕ is used to control the power flow (Figure 1b), was the most common scheme. Nevertheless, using SPS control causes a reduction in the operating range in which semiconductors are switched to soft conditions, especially when the input-to-output voltage ratio is significantly different from 1. Another disadvantage of the application of the SPS modulation scheme is an increase in the rms value of the transformer current at the converter's low output power. As a result, a significant reactive power flow is then observed, which increases the conduction loss and the current stress of transistors and diodes [22,23]. To improve the converter efficiency by reducing the circulating power flow and limiting the current rms value, other control methods, which provide an extra degree of freedom, have been proposed such as extended phase shift (EPS), dual phase shift (DPS), or triple phase shift (TPS) modulation [24,25].

Despite the undeniable advantages of EPS, DPS, and TPS, in comparison with SPS, a practical application of these types of modulation is more complex. These methods significantly complicate the implementations of the modulator, and their efficiency characteristics in relation to the output power, with the change in the voltage ratio, decreases significantly. Hence, in this paper, the authors considered a DAB controlled with a SPS control scheme, however, the proposed approach may be adopted to other modulation types.

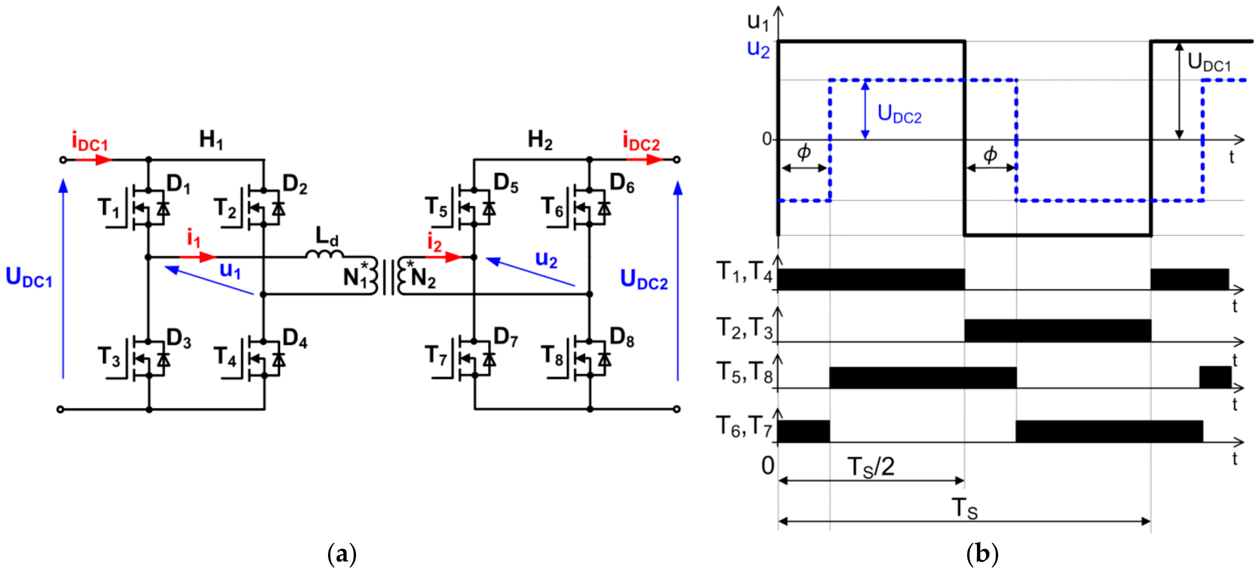


Figure 1. (**a**) Dual active bridge DC/DC converter topology; (**b**) single phase shift modulation scheme.

3. Currents Estimation in a DAB Converter

An equivalent circuit of the single-phase DAB converter (Figure 1a) is presented in Figure 2. A resultant inductance L represents a sum of inductances in the AC-circuit:

$$L = L_d + L_{\delta 1} + L'_{\delta 2}, \tag{1}$$

where:

- L_d—inductance of the additional inductor;
- $L_{\delta 1}$, $L_{\delta 2}{}'$—leakage inductance of each transformer winding converted to the bridge H_1 side: $L_{\delta 2}{}' = L_{\delta 2}/n^2$;
- $L_{\delta 2}$—leakage inductance of transformer winding at the H_2 bridge side; $n = N_2/N_1$—transformer turns ratio.

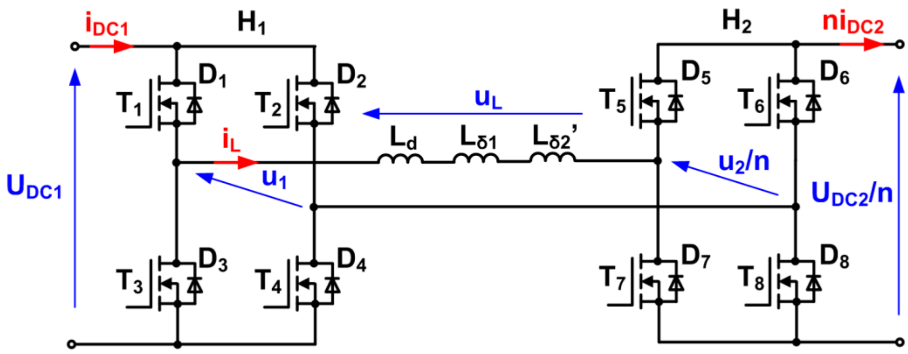


Figure 2. Equivalent circuit of the single-phase DAB converter.

In the presented equivalent scheme, values of the H_2 bridge voltages and currents are also referred to the H_1 bridge side.

In this study, the DAB converter features were considered when the SPS modulation strategy was applied. Each bridge generated a quasi-square wave voltage u_1 and u_2/n with a 50% duty cycle (Figure 3).

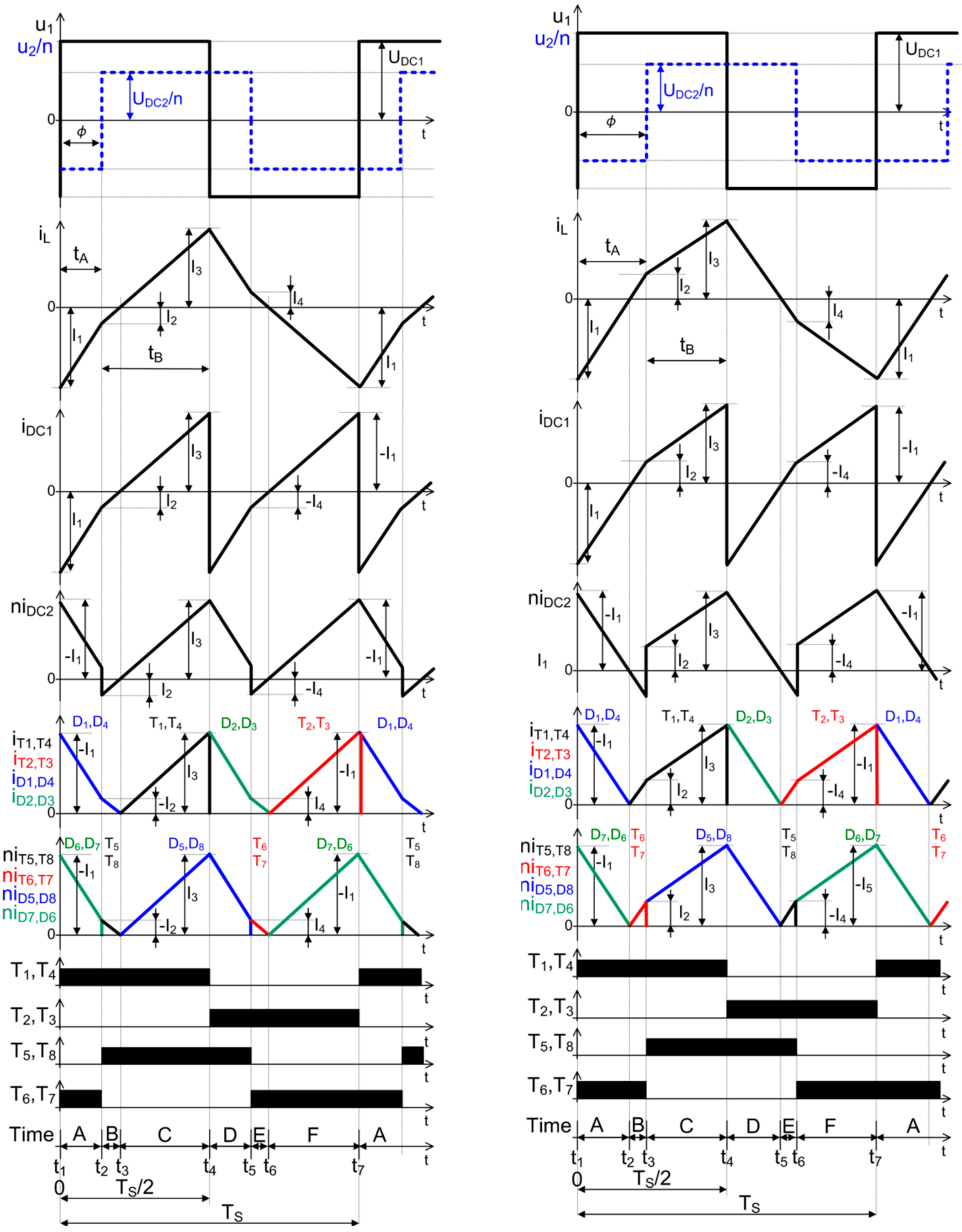


Figure 3. Simplified voltage and current waveforms of DAB converter for $U_{DC1} > U_{DC2}/n$: (**a**) with $I_2 < 0$; (**b**) with $I_2 > 0$.

The value and power flow direction between bridges H_1 and H_2 are controlled by the phase shift ϕ. To simplify the calculations, the impact of the transistors' dead time may be neglected. Similarly, it can be assumed that the values of voltages U_{DC1} and U_{DC2}/n are high enough, which enables the voltage drop to be omitted at the transistors and diodes. In brief, positive values of the phase shift are used when $U_{DC1} > U_{DC2}/n$, however, for a negative value of ϕ, the results may be obtained using a similar approach. In Figure 4, exemplary theoretical waveforms are presented, when $U_{DC1} < U_{DC2}/n$ and $\phi > 0$.

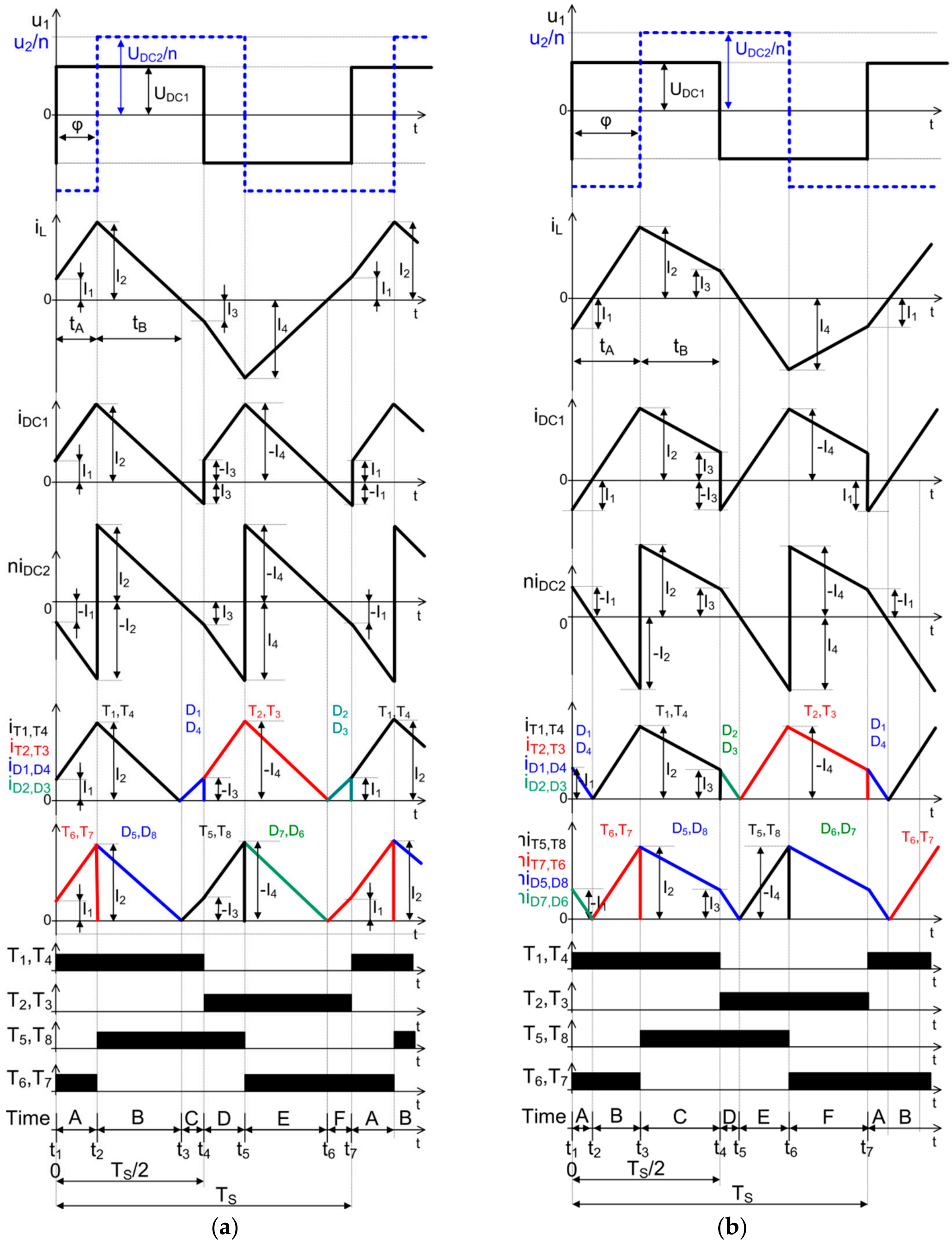


Figure 4. Simplified voltage and current waveforms of the DAB converter for $U_{DC1} < U_{DC2}/n$: (**a**) with $I_1 > 0$; (**b**) with $I_1 < 0$.

Based on Figure 3a and an equivalent scheme of the DAB converter (Figure 2), voltage u_L, affecting the inductances in the AC-link, is described by:

- for the time interval t_A:

$$u_{L(A)} = u_1 - \frac{u_2}{n} = U_{DC1} + \frac{U_{DC2}}{n}, \tag{2}$$

- for the time interval t_B:

$$u_{L(B)} = u_1 - \frac{u_2}{n} = U_{DC1} - \frac{U_{DC2}}{n}. \tag{3}$$

Hence, the current i_L in specified time moments is described by:

$$i_L(t_1) = I_1, \tag{4}$$

$$i_L(t_2) = I_2 = I_1 + \frac{u_{L(A)}}{L} t_A \tag{5}$$

and

$$i_L(t_4) = i_L\left(\frac{T_S}{2}\right) = I_3 = I_2 + \frac{u_{L(B)}}{L} t_B = -I_1. \tag{6}$$

Thus, the average values of the input and output currents I_{DC1} and I_{DC2} are given by:

$$I_{DC1(av)} = \frac{2}{T_S}\int_0^{T_S/2} i_{DC1}(t)dt = \frac{1}{T_S}[I_2(t_A + t_B) + I_3(t_B - t_A)], \tag{7}$$

and

$$I_{DC2(av)} = \frac{2}{T_S}\int_0^{T_S/2} i_{DC2}(t)dt = \frac{1}{nT_S}[I_2(t_B - t_A) + I_3(t_A + t_B)]. \tag{8}$$

Because $t_A = T_S/2 - t_B$ and substitutions (2) and (3) to (8), (9) leads to:

$$I_{DC1(av)} = \frac{1}{nT_S}\left[-\frac{2U_{DC2}}{L}{t_B}^2 + \frac{T_S \cdot U_{DC2}}{L} t_B\right], \tag{9}$$

and

$$I_{DC2(av)} = \frac{1}{nT_S}\left[-\frac{2U_{DC1}}{L}{t_B}^2 + \frac{T_S \cdot U_{DC1}}{L} t_B\right]. \tag{10}$$

For known values of $I_{DC1(av)}$ or $I_{DC2(av)}$, n and U_{DC1} or U_{DC2}, the length of the time interval t_B may be easily extracted by solving Equations (9) or (10). Next, the length of interval t_A may be obtained for a specified switching time T_S, which allows for a calculation of the values of current i_L at characteristic moments of the DAB converter operating cycle.

4. Estimation of Transistor and Diode Power Losses

The total power loss P_T of a single transistor operating in a H-bridge is the sum of commutation losses and conduction loss $P_{C(T)}$:

$$P_T = P_{ON(T)} + P_{C(T)} + P_{OFF(T)}, \tag{11}$$

where $P_{ON(T)}$ and $P_{OFF(T)}$ are the turn-on and turn-off switching losses, also called the commutation losses. The total power loss of a single diode P_D may be defined in an analogous way.

Conduction losses result from voltage drops on conducting transistors and diodes. If MOSFET transistors are applied in a converter construction, using a linear approximation of the transistor output characteristic $i_D(u_{DS})$ (Figure 5) allows one to estimate a voltage drop u_{DS} depending on a drain current i_D:

$$u_{DS} = \frac{U_{DS(N)}}{I_{D(N)}} i_D, \tag{12}$$

where $U_{DS(N)}$ and $I_{D(N)}$ are the rated values of the transistor drain-to-source voltage u_{DS} and drain current i_D (given in the manufacturer's datasheet).

Similarly, using a linear approximation of the datasheet diode characteristic $i_{DZ}(u_D)$, the voltage drop u_D caused by a flow of current i_{DZ} may be calculated as:

$$u_D = r_D \cdot i_{DZ} + U_{FO}, \tag{13}$$

where U_{FO} is a diode threshold voltage and r_D is the diode dynamic resistance $r_D = \Delta u_D/\Delta i_{DZ}$ (Figure 5).

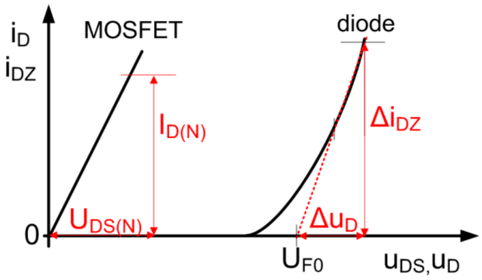


Figure 5. Linearization of the diode and MOSFET steady-state characteristics.

Hence, the conduction power loss of the MOSFET transistor and diode calculated for one switching period T_S are given as follows:

- for MOSFET:

$$P_{C(T)} = \frac{U_{DS(N)}}{I_{D(N)}\,T_S} \int_{t_0}^{t_O+T_S} [i_D(t)]^2 dt = \frac{U_{DS(N)}}{I_{D(N)}} \cdot I_{D(rms)}{}^2 \tag{14}$$

- and for the diode:

$$P_{C(D)} = U_{FO} \cdot I_{DZ(av)} + r_D \cdot I_{DZ(rms)}{}^2, \tag{15}$$

where $I_{D(rms)}$ and $I_{DZ(rms)}$ are rms values of transistor and diode currents and $I_{DZ(av)}$ is an average value of a diode current i_{DZ} calculated for one switching period T_S.

Commutation losses result from finite values of the rise and fall times of the transistor voltage and current waveforms during switching processes. Considering the theoretical voltages and current waveforms obtained in a basic switching cell (Figure 6) during the transistor turn-on process under hard conditions, the transistor current i_D reaches the value of the load current I_O before the reduction in the drain-to-source voltage u_{DS} [26] (Figure 7).

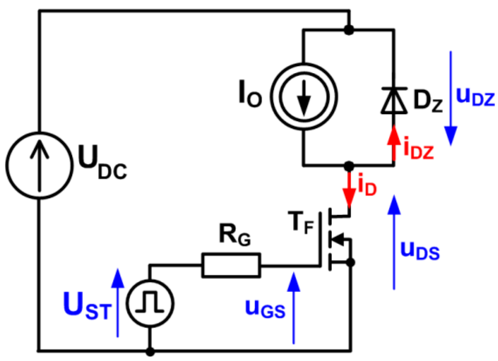


Figure 6. Basic switching cell.

Hence, in the turn-on process of a transistor, two characteristic sub periods may be described. Impacted by the diode D_Z reverse recovery, during the first stage of the turn-on process, the drain current rises to the value, which is a sum of the absolute values of load current I_O and reverse recovery current I_{RM} of diode D_Z (Figure 7b). Considering the waveforms presented in Figure 6, the transistor current i_D derivative with time is expressed by:

$$a_{iD} = \frac{di_D}{dt} = \frac{I_O + |I_{RM}|}{t_{RI}\prime} = \frac{I_O}{t_{RI}}. \tag{16}$$

To estimate the current i_D rise time t_{RI}, a MOSFET gate circuit should be analyzed (Figure 8). During the transistor switching process, which is caused by drive voltage U_{DR} changes, transistor parasitic capacitances C_{GD} and C_{GS} are recharged by the gate current i_G [27]:

$$i_G = C_{GD}\frac{du_{GD}}{dt} + C_{GS}\frac{du_{GS}}{dt}. \tag{17}$$

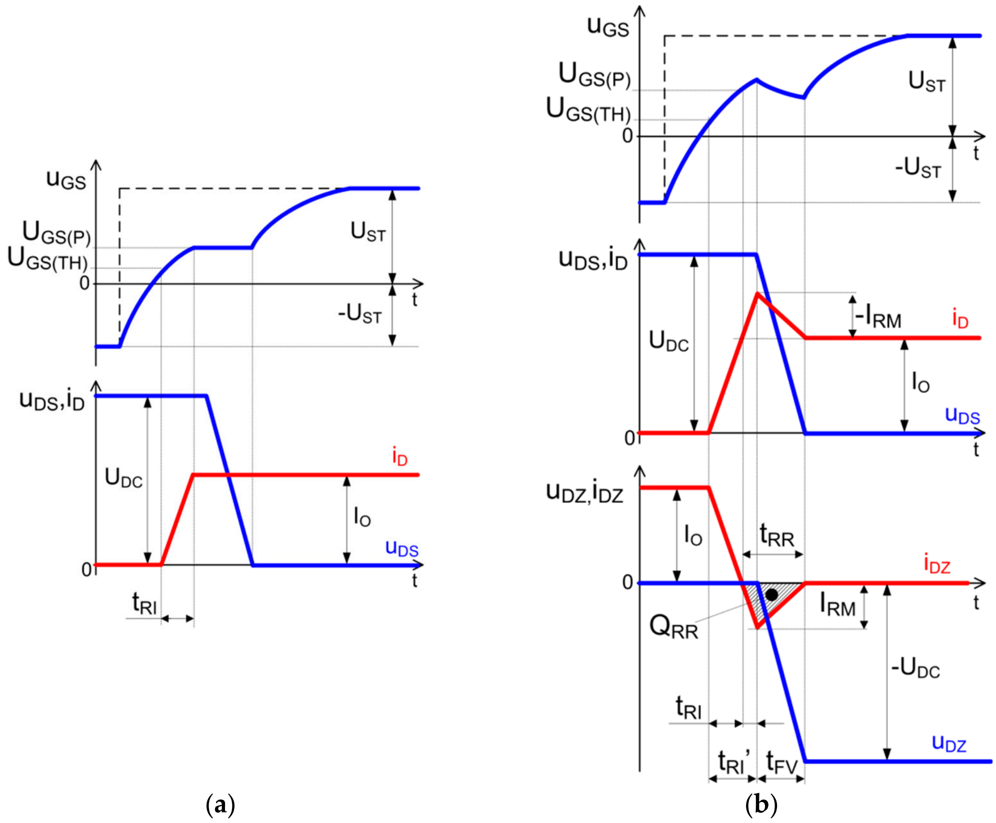


Figure 7. Voltage and current waveforms in a basic switching cell during transistor turn-on process: (**a**) without the diode D_Z reverse recovery; (**b**) with the diode D_Z reverse recovery.

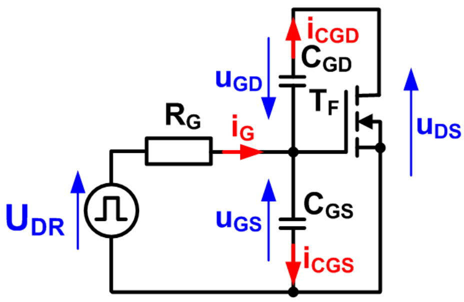


Figure 8. A gate circuit of the MOSFET transistor.

The gate current i_G may also be described by the equation:

$$i_G = \frac{U_{DR} - u_{GS}}{R_G}, \tag{18}$$

where R_G is an external gate resistance. In the manufacturer's datasheet, the values of capacitances C_{GD} and C_{GS} are given as an input capacitance C_{iss} and a reverse transfer capacitance C_{rss} with the following relationships:

$$C_{iss} = C_{GD} + C_{GS} \tag{19}$$

and

$$C_{rss} = C_{GD}. \tag{20}$$

Next, substituting (18)–(20) to Equation (17):

$$\frac{U_{DR} - u_{GS}}{R_G} = C_{rss}\frac{d(u_{GS} - u_{DS})}{dt} + (C_{iss} - C_{rss})\frac{du_{GS}}{dt}, \tag{21}$$

which leads to:

$$\frac{U_{DR} - u_{GS}}{R_G} = C_{iss}\frac{du_{GS}}{dt} - C_{rss}\frac{du_{DS}}{dt}. \tag{22}$$

During the current i_D rise phase of the turn-on process, to simplify the calculations, it can be assumed that the voltage u_{DS} remains constant and its derivative with time equals zero (Figure 7). Hence, Equation (22) may be modified as follows:

$$\frac{U_{DR} - u_{GS}}{R_G} = C_{iss}\frac{du_{GS}}{dt}. \tag{23}$$

Next, transforming Equation (23):

$$dt = \frac{R_G \cdot C_{iss}}{U_{DR} - u_{GS}}du_{GS} \tag{24}$$

the rise time t_{RI} is given by:

$$t_{RI} = \int_{U_{GS(TH)}}^{U_{GS(P)}} \frac{R_G \cdot C_{iss}}{U_{DR} - u_{GS}}du_{GS} = R_G C_{iss} ln\frac{\left|U_{DR} - U_{GS(TH)}\right|}{\left|U_{DR} - U_{GS(P)}\right|}. \tag{25}$$

where $U_{GS(TH)}$ is a MOSFET gate threshold voltage and $U_{GS(P)}$ is a minimal value of the gate-to-source voltage, enabling the conduction of the load current I_O. These values may be obtained from a datasheet transfer characteristic $i_D(u_{GS})$. After the calculation of parameter t_{RI}, the value of derivative di_D/dt may be easily estimated using (16).

To estimate the diode turn-off power loss under hard-switching conditions, a reverse-recovery process must be used. Hence, the values of reverse current I_{RM} and diode reverse recovery time t_{RR} should be evaluated (Figure 7b). To solve this problem, a number of analytical methods using datasheet information have been proposed. For example, in [28], a regression method was proposed to obtain the reverse-recovery parameters during switching intervals, and in [29], a set of equations including, additionally, the impact of parasitic inductances and diode capacitance, was proposed. These methods offer satisfactory accuracy with a maximum error of parameter estimation lower than 10%, however, their application seems to be complex and time consuming. Considering the waveforms presented in Figure 7b, the values of parameters t_{RR}, I_{RM}, and Q_{RR} depend on the load current I_O, diode current derivative with time a_{iDz}, and temperature [30]. In this paper, to be concise, the effect of temperature was omitted. Based on the results of the measurements and the manufacturer's data, the following empirical relations enabling the estimation of t_{RR} and I_{RM} for various values of load current I_O and $a_{iDZ} = di_{DZ}/dt$ were derived:

$$t_{RR} = t_{RR(N)}\left(-0.15\left|\frac{a_{iDz}}{A_{iDz(N)}}\right| + 0.2\frac{I_O}{I_{O(N)}} + 0.9\right) \tag{26}$$

and:

$$I_{RM} = 0.2 I_{RM(N)}\left(\frac{I_O}{I_{O(N)}} + 1.25\right)\left(\left|\frac{a_{iDz}}{A_{iDz(N)}}\right| + 1\right), \tag{27}$$

where:

- $a_{iDZ} = di_{DZ}/dt = -a_{iD}$ (from Equation (16) and Figure 7b);
- $t_{RR(N)}$ is a nominal value of the diode D_Z reverse recovery time measured for the nominal load current $I_{O(N)}$ and nominal derivative with time of the diode current $A_{iDZ(N)}$. These nominal values are usually given in the manufacturer's datasheet.

Thus, the total length of interval t_{RI}' (Figure 7b) is given by:

$$t'_{RI} = t_{RI} + \frac{|I_{RM}|}{a_{iD}}. \tag{28}$$

When the transistor drain current reaches the maximum value, the next phase of the turn-on process begins. Voltage u_{DS} starts to fall and, by the end of interval t_{FV}, the recombination process of the diode charge is finished—voltage u_{DS} is reduced to zero and the diode current is zero (Figure 7b) [12]. Factually, at that moment, the diode current was limited to about 10% of I_{RM} and the voltage u_{DS} was reduced to the value resulting from the voltage drop on the conducting transistor. Hence, the transistor voltage fall time t_{FV} is described by:

$$t_{FV} = t_{RR} - \frac{|I_{RM}|}{a_{iD}}. \tag{29}$$

Considering the waveforms presented in Figure 7b and based on the estimated values of t_{RI}' and t_{FV}, the turn-on power loss of the MOSFET $P_{ON(T)}$ under hard switching conditions is expressed by:

$$P_{ON(T)} = \frac{1}{T_S} \int_0^{t_{FV}+t_{RI}'} u_{DS}(t) \cdot i_D(t) dt. \tag{30}$$

which leads to:

$$P_{ON(T)} = \frac{U_{DC}}{T_S} \left[\frac{t_{RI}'}{2} (I_O + |I_{RM}|) + t_{FV} \left(\frac{I_O}{2} + \frac{|I_{RM}|}{3} \right) \right]. \tag{31}$$

Similarly, the diode reverse recovery power loss is given by:

$$P_{OFF(D)} = \frac{1}{T_S} \int_0^{t_{FV}} u_{DZ}(t) \cdot i_{DZ}(t) dt = \frac{U_{DC} \cdot |I_{RM}| \cdot t_{FV}}{6T_S}. \tag{32}$$

During the MOSFET turn-off process under hard conditions, the transistor u_{DS} voltage reaches the value of the supply voltage U_{DC} before a reduction in the drain current i_D (Figure 9) [26,31]. Analyzing the MOSFET turn-off process (Figure 9), two characteristic phases may be recognized:

- during time interval t_{RV}, voltage u_{DC} rises to U_{DC};
- during time interval t_{FI}, drain current i_D decreases do zero.

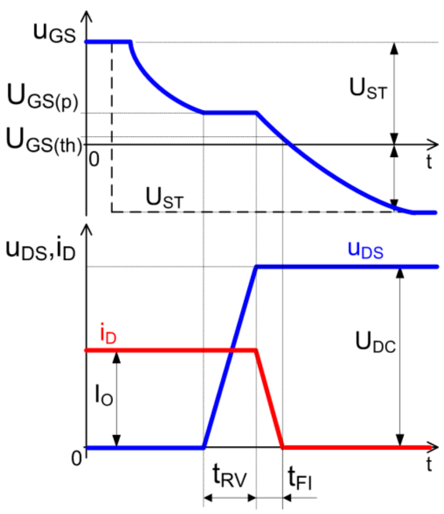


Figure 9. Voltage and current waveforms in a basic switching cell during the transistor turn-off process.

During time interval t_{RV}, assuming the gate-to-source voltage u_{GS} is constant, the transistor is turned off within the flat Miller Plateau Region. Because $u_{GS} = U_{GS(P)}$ and $du_{GS}/dt = 0$, Equation (22) may be simplified:

$$\frac{U_{DR} - U_{GS(P)}}{R_G} = -C_{rss}\frac{du_{DS}}{dt}\,, \tag{33}$$

which leads to:

$$t_{RV} = \frac{R_G \cdot C_{rss}}{U_{GS(P)} - U_{DR}}\int_0^{U_{DC}} du_{DS} = \frac{R_G \cdot C_{rss} \cdot U_{DC}}{U_{GS(P)} - U_{DR}}\,. \tag{34}$$

The relation describing a current i_D fall time may also be derived in an analogous way:

$$t_{FI} = \int_{U_{GS(P)}}^{U_{GS(TH)}} \frac{R_G \cdot C_{iss}}{U_{DR} - u_{GS}} du_{GS} = R_G C_{iss} ln \frac{\left|U_{DR} - U_{GS(P)}\right|}{\left|U_{DR} - U_{GS(TH)}\right|}\,. \tag{35}$$

Thus, MOSFET turn-off power losses are given by:

$$P_{\mathrm{OFF(T)}} = \frac{1}{T_S}\int_0^{t_{RV}+t_{FI}} (u_{\mathrm{DS}}(t) \cdot i_{\mathrm{D}}(t))dt = \frac{U_{\mathrm{DC}} \cdot I_{\mathrm{O}}}{2T_S}(t_{RV} + t_{FI}). \tag{36}$$

For example, from Figure 3, it can be distinguished that transistor pair T_1 and T_4 in bridge H_1 is switched on when diodes D_1 and D_4 conduct, which forms soft switching conditions. Similarly, the turn-on process of transistors T_2 and T_3 also occurs under ZCS (zero current switching) conditions. Hence, it can be assumed that the turn-on power loss for these transistor pairs $P_{ON(T)} = 0$. At moments t_4 and t_7, transistor pairs T_1, T_4 and T_2, T_3 are switched off. In this study, the least favorable operating conditions of semiconductors were assumed, hence, to calculate the power loss $P_{OFF(T)}$ from Equation (36), it was assumed that transistor pairs T_1, T_4 and T_2, T_3 were turned off under hard-switching conditions with a current $i_{T1,T4}(t_4) = i_{T2,T3}(t_7) = -I_1 = I_3$ and supply voltage $U_{DC} = U_{DC1}$. From Figure 3, it can also be distinguished, that if $I_2 < 0$, then transistors T_5, T_8 are switched on and diodes D_6, D_7 are turned off under hard-switching conditions. To calculate transistor T_5 turn-on power losses $P_{ON(T5)}$ and diode D_6 turn-off power losses $P_{OFF(D6)}$, Equations (31) and (32) should then be used for $U_{DC} = U_{DC2}$ and $I_O = I_2/n$. The turn-off process of transistors T_5, T_8 occurs under ZCS conditions, hence, the commutation loss $P_{OFF(T5)}$ equals zero. If $I_2 > 0$, the transistor T_5, T_8 turn-on process ensues when diodes D_1, D_4 conduct, which allows for the development of soft-switching conditions. Nevertheless, the H_2 bridge transistors' turn-off process occurs under hard switching conditions. To calculate the commutation power loss $P_{OFF(T5)}$, Equation (36) may be applied for $U_{DC} = U_{DC2}$ and $I_O = I_2/n$. Notably, that power loss may be calculated only for one transistor and diode for each of bridges H_1 and H_2. Hence, the power loss of transistor T_1 is given by:

$$P_{T1} = P_{C(T1)} + P_{OFF(T1)}\,, \tag{37}$$

where the transistor T_1 conduction power loss $P_{C(T1)}$ may be calculated from (14):

$$P_{C(T1)} = \frac{U_{DS(N)}}{I_{D(N)}} \cdot {I_{T1(rms)}}^2\,, \tag{38}$$

and ${I_{T1(rms)}}^2$ is obtained by:

If $I_2 < 0$ (from Figure 3a):

$${I_{T1(rms)}}^2 = \frac{1}{T_S}\int_{t_3}^{t_4} i_L^2(t)dt = \frac{1}{3T_S}\left(\frac{T_S}{2} - t_3\right)I_3^2\,, \tag{39}$$

and if $I_2 > 0$ (from Figure 3b):

$$I_{T1(rms)}{}^2 = \frac{1}{T_S}\int_{t_2}^{t_4} i_L^2(t)dt = \frac{1}{3T_S}\left[(t_3 - t_2)I_2^2 + \left(\frac{T_S}{2} - t_3\right)\frac{I_3^3 - I_2^3}{I_3 - I_2}\right]. \quad (40)$$

The commutation power loss $P_{OFF(T1)}$ is described in Equation (36). Because diode D_1 is turned off under soft-switching conditions, only a conduction loss (see Equation (15)) may be taken into account:

$$P_{D1} = P_{C(D1)} = U_{FO} \cdot I_{D1(av)} + r_D \cdot I_{D1(rms)}{}^2, \quad (41)$$

where $I_{D1(av)}$ and $I_{D1(rms)}{}^2$ are given as follows:

If $I_2 < 0$ (from Figure 3a):

$$I_{D(av)} = \frac{1}{T_S}\int_0^{t_3}[-i_L(t)]dt = \frac{1}{2T_S}[I_3 t_A - I_2(t_A + t_3 - t_2)], \quad (42)$$

$$I_{D(rms)}{}^2 = \frac{1}{T_S}\int_0^{t_3}[-i_L(t)]^2 dt = \frac{1}{3T_S}\left[\frac{I_1^3 - I_2^3}{I_1 - I_2}t_A + I_2^2(t_3 - t_2)\right]. \quad (43)$$

and if $I_2 > 0$ (from Figure 3b):

$$I_{D(av)} = \frac{1}{T_S}\int_0^{t_2}[-i_L(t)]dt = \frac{1}{2T_S}[I_3(t_2 - t_1)], \quad (44)$$

$$I_{D(rms)}{}^2 = \frac{1}{T_S}\int_0^{t_2}[-i_L(t)]^2 dt = \frac{1}{3T_S}\left[I_3^2(t_2 - t_1)\right]. \quad (45)$$

For the known values I_1, I_2, and I_3, the length of the time intervals ($t_2 - t_1$), ($t_3 - t_2$), and ($T_S/2 - t_3$) for specific values of voltage U_{DC1} and U_{DC2}/n may be obtained from modified Equations (4)–(6).

The total power losses of the H_1 bridge transistors is equal to:

$$P_{TH1} = 4 \cdot P_{T1}, \quad (46)$$

and the total power losses for the bridge H_1 diodes are given by:

$$P_{DH1} = 4 \cdot P_{D1}. \quad (47)$$

Hence, the total power losses of bridge H_1 is equal to:

$$P_{H1} = P_{TH1} + P_{DH1}. \quad (48)$$

The total power losses of all transistors (P_{TH2}) and diodes (P_{DH2}) in a H_2 bridge may be obtained in an analogous way.

5. Transformer Losses

For the analytical evaluation, it was assumed that the transformer total power loss P_{TR} is a sum of the power loss in the core P_{FE}, and the power losses generated in the primary and secondary windings are $P_{CU(prim)}$ and $P_{CU(sec)}$.

$$P_{TR} = P_{FE} + P_{CU(prim)} + P_{CU(sec)}. \quad (49)$$

To calculate the core power loss P_{FE}, a modified Steinmetz's formula may be used, which for rectangular voltages is given as follows [32,33]:

$$P_{FE} = \frac{8}{\pi^2}kf^{\alpha}B_M^{\beta}\left(c_0 - c_1 T_C + c_2 T_C^2\right)V_C, \quad (50)$$

- f—inducplified waveforms of voltages;
- B_M—induction peak value [T];
- T_C—core temperature [°C];
- V_C—core volume [cm^3].

The coefficients of Equation (50) may be directly obtained from datasheets developed by the core manufacturers.

Considering the scheme presented in Figure 2, an equivalent circuit of the transformer connected in series with an additional choke placed at the primary side is shown in Figure 10. Thus, a magnetizing voltage u_{Lm} affecting the magnetizing inductance L_m is described by:

$$u_{Lm} = \frac{L_{\delta 2}\prime}{L_d + L_{\delta 1} + L_{\delta 2}\prime} u_1 + \frac{L_d + L_{\delta 1}}{L_d + L_{\delta 1} + L_{\delta 2}\prime} \frac{u_2}{n}, \tag{51}$$

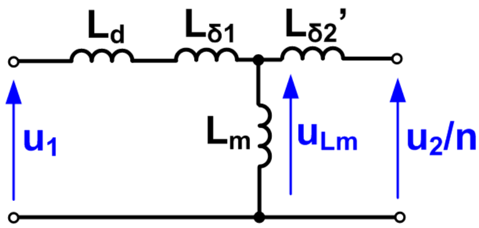


Figure 10. An equivalent circuit of the transformer with an additional choke L_d with values transferred to the DAB H_1 bridge side.

From Figure 2, neglecting a voltage drop on the diodes and transistors and assuming a rectangular shape of the voltage waveforms, the voltages u_1 and u_2/n were equal to, respectively, $\pm U_{DC1}$ and $\pm U_{DC2}/n$. From (51), it may be distinguished that the worst working conditions of core occurred when L_d = 0 and $L_{\delta 2} = L_{\delta 2}'$. Hence, the magnetizing voltage u_{Lm} is then given by:

$$u_{Lm} = \frac{1}{2}\left(u_1 + \frac{u_2}{n}\right), \tag{52}$$

and induction B_M reaches the maximum possible values. Based on waveforms presented in Figure 11, B_M may be described in the following way:

- if $U_{DC1} = U_{DC2}/n$ (Figure 11a):

$$B_M = \frac{\Delta B_1}{2} = \frac{U_{DC1}}{2N_1 S_c} t_B, \tag{53}$$

- if $U_{DC1} > U_{DC2}/n$ (Figure 11b):

$$B_M = \frac{\Delta B_1 + \Delta B_2}{2} = \frac{1}{4N_1 S_c}\left[U_{DC1}\frac{T_S}{2} + \frac{U_{DC2}}{n} t_B\right], \tag{54}$$

- if $U_{DC1} < U_{DC2}/n$ (Figure 11c):

$$B_M = \frac{\Delta B_1 + \Delta B_2}{2} = \frac{1}{4N_1 S_c}\left[U_{DC1} t_B + \frac{U_{DC2}}{n}\frac{T_S}{2}\right], \tag{55}$$

where S_C is a cross-sectional area of the core.

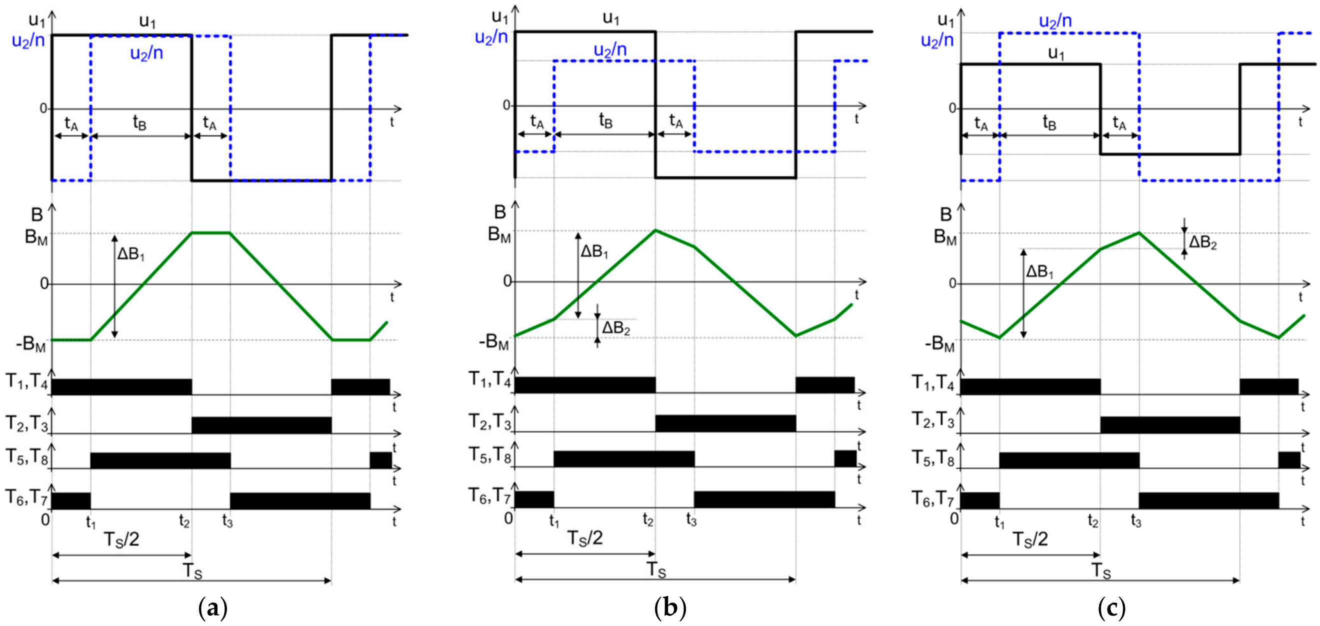


Figure 11. Simplified waveforms of voltages u_1, u_2/n and magnetic induction B for (**a**) $U_{DC1} = U_{DC2}/n$; (**b**) $U_{DC1} > U_{DC2}/n$; (**c**) $U_{DC1} < U_{DC2}/n$.

To simplify the estimation of the transformer windings' power loss P_{CU}, calculations may be performed for the windings' resistance measured for the switching frequency $f_S = 1/T_S$ and the rms value of the windings' currents according to the formula [32]:

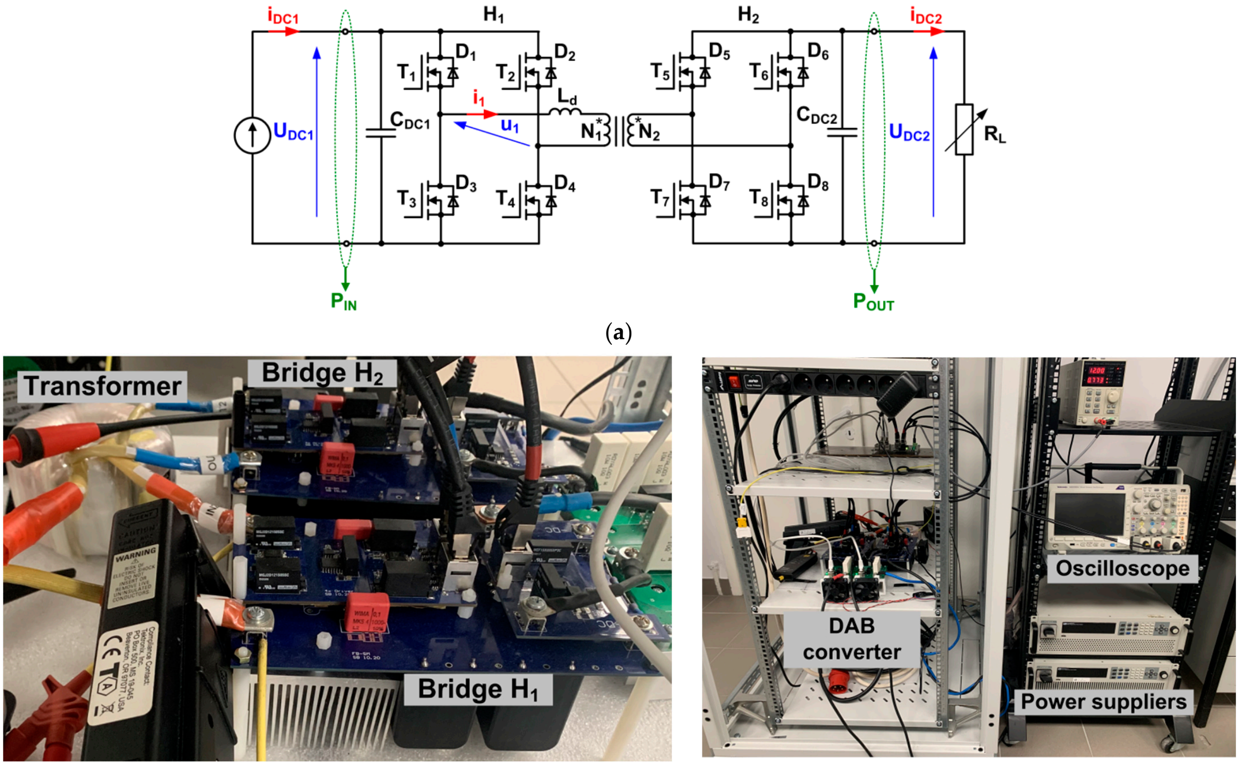
$$P_{\mathrm{CU(prim)}} + P_{\mathrm{CU(sec)}} = R_{\mathrm{CU(prim)}} \cdot I^2_{1\mathrm{(rms)}} + R_{\mathrm{CU(sec)}} \cdot I^2_{2\mathrm{(rms)}}, \tag{56}$$

where $R_{CU(prim)}$, $R_{CU(sec)}$ are the resistances of the transformer windings (respectively at the H_1 bridge side and H_2 bridge side) measured for the switching frequency f_S; $I_{1(rms)}$ is the rms value of the transformer current at the bridge H_1 side; $I_{2(rms)}$ is the rms value of the transformer current at the bridge H_2 side given by:

$$I_{2(rms)} = \frac{I_{1(rms)}}{n} = \frac{1}{n}\sqrt{\frac{2}{3T_S}\left[\frac{I_3^3 + I_2^3}{I_3 + I_2}t_A + \frac{I_3^3 - I_2^3}{I_3 - I_2}t_B\right]}. \tag{57}$$

6. Validation

The parameters that are required for DAB converter efficiency calculation using the proposed approach were collated and are explained in Table 1. The described approach was validated by a comparison of the estimated DAB efficiency characteristics with the experimental ones measured for the converter, whose parameters are shown in Table 2. To measure the input P_{IN} and output P_{OUT} power (Figure 12) of the tested DAB converter, a Yokogawa WT5000 precision power analyzer was used. Importantly, the experimental measurements were performed for the DAB converter in a basic configuration without any additional sub-circuits (e.g., start-up resistors were disconnected). Voltages U_{DC1} and U_{DC2} were kept at a constant level U_{DC1} = 670 V and U_{DC2} = 385 V and the output P_{OUT} power was controlled by changes in the load resistance R_L. In the applied laboratory conditions, the maximum output power was limited to 5 kW due to the limitation of the measurement range of the used power analyzer. Waveforms of the current i_1 and voltage u_1 in the AC circuit were measured using a Tektronix DPO3034 oscilloscope equipped with the high-voltage differential probe P5210A and the current probe TCP404XL.



(**a**)

(**b**) (**c**)

Figure 12. Laboratory setup for the experimental tests: (**a**) Scheme; (**b**) tested DAB converter; (**c**) laboratory stand.

Table 1. The parameters required for the DAB efficiency estimation.

Parameter	Explanation
P_{OUT}	Output power [W]
U_{DC1}	Input voltage [V]
U_{DC2}	Output voltage [V]
$n = N_1/N_2$	Transformer turns ratio
T_S	Switching period [s]
L_d	Inductance of the additional inductor [-]
$L_{\delta 1}$	Leakage inductance of transformer winding at the H_1 bridge side [-]
$L_{\delta 2}$	Leakage inductance of transformer winding at the H_2 bridge side [-]
$U_{DS(N)}$	Rated value of MOSFET drain–to–source voltage [V]
$I_{D(N)}$	Rated value of MOSFET drain current [A]
U_{FO}	Diode threshold voltage [V]
r_D	Diode dynamic resistance [Ω]
C_{iss}	MOSFET input capacitance [F]
C_{rss}	MOSFET reverse transfer capacitance [F]
R_G	MOSFET external gate resistance [Ω]
U_{DR}	MOSFET gate driver voltage [V]
$U_{GS(TH)}$	MOSFET gate threshold voltage [V]
$U_{GS(P)}$	Minimal value of the MOSFET gate-to-source voltage enabling the conduction of load current I_O [V]
$t_{RR(N)}$	Nominal value of the diode D_Z reverse recovery time measured for the nominal load current $I_{O(N)}$ [s]
$A_{iDZ(N)}$	Nominal derivative with time of the diode current during reverse recovery current measurement [A/s]
$I_{RM(N)}$	Diode nominal reverse current measured for $A_{iDZ(N)}$ and $I_{O(N)}$
f	Induction frequency [Hz]
B_M	Induction peak value [T]
T_C	Transformer core temperature [°C]
V_C	V_C—core volume [cm^3]

Table 2. The DAB converter specifications.

Parameter	Specification
Rated output power	5 kW
U_{DC1}	670 V
U_{DC2}	385 V
T_1–T_8, D_1–D_8	F4-23MR12W1M1_B11 (Infineon)
Switching frequency	50 kHz
N_1/N_2	33/18
Transformer	3C95 ferrite core (SMA Magnetics) $O_D = 87/I_D = 5\ 6/H = 50$ mm
L_d	25 µH

At the first step, the accuracy of the input current average value estimation $I_{DC1(av)}$ was evaluated. For the known values of the output power P_{OUT} and voltage U_{DC2}, based on Equations (7)–(10), the average value of the input current was calculated and compared with the experimental results. The maximum noted difference between the estimated and measured values did not exceed 10% and the accuracy increased with the growth in the output power and input current value (Figure 13). Crucially, the proposed analytical approach was simplified, so the impact of some factors (e.g., time dead influence) was not factored in. As a result, the accuracy of the estimation at a lower level of load may be worse.

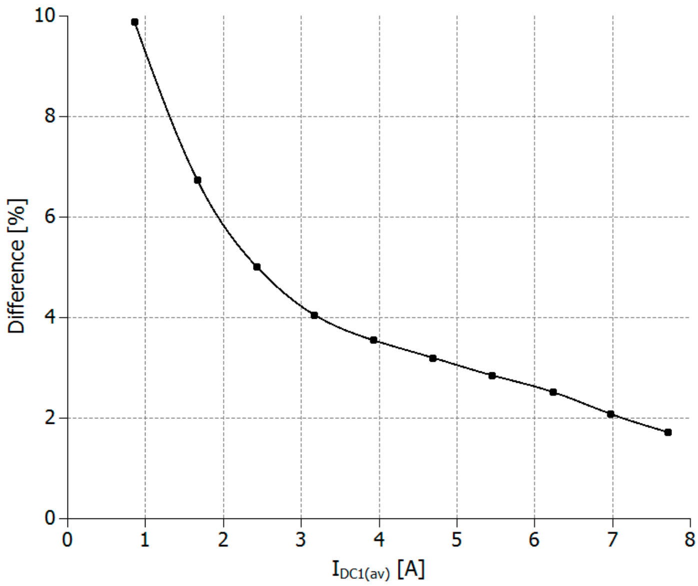


Figure 13. Difference between the measured and estimated average value of the input current i_{DC1}.

A similar conclusion may be drawn for the comparison of the DAB estimated and measured energy efficiency characteristics (Figure 14). The estimated η (P_{OUT}) characteristic followed the shape of the measured one with the highest accuracy noted for the output power exceeding 50% of the maximum out-power. The maximum noted efficiency for the tested DAB converter in a specific range of output power up to 5 kW reached 98%, which was confirmed by both the experimental and analytical results.

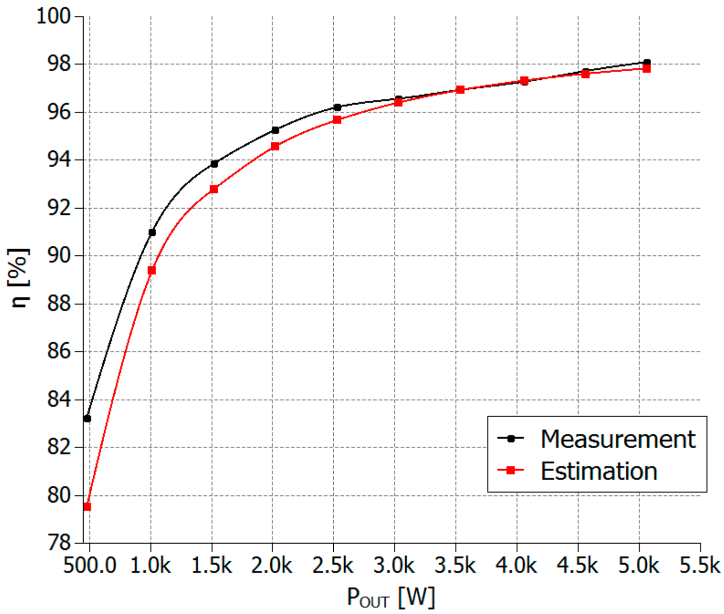


Figure 14. The estimated and measured energy efficiency characteristics of the tested DAB converter.

The application of the proposed analytical method enabled an estimation of the power loss distribution for the main converter components. Based on the estimated characteristics presented in Figure 15, it can be stated that the power losses were mainly generated in bridges H_1 and H_2. Notably, the considered DAB converter operated in conditions that correlated with the theoretical current and voltage waveforms presented in Figure 4a. As a result, transistors T_1–T_4 were turned on under hard-switching conditions with current $I_1 > 0$ and $I_1 = -I_3$. Thus, the commutation power losses in bridge H_1 resulted from the transistor's turn-on process and the reverse recovery process of diodes D_1–D_4. Because value I_1 decreases with the growth of the DAB output power (Figure 16), the commutation losses in bridge H_1 also decrease, so, as a consequence, the bridge H_1 total power loss P_{H1} is reduced.

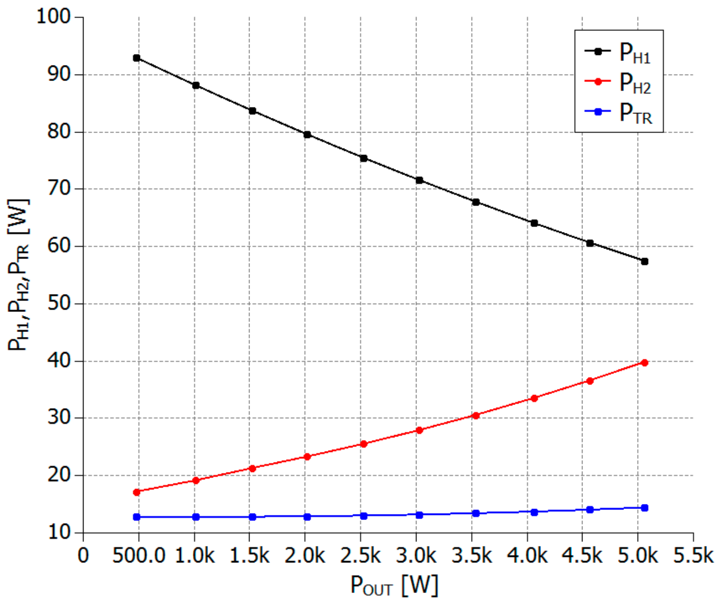


Figure 15. The estimated power loss distribution of the tested DAB converter.

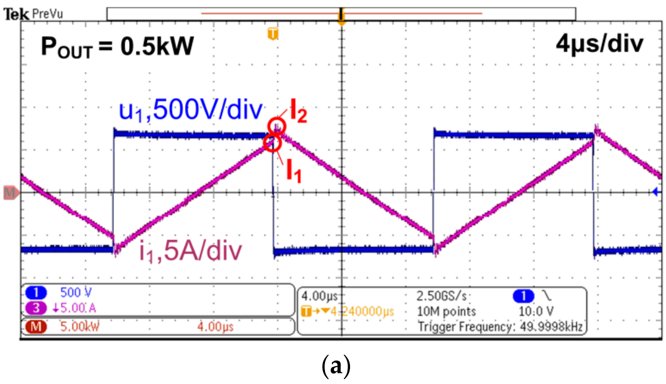


Figure 16. Experimental waveforms of the current i_1 and voltage u_1 measured for: (**a**) P_{OUT} = 0.5 kW; (**b**) P_{OUT} = 2 kW.

From Figure 4a, T_5–T_8 were turned off under hard-switching conditions with the current determined by the value of $I_2/n = -I_4/n$. Similarly, since the I_2 value increased with the growth of the out-power P_{OUT} (Figure 16), the transistor's commutation losses increased, so in bridge H_2, the total power loss P_{H2} grew. From Figure 15, the transformer loss P_{TR} obtained using Equation (49) was significantly lower than the losses noted for bridges H_1 and H_2.

Losses generated in each of the bridges H_1 and H_2 were mainly determined by switching losses, however, the share of conduction losses increased with the growth in the DAB converter output power, which resulted from Equations (14) and (15) (Figure 17).

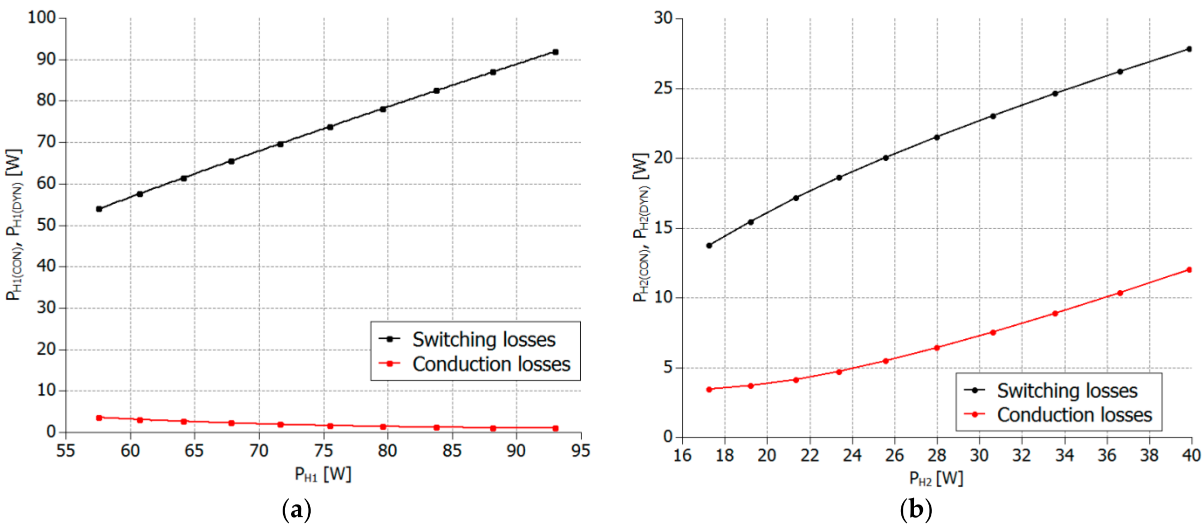


Figure 17. Estimated power loss distribution in the considered DAB converter bridges: (**a**) bridge H_1; (**b**) bridge H_2.

Based on the results of the analytical calculation, transformer losses P_{TR} are determined by the loss in the core P_{FE} (Figure 18). In the tested DAB converter, for the specified range of output power up to 5 kW, the value t_B changed within a small range (coefficient $t_B/(0.5T_S)$ does not fall below 0.95), hence, according to Equations (50)–(55), a slight reduction in the core loss P_{FE} was observed. The windings' total power loss P_{CU} depends on the rms value of the primary and secondary windings currents, so it should grow with the increase in the DAB converter output power, which was confirmed by the results of the analytical calculations.

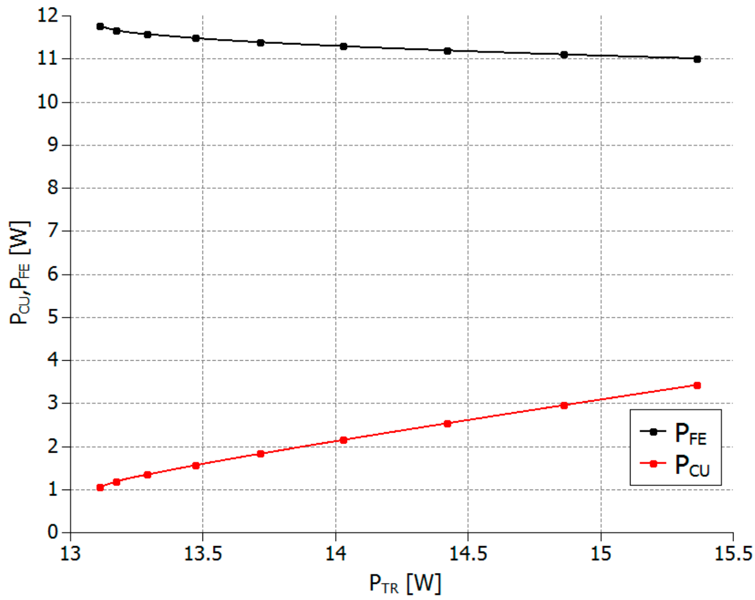


Figure 18. The estimated transformer power loss distribution in the DAB converter.

The presented calculations were also performed for the case when energy was transmitted from bridge H_2 to H_1. In this case, the obtained analytical characteristic $\eta(P_{OUT})$ was also confirmed by the results of the experimental measurements, which validated the adopted approach (Figure 19). Moreover, the results of a detailed analysis of power loss distribution were also convergent with the description above.

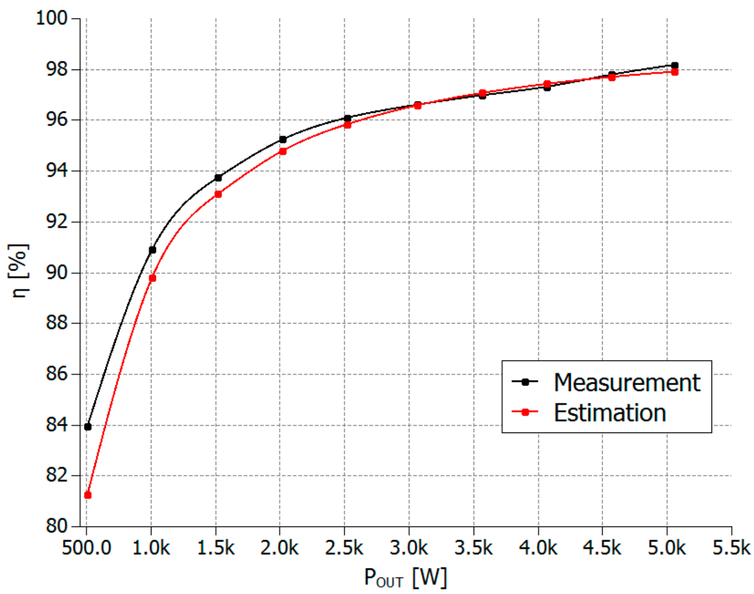


Figure 19. The estimated and measured energy efficiency characteristics of the tested DAB converter for the case when energy is transferred from bridge H_2 to H_1.

Obtained results were compared with ones calculated using the approach proposed in [19]. Adapting this solution is not time-consuming, and all of the required parameters may be obtained based on the manufacturer's datasheet. However, in [19], no methods of transformer loss estimation were proposed, so in both approaches, the same setup of equations based on Steinmetz's formula was used to evaluate the transformer losses. Using both of the compared methods, the obtained efficiency characteristics, calculated for the case when energy was transferred from bridge H_1 to H_2, are presented in Figure 20a. Higher accuracy of the proposed solution was noted, especially for the light load of the converter.

At higher loads, the predominance of the proposed method was also distinguishable. However, the difference between the measured and estimated results using the approach in [19] decreased with the growth in the output power P_{OUT}. One of the main assumptions of the method in [19] is that all transistors are switched-on under soft conditions. It should be noted that considering the assumed direction of energy flow, the transistors in bridge H_1 are turned on under hard-switching conditions. As a result of the transistors' turn-on power losses omission, the total losses of bridge H_1 were underestimated, as presented in Figure 20b. Both compared methods enabled the estimation of the transistors' turn-off losses. However, to simplify the calculations, in the method [19], constant values of the current fall time were assumed. For the converter light load, the obtained power losses of bridge H_2 were comparable. However, the difference between the calculated results slightly increased with the growth in the output power P_{OUT}.

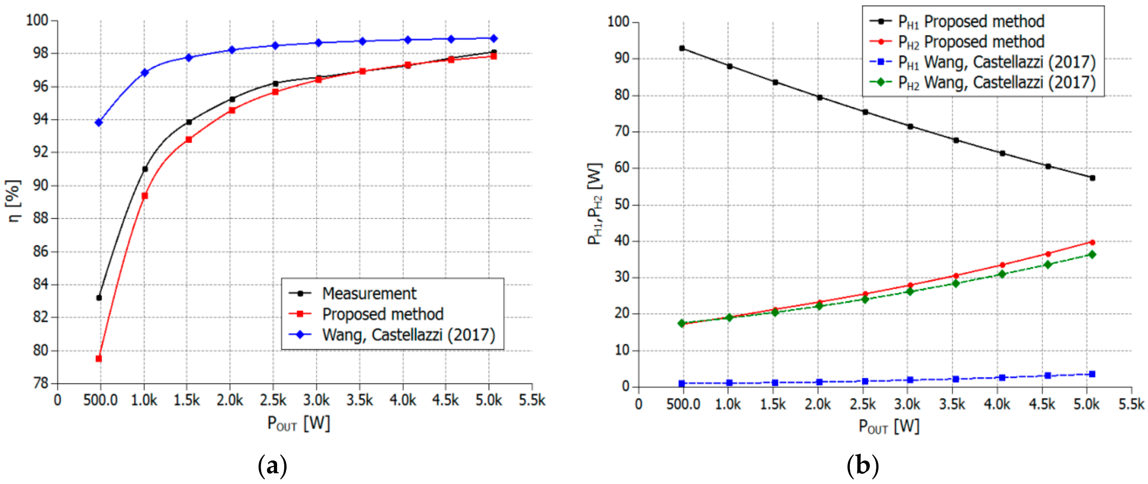


Figure 20. Comparison of the results obtained using the proposed method and approach presented by Wang and Castellazzi in [19]: (**a**) estimated and measured energy efficiency characteristics of the tested DAB converter; (**b**) power loss characteristics of bridges H_1 and H_2.

7. Conclusions

In this paper, an analytical method of power loss estimation in a single-phase DAB converter controlled with a SPS modulation scheme is presented. The obtained results of the calculations were confirmed by the results of the measurements, which proved the correctness of the adopted approach. The method of optimizing the efficiency of the DAB converter proposed and confirmed in the simulation tests can be used in the process of designing converters at the HW level. The proposed method will allow us to complete the calculation of the correct operating point of the system, which will reduce the risk of failure by reducing the operating temperature of the transistors and passive components. Future studies will be focused on the validation of the presented method in a three-phase DAB converter and for DAB converters driven with other switching schemes.

Author Contributions: Conceptualization, M.T., S.B. and M.J.; Methodology, M.T., S.B. and S.P.; Validation, M.T., S.B., M.R. and S.P.; Formal analysis, M.T., M.J. and H.-J.C.; Investigation, M.T., S.B., M.R., M.J. and S.P.; Resources, M.T., S.B., M.R., S.-H.K. and Y.-C.C.; Data curation, M.T., M.J. and H.-J.C.; Writing—original draft preparation, M.T., M.J. and H.-J.C.; Writing—review and editing, M.T., M.J., S.B., S.P., H.-J.C., S.-H.K. and Y.-C.C.; Visualization, M.T. and S.B.; Supervision, M.T. and M.J.; Project administration, M.J and H.-J.C.; Funding acquisition, M.J. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Center for Research and Development, and the National Science and Technology Council of Taiwan, Grant NSTC 111-2622-8-011-014-SB within the framework of the project entitled Poland–Taiwan cooperation POLTAJ VII 7th competition Path 1.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Han, W.; Ma, R.; Liu, Q.; Corradini, L. A conduction losses optimization strategy for DAB converters in wide voltage range. In Proceedings of the IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, Italy, 23–26 October 2016; pp. 2445–2451. [CrossRef]
2. Zeng, J.; Rao, Y.; Lan, Z.; He, D.; Xiao, F.; Liu, B. Multi-Objective Unified Optimal Control Strategy for DAB Converters with Triple-Phase-Shift Control. *Energies* **2021**, *14*, 6444. [CrossRef]
3. Zhu, M.; Shao, C.; Wang, S.; Hang, L.; He, Y.; Fan, S. System Design of Dual Active Bridge (DAB) Converter Based on GaN HEMT Device. In Proceedings of the 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), Harbin, China, 11–14 August 2019; pp. 1–6. [CrossRef]
4. Xu, X.; Bao, G.; Ma, M.; Wang, Y. Multi-Objective Optimization Phase-Shift Control Strategy for Dual-Active-Bridge Isolated Bidirectional DC-DC Converter. *Inf. MIDEM J. Microelectron. Electron. Compon. Mater.* **2021**, *51*, 179. [CrossRef]
5. Hoang, K.D.; Wang, J. Design optimization of high frequency transformer for dual active bridge DC-DC converter. In Proceedings of the 2012 XXth International Conference on Electrical Machines, Marseille, France, 2–5 September 2012; pp. 2311–2317. [CrossRef]
6. Yao, P.; Jiang, X.; Xue, P.; Li, S.; Lu, S.; Wang, F. Design Optimization of Medium-Frequency Transformer for DAB Converters with DC Bias Capacity. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *9*, 5043–5054. [CrossRef]
7. Xiao, Y.; Zhang, Z.; Andersen, M.A.E.; Sun, K. Impact on ZVS Operation by Splitting Inductance to Both Sides of Transformer for 1-MHz GaN Based DAB Converter. *IEEE Trans. Power Electron.* **2020**, *35*, 11988–12002. [CrossRef]
8. Yan, H.; Zhao, W.; Buticchi, G.; Gerada, C. Active Thermal Control for Modular Power Converters in Multi-Phase Permanent Magnet Synchronous Motor Drive System. *IEEE Access* **2021**, *9*, 7054–7063. [CrossRef]
9. Mukunoki, Y.; Horiguchi, T.; Nakayama, Y.; Nishizawa, A.; Nakamura, Y.; Konno, K.; Kuzumoto, M.; Akagi, H. Modeling of a silicon-carbide MOSFET with focus on internal stray capacitances and inductances, and its verification. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 2671–2677. [CrossRef]
10. Zhuolin, D.; Dong, Z.; Tao, F.; Xuhui, W. A simple SiC power MOSFET model. In Proceedings of the IECON 2017-43rd Annual Conference of the IEEE Industrial Electronics Society, Beijing, China, 29 October 2017–1 November 2017; pp. 704–708. [CrossRef]
11. Rabkowski, J.; Płatek, T. A study on power losses of the 50 kVA SiC converter including reverse conduction phenomenon. *Bull. Pol. Acad. Sci. Tech. Sci.* **2016**, *64*, 907–914. [CrossRef]
12. Kolar, J.; Zach, F.; Casanellas, F. Losses in PWM inverters using IGBTs. *IEE Proc. Electr. Power Appl.* **1995**, *142*, 285–288. [CrossRef]
13. Meng, Z.; Wang, Y.-F.; Yang, L.; Li, W. Analysis of Power Loss and Improved Simulation Method of a High Frequency Dual-Buck Full-Bridge Inverter. *Energies* **2017**, *10*, 311. [CrossRef]
14. Mestha, L.K.; Evans, P.D. Optimisation of losses in PWM inverters. In Proceedings of the Third International Conference on Power Electronics and Variable-Speed Drives, London, UK, 13–15 July 1988; pp. 394–397.
15. Gopalan, A. Calculating Power Dissipation for a H-Bridge or Half Bridge Driver. 2022. Available online: https://www.ti.com/lit/an/slva504a/slva504a.pdf (accessed on 1 October 2022).
16. Barlik, R.; Nowak, M.; Grzejszczak, P. Power transfer analysis in a single phase dual active bridge. *Bull. Pol. Acad. Sci. Tech. Sci.* **2013**, *61*, 809–828. [CrossRef]
17. Saha, J.; Gorla, N.B.Y.; Subramaniam, A.; Panda, S.K. Analysis of Modulation and Optimal Design Methodology for Half-Bridge Matrix-Based Dual-Active-Bridge (MB-DAB) AC–DC Converter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *10*, 881–894. [CrossRef]
18. De Freitas Lima, G.; Lembeye, Y.; Ndagijimana, F.; Crebier, J.-C. Modeling of a DAB under phase-shift modulation for design and DM input current filter optimization. In Proceedings of the 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, 7–11 September 2020; pp. P.1–P.10. [CrossRef]
19. Wang, Z.; Castellazzi, A. Device loss model of a fully SiC based dual active bridge considering the effect of synchronous rectification and deadtime. In Proceedings of the 2017 IEEE Southern Power Electronics Conference (SPEC), Puerto Varas, Chile, 4–7 December 2017; pp. 1–7. [CrossRef]
20. Jean-Pierre, G.; Altin, N.; El Shafei, A.; Nasiri, A. Overall Efficiency Improvement of a Dual Active Bridge Converter Based on Triple Phase-Shift Control. *Energies* **2022**, *15*, 6933. [CrossRef]
21. Krismer, F.; Kolar, J.W. Accurate Power Loss Model Derivation of a High-Current Dual Active Bridge Converter for an Automotive Application. *IEEE Trans. Ind. Electron.* **2009**, *57*, 881–891. [CrossRef]
22. Das, A.K.; Fernandes, B.G. Fully ZVS, Minimum RMS Current Operation of Isolated Dual Active Bridge DC-DC Converter Employing Dual Phase-Shift Control. In Proceedings of the 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, 3–5 September 2019; pp. P.1–P.10. [CrossRef]
23. Calderon, C.; Barrado, A.; Rodriguez, A.; Alou, P.; Lazaro, A.; Fernandez, C.; Zumel, P. General Analysis of Switching Modes in a Dual Active Bridge with Triple Phase Shift Modulation. *Energies* **2018**, *11*, 2419. [CrossRef]
24. Guzmán, P.; Vázquez, N.; Liserre, M.; Orosco, R.; Castillo, S.E.P.; Hernández, C. Two-Stage Modulation Study for DAB Converter. *Electronics* **2021**, *10*, 2561. [CrossRef]

25. Zhang, H.; Isobe, T. An Improved Charge-Based Method Extended to Estimating Appropriate Dead Time for Zero-Voltage-Switching Analysis in Dual-Active-Bridge Converter. *Energies* **2022**, *15*, 671. [CrossRef]
26. Ahmed, R.M.; Todd, R.; Forsyth, A.J. Predicting SiC MOSFET Behavior Under Hard-Switching, Soft-Switching, and False Turn-On Conditions. *IEEE Trans. Ind. Electron.* **2017**, *64*, 9001–9011. [CrossRef]
27. Agrawal, B.; Preindl, M.; Bilgin, B.; Emadi, A. Estimating switching losses for SiC MOSFETs with non-flat miller plateau region. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 2664–2670. [CrossRef]
28. Naseri, F.; Farjah, E.; Ghanbari, T. KF-based estimation of diode turn-off power loss using datasheet information. *Electron. Lett.* **2019**, *55*, 1082–1084. [CrossRef]
29. Kundu, U.; Sensarma, P. Accurate Estimation of Diode Reverse-Recovery Characteristics from Datasheet Specifications. *IEEE Trans. Power Electron.* **2018**, *33*, 8220–8225. [CrossRef]
30. Jahdi, S.; Alatise, O.; Bonyadi, R.; Alexakis, P.; Fisher, C.A.; Gonzalez, J.A.O.; Ran, L.; Mawby, P. An Analysis of the Switching Performance and Robustness of Power MOSFETs Body Diodes: A Technology Evaluation. *IEEE Trans. Power Electron.* **2014**, *30*, 2383–2394. [CrossRef]
31. Yin, S.; Liu, Y.; Liu, Y.; Tseng, K.J.; Pou, J.; Simanjorang, R. Comparison of SiC Voltage Source Inverters Using Synchronous Rectification and Freewheeling Diode. *IEEE Trans. Ind. Electron.* **2017**, *65*, 1051–1061. [CrossRef]
32. Barlik, R.; Nowak, M.; Grzejszczak, P.; Zdanowski, M. Analytical description of power losses in a transformer operating in the dual active bridge converter. *Bull. Pol. Acad. Sci. Tech. Sci.* **2016**, *64*, 561–574. [CrossRef]
33. Rodriguez-Sotelo, D.; Rodriguez-Licea, M.A.; Araujo-Vargas, I.; Prado-Olivarez, J.; Barranco-Gutiérrez, A.-I.; Perez-Pinal, F.J. Power Losses Models for Magnetic Cores: A Review. *Micromachines* **2022**, *13*, 418. [CrossRef] [PubMed]