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A Generalized Switched-Capacitor Multilevel Inverter Topology with Voltage Boosting Ability and Reduced Inrush Current

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Abstract: This article presents a novel quadruple boost inverter (QBI) with an integrated boost stage that comprises an inductor, a capacitor, a switch, and an input source. The inductor on the input side limits the inrush current and also the capacitor charging current ripples. The QBI topology comprises a dc source, an input inductor, nine switches, three diodes, and capacitors. This produces a nine-level waveform, which reduces the need for additional filters such as inductors and capacitors. The proposed QBI is elementary, compact, and needs fewer components than existing nine levels inverter. Compared to the typical triangular carrier-based sinusoidal pulse width modulation, the newly developed parabolic level-shifted carrier has a much greater RMS value. Another advantage of the proposed topology is extension for generating higher voltage levels without increment in the blocking voltage across the switches. This makes the topology ideal for medium voltage high power applications. The output voltage has been determined in terms of selection, sizing, and expression. The proposed QBI is compared to existing similar nine-level inverters in order to assess its efficacy. The experiment is performed on a laboratory prototype to state the practical feasibility of QBI topology for the inductive load, variation in input, load, and modulation index.

Keywords: switched-capacitor cell; harmonics; multilevel inverter; boost inverter; power loss

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1. Introduction

The current power electronics converter design trend emphasizes high power density while maintaining great efficiency. The multilevel inverters (MLIs) with these features are widely accepted for grid-connected photovoltaic applications [1,2]. Variable frequency drives (VFDs), uninterrupted power supply (UPS), and several industrial drives [3] are some of the other uses of MLIs. Compared to previously available two-level inverters, the virtues of MLI arose from the increase in output voltage waveform performance. The improvement may be seen in the size of DC links and filters. Another merit is less voltage stress across components that includes switches, diodes, and capacitors. The power loss across the DC links and filter are also reduced due to reduction in size. Another benefit of MLI is the outstanding output voltage and better harmonic profile. It also means that switches with lower voltage ratings (IGBTs/MOSFETs) can be employed, as well as a smaller output filter.

The capacitor is an energy storing element with the ability to use the power converters for medium-to-high power applications. Thus, switched-capacitor inverters are commonly accepted. The switched-capacitor inverters were created as a result of a topology described in [4–6]. Many more topologies have emerged in the case of switched-capacitor MLIs [7–11]. In these topologies, all the dc sources and capacitors come in a series for generating the peak voltage level. Thus, all capacitors must discharge for peak level generation, eventually

featuring voltage boosting across inverter's output. The capacitors charge in a closed circuit during intermediate stages. In certain cases, multiple switched capacitors are charged using additive potential of the DC source and the capacitors [12]. Topologies based on switching capacitors aid in increasing power density. However, owing to capacitor ripples, which can be observed in the harmonic profile, the power quality degrades dramatically. Refs. [13–22] is a nine-level output waveform produced by several SCMLI. Voltage boosting topologies have several disadvantages, such as high voltage stress across components (switches and capacitors). However, the topologies reported in [12,15,17,19,20] employ fewer switches. However, the number of switches at maximum blocking voltage (MBV) is high. The topologies in [14,16,18,21,22] uses arelatively higher number of switches. A seven switch packed E cell (PEC) to generate nine-level is presented in [23,24]. However, these topologies require two voltage sensors to maintain constant voltage across the flying capacitors. In Siddique et al. and Naik et al. [25,26], an eight switch switched-capacitor topology generate nine levels. However, this topology lacks inductive loading ability due to the usage of unidirectional switches. In Kala and Arora [27], nine levels are obtained using four symmetrical DC sources and ten switches. However, the feasibility of discrete DC sources is difficult here. A few SC-MLI topologies are reported in [8,16] and depicted in Figure 1a,b, respectively. The topology presented in [8] uses nine switches, two diodes, and two capacitors along with an input source. This topology has a lower component count but the problem of high capacitor charging current ripples is not addressed. Similarly, the topology reported in [16] uses ten switches, a diode and an input source. Here, two problems persist: the usage of unidirectional switches does not allow free-wheeling operation, and another problem is high inrush current. To demonstrate the above-mentioned problems the proposed topologies are depicted in Figure 1c,d, which aims to reduce the inrush current, which is a major problem with SC-MLI topologies.

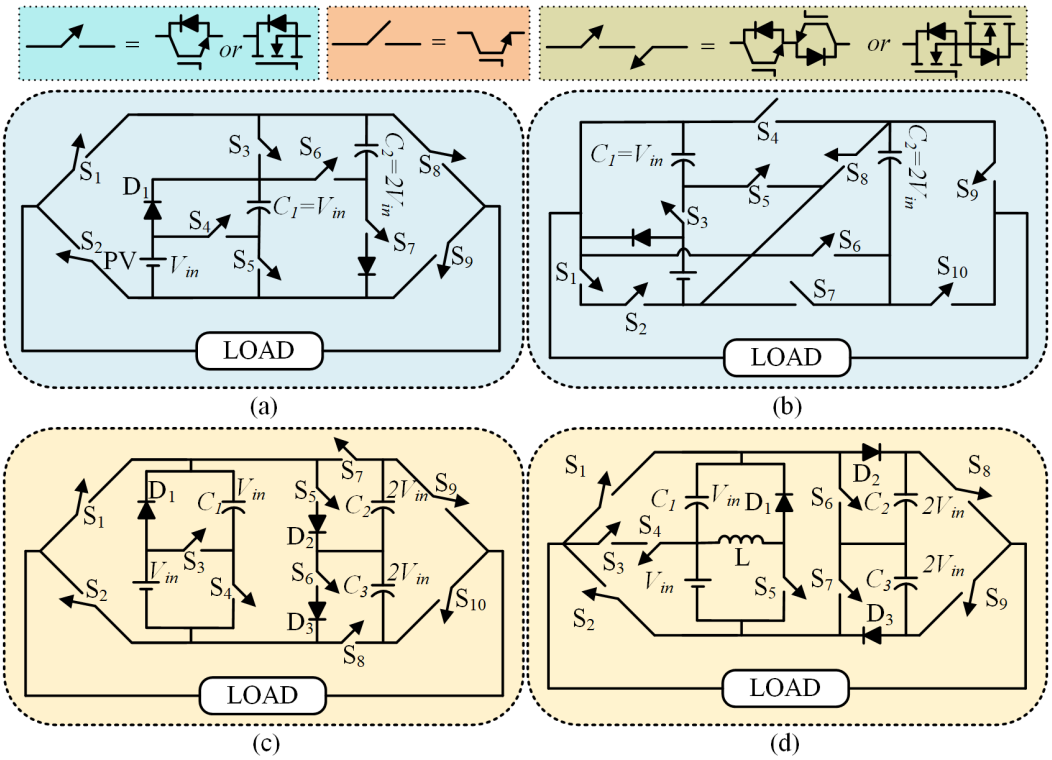

Figure 1. Existing nine-level inverter (**a**) [8], (**b**), [16], (**c**) [1], (**d**) Proposed extended structure.

The performance of SCMLI is compared to the other parameters that affect it. Using switched capacitors, a unique QBI single-phase nine-level inverter is suggested in this

study. The suggested topology offers the following benefits over current nine-level voltage boosting topologies:

1. Component count is reduced (switches, diodes, and capacitors).
2. For an extended structure, lower voltage stress across capacitors.
3. Self-balancing of switched capacitors and inherent polarity generation.
4. Since only four switches conducts at the fundamental frequency, switching losses are greatly reduced.
5. Reduction of high current ripples and smooth charging of switched capacitors.

This work is arranged in Section 2 according to the suggested QBI, which discusses the operation, control, and modulation technique used. The performance analysis is discussed in Section 3 to determine the structure's applicability. Section 4 presents a comparison that illustrates the merits, and conclusions are presented in Section 5.

2. Proposed Topology: Hybrid Modulation Scheme, Operation and Control

2.1. Hybrid Modulation Scheme

The topology presented uses level shifted parabolic carrier pulse width modulation as reported in [12] and depicted in Figure 2. For negative cycle, it is represented on same side as waveform are symmetric. The modulating signal is compared with the reference signal to obtain PWM pulses. The proposed nine-level output voltage (V_O) is quasi-symmetry, V_O is a combination of (V_{Ok}) ($k = 1,2,3,4$) and corresponding time is $0 < t_1 < t_2 < t_3 < t_4 < t_5 = \frac{\pi}{2}$. The Fourier series expansion for quasi-square wave for output voltage is expressed as

$$V_{Ok} = \frac{2V_{in}}{\pi} \sum_{m=1,2,3,4}^{\infty} \frac{cos(m\omega t_k)}{m} sin(m\omega t) \quad (1)$$

$$V_O = \frac{2V_{in}}{\pi} \sum_{m=1,2,3,4}^{\infty} \sum_{k=1}^{4} \frac{cos(m\omega t_k)}{m} sin(m\omega t) \quad (2)$$

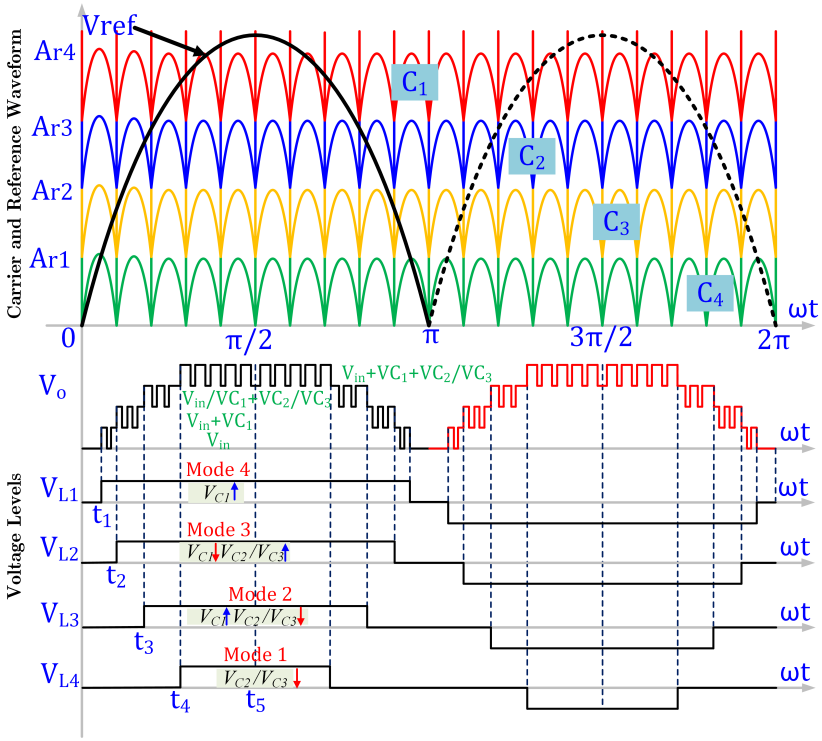

Figure 2. Parabolic carrier-based modulation scheme for QBI.

From Equation (2) the fundamental component for the output voltage is expressed as

$$V_{fund.} = \frac{2V_{in}}{\pi} \sum_{k=1}^{4} cos(\omega t_k) sin(\omega t) \tag{3}$$

Now, the modulation index for the fundamental ($M_{fund.}$) is formulated as

$$M_{fund.} = \frac{1}{4} \sum_{k=1}^{4} cos(\omega t_k) \tag{4}$$

2.2. Operation of QBI Topologies

The first topology uses ten switches, three diodes, and three capacitors. The second topology uses nine switches, three diodes, and three capacitors. Here, two switches are operated as a bidirectional switch to block the voltage from the boost module. The boost module in the second topology has an inductor (L), capacitor C_1, a diode, and the switch S_5. The voltage across the boost module is expressed as $V_{in} = V_L = V_{C1}$.

The operating modes are enlisted in both topologies in Figure 3a,b. As shown in Figure 3a, topology I in Table 1 has the following modes of operation:

Mode I ($\pm 4V_{in}$):- During in this mode, all the capacitors C_1–C_3 will be series with the dc-source by turning ON the corresponding switches to obtain the maximum output voltage of $\pm 4V_{in}$ for both the positive and negative half-cycle at the load.

Mode II ($\pm 3V_{in}$):- In this mode, the input voltage will be directly series with either C_2 or C_3, i.e., discharging the capacitor C_2/C_3 with respect to the direction of the current flow. However, the capacitor C_1 will charge for both the half cycle.

Mode III ($\pm 2V_{in}$):- In this mode the capacitors C_2 or C_3 will be charged to $V_{in} + V_{C1}$ based on the positive or negative cycle and the C_1 will be discharged.

Mode IV ($\pm V_{in}$):- The output voltage will be equal to the input voltage and the capacitor C_1 is sending charge to the source voltage and the capacitors C_2 and C_3 in ideal mode.

Table 1. Operation Table for 9–Level QBI (Figure 1c).

Modes	V_O	**Conducting Switches**	**Capacitor Profile**					
			$I_L > 0$			$I_L < 0$		
			C_1	C_2	C_3	C_1	C_2	C_3
1	$+4V_{in}$	S_2, S_3, S_5, S_9	↓	↓	-	↑	↑	-
2	$+3V_{in}$	S_2, S_4, S_5, S_9	↑	↓	-	↓	↑	-
3	$+2V_{in}$	S_2, S_3, S_6, S_7, S_9	↓	↑	-	↑	↓	-
4	$+1V_{in}$	S_2, S_4, S_7, S_9	↑	-	-	↓	-	-
5	0	S_2, S_4, S_8, S_{10}	↑	-	-	↓	-	-
5	0	S_1, S_4, S_7, S_9	↑	-	-	↓	-	-
4	$-1V_{in}$	S_1, S_4, S_8, S_{10}	↑	-	-	↓	-	-
3	$-2V_{in}$	$S_1, S_3, S_5, S_8, S_{10}$	↓	-	↑	↑	-	↓
2	$-3V_{in}$	S_1, S_4, S_5, S_{10}	↑	-	↓	↓	-	↑
1	$-4V_{in}$	S_1, S_3, S_6, S_{10}	↓	-	↓	↑	-	↑

It is observed that capacitor C_1 charges for almost all odd voltage levels, and discharges for all even levels. The case is similar for C_2, and C_3 for negative levels. The voltage across the balanced capacitor is represented as to achieve quadruple voltage boosting using the expression:

$$V_{C1} = V_{in}; V_{C2} = V_{C3} = V_{in} + V_{C1} \simeq 2V_{in} \tag{5}$$

As shown in Figure 3b, topology II has the following modes of operation, and the corresponding switching sequence are given in Table 2. Assume the inductor charging and discharging is same as conventional boost converter:

Mode I ($\pm 4V_{in}$):- In this mode, either the capacitors C_1, C_2 or C_1, C_3 pair will be discharged

to obtain the maximum output voltage $\pm 4V_{in}$. The corresponding switching sequence for proposed topology is presented in Table 1.

Mode II ($\pm 3V_{in}$):- during in this mode, the capacitor C_1 and C_2 will be discharged but the C_3 will be charged for the positive half cycle. Similarly, the capacitor C_3 and Vin will supply the voltage to the load and C_2 will be charged.

Mode III ($\pm 2V_{in}$):- The sum of the capacitor voltage and source voltage will be added together to produce the maximum output voltage of $\pm 2V_{in}$.

Mode IV ($\pm V_{in}$):- This is the first level of output voltage which is obtained by either discharging the capacitor C_1 for positive half cycle or input voltage for negative output voltage.

Table 2. Operation Table for 9–Level QBI (Figure 1d).

Modes	V_O	Conducting Switches	Capacitor Profile					
			$I_L > 0$			$I_L < 0$		
			C_1	C_2	C_3	C_1	C_2	C_3
1	$+4V_{in}$	S_2, S_6, S_8	↓	↓	-	↑	↑	-
2	$+3V_{in}$	S_3, S_4, S_6, S_8	↓	↓	-	↑	↑	-
3	$+2V_{in}$	S_2, S_5, S_7, S_8	↓	↑	-	↑	↓	-
4	$+1V_{in}$	S_3, S_4, S_8	↓	-	-	↑	-	-
5	0	S_1, S_5, S_8	↑	-	-	↓	-	-
5	0	S_2, S_5, S_9	↑	-	-	↓	-	-
4	$-1V_{in}$	S_3, S_4, S_9	↓	-	-	↑	-	-
3	$-2V_{in}$	S_1, S_5, S_6, S_9	↓	-	↑	↑	-	↓
2	$-3V_{in}$	S_3, S_4, S_7, S_9	↓	-	↓	↑	-	↑
1	$-4V_{in}$	S_1, S_7, S_9	↓	-	↓	↑	-	↑

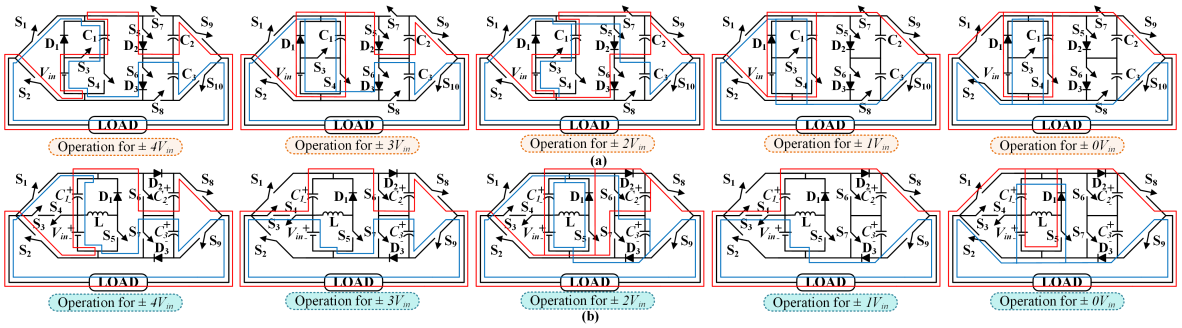

Figure 3. Modes of Operation for QBI (**a**) Topology 1, (**b**) Topology 2.

For both the topologies, the zero state is achieved by either turning on top switches or bottom switches as shown in Figure 3a,b.

According to Table 1, each capacitor charges/discharges for the positive and negative cycles, respectively. The capacitors chosen are determined by the circuit's time constant. This keeps the capacitor balanced, and enough energy is stored to keep the output voltage at excellent quality. Using a mix of DC sources and capacitors, there are five operational modes for obtaining ± 4, ± 3, ± 2, ± 1, and 0. The blocking voltage (BV) of the switch is a significant factor that must be considered in MLI design. The switches S_3,S_4 have a BV of V_{in}, the switches S_1, S_2 have a BV of $2V_{in}$, the switches S_5, S_6, S_7, S_8 have a BV of $3V_{in}$, and the switches S_9, S_{10} have a BV of $4V_{in}$ in the first topology shown in Figure 1c. Similarly, the switches S_3, S_4, have a BV of V_{in}, the switches S_1, S_2, S_5 have a BV of $2V_{in}$, the switches S_6, S_7 have a BV of $3V_{in}$, and the switches S_8, S_9 have a BV of $4V_{in}$ in the second topology shown in Figure 1d. When compared to the first topology, the second topology has a lower total blocking voltage (TBV).

2.3. Selection and Energy Balancing of Capacitors

It is observed from Table 1 and Figure 2, that the capacitors C_1, C_2/C_3, and the voltage source (V_{in}) appears in series for peak voltage levels or Mode 1. The capacitors have a considerable amount of voltage ripples due to the materialistic properties, and numerically it is nearly 10% as mentioned in [18]. The knowledge of charge/discharge period of each capacitor is necessary criteria for selecting the capacitance in the SC-MLI design. Moreover, the size of capacitance also depends on switching frequency, and the load in application. The high switching frequency ensure faster charge/discharge and limiting the size of capacitor. Furthermore, for light load (<1 kW) a relatively small capacitance can fulfil the application and vice versa. As depicted in Figure 2, all the capacitors C_1, C_2/C_3 discharges during Mode 1. Similarly, during Mode 2, the capacitors C_2/C_3 discharge. During Mode 3, the capacitor C_1 charges, and capacitors C_2/C_3 charge. The capacitor C_1 charges during Mode 4. To summarize, the maximum discharge period (MDP) for the capacitors C_2/C_3 occurs in Mode 2, while the MDP for capacitor C_1 occurs in Mode 3 or this capacitor discharges four times for the duration t_2 to t_3 in a fundamental cycle. The staircase waveform for time period ranging from 0 to t_5 is quarter symmetry so the MDP for C_1 and C_2/C_3 for pure resistive load (R_L), and switching frequency (f_{sw}) are expressed as in Equations (6) and (7), respectively.

$$\Delta Q_{C1} = \frac{V_{in}}{4\pi f_{sw} R_L}[4\pi - 3t_3 - 2t_2] \tag{6}$$

$$\Delta Q_{C2,C3} = \frac{V_{in}}{4\pi f_{sw} R_L}[4\pi - 5t_5 - 3t_3] \tag{7}$$

The corresponding voltage ripples for the capacitors C_1, and C_2/C_3 is expressed as

$$\Delta V_{C1} = \frac{V_{in}}{4\pi f_{sw} R_L C_1}[4\pi - 3t_3 - 2t_2] \tag{8}$$

$$\Delta V_{C2,C3} = \frac{V_{in}}{4\pi f_{sw} R_L C_2, C_3}[4\pi - 5t_5 - 3t_3] \tag{9}$$

Considering the maximum allowable voltage ripple (ΔV_{C1}, $\Delta V_{C2,C3}$) the minimum requirement for capacitance is expressed as

$$C1_{min} = \frac{V_{in}}{4\pi f_{sw} R_L \Delta V_{C1}}[4\pi - 3t_3 - 2t_2] \tag{10}$$

$$C_2, C_{3_{min}} = \frac{V_{in}}{4\pi f_{sw} R_L \Delta V_{C1}}[4\pi - 5t_5 - 3t_3] \tag{11}$$

Equations (6)–(10) explain how the size of capacitance is related to the output power and the switching frequency. Here, both the parameters are directly proportional.

The ripple loss across these capacitors is a small percentage of power loss across the voltage ripples and expressed as

$$P_{Rip} = f_{sw}.C_1.(\Delta V_{C1} + \Delta V'_{C1}) + f_{sw}.C_2, C_3 \\ (\Delta V_{C2,C3} + \Delta V'_{C2,C3}) \tag{12}$$

where $\Delta V'_{C1}$ and $\Delta V'_{C2,C3}$ are the small power loss across capacitors C_1, and C_2/C_3 due to continuous switching transition.

2.4. Power Loss Analysis

The following assumptions are used in the power loss study:

- Switch and diode parasitic capacitance are negligible.
- Switches and diodes have a constant junction temperature.

- Temperature variations have no influence on magnets or capacitors in the circuit.
- On-state resistance (R_{DS}), forward resistance (R_D), and equivalent series resistance (ESR) for capacitors C_1, C_2/C_3 are all equal (r_{C1}, r_{C2}, r_{C3}).

The circuit's switching loss is determined by the transition from ON to OFF, OFF to ON, and conduction to OFF. The switching loss for the converter at fundamental cycle is expressed as follows

$$P_{sw} = \frac{1}{6}\left[V_{BV}.I_{DS,on}.t_{on}.f_{sw} + V_{BV}.I_{DS,off}.t_{off}.f_{sw}\right] \quad (13)$$

where V_{BV}—blocking voltage across switches; f_{sw}—switching frequency; t_{on}—on; t_{off}—off times for each switch(es). The current flowing from drain to source in the on and off states is $I_{DS,on}$ and $I_{DS,off}$, respectively.

Each mode conduction loss is listed in Table 3, using the modes of operation for both the topologies as shown in Figure 3. The on-state resistance of the switch $R_{DS,on}$; diode forward resistance r_D, and ESR of capacitors C_1, C_2, and C_3 are r_{C1}, r_{C2}, and r_{C3}, respectively. Considering the input source as V_{in}; diode forward voltage as V_D, and capacitor voltages are represented by v_C. The changing currents of capacitors C_1, C_2, and C_3 are represented by I_{C1}, I_{C2}, and I_{C3}, respectively. However, the conduction loss depends on the voltage drop of the device and current flowing through the device. Here, the other topologies have a high switching current due to non-smooth charging, whereas the proposed topology has a low charging current that highly minimizes the conduction loss. The conduction loss is the combination of loss across the power switches and the diode forward conduction loss. This is calculated by using a generalized expression for conduction loss in switches and diodes presented in Equations (14) and (15), respectively.

$$P_{Cond.Sw} = V_{on,sw}.i_o + r_{DS,on}.i_o \quad (14)$$

$$P_{Cond.D} = V_D.i_o + r_D.i_o^2 \quad (15)$$

where $V_{on,Sw}$ represents the on-state resistance of the switch, V_D is the diode forward voltage drop, and i_O is the load current. Further, the load current expression depends on each voltage level generation and the corresponding equivalent resistance. The ripple loss across the capacitor is evaluated using the formula in Equation (12).

Table 3. Equivalent Circuit for Each Modes.

Modes	Equivalent Circuit	
	Proposed Topology 1	**Proposed Topology 2**
1	$4r_{DS,on} + r_D + r_{C1} + r_{C2/C3}$	$3r_{DS,on} + r_{C1} + r_{C2/C3}$
2	$4r_{DS,on} + 2r_D + r_{C1} + r_{C2/C3}$	$4r_{DS,on} + r_{C1} + r_{C2/C3}$
3	$5r_{DS,on} + r_D + r_{C1} + r_{C2/C3}$	$4r_{DS,on} + r_{C1} + r_{C2/C3}$
4	$4r_{DS,on} + r_D + r_{C1}$	$3r_{DS,on} + r_{C1}$
5	$4r_{DS,on} + r_D + r_{C1}$	$3r_{DS,on} + r_{C1} + r_D$

Figure 4a,b shows the power loss in each of the components (switches, diodes, and capacitors) for the first and second topologies, respectively. It is observed that the efficiency for topology I is 96.1%, while the efficiency for second topology is 96.9%. The considerable reduction in power loss for second topology occurs due to decrease in a switch.

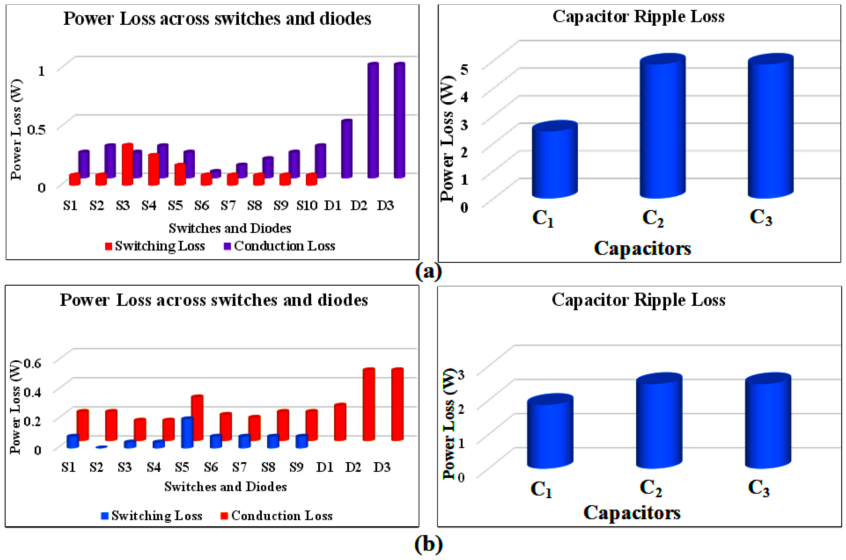

Figure 4. Power loss profile across switches, diodes, and capacitors (**a**) Topology 1 [1], (**b**) Topology 2.

2.5. Generalized Extension of Proposed Topologies

As shown in Figure 5a,b, the suggested topologies may be expanded utilising the module marked in blue colour. This module serves as a voltage doubling network. Table 4 lists the generalized equations for the suggested topology's extension dependent on the number of levels (N_L), switches (N_{Sw}), diodes (N_D), capacitors (N_C), DC sources (N_{DC}), total blocking voltage (TBV), and maximum blocking voltage (MBV). The merit of the extended topology is that it requires only one DC source.

Section 2 confirms that the topology 2 depicted in Figure 1d has better features in terms of component count, lower inrush current and efficiency. Thus, the next section quantifies the performance analysis with the help of experimental validation.

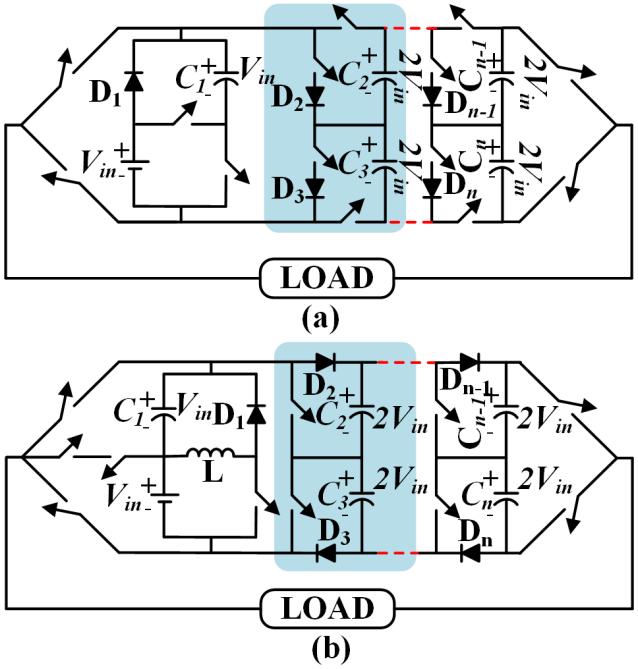

Figure 5. Representation of extended proposed topology (**a**) Topology 1 [1], (**b**) Topology 2.

Table 4. Generalized Formula for Extended Topology.

Parameters	Modular Extension		Level Extension	
	Topology 1	**Topology 2**	**Topology 1**	**Topology 2**
N_L	$4n+5$	$4n+5$	N_L	N_L
N_{Sw}	$4n+6$	$4n+5$	N_L+1	N_L
N_D	$2n+1$	$2n+1$	$\frac{N_L-3}{2}$	$\frac{N_L-3}{2}$
N_C	$2n+1$	$2n+1$	$\frac{N_L-3}{2}$	$\frac{N_L-3}{2}$
MBV	$2n+2$	$2n+2$	$\frac{N_L-1}{2}$	$\frac{N_L-1}{2}$
TBV	$16n+10$	$16n+6$	$4N_L-10$	$4N_L-14$

3. Experimental Validation

The proposed QBI topology presented in Figure 1d is validated with various parameters reported in this section. The power circuit of the experimental prototype consists of 2SK2611 MOSFETs driven using a HPCLA3120 gate drivers. FR604GTA is used as a discrete diode. The APLABL3205 is used as a voltage source. The boost stage is developed using an inductor of 2 mH, and a capacitor C_1 of 2200 µF, 200 V. The other two capacitors, C_2 and C_3, are 4700 µF, 200 V. The controlled gate pulses are provided using dSPACE 1104 RTI controller. The switching frequency of the parabolic carrier signal is set to be 2.5 kHz. The experimental photograph and the gate pulses across all the switches are exemplified in Figure 6a,b, respectively.

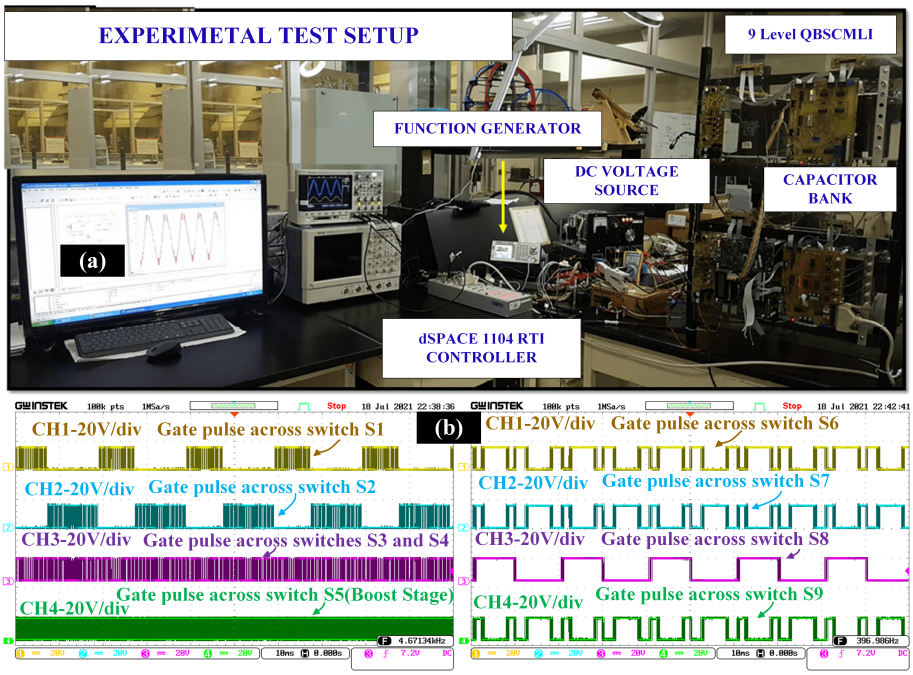

Figure 6. (**a**) Experimental Setup, (**b**) Gate pulses across switches S_1 to S_8.

Initially, the experiment is performed with a resistive-inductive load with the value of 50 Ω, 20 mH depicted in Figure 7. The experimental results for the output voltage, current, inductor voltage, inductor current is presented in Figure 7a, while the capacitor voltage profile, and capacitor charging current is exemplified in Figure 7b,c, respectively. The inductor in the input side limits the high charging current across the capacitors, which is huge in other switched-capacitor topologies. The voltage across the capacitors is $V_{C1} \simeq 30V$,$V_{C2} = V_{C3} \simeq 60V$. The blocking voltages (BV) across the switches is presented in Figure 7c–e, respectively. It is observed that the voltage stress across switches $V_{S1} = V_{S2} = V_{S5} = V_{S6} = V_{S7} \simeq 60V$, switched-capacitor$V_{S3} = V_{S4} \simeq 30V$, $V_{S8} = V_{S9} \simeq 120V$. Later, the experiment was performed for the change in input source voltage, where V_{in}

changes from 20 V to 30 V for same load conditions. The dynamic change transition condition for the output voltage, current, the corresponding changes in the capacitor voltage, and charging current profile is shown in Figure 8a–c, respectively. Here, it is observed that each waveform responds to the dynamic changes and settles in steady state condition. The other case of experiment, the input source voltage (V_{in}) is set to 30 V and the load power factor varies from 0.85 to 1. The corresponding changes in the output voltage, current, capacitor voltage and the charging current is exemplified in Figure 9a–c, respectively. Here, minimal variation is seen in the output voltage and capacitor voltage. However, the load current and the capacitor charging current changes extensively. Finally, the experiment for the variation in modulation index from 0.6 to 1 is carries same load and input conditions. The waveform for the output voltage, output current, voltage and current across capacitor, is exemplified in Figure 10a–c, respectively. It is observed that at low modulation index the output yield is low, along with fewer voltage ripples across the capacitors and vice versa. The voltage and current THD is exemplified in Figure 11a,b, respectively. It is found that the voltage THD is 13.28% and 3.01% respectively at 50 Ω, 20 mH load.

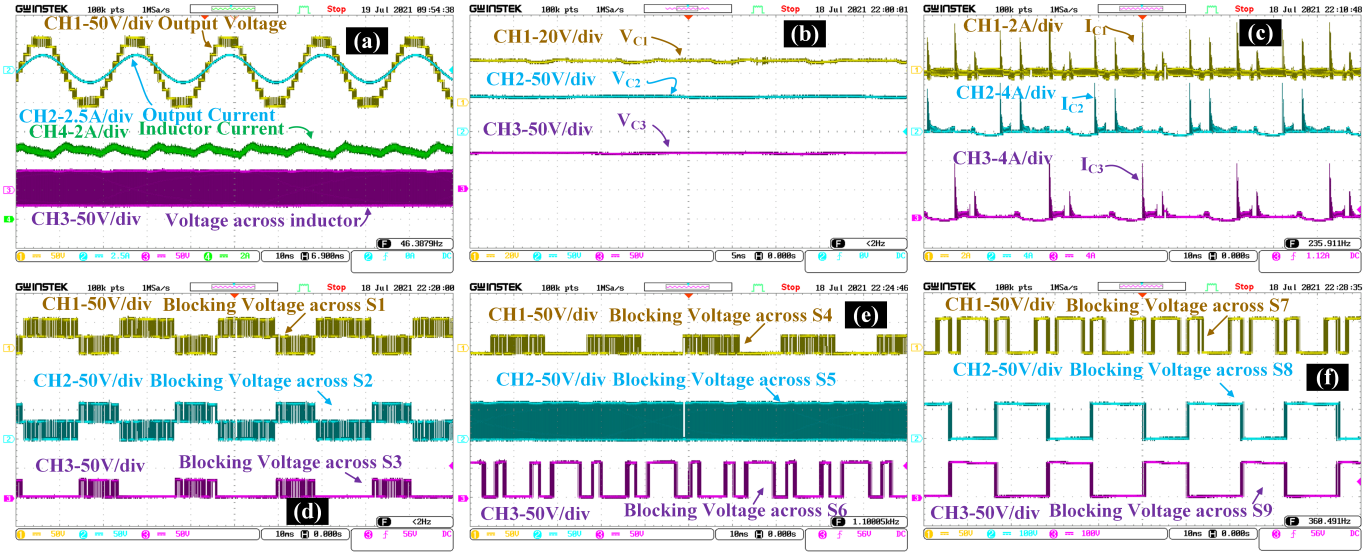

Figure 7. Experimental Results for load 50 Ω, 20 mH at $V_{in} = 30V$. (**a**) Output voltage and Output current, (**b**) Voltage across capacitor (V_{C1}, V_{C2}, V_{C3}), (**c**) Capacitor current profile (I_{C1}, I_{C2}, I_{C3}), (**d**) Blocking Voltage across S_1 to S_3, (**e**) Blocking Voltage across S_4 to S_6, (**f**) Blocking Voltage across S_7 to S_9.

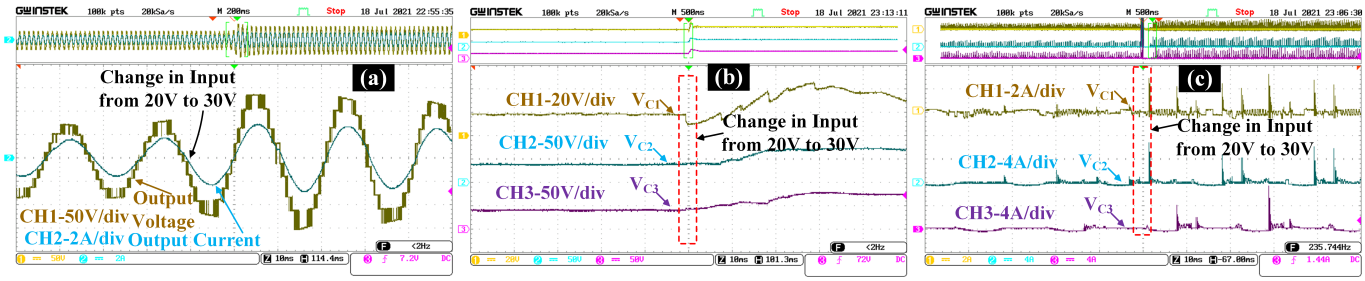

Figure 8. Experimental Results for load 50 Ω, 20 mH when V_{in} changes from 20 V to 30 V. (**a**) Output voltage and Output current, (**b**) Voltage across capacitor (V_{C1}, V_{C2}, V_{C3}), (**c**) Capacitor current profile (I_{C1}, I_{C2}, I_{C3}).

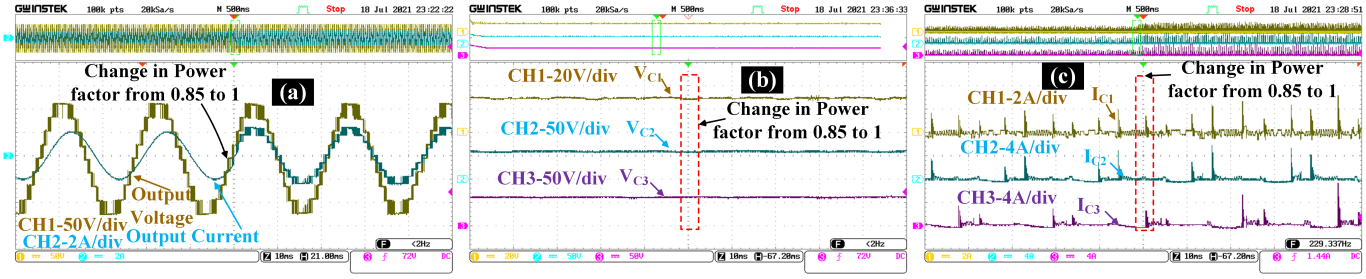

Figure 9. Experimental Results for load when power factor changes from 0.85 to 1 at $V_{in} = 30V$. (**a**) Output voltage and Output current, (**b**) Voltage across capacitor (V_{C1}, V_{C2}, V_{C3}), (**c**) Capacitor current profile (I_{C1}, I_{C2}, I_{C3}).

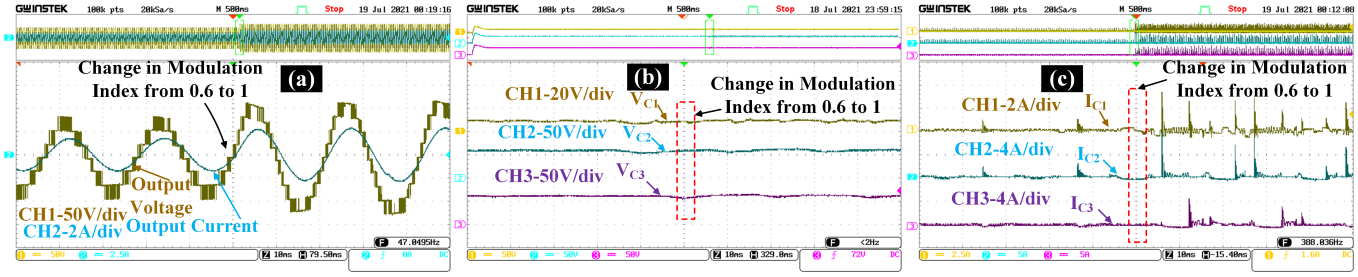

Figure 10. Experimental Results for load 50 Ω, 20 mH when modulation index changes from 0.6 to 1 at fixed $V_{in} = 30$ V. (**a**) Output voltage and Output current, (**b**) Voltage across capacitor (V_{C1}, V_{C2}, V_{C3}), (**c**) Capacitor current profile (I_{C1}, I_{C2}, I_{C3}).

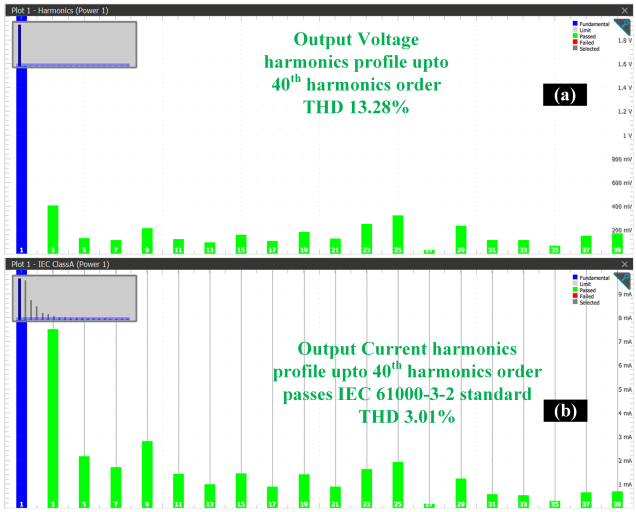

Figure 11. (**a**) Voltage THD using FFT analysis (13.28%), (**b**) Current THD using FFT analysis (3.01%).

4. Comparison Assessment

The usefulness of the suggested topology is demonstrated by comparing it to current quadruple voltage boosting topologies. Table 5 shows that some topologies use fewer switches in comparison to suggested topologies [13,15,19,20]. However, the number of switches with higher MBV is greater in such topologies, which makes the inverter less reliable. The other component that is critical in design is the number of diodes that impacts the inverter's efficiency, as the diode's forward conduction loss is higher in comparison to switches [19,20]. The capacitor ripples are another important aspect in determining the inverter's efficiency. To attain peak voltage, the suggested architecture needs a maximum of two capacitors in series, whereas [13,19,20] use more than two capacitors to achieve the same peak voltage. Similarly, the inverter's efficiency is determined by the number of conducting switches. Table 5 shows that only a few topologies have fewer conducting switches than the suggested topologies [13,16,20], while others constitute larger or equiva-

lent N_{SC}. The other suggested topology has a similar MBV to the previous topologies, but a lower TBV that includes all semiconductor devices than the topologies stated in [20,22]. The topology's extension is a critical feature that contributes to lower the filter size. Few topologies with extension have been published in [17–22] to give greater voltage levels. Finally, the charging current of capacitors is a critical factor in defining the capacitor's life-cycle, which has an impact on the topology's dependability. In existing literature most of the topologies are prone the problem of high charging current which is not discussed in existing literature. Other nine-level topologies, such as [23–27] are not included in the table. These topologies provide nine levels, but no voltage boosting [23] and double voltage boosting [24–26]. All DC sources must have a nine-level voltage waveform, according to the structure stated in [27]. Figure 12 shows a comparison of efficiency for a few topologies. The suggested topology is shown to have a higher efficiency than [13,16,20,21].

Table 5. State-of-art Single Source Nine Level Inverter Topologies.

Ref	N_{Sw}	N_D	N_{Cap}	N_{DSS}	MBV_D	V_{Cap}			N_{SC}	MBV_{Sw}	TBV_{SC}	EP	CC	Efficiency (%)
						V_{in}	$2V_{in}$	$3V_{in}$						
[13]	8	3	3	2	2	2	1	-	4	$4V_{in}$	$28V_{in}$	No	High	>93% at 50 Hz
[14]	12	-	2	-	-	1	1	-	6	$2V_{in}$	$21V_{in}$	No	NR	NR
[15]	9	3	3	-	1	2	-	1	5	$4V_{in}$	$29V_{in}$	No	High	95.2% at 1 kHz
[16]	10	1	2	1	2	1	1	-	4	$4V_{in}$	$25V_{in}$	No	NR	>94.3% at 50 Hz
[17]	9	1	2	-	1	1	1	-	5	$4V_{in}$	$29V_{in}$	Yes	High	NR
[18]	12	0	3	-	-	1	2	-	6	$4V_{in}$	$24V_{in}$	Yes	NR	96% at 50 Hz
[19]	8	4	4	3	4	2	1	1	4	$4V_{in}$	$29V_{in}$	Yes	NR	95.9% at 50 Hz
[20]	8	6	3	4	4	1	1	1	5	$4V_{in}$	$36V_{in}$	Yes	NR	92.2% at 400 Hz
[21]	13	-	4	-	-	1	2	1	7	$4V_{in}$	$29V_{in}$	Yes	NR	85.9% at 1 kHz
[22]	12	3	2	2	3	1	1	1	7	$4V_{in}$	$30V_{in}$	Yes	NR	NR
P1	10	3	3	-	1	1	2	-	5	$4V_{in}$	$29V_{in}$	Yes	Low	96.1% at 50 Hz
P2	9	3	3	2	2	1	2	-	5	$4V_{in}$	$25V_{in}$	Yes	Low	96.9% at 50 Hz

N_{Sw}—Number of Switches; N_D—Number of Diodes; N_{Cap}—Number of Capacitors; $Cap_{Mag.}$—Magnitude of Capacitance; N_{DSS}—Number of Diodes with voltage stress more than input source; MBV_D—Maximum blocking voltage across diode (in V_{in}); V_{Cap}—Voltage Stress across capacitors (in V_{in}); N_{SC}—Maximum number of conducting switches; MBV_{Sw}—Maximum Blocking Voltage across switch (in V_{in}) TBV_{SC}—Total blocking voltage of all semiconductor devices (in V_{in}); EP—Extension Possibility; CC—Charging Current; NR—Not Reported P1/P2—Proposed topology 1 and 2.

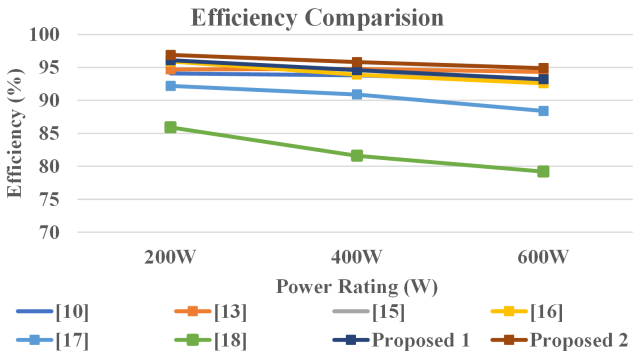

Figure 12. Efficiency comparison with existing literature.

5. Conclusions

A novel two-voltage gain, nine-level switched-capacitor topology has been developed, and the measured findings are discussed. The topology was validated in simulation and prototype hardware. According to the findings, the proposed topology features low current and voltage stress, self-voltage balancing, etc. The inrush current is eliminated by the input side inductor. Additionally, these switched capacitors provide equal energy distribution for the positive and negative cycles and are self-balanced. Additionally, the improved parabolic carriers signal validity test was performed, and the findings show

that the recommended carrier signal contributes to a considerable high RMS voltage than the conventional modulation technique. Shown also are the power loss and efficiency for various load powers are presented. The proposed topology is an appropriate choice for applications involving renewable energy sources based on the above findings.

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