ZVS Realization of H-Bridge Low-Voltage High-Current Converter via Phase-Shift and Saturable Control

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Abstract: A zero-voltage switching (ZVS) H-bridge phase-shifted low-voltage high-current converter with saturable inductors is proposed in this paper. The introduction of saturable inductors solves the short circuit problem caused by high-frequency on–off of the power tube, and effectively inhibits high-frequency voltage oscillation and voltage spikes of the rectifier tube. In addition, when the current flowing through the saturable inductor does not change rapidly, it exhibits a low impedance and consumes very little power. The detailed design process of main parameters in the converter is presented to provide design reference for power supply workers. To verify the effectiveness of design, a 3 kW(15 V/200 A) prototype converter is built. This low-voltage high-current prototype has around 90% efficiency, and can suppress high-frequency voltage oscillation and voltage spikes, avoiding the short circuit problem of power tube, all of which are verified by experimentation.

1. Introduction

The full-bridge (also named as H-bridge) zero-voltage switching PWM (FB-ZVS PWM) converter [1–7] uses the leakage inductance of the transformer and the parasitic capacitance of the power tube to achieve zero-voltage switching [8–10], which greatly reduces the switching loss and has been widely used in high power DC–DC converters [11–18]. However, in the bridge converter, high-frequency on–off of the power tube causes serious interference signals, which can cause short circuit problems of power tubes in the same bridge arm [19]. When the rectifier tube is in the reverse recovery state, it will generate high-frequency voltage oscillations and voltage spikes, which exacerbate voltage stresses as well as reverse recovery power loss, and cause serious EMI problems [14,20–22].

In order to solve the short circuit problem caused by the high-frequency voltage oscillation and voltage spikes, many methods have been proposed. For example, some have adopted the RC absorption circuit in the converter [23]. When the switch is turned off, the energy accumulated in the parasitic inductor charges the absorption capacitor to suppress the voltage surge. However, parameter design of RC absorption circuit is difficult, and inappropriate parameter design will increase the power loss of the circuit, and it cannot achieve the expected ripple suppression. Some have used the RCD absorption circuit in the converter [9,23]. When the switching voltage rises to the voltage of the absorption capacitor, the absorption diode is turned on, so the switch is embedded by the diode. However, the diode of the RCD absorption circuit has large power loss and RCD absorption circuit is not suitable for the absorption of diode reverse voltage spike, because it may exacerbate the diode reverse recovery current. Some have employed the Zener clamp circuit [24,25], which adds the Zener diode at the primary or secondary side. The voltage

of the Zener diode aggravates the clamped below the maximum voltage when the current rises. However, the rapid conduction of Zener diode will exacerbate EMI problem. Some researchers proposed the chaotic spread spectrum technique [20,26]. It utilizes the wide spectrum characteristics of chaotic signals to distribute the energy to a wider continuous frequency band, so as to achieve EMI suppression. Some scholars put forward that the understanding of the DCM resonance mechanism is the key to fulfilling ZVS and ZCS simultaneously [27]. Some researchers proposed the new modulation strategy without introducing an auxiliary circuit [28]. However, these methods generally are complex and lack of practicability. Some researchers introduce an auxiliary current source network to realize the zero-voltage turn-on of the lagging bridge arm, but it is complex [29]. Some proposed FFM modulation-based soft-switched isolated SRC to reduce the conduction losses by blocking the reverse current [30]. Figure 1 shows the methods used in resolving voltage oscillation and voltage spike problems.

In this paper, a ZVS H-bridge phase-shifted low-voltage high-current converter with saturable inductors (ZVS-HBPS-LVHC-SI) is proposed. Its overall topology is similar to FB-ZVS PWM, but compared with FB-ZVS PWM, the proposed method adds saturable inductors before the rectifier diode at the secondary side and saturable inductors to the drive circuit. In this way, circuit performance can be improved without changing the circuit structure. Saturable inductors are used to inhibit the turn-off voltage spike of the power tubes as well as diodes, and reduce the influence of resonance on the driving waveform, which resolve the short circuit problem of the bridge arm. Finally, a detailed saturable inductor design is provided and a 3 KW (15 V/200 A) ZVS H-bridge phase-shifted low-voltage high-current converter is built to verify the effectiveness of the design.
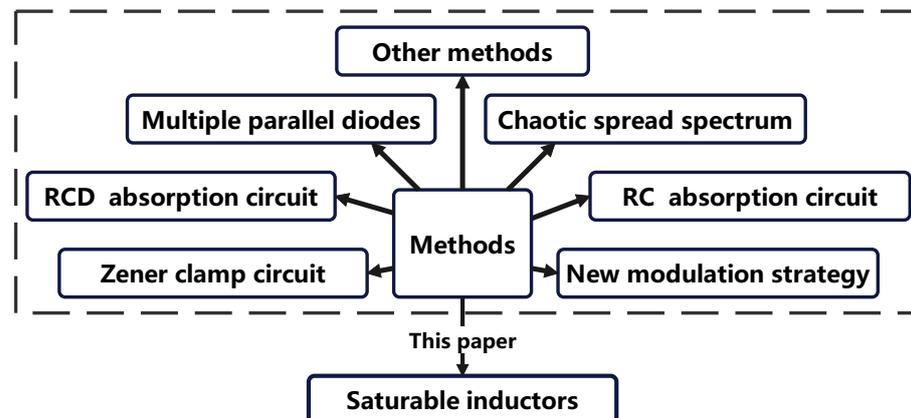
Figure 1. The methods used in resolving voltage oscillation and voltage spikes problems.

2. Voltage Spikes Generation and Suppression

2.1. Voltage Spike Generation Mechanism

Due to the existence of junction capacitance, the rectifier tube must experience a transient process when it switches state among zero bias, forward bias and reverse bias. It takes the rectifier tube a certain amount of time to restore the reverse blocking ability when the reverse voltage is suddenly applied to it. The dynamic reverse recovery characteristics of the rectifier tube are shown in Figure 2, where I_F is the forward conduction current, and t_{rr} is the reverse recovery time of the rectifier tube.

After t_1, the rapid decline in reverse current results in a high value of $\frac{di_R}{d_t}$. Then, due to the influence of inductance, reverse voltage spike U_{RP} is generated. The spike may reach more than three times the voltage at the secondary side.
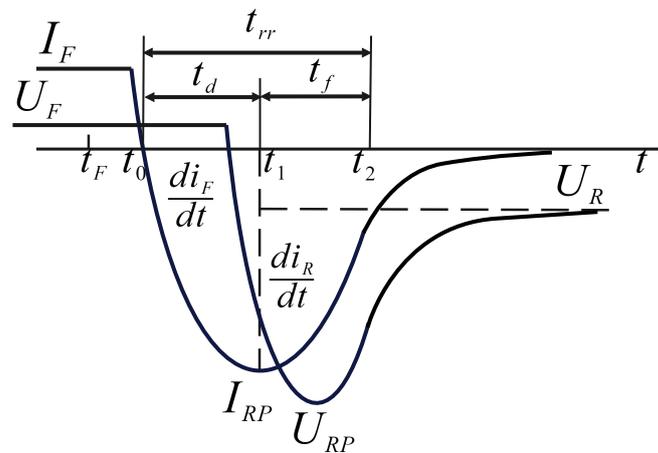
Figure 2. Reverse recovery voltage and current waveform of the rectifier tube.

2.2. Voltage Spike Suppression with Saturable Inductors

In order to better understand the mechanism of voltage spike suppression with saturable inductors, secondary circuit of ZVS-HBPS-LVHC-SI is used to illustrate. Figure 3 shows the secondary circuit of ZVS-HBPS-LVHC-SI, where both L_{s_1} and L_{s_2} are saturable inductors and reach their saturation regions when the reverse current rises. Figure 4 shows working modes of the secondary circuit. When rectifier tube D_{S_1} and D_{S_1} convert from one state to another, they will experience reverse recovery state and then generate high-frequency voltage oscillation and voltage spikes, which lead to voltage stress increase, reverse recovery power loss, and serious EMI problems.
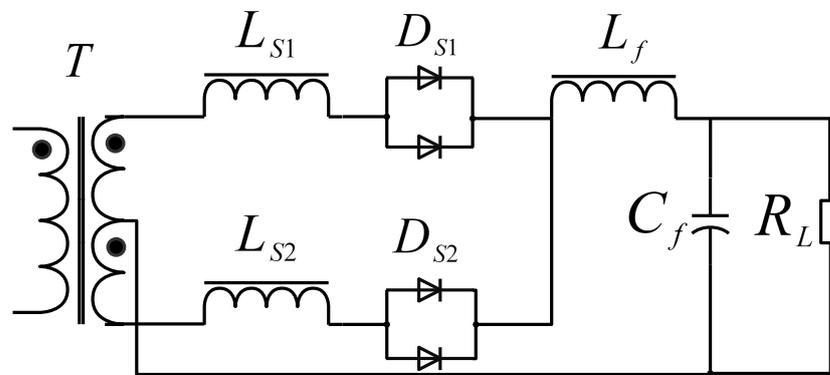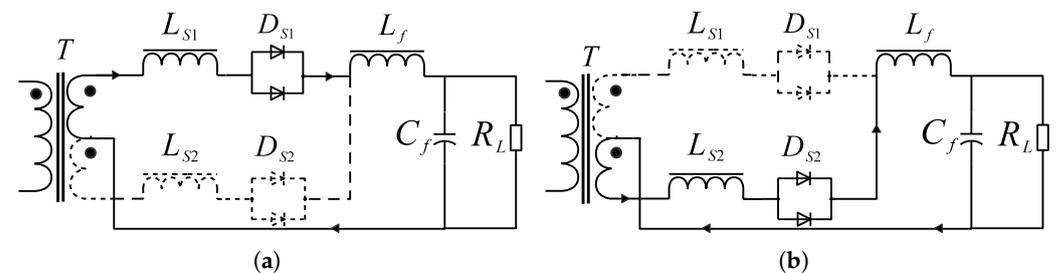

Figure 3. The secondary circuit of ZVS-HBPS-LVHC-SI.

(a)　　　　　　　　　　　　　　　**(b)**

Figure 4. Working modes of the secondary circuit. (**a**) Stage I; (**b**) Stage II.

To resolve this problem, saturable inductors are introduced as shown in Figure 3. Saturable inductors are the inductors with high rectangular hysteresis loop, high initial permeability and obvious magnetic saturation point. When the current is small, saturable inductor is equivalent to open circuit and the inductor is not saturated. When the current is

large, saturable inductor is equivalent to a short circuit and the inductor is saturated. When the external voltage is applied, the initial current inside the inductor increases slowly at first. Only when the current in the inductor reaches a certain value do inductors L_{s_1} and L_{s_2} become saturated immediately.

Figure 5 is the reverse recovery current waveform of the rectifier tube after adding saturable inductors. When current rises rapidly, the inductors become saturated immediately and have high impedance, so the upward trend of reverse current becomes flat and the peak current I_{RP} as well as peak voltage U_{RP} are reduced. In addition, the reverse recovery time of the rectifier tube after adding saturable inductors is approximately πt_{rr}.
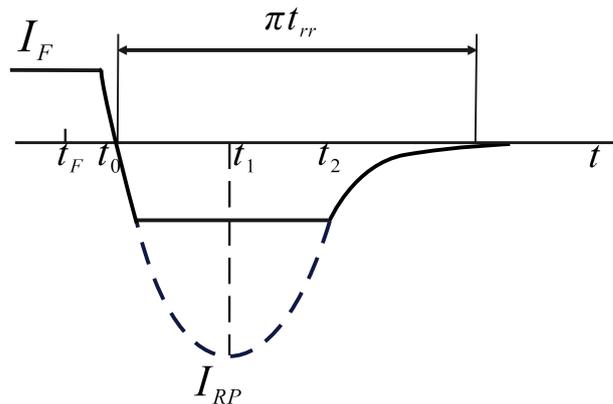
Figure 5. Reverse recovery current waveform of rectifier tube with saturable inductors.

Saturable inductors can inhibit current growth and thus can suppress voltage spike effectively. In addition, saturable inductors have low power loss because they only have high impedance when current changes rapidly, and the impedance is kept low.

3. Parameters Design in the Converter

3.1. Design of the Circuit

The main circuit of ZVS-HBPS-LVHC-SI is shown in Figure 6. Q_1 and Q_3 are the leading-bridge power tubes. Q_2 and Q_4 are the lagging-bridge power tubes. These four power tubes make up the H-bridge inverter circuit. C_b is the DC-blocking capacitor. L_r is the leakage inductance of transformer T. D_5 and D_6 are the clamping diodes of the leading-bridge circuit. D_c, R_c and C_c constitute up the RCD circuits of the lagging-bridge arm. L_{s_1} and L_{s_2} are saturable inductors at the secondary side. D_{s_1} and D_{s_2} are rectifier diodes at the secondary side. D_{s_3} is the freewheeling diode at the secondary side. In Figure 6, inductors in the dotted box are saturable inductors. Compared with the traditional ZVS circuit, ZVS-HBPS-LVHC-SI has a similar structure but adds saturable inductors L_{s1} and L_{s2} to inhibit high-frequency voltage oscillation and voltage spikes. When current rises, the saturable inductors will have high impedance, which slows the rising of current and consequently suppresses voltage.
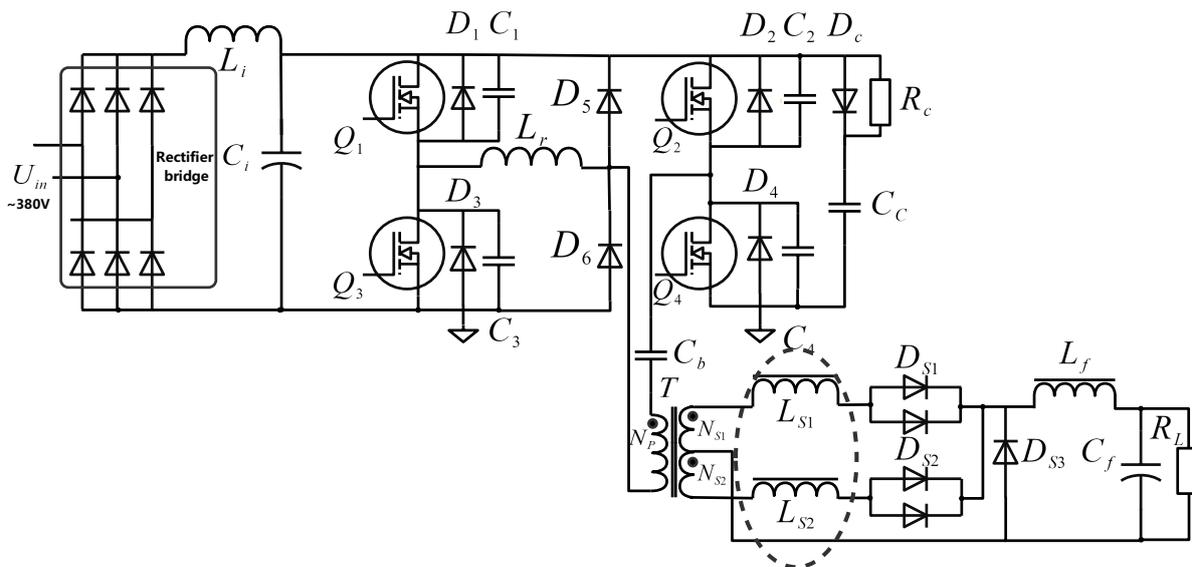
Figure 6. Main circuit structure of ZVS-HBPS-LVHC-SI.

3.2. Design of Drive Circuit

In order to avoid misleading power tubes in the same bridge arm caused by interference signal, this paper designs a drive circuit that can effectively suppress the voltage amplitude of the interference signal, as shown in Figure 7.
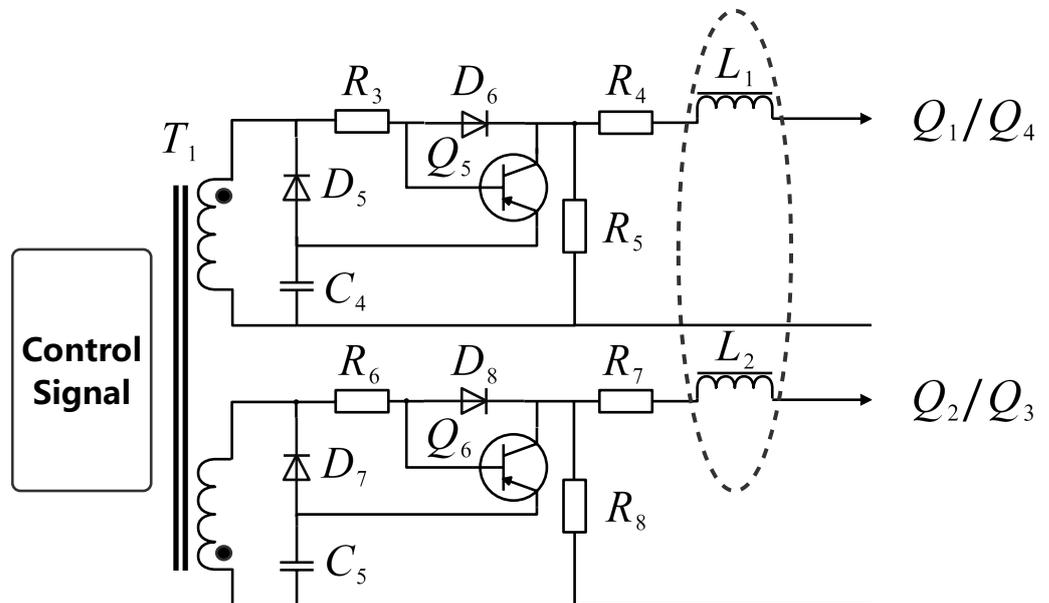

Figure 7. Structure of the drive circuit.

In Figure 7, capacitors C_4 and C_5 are equivalent to voltage sources to achieve rapid turn-off together with the transistor Q_5 and Q_6. L_1 and L_2 are saturable inductors. The drive circuit outputs the PWM signal to $Q1, Q2, Q3, Q4$ when receiving the control signal. Compared with the drive circuit of traditional FB-ZVS PWM, saturable inductors L_1 and L_2 are used before the output drive signal to reduce high-frequency interference signal peak, which causes the short-circuit problem of the power tubes. Its mechanism is the same as diode peak suppression. Both of them make use of the characteristics of the saturable inductor to inhibit current growth.

3.3. Detailed Design of High-Frequency Transformer

The minimum input value of the three-phase AC voltage U_{acmin} is calculated as follows,

$$U_{acmin} = 380(1 - 10\%) = 342 \text{ V} \tag{1}$$

Therefore, the DC bus voltage is about 483V. Calculated with the bus voltage change rate of 10% , the minimum bus output voltage U_{dcmin} is expressed as follows,

$$U_{dcmin} = 483(1 - 10\%) = 435 \text{ V} \tag{2}$$

Ignoring the voltage drop of diodes and setting the largest voltage drop on the DC blocking capacitor as 5% of the bus voltage, the input voltage in the primary side is calculated as

$$U_{Tpri} = U_{dcmin}(1 - 5\%) \tag{3}$$

Insert (2) into (3),

$$U_{Tpri} = 435 \times (1 - 5\%) = 413 \text{ V} \tag{4}$$

To calculate the output voltage U_{Tsec} required for the secondary side of the transformer, the duty cycle loss, the voltage drop of the rectifier diode at the secondary side and the voltage drop of the output filtering inductor should be considered. The ideal output voltage of the power supply U_o is 15 V. The maximum effective duty ratio D_{max} is 0.85. The tube voltage drop U_r is 0.7 V and U_L is 0.3 V. Output voltage U_{Tsec} is calculated as

$$U_{Tsec} = \frac{U_o + U_r + U_L}{D_{max}} = \frac{15 + 0.7 + 0.3}{0.85} = 18.8 \text{ V} \tag{5}$$

From (4) and (5), the transformer ratio K is calculated as follows,

$$K = \frac{U_{Tpri}}{U_{Tsec}} = \frac{413}{18.8} = 22 \tag{6}$$

The switching period T is 10 μs calculated with 100 kHz switching frequency, and the maximum duty ratio Δ_{max} is 45%. Considering the shielding electromagnetic interference and volume of the transformer, PQ40 magnetic core is selected in this paper. According to the TDK magnetic core parameter manual, the effective magnetic flux area A_e is 201 mm^2 and the maximum magnetic flux density B is 3000 Gs. Therefore, the number of turns of the transformer at the primary side is calculated as

$$N_{pri} = \frac{U_{dcmin}T\Delta_{max}}{2BA_e} = \frac{413 \times 10 \times 0.45 \times 10^{-6}}{2 \times 3000 \times 201} \times 10^{10} = 16 \tag{7}$$

Since the transformer ratio k is 22 and the number of turns of the secondary side transformer is minimum 1 turn, the number of turns of the primary side transformer is at least 22 turns. Therefore, the transformer magnetic core can reserve 30% magnetic flux. The decrease of magnetic flux density can greatly reduce the iron loss of the magnetic core and temperature rise of the working transformer.

3.4. Detailed Design of Saturable Inductors

Saturable inductors have large inductance when the rectifier tube is in the reverse recovery state. To eliminate the impact of minority carrier's reverse recovery, its volt-second characteristics must meet the following,

$$2V_s t_s = N\Delta BA_e \tag{8}$$

In (8), V_s is the voltage of the transformer's secondary side. t_s is the recombination time of minority carrier in rectifier tubes' reverse recovery state. n is the number of turns of the depressor. B is the range of magnetic density. A_e is the effective magnetic core area.

According to (8), the number of turns of the saturable inductors N is calculated as follows:

$$N = \frac{2V_s t_s}{\Delta B A_e} \tag{9}$$

After adding the saturable inductors, the reverse recovery time of the rectifier tube is about πt_{rr}, where t_{rr} is the reverse recovery time of the rectifier tube without saturable inductors. The number of turns of the saturable inductors N must satisfy

$$N = \frac{2V_s I_F \pi t_{rr}}{\Delta B A_e}\left(\frac{F_{cu}}{JW}\right) \tag{10}$$

The VITROVAC 6025Z, a cobalt-based amorphous magnetic core, is selected as the magnetic core of the saturable inductor. It has the characteristics of high permeability, low core loss and high rectangular ratio B_s/B_r. Its saturation magnetic induction intensity B_s is 0.8~1.2 T, and its coercivity H_C is less than 1 A/m. Small coercivity, small area of hysteresis loop and low core iron loss make it suitable for converters with large output currents.

4. Efficiency Analysis

As a result of the introduction of saturable inductors and realization of zero voltage switch, reverse conduction losses of diodes P_{DR} and switching on-off losses of power tubes P_{QS} are reduced greatly compared with FB-ZVS PWM without saturable inductors. Therefore, the power loss P_{loss} of the ZVS-HBPS-LVHC-SI mainly comes from the power tube conduction loss P_{QC}, control loss of power tubes P_{QG}, diode conduction loss P_{DC} and transformer loss P_T. These are the power losses that inevitably occur when components work. The power loss P_{loss} can be calculated as follows:

$$P_{loss} = P_{QC} + P_{QG} + P_{DC} + P_T \tag{11}$$

V_{out} is the output voltage of the ZVS-HBPS-LVHC-SI, and the output power P_{out} of the ZVS-HBPS-LVHC-SI can be calculated as follows:

$$P_{out} = \frac{V_{out}^2}{R_L} \tag{12}$$

Table 1 is the main power loss of the ZVS-HBPS-LVHC-SI [31].

Table 1. The power loss of the ZVS-HBPS-LVHC-SI.

Losses Type	Equation	Conditions
P_{QC}	$\sum_{i=1}^{4} I_{Qi_{rms}}^2 R_{Qi}$	$I_{Qi_{rms}}$: the average current through Q_i R_{Qi}: the DC resistance of Q_i
P_{QG}	$4Q_g V_g f$	Q_g: switch gate charge D_i or D_s V_g: voltage needed to charge the gate f: switching frequency
P_{DC}	$\sum_{i=1}^{6} I_{D_{i_{rms}}}^2 R_{Di} + 5 I_{D_{S_{rms}}}^2 R_{Ds}$	$I_{Di_{rms}}$ or $I_{Ds_{rms}}$: the average current through D_i or D_s R_{Di} or R_{Ds}: the DC resistance of D_i or D_s
P_T	$\frac{\pi}{4}K f^\alpha B^\beta + I_{T_{rms}}^2 R_T$	α, β, K: Constants related to magnetic materials $I_{T_{rms}}$: the average current through the transformer R_T: the DC resistance of the transformer

The efficiency η of the ZVS-HBPS-LVHC-SI can be calculated as follows:

$$\eta = \frac{P_{out}}{P_{loss} + P_{out}} \times 100\% \tag{13}$$

5. Experimental Verification

In order to verify the performance of the improved circuit, a 3 kW(15 V/200 A) ZVS-HBPS-LVHC-SI is designed. The prototype parameters are shown in Table 2. In addition, an application field of the ZVS-HBPS-LVHC-SI is electroplating power supply, which is always high-power-consuming and with low efficiency. The power design and component parameter design of the prototype are carried out according to the electroplating power supply standard, which can prove that the introduction of saturable inductance reduces the power consumption and improves the efficiency.

Table 2. The prototype parameters.

Device	Parameter
Three-phase AC input voltage U_{in}	$380(\pm 10\%)U_{\text{ac}}$
Control chip	UCC2895
Power cube	SPP17N80C3 (800 V, 17 A, 0.29 ω)
Output rectifier tube	MBRP400100CT
Main transformer ferrite core	PQ40/40Z (TDK)

The prototype and experimental environment are shown in Figure 8.

Figure 8. The prototype and experimental environment.

Figure 9 presents the efficiency curve of the converter. As the power increases, at half load, the efficiency of the power supply reaches 91%. When the current is 200 A, due to the increase of conduction loss, the efficiency of circuit declines, but it is still approximately 90%.
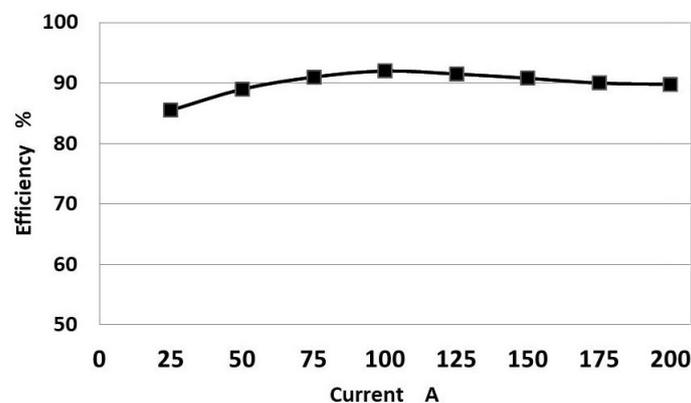

Figure 9. Efficiency curve.

Figure 10a shows the driving voltage waveform without saturable inductors. Figure 10b shows the driving voltage waveform with saturable inductors. Figure 11a shows the voltage waveform of the rectifier tube without adding saturable inductors when V_{in} = 200 VAC. Figure 11b shows the voltage waveform of the rectifier tube after adding saturable inductors. In Figure 10a, the high-frequency on–off switch brings serious EMI problems to the drive signal. In Figure 11a, the peak value is more than twice the normal value. After adding saturable inductors, as shown in Figures 10b and 11b, interference and voltage spikes are effectively suppressed.


| (a) | (b) |
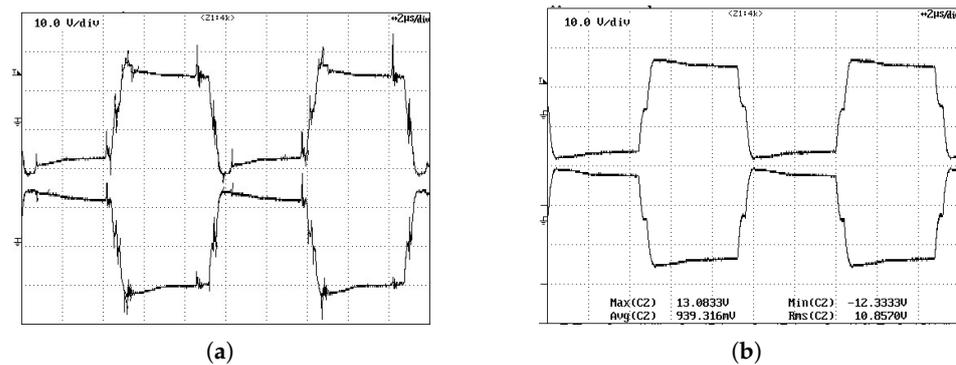
Figure 10. Voltage waveforms of the drive signal. (**a**) Without saturable inductors; (**b**) With saturable inductors.

| (a) | (b) |
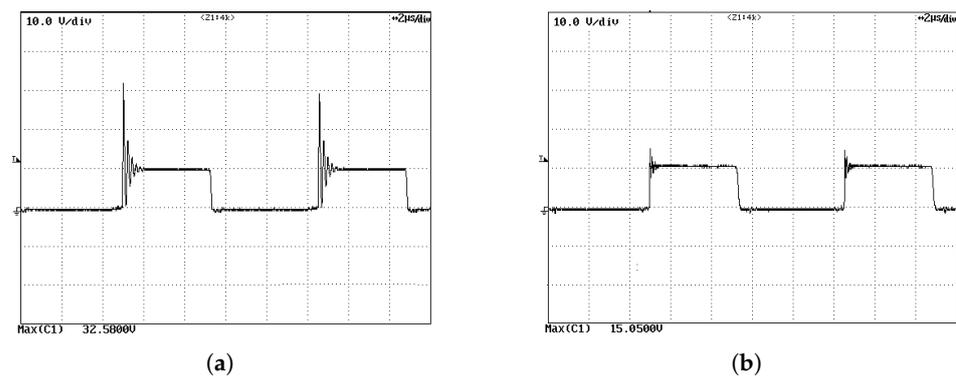
Figure 11. Voltage waveforms of the rectifier tube. (**a**) Without saturable inductors; (**b**) With saturable inductors.

Figure 12 shows voltage and current waveforms of the switch after adding saturable inductors. Figure 12a shows switch waveforms when circuit is at full load, and Figure 12b shows switch waveforms when circuit is at 75% load.

| (a) | (b) |
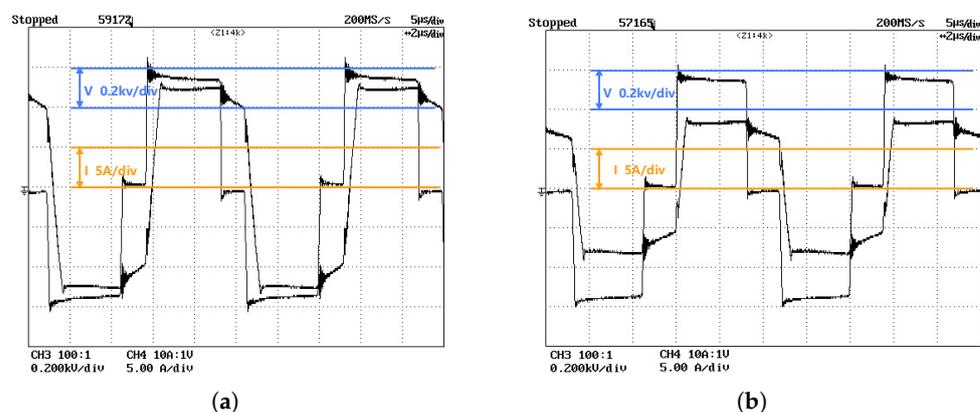
Figure 12. Voltage and current waveforms of the switch after adding saturable inductors. (**a**) Waveforms at full load; (**b**) Waveforms at 75% load.

6. Conclusions

The high-frequency on-off of the power tube causes high-frequency voltage oscillations, voltage spikes and serious EMI problems, which are the main reasons for short circuit problem of the bridge arm and the spike of the secondary rectifier tube.

In this paper, a ZVS H-bridge phase-shifted low-voltage high-current converter with saturable inductors (ZVS-HBPS-LVHC-SI) is designed. It can effectively inhibit the high-frequency oscillations, improves the electromagnetic compatibility of the converter, and resolves the short circuit problem of the bridge arm by inhibiting interference of the main circuit to the drive circuit.

The circuit analysis and the calculation of the main parameters of the power supply are detailed. To verify the feasibility, a 3 KW (15 V/200 A) low-voltage high-current power supply prototype is designed. This low-voltage high-current prototype has high efficiency around 90%. After adding saturable inductors, high-frequency voltage oscillation and voltage spikes are suppressed well and short circuit problem of power tube can be avoided, which are verified well by experimental waveforms. Compared with other methods, the ZVS-HBPS-LVHC-SI only uses saturable inductors to achieve voltage suppression with simple parameter design. In addition, the introduction of saturable inductors helps to improve the efficiency of the circuit because it reduces the power loss of diodes and power tubes. The proposed design can provide practical references for large power switching power supply workers.

Data Availability Statement: Not applicable.

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