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High Frequency Resonance Suppression Strategy of Three-Phase Four-Wire Split Capacitor Inverter Connected to Parallel Compensation Grid

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Abstract: With the continuous penetration and development of renewable energy power generation, the distributed grid and the microgrid are becoming increasingly important in modern power systems. In distribution networks and the microgrid, the grid impedance is comparatively large and cannot be ignored. Usually, the parallel compensation is used to improve the grid quality. In the grid with parallel compensation, the large phase angle difference between the impedance of the grid-connected inverter and the impedance of the grid at amplitude intersection will result in high frequency resonance (HFR). Because the inverter shows filter characteristics due to limited bandwidth of the controller, the parallel compensation grid, respectively, performs as the capacitance characteristic and inductance characteristic in different high frequency range. Compared with the three-phase, three-wire system, an additional zero-sequence path exists in the three-phase four-wire split capacitor inverter (TFSCI) system, so that the existing high frequency resonance suppression methods will be not effective. Since the zero-sequence component is neglected, HFR will also occur, in addition to the positive-sequence component and the negative-sequence component. Therefore, in order to suppress the high frequency resonance caused by positive-sequence, negative-sequence and zero-sequence components, an impedance reshaping strategy based on current feedback is proposed in this paper. This proposed method can reshape the amplitude and phase of the inverter impedance in a high frequency range without affecting the performance of the fundamental frequency control and ensure that the inverter contains a sufficient phase margin. Additionally, the proposed method can reshape the impedance of TFSCI within a wide frequency range, which makes it able to cope with the challenge of the parallel compensation degree change. Theoretical analysis and experiments verify the availability of the proposed control strategy.

Keywords: three-phase four-wire split capacitor grid-connected inverter; impedance reshaping; high frequency resonance

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1. Introduction

With the continuous penetration and development of renewable energy power generation, distribution networks and micro-grids account for an increasing proportion of contemporary power grids [1–3]. In the distribution network and microgrid, the three-phase four-wire system has been widely promoted and applied [4–11], because it has a zero-sequence current path and is suitable for both symmetrical and asymmetrical conditions. In the three-phase four-wire system, the three-phase four-wire inverter is an important part that plays important functions such as power transmission and power quality improvement devices. Among them, the three-phase four-wire split capacitor inverter has been widely used due to its low cost and simple control, whose application scenarios include as an active filter [5], power redistribution device [6], renewable energy power

generation system [7] and power distribution system [9]. At the same time, because the distribution network and microgrid are usually weak grids with large impedance, parallel compensation capacitors are typically equipped to perform reactive power compensation and harmonic filtering to improve voltage quality and enlarge power transmission capacity [12–14]. Therefore, it is a very common scenario for a three-phase four-wire system that a capacitor split inverter connects to a weak grid with parallel compensation capacitors.

The impedance-based analysis is proved an attractive method to analyze and resolve the small-signal instability problems caused by the interaction between the converter and the grid [15–19]. Reference [15] presents a stability criterion for grid-connected converters based on impedance models and Gershgorin's theorem, which consider the effect of the non-diagonal elements. Ref. [16] establishes the entire impedance of RSC and VSC considering coupling factors to analyze the system stability. In [17], a single-in-single-out impedance model of grid-connected converters with virtual synchronous generator using a cascaded inner control loop has been established to analyze the system stability under different kinds of weak grid.

Due to the fact that grid impedance cannot be neglected, when TFSCI connects, small-signal instability may be caused by the interactions between the inverter systems and the weak grid. According to the stability theory of impedance proposed in reference [16], when the phase angle difference of impedance between grid-connected devices and the weak grid impedance amplitude intersection closes to 180°, it may cause system resonance. Especially in the parallel compensation grid, the large phase angle difference will result in the high frequency resonance (HFR). In high frequency, the inverter system shows filter characteristics because of the limited control bandwidth of the controller. Moreover, in a different high frequency zone, the parallel compensation grid, respectively, performed as the capacitance characteristic and inductance characteristic. The HFR existed in the power system will not only disintegrate the PCC voltage, but also deteriorate output power and work conditions of other grid-connected devices [20–26]. Hence, it is necessary to consider the HFR suppression when TFSCI is connected to parallel compensation grid.

In order to suppress HFR, the virtual RC impedance was introduced in [20,21] to deal with resonances of specific frequency. By introducing positive resistance to improve the performance of harmonic resonance damping. neegative inductance to achieve better performance of harmonic distortion mitigation due to reducing the grid-side inductance. This kind method could achieve well HFR suppression performance by choosing reasonable parameters, but it can only achieve well performance for some specific frequencies. Ref. [22] presented a series-LC-filtered active damper to suppress HFR inac power-electronics-based power systems by applying the fourth-order resonant controller. This strategy could achieve well HFR suppression performance in wider frequency range by using cascaded adaptive notch filter (ANF) [23] to identify the unknown resonance frequency. However, the performance of the active damping control based on the resonant controller will be weakened due to the limited dynamic performance of the resonant frequency identified process when the parallel compensation degree varies. Ref. [24] proposed a control strategy for the converter to suppress HFR based on voltage feedback, which can reshape the phase of the converter impedance without a resonant frequency identified process. However, it may increase the harmonic currents caused by the background harmonic voltages of the grid because it significantly reduces the impedance magnitude of the inverter at high frequency region.

It can be found that the HFR issue of the grid-connected converter have been widely concerned, while it should be noted that these damping strategies mentioned above are only suitable for three-phase three-wire system. When it comes to three-phase four-wire systems, these methods are not completely applicable, because the zero-sequence component will also cause high-frequency resonance in addition to the positive-sequence component and the negative-sequence component [26]. Ref. [26] established the impedance models of positive-sequence, negative-sequence and zero-sequence, which reveals that the positive-sequence, negative-sequence and zero-sequence components all may bring small signal

instability problems. However, the strategy to solve these stability problems has not been proposed. Due to the decoupled relationship between zero-sequence components and positive-sequence, negative-sequence components, the resonance problems caused by the zero-sequence components cannot be solved by the existing HFR suppression strategies which are applied to the positive-sequence and negative-sequence components.

Hence, in order to suppress the HFR problem for the TFSCI, the paper reshapes the zero-sequence impedance positive-sequence impedance, and negative-sequence impedance of the TFSCI. The proposed method can suppress the HFR caused by the zero-sequence component, positive-sequence component and negative-sequence component of TFSCI. In addition, the proposed control strategy reshapes the impedance in a wide frequency band, which enables it to cope with the HFR frequency deviations challenge caused by the parallel compensation degree variations.

The rest of this paper is organized as follows. System description and simplified impedance modeling of the TFSCI is given in Section 2 as a foundation of the following analysis. Then, the proposed control strategy is studied in Section 3. The controller parameter analysis of the proposed control strategy is studied in Section 4. The effectiveness of the proposed control strategy is verified by experiments in Section 5. Section 6 concludes this paper.

2. System Description and Simplified Impedance Modelling of TFSCI

2.1. System Description

The block diagram of the TFSCI connected to the parallel compensation grid is shown in Figure 1. In Figure 1, L_f, L_n represent the filter inductors, R_f, R_{fn} represent the corresponding parasitic resistances. C_1 and C_2 are the DC side capacitors, where $C_1 = C_2 = C_{dc}$. C_g and R_{Cg}, respectively, represent the capacitance and parasitic resistance of the parallel compensation capacitor. L_g and R_{Lg} respectively, represents the inductance and parasitic resistance of transmission line.

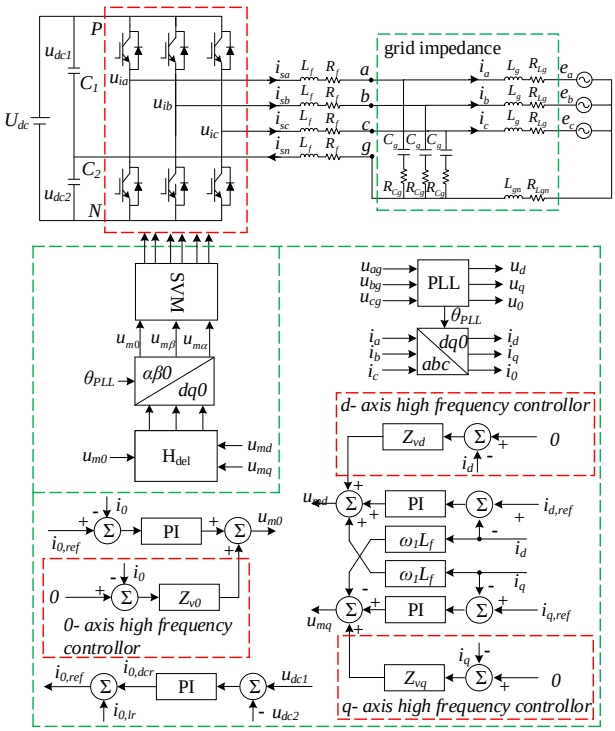


Figure 1. Block diagram of three-phase four-wire split capacitor inverter.

The impedance of the grid can be achieved as follow [10–12],

$$\begin{cases} Y_{gp} = Y_{gn} = 1/Z_{gp} = 1/Z_{gn} = \frac{R_{Cg}\left(sL_g+R_{Lg}\right)+sC_gR_{Cg}+1}{\left(sL_g+R_{Lg}\right)\left(sC_gR_{Cg}+1\right)} \\ Y_{g0} = 1/Z_{g0} = \frac{sC_g\left(s\left(L_g+3L_{gn}\right)+R_{Lg}+3R_{Lgn}\right)+1+sC_gR_{Cg}}{\left(1+sC_gR_{Cg}\right)\left(s\left(L_g+3L_{gn}\right)+R_{Lg}+3R_{Lgn}\right)} \end{cases} \quad (1)$$

Figure 2 shows the equivalent impedance of TFSCI and the grid. It is assumed that TFSCI can be considered as a current source $I_{s,pn}$ which is paralleled with the output impedance $Z_{inv,pn0}$, while the grid can be considered as an ideal voltage source $V_{g,pn0}$ series with grid impedance $Z_{g,pn0}$. where, Z_{g0}, Z_{gp}, Z_{gn} represents zero-sequence impedance, positive-sequence impedance and negative-sequence impedance of grid, respectively.

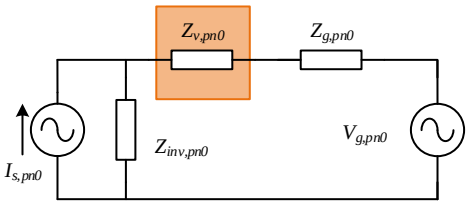


Figure 2. Equivalent impedance of TFSCI system and grid.

Figure 3 shows the voltage, currents, active power and negative power of TFSCI connected to parallel compensation grid when the HFR occurs. The parameters can be seen in Table A1 in Appendix C. Figure 4 shows the FFT of i_a. From Figures 3 and 4, there are two resonance points at 365 Hz and 930 Hz in the system. From Figure 3 it can be found that the resonance at 431 Hz is caused by the zero-sequence components and the resonance at 930 Hz is caused by the positive-sequence and negative-sequence components. Therefore, in order to suppress these resonances, it is necessary to analyze how these resonances occurs.

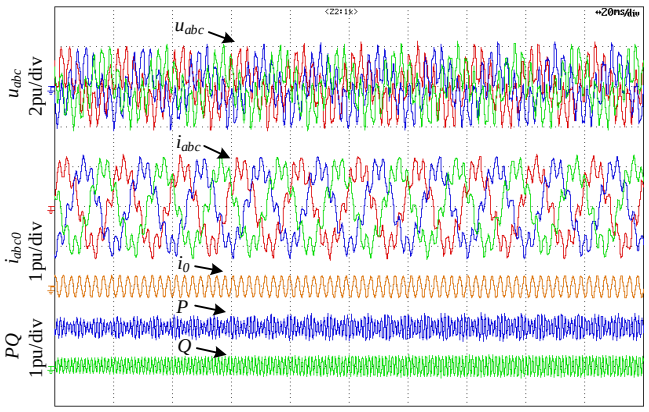


Figure 3. Voltage and currents of TFSCI when HFR occurs.

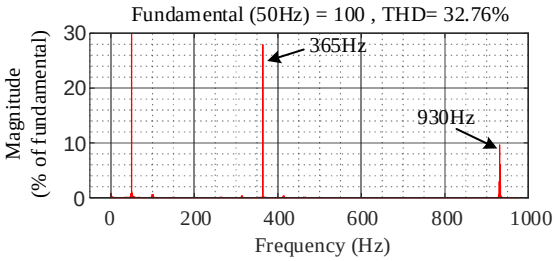


Figure 4. FFT result of i_a when HFR occurs.

2.2. Simplified Impedance Modelling of TFSCI

In order to analyze how these HFR occurs clearly, some simplifications need to be done. Since the bandwidth of the PLL is usually within a few tens of hertz, the influence of the phase-locked loop on the impedance characteristics of the inverter can be ignored when studying the problem of high-frequency resonance [24].

After the simplification, the block diagram of the TFSCI impedance model can be shown in Figure 5. The detailed derivation process of Figure 5 can be seen in Appendix A.

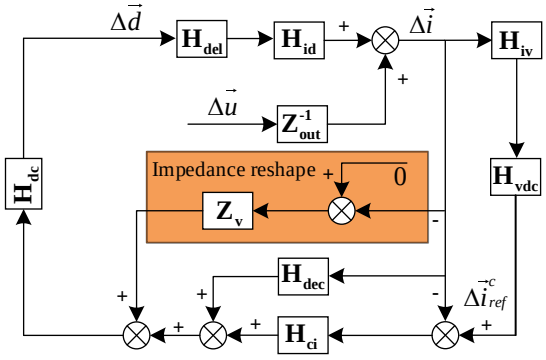


Figure 5. The block diagram of the TFSCI impedance model.

In Figure 5, $\mathbf{H_{dec}}$ denotes the decoupling term matrix caused by the *d*-*q* decoupling control. $\mathbf{H_{ci}}$ denotes the current controller matrix. $\mathbf{H_{del}}$ denotes a delay transfer matrix caused by the control delay. $\mathbf{H_{iv}}$ denotes the relationship between current Δi to Δu_{dc2}. $\mathbf{H}_{\mathrm{vdc}}$ is the dc voltage balance PI controller to balance the up and down capacitor voltages.

$$\mathbf{H_{dec}} = \begin{bmatrix} 0 & -\omega_1 L_f & 0 \\ \omega_1 L_f & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{2}$$

$$\mathbf{H_{dc}} = \begin{bmatrix} 1/U_{dc} & 0 & 0 \\ 0 & 1/U_{dc} & 0 \\ 0 & 0 & 1/U_{dc} \end{bmatrix} \tag{3}$$

$$\mathbf{H_{del}} = \begin{bmatrix} \mathrm{e}^{-T_{del}s} & 0 & 0 \\ 0 & \mathrm{e}^{-T_{del}s} & 0 \\ 0 & 0 & \mathrm{e}^{-T_{del}s} \end{bmatrix} \tag{4}$$

$$\mathbf{H_{ci}} = \begin{bmatrix} k_{dip} + \frac{k_{dii}}{s} & 0 & 0 \\ 0 & k_{qip} + \frac{k_{qii}}{s} & 0 \\ 0 & 0 & k_{0ip} + \frac{k_{0ii}}{s} \end{bmatrix} \tag{5}$$

$$\mathbf{H_{iv}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{3}{2sC_{dc}} \end{bmatrix} \tag{6}$$

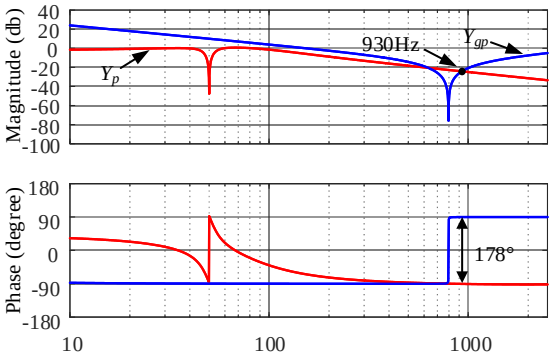
$$\mathbf{H_{vdc}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & k_{dc0ip} + \frac{k_{dc0ii}}{s} \end{bmatrix} \tag{7}$$

According to Figure 5, the admittance from $\Delta\vec{i}$ to $\Delta\vec{u}$ can be expressed as Equation (8). The detailed derivation process of Equation (8) can be seen in Appendix B.

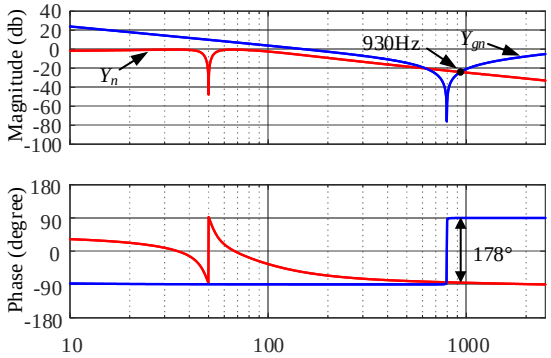
$$\begin{cases} Y_p = \dfrac{1}{K_m \times \left(\frac{1}{2} \times \left(k_{dip} + k_{dii}/(s - j\omega_1) + k_{qip} + k_{qii}/(s - j\omega_1)\right) - j\omega_1 L_f k_{dq}\right) + sL_f + R_f} \\ Y_n = \dfrac{1}{K_m \times \left(\frac{1}{2} \times \left(k_{dip} + k_{dii}/(s - j\omega_1) + k_{qip} + k_{qii}/(s - j\omega_1)\right) + j\omega_1 L_f\right) + sL_f + R_f} \\ Y_z = \dfrac{1}{K_m \times (k_{0ip} + k_{0ii}/s + \frac{3}{2sC_{dc}}(k_{0vp} + k_{0vi}/s)) + s(3L_n + L_f) + 3R_n + R_f} \end{cases} \tag{8}$$

where, $K_m = e^{-T_{del}s}$ is the system delay. k_{0ip}, k_{0ii}, k_{qip}, k_{0ii}, k_{0ip}, k_{0i} represent respectively the proportional parameter and integral parameter of the d-axis, q-axis and 0-axis current PI controller, k_{0vp}, k_{0vi} represent the proportional parameter and integral parameter of DC voltage balance PI controller.

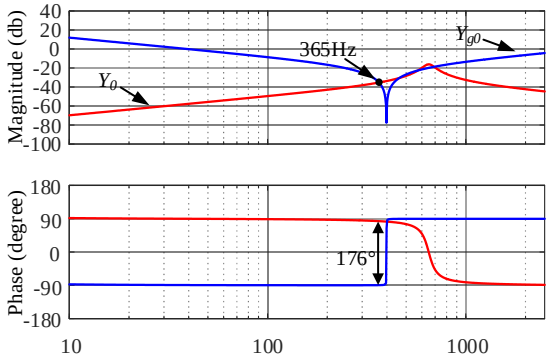
The Bode diagram of the inverter admittance after the simplification is shown in Figure 6. In Figure 6, Y_p, Y_n, and Y_0 represents the admittance of the inverter after simplification, Y_{gp}, Y_{gn} and Y_{g0} are the admittance of the grid.



(**a**) positive-sequence admittance Y_p.



(**b**) negative-sequence admittance Y_n.



(**c**) zero-sequence admittance Y_0.

Figure 6. Admittance model of TFSCI after simplification.

Based on the impedance stability theory, system stability is determined by $Z_{inv,pn0}/(Z_{inv,pn0} + Z_{g,pn0})$ [14]. When there is a lack of enough phase margin between $Z_{inv,pn0}$ and $Z_{g,pn0}$ at the amplitude intersection point, the resonance will occur. According to Figure 6, the positive-sequence impedance and negative-sequence impedance of the inverter are inductive at high frequency, the phase difference between the impedance of TFSCI and the impedance of grid is 178° close to 180° atamplitude intersection point 930 Hz. The zero-sequence impedance characteristic of the inverter the zero-sequence impedance characteristic gradually transitions from capacitive to inductive and the phase difference between the impedance of TFSCI and the impedance of grid is 176° close to 180° atamplitude intersection point 356 Hz. Figure 6 also reveals that the system has a risk of resonance at 356 Hz and 930 Hz. Combination of Figures 3–5 and the above theoretical analysis, the following conclusions can be obtained,

(1) The reason of HFR in the TFSCI system is that the phase difference between the zero-sequence impedance, positive-sequence impedance and negative-sequence impedance of TFSCI and grid are close to 180°.
(2) The simplified model obtained in this section can accurately reflect the high-frequency impedance of TFSCI and can be applied to the analysis and resolution of the high-frequency resonance.

Therefore, in order to suppress these resonances, it is necessary to reshapes the zero-sequence impedance, positive-sequence impedance and negative-sequence impedance of the TFSCI.

(1) The reason of HFR in the TFSCI system is that the phase difference between the positive-sequence, negative-sequence, zero-sequence impedance of TFSCI system and grid is close to 180°.
(2) The simplified model obtained in the previous section can accurately reflect the high-frequency impedance of TFSCI and can be used for the analysis and resolution of high-frequency problems.

Therefore, in order to suppress these resonances, it is necessary to reshapes the positive-sequence, negative-sequence and zero-sequence impedance of the TFSCI.

3. Control Strategy Based on Impedance Reshaping

Based on the analysis in Section 2, the key to maintain system stability is to ensure sufficient phase margin between the impedance of TFSCI and the impedance of grid. In other words, the phase of TFSCI system should be closed to 0°. Hence, an impedance reshaping strategy for TFSCI is proposed in this paper. In the proposed impedance reshaping strategy, a second-order high-pass filter and a negative second order differential block are introduced to reshape the zero-sequence impedances, positive-sequence impedances and negative-sequence impedances of TFSCI.

A high pass filter will be selected to ensure well performance of fundamental frequency control. The high pass filter is used to ensure a sufficiently large amplitude difference of TFSCI impedance between HFR frequency and fundamental frequency. It is vitally important to prevent fundamental frequency control from being influenced by the influence which is caused by the proposed HFR suppression controller. Considering the proposed control strategy is developed under the dq0 frame and the second-order filter is widely used in the industrial control, the second-order high-pass filter is selected.

In addition to the high-pass filter, a virtual impedance is needed to change the impedance of TFSCI. In order to reshape the phase of TFSCI impedance close to 0°, a virtual impedance H_v with resistive characteristic is needed. Figure 6 shows that the amplitude of TFSCI system impedance increases as the frequency increases, so it's hard for a constant resistance to adapt the increasing impedance amplitude of the TFSCI. Based on this demand, a negative second-orders differential control (H_v) is used in this paper to adjust

both the amplitude and phase of TFSCI impedance by means of its phase-frequency resistance characteristic. Therefore, the high-frequency controller can be expressed as follow,

$$\begin{aligned} Z_v &= G_{filter} * H_v \\ &= s^2/\left(s^2 + 2\zeta\omega_{cut}s + \omega_{cut}^2\right) * \left(-ks^2\right) \end{aligned} \tag{9}$$

where G_{filter} is the second order high-pass filter, cut-off frequency f_{cut} = 100 Hz. H_v= $-ks^2$, in which H_v can be regarded as a resister whose resistance increases as the frequency increasing, k is the controller gain. Here $\omega_{cut} = 2\pi f_{cut}$.

From the control block shown in Figure 1, the output reference voltage of the inverter consists of PI controller output, decoupled controller output and high frequency control output. So, the output reference voltage of the inverter can be shown in Equation (10). It should be noted that the purpose of the high frequency controller is to suppress the high frequency harmonic component in the system, so the reference currents $i_{d,HF}^*$, $i_{q,HF}^*$ and $i_{0,HF}^*$ of the high frequency controller are set to zero. In Equation (10), G_{id}, G_{iq} and G_{i0} represents d-axis, q-axis and 0-axis PI controller respectively. And Z_{vd}, Z_{vq} and Z_{v0} represents d-axis, q-axis and 0-axis high frequency controller respectively.

$$\begin{cases} u_{md} = G_{id} * \left(i_d^* - i_d\right) + Z_{vd} * \left(i_{d,HF}^* - i_d\right) - j\omega_1 L_f i_q + u_d \\ u_{mq} = G_{iq} * \left(i_q^* - i_q\right) + Z_{vq} * \left(i_{q,HF}^* - i_q\right) + j\omega_1 L_f i_d + u_q \\ u_{m0} = G_{i0} * \left(i_0^* - i_0\right) + Z_{v0} * \left(i_{0,HF}^* - i_0\right) + u_0 \end{cases} \tag{10}$$

According to Figure 6, the impedance after reshaping can be expressed as,

$$\begin{cases} Y_p = \frac{1}{K_m * \left(\frac{1}{2} * \left(k_{dip} + k_{dii}/(s - j\omega_1) + k_{qip} + k_{qii}/(s - j\omega_1)\right) - j\omega_1 L_f k_{dq} + G_{\text{filter}} H_v\right) + sL_f + R_f} \\ Y_n = \frac{1}{K_m * \left(\frac{1}{2} * \left(k_{dip} + k_{dii}/(s - j\omega_1) + k_{qip} + k_{qii}/(s - j\omega_1)\right) + j\omega_1 L_f + G_{\text{filter}} H_v\right) + sL_f + R_f} \\ Y_z = \frac{1}{K_m * \left(k_{0ip} + k_{0ii}/s + \frac{3}{2sC_{dc}}\left(k_{0vp} + k_{0vi}/s\right) + G_{\text{filter}} H_v\right) + s * (3L_n + L_f) + 3R_n + R_f} \end{cases} \tag{11}$$

It should be noted that not only three-phase four-wire inverters, but also three-phase three-wire photovoltaic inverters, wind turbines or energy storage inverters may also have the risk of high frequency resonance. Because the grid-connected devices show filter characteristic due to limited control bandwidth of the controller in high frequency range, and the parallel compensation grid respectively performs as the capacitance characteristic and inductance characteristic in different high frequency range, which will bring large phase angle difference between the impedance of the grid-connected devices and the impedance of the grid at amplitude intersection and results the high frequency resonance (HFR). The impedance reshaping method proposed in this paper can also be applied to these devices, because the essence of this method is equivalent to connecting a virtual resistor in series with the impedance of the high-frequency band of the grid-connected inverter by adding an extra current feedback branch into the control structure. Therefore, the damping of the grid-connected equipment is increased, the phase margin of the grid-connected system is improved, and the high-frequency resonance can be suppressed.

4. Analyses of Parameters Variation

In order to analyze the performance of the proposed method with different parameters, the performance of the proposed method under deviations of parameters is given in this section.

4.1. Choosing of High Frequency Controller Gain

In order to analyze the proposed control strategy and achieve well control performance, the analysis on high frequency controller k for the proposed control strategy is of vital importance, since k is decisive to high frequency suppression effect.

Figure 7 shows the Bode diagram of H_v with different controller gains. From Figure 7, it can be seen that increasing of the k can magnify the amplitude of H_v at high frequency; however, the magnitude at low frequency is also increased. At 50 Hz, GD is -43 dB and 17.7 dB when k = 1 and 100, which indicates that the overlarge k will affect the control performance at the fundamental frequency. Figure 8 shows the bode diagram of TFSCI's reshaped impedance with different values of k, which validates the above analyses that overlarge k will affect the fundamental frequency control performance. The TFSCI system parameters used in the analyses are shown in Table A1 in Appendix C.

From Figure 7, when k = 5, the magnitude of H_v at 50 Hz is -23 dB, which means the high frequency controller can hardly affect the fundamental frequency control performance. From Figure 8, when $k_d = k_q = k_0 = 5$, the high frequency controller shows well reshaping effect on the impedance of the inverter, which ensures at least 30°phase margin in the system. So, choose $k_d = k_q = k_0 = 5$ as the high frequency controller gain of d-axis, q-axis and 0-axis.

4.2. Filter Parameters Deviations

In the actual operation of the inverter, due to the deviation between the actual inductance value and the nominal inductance value, it is necessary to analyze the influence of the variation of the filter inductance value on the impedance reshaping effect. The following figure shows the impedance reshaping effect with ±30% deviation of the filter inductor L_f. It can be seen from Figure 9 that the inductance deviation basically hardly affects the impedance reshaping effect.

4.3. Parallel Compensation Degree Variations

In the actual grid operation, the parallel compensation degree of the grid will change with the actual demand. The following figure shows the suppression effect of the proposed impedance reshaping method on HFR when the parallel compensation of the power grid changes. It can be seen from Figure 10 that even if the degree of parallel compensation changes, the proposed impedance reshaping method can still ensure sufficient phase margin for the inverter impedance to effectively suppress HFR.

4.4. Dc Side Capacitance Variations

In the actual operation of the inverter, due to the deviation between the actual capacitance value and the nominal capacitance value, it is necessary to analyze the influence of the variation of the DC side capacitance value on the impedance reshaping effect. The following figure shows the impedance reshaping effect with ±30% deviation of the DC side capacitance C_{dc}. It can be seen from Figure 11 that the capacitance deviation basically hardly affects the impedance reshaping effect.

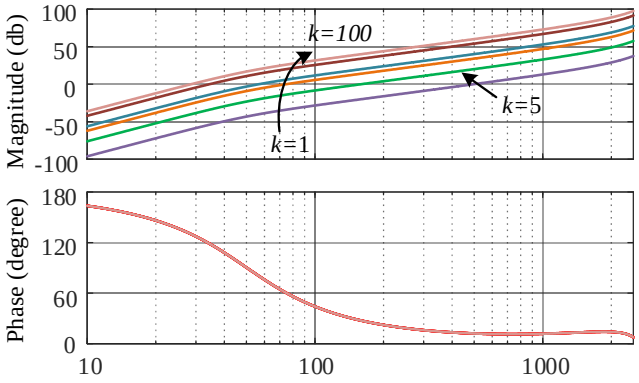
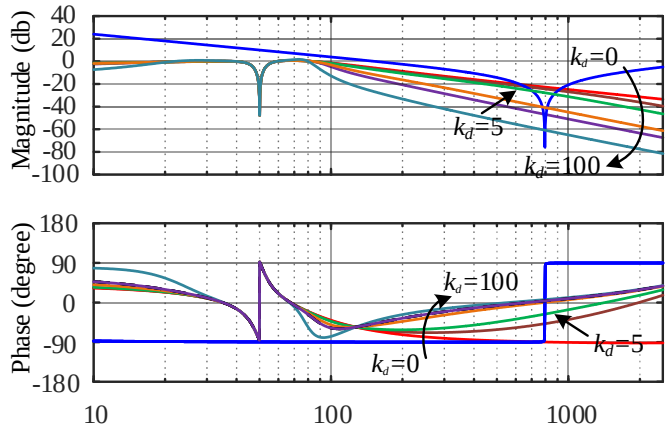
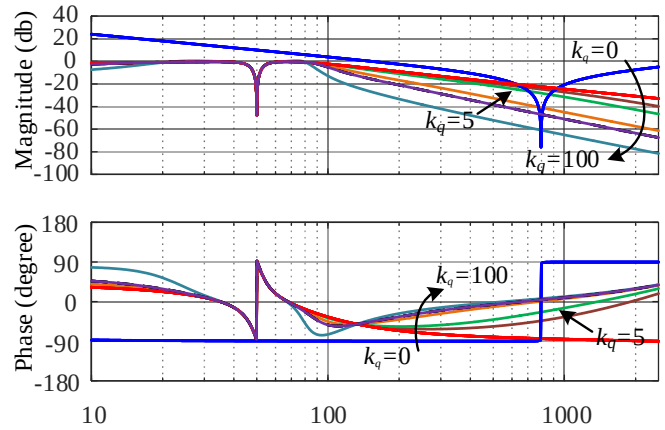


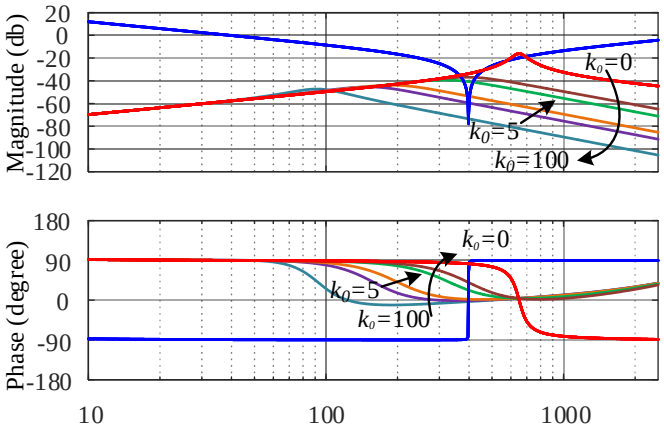
Figure 7. Bode diagram of H_v with different controller gain k.



(**a**) positive-sequence admittance Y_{p_re}.

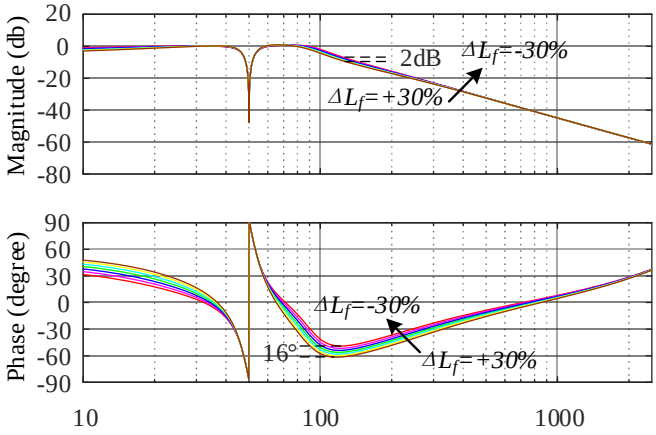


(**b**) negative-sequence admittance Y_{n_re}.

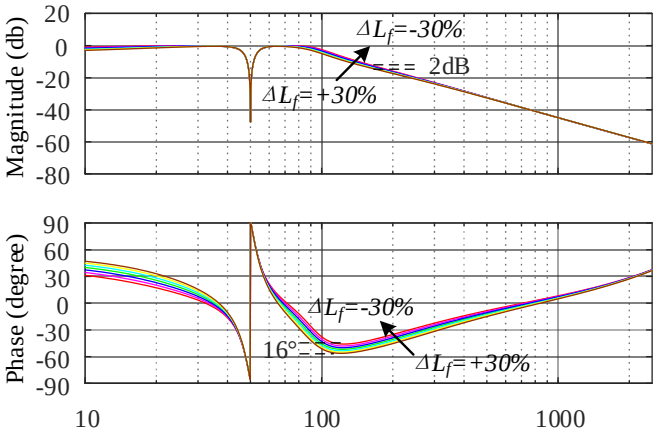


(**c**) zero-sequence admittance Y_{0_re}.

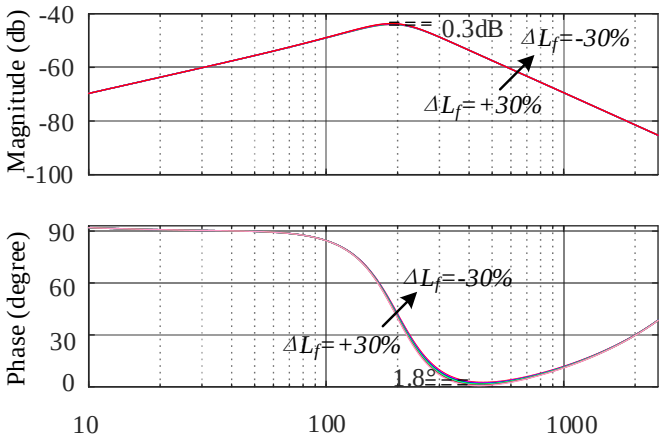
Figure 8. Bode diagram of Y_{p_re}, Y_{n_re} and Y_{0_re} with different controller gain k_d, k_q and k_0.



(**a**) positive-sequence admittance Y_{p_re}.

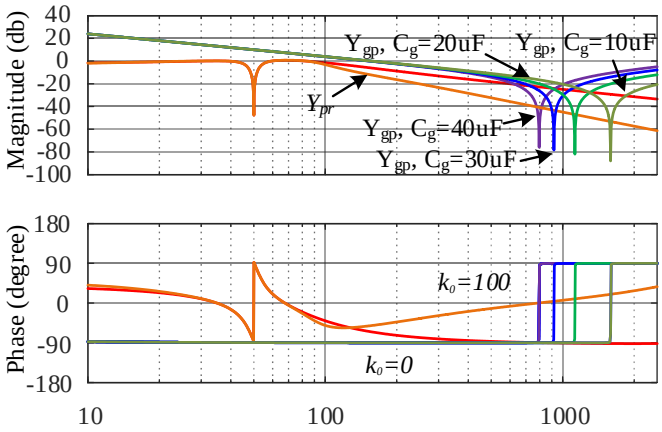


(**b**) negative-sequence admittance Y_{n_re}.

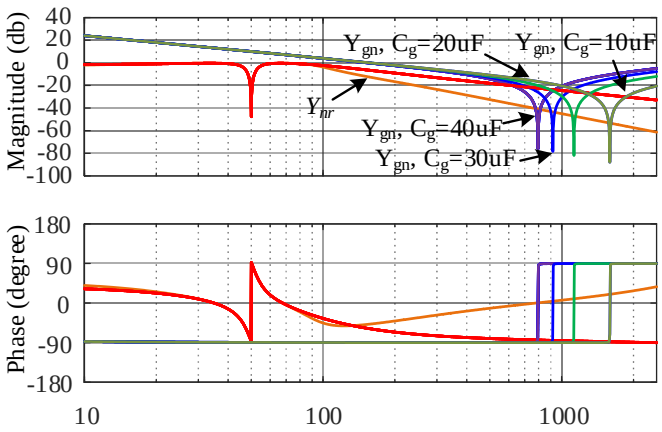


(**c**) zero-sequence admittance Y_{0_re}.

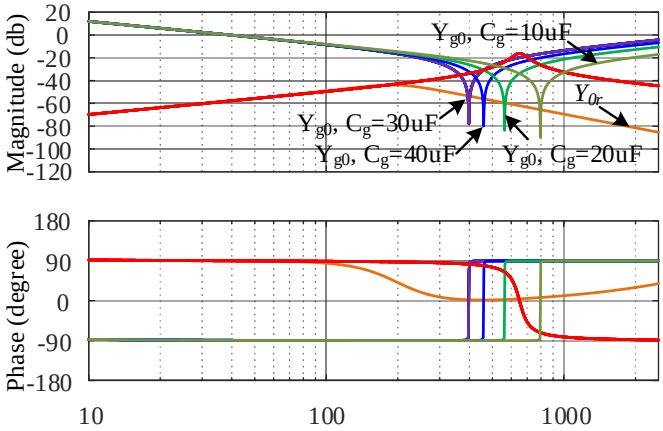
Figure 9. Verification of adaptability for deviation of filter parameter L_f.



(**a**) positive-sequence admittance Y_{p_re}.

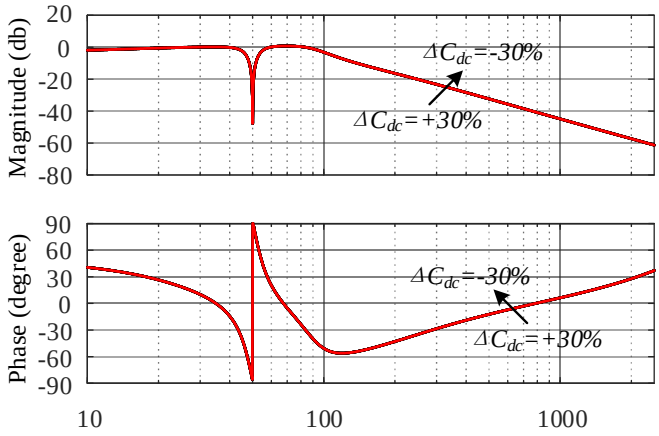


(**b**) negative-sequence admittance Y_{n_re}.

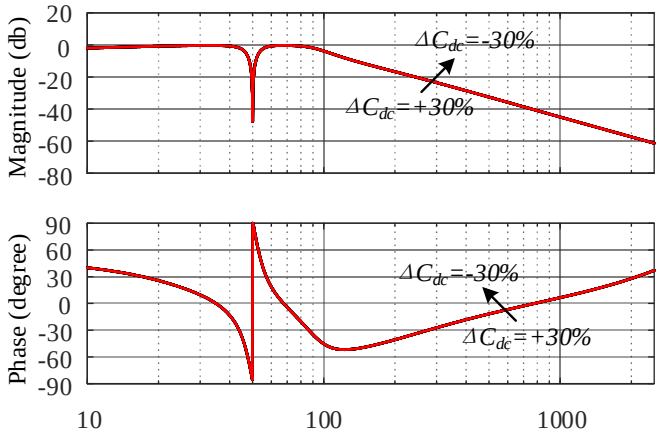


(**c**) zero-sequence admittance Y_{0_re}.

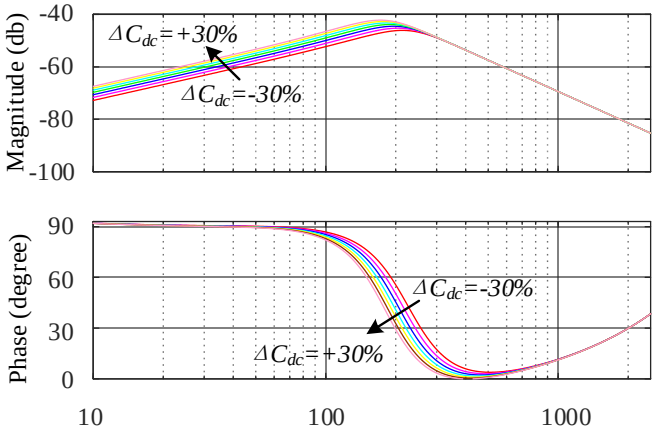
Figure 10. Verification of adaptability for variations of parallel compensation degree.



(**a**) positive-sequence admittance Y_{p_re}.



(**b**) negative-sequence admittance Y_{n_re}.



(**c**) zero-sequence admittance Y_{0_re}.

Figure 11. Verification of adaptability for variations of dc side capacitance.

4.5. Discussion of Non-Linearities System

It should be noted that the above analyses are based on the grid impedance presented in Figure 1. It is worth discussing whether the proposed control method is still effective if there are non-linearities devices connected to the system.

The high frequency resonance studied in this paper is caused by the small signal instability when the three-phase four-wire split capacitor inverter is connected to the parallel compensation grid. The high frequency resonance suppression method proposed in this paper is also realized based on impedance reshaping under small signal. So, the whole system can be linearized is a basis of this paper.

In fact, when the system reaches stable working state, the devices can be linearized, whether it is a power electronic device, a motor or other device with nonlinear characteristics based on the stable working state. Under this premise, regardless of whether there are nonlinear devices in the grid, the grid impedance and device impedance can be aggregated into an equivalent impedance by linearizing. Then, the Bode diagram of equivalent impedance is similar to that of grid impedance shown in Figure 6 in the paper. The high-frequency resonance suppression method proposed in this paper is to change the impedance characteristics of the inverter in the high-frequency band from pure capacitive or pure inductive to pure resistive, which increases the damping of the system. So even if there are nonlinear devices in the system, it will not affect the effectiveness of the proposed method. In addition, the grid impedance model used in this paper is an extreme case, which has both purely capacitive and purely inductive characteristics in different frequency bands of grid impedance. Therefore, the proposed control method is still effective in non-linearities system

5. Experimental Verification

To better verify the achieved conclusions, the hardware platform based on Control-hardware-in-loop (CHIL) is established, which can be seen in Figure 12. The model of three-phase four-wire split capacitor Grid-connected inverter system is established in Typhoon 602+ with the time step of 1 µs. The controllers of the three-phase four-wire split capacitor inverter are carried out in a TMS320F28335/Spartan6 XC6SLX16 DSP+FPGA control board. And the CHIL has been used to analyze and verify the conclusion presented in [27,28]. The parameters of the system are listed in Table A1 in section Appendix C.

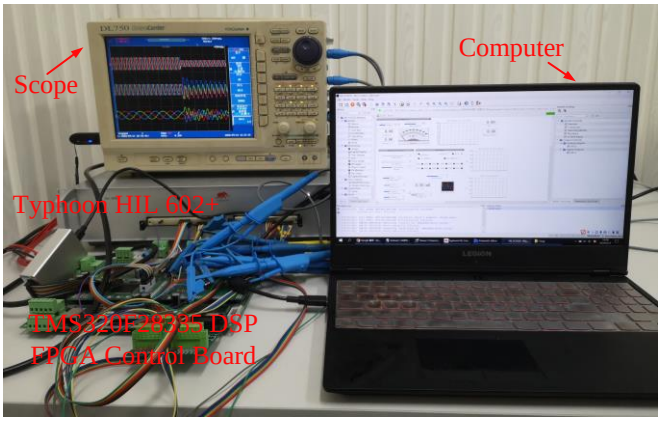
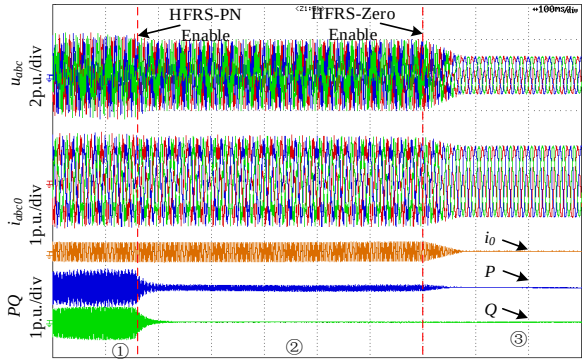
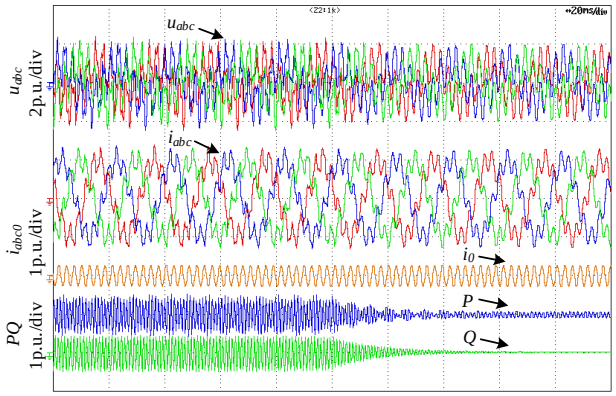


Figure 12. Hardware platform of CHIL experiment. Reproduced from [26] IEEE Access 2021.

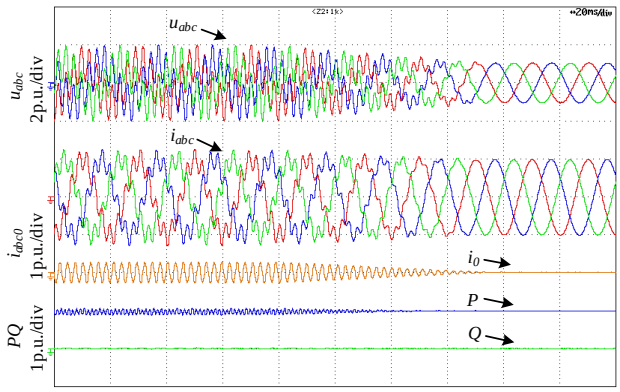
Figure 13 shows the Steady-state performance verification of HFR suppression control strategy. There are three stages in Figure 13a. State ① shows the voltages, currents, active power and reactive power of the TFSCI when HFR occurs. It can be seen that there are high frequency harmonics in the inverter's voltages, currents, active power and reactive power. State ② shows waveforms when only HFR suppression of positive-sequence and negative-sequence is enabled. It can be seen that the resonance caused by the positive-sequence and negative-sequence components is well suppressed after enabling the HFR suppression of positive-sequence and negative-sequence. However, there are still high-frequency resonance caused by zero-sequence component in the system. State ③ shows the waveforms after further enabling HFR suppression of zero-sequence, which shows that the resonance caused by the zero-sequence component has been well suppressed.



(**a**) Steady-state performance verification of HFR suppression control strategy.



(**b**) The enlarged part when the HFR suppression of positive-sequence and negative-sequence enabled.



(**c**) The enlarged part when the HFR suppression of zero-sequence enabled.

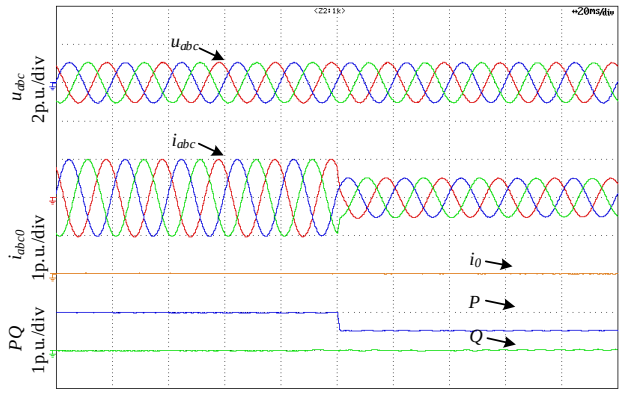
Figure 13. Steady-state performance verification of HFR suppression control strategy.

Figure 13b shows the enlarged part when the HFR suppression of positive-sequence and negative-sequence enabled. Figure 13c shows the enlarged part when the HFR suppression of zero-sequence enabled. From Figure 13b,c, it can be seen that the HFR can be suppressed within 50 ms after the proposed HFR suppression strategy enabled, which demonstrates that the proposed HFR strategy is provided with well dynamic performance.

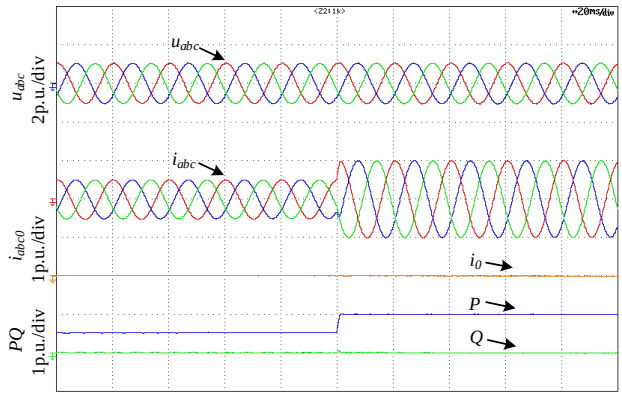
Figure 14 shows the effect of HFR control strategy on the dynamic performance of fundamental frequency control. Figure 14a shows the voltages, currents of and powers of the TFSCI when the active power step form 1 p.u. to 0.5 p.u., Figure 14b shows the voltages, currents of and powers of the TFSCI when the active power step form 0.5 p.u. to 1 p.u. It can be seen from Figure 14 that the proposed control strategy hardly has negative effect on the dynamic performance of fundamental frequency.

Figure 15 shows the adaptability verification of the proposed control strategy to the variation of the power grid short-circuit ratio. Figure 15 shows the voltage, current, and

power waveforms of the inverter when the short-circuit ratio of the grid changes from 4.6 to 9.2 and the short-circuit ratio changes from 9.2 to 2. When the short-circuit ratio changes, the inverter can still remain stable and well HFR suppression performance, indicating that the proposed high-frequency oscillation control strategy has strong adaptability to the changes in the grid impedance.



(**a**) Active power step form 1 p.u. to 0.5 p.u.



(**b**) Active power step form 0.5 p.u. to 1 p.u.

Figure 14. Effect of HFR control strategy on the performance of fundamental frequency control.

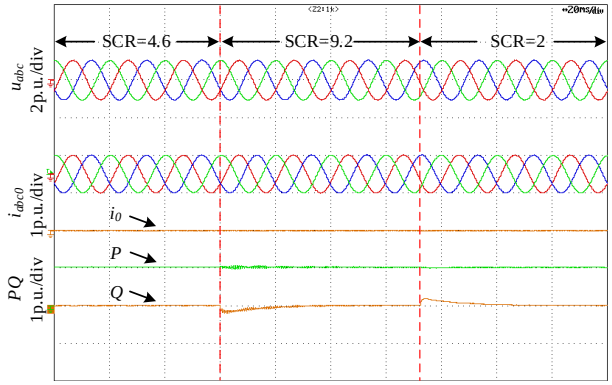


Figure 15. Adaptability verification to the change of the power grid short-circuit ratio.

6. Conclusions

This paper studies the HFR issue when the TFSCI connects to parallel compensation grid. The conclusions achieved by this paper can be shown as following.

(1) From the perspective of impedance, the essence which causes the HFR is the insufficient phase margin at the intersection of positive-sequence, negative-sequence, and

zero-sequence impedance amplitude between TFSCI and grid based on a simplifying impedance of the TFSCI, when the TFSCI connects to the grid.

(2) In order to suppress the HFR, an impedance reshaping method has been proposed in this paper. This method can reshape the amplitude and phase of the TFSCI impedance in high frequency band without affecting the performance of fundamental frequency control and ensure that the system has sufficient phase margin.

(3) The impedance reshaping method can reshape the impedance of TFSCI within wide frequency range which makes it able to cope with the challenge of the parallel compensation degree change.

Author Contributions: Conceptualization, G.F.; Methodology, Z.Y.; Project administration, Y.X. and H.N.; Resources, H.N.; Software, L.H.; Validation, Z.W.; Writing—original draft, G.F. All authors have read and agreed to the published version of the manuscript.

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Appendix A

Figure A1 shows the small-signal circuit model of inverter in *dq*0-domain.

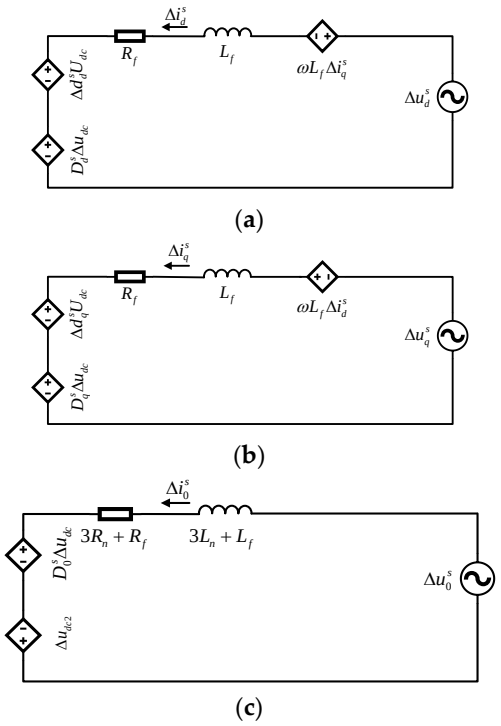

Figure A1. Small-signal circuit model of inverter in *dq*0-domain. (**a**) *d*-axis small-signal circuit; (**b**) *q*-axis small-signal circuit; (**c**) 0-axis small-signal circuit. Reproduced from [26] IEEE Access 2021.

From Figure A1, assuming $\Delta d_d^s = \Delta d_q^s = 0$ the transfer function matrix from perturbation voltage to current response in the system frame can be expressed as,

$$\mathbf{Z_{out}} = \begin{bmatrix} sL_f + R_f & \omega L_f & 0 \\ -\omega L_f & sL_f + R_f & 0 \\ 0 & 0 & s(L_f + 3L_n) + R_f + 3R_n - \frac{3}{2sC} \end{bmatrix} \tag{A1}$$

Similarly, in Figure A1, assuming $\Delta u_d^s = \Delta u_q^s = 0$ the transfer function matrix from duty ratio to the corresponding current response in the system frame can be expressed as,

$$\mathbf{H_{id}} = \begin{bmatrix} \frac{-(sL_f+R_f)U_{dc}}{(sL_f+R_f)^2+(\omega L_f)^2} & b = \frac{\omega L_f U_{dc}}{(sL_f+R_f)^2+(\omega L_f)^2} & 0 \\ -\frac{\omega L_f U_{dc}}{(sL_f+R_f)^2+(\omega L_f)^2} & \frac{-(sL_f+R_f)U_{dc}}{(sL_f+R_f)^2+(\omega L_f)^2} & 0 \\ 0 & 0 & \frac{-U_{dc}}{s(3L_n+L_f)+3R_n+R_f-\frac{3}{2sC}} \end{bmatrix} \tag{A2}$$

Additionally, through Kirchhoff's current law, the zero-sequence current can be written as,

$$i_0 = \frac{C_f}{3}\frac{d(u_{c2} - u_{c1})}{d_t} \tag{A3}$$

Then, matric $\mathbf{H_{iv}}$ can be achieved as follow,

$$\mathbf{H_{iv}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{3}{2sC_{dc}} \end{bmatrix} \tag{A4}$$

Matrix $\mathbf{H_{vdc}}$ represents the dc voltage balance PI controller to balance the up and down capacitor voltages, which can be expressed as follow,

$$\mathbf{H_{vdc}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & k_{dc0ip} + \frac{k_{dc0ii}}{s} \end{bmatrix} \tag{A5}$$

Then, ignoring the influence of the SRF-PLL and considering time delay $\mathbf{H_{del}}$, current controller H_{ci} and the *d*-*q* decoupling control $\mathbf{H_{dec}}$, the impedance model block diagram of the three-phase four-wire split capacitor inverter can be obtained as shown in Figure 6.

$$\mathbf{H_{del}} = \begin{bmatrix} e^{-T_{del}s} & 0 & 0 \\ 0 & e^{-T_{del}s} & 0 \\ 0 & 0 & e^{-T_{del}s} \end{bmatrix} \tag{A6}$$

$$\mathbf{H_{dec}} = \begin{bmatrix} 0 & -\omega_1 L_f & 0 \\ \omega_1 L_f & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{A7}$$

$$\mathbf{H_{ci}} = \begin{bmatrix} k_{dip} + \frac{k_{dii}}{s} & 0 & 0 \\ 0 & k_{qip} + \frac{k_{qii}}{s} & 0 \\ 0 & 0 & k_{0ip} + \frac{k_{0ii}}{s} \end{bmatrix} \tag{A8}$$

Appendix B

According to Figure 6, when the proposed HFR suppression strategy is not enabled which means the branch containing $\mathbf{Z_v}$ is opened. So, the admittance from Δi to Δu can be obtained as,

$$\mathbf{Y_{idq0}}=\frac{\mathbf{Z_{out}^{-1}}}{\mathbf{I}-\mathbf{H_{id}H_{del}}*\mathbf{H_{dc}}(\mathbf{H_{dec}}-\mathbf{H_{ci}})-\mathbf{H_{dc}H_{ci}H_{iv}H_{vdc}H_{id}H_{del}} \quad \text{(A9)}$$

By reference [29], the admittance in the *d*-*q*-0 domain can be equivalently transformed into the admittance in sequence domain as,

$$\mathbf{Y_{ipn0}}=\mathbf{T}_Z\mathbf{Y_{dq0}}\mathbf{T}_Z^{-1}=\begin{bmatrix}\mathbf{Y_{ipn}} & 0\\ 0 & \mathbf{Y_{i0}}\end{bmatrix}=\begin{bmatrix}Y_{11} & Y_{12} & 0\\ Y_{21} & Y_{22} & 0\\ 0 & 0 & Y_{33}\end{bmatrix} \quad \text{(A10)}$$

where,

$$\mathbf{T_Z}=\frac{1}{\sqrt{2}}\begin{bmatrix}1 & j & 0\\ 1 & -j & 0\\ 0 & 0 & \sqrt{2}\end{bmatrix} \quad \text{(A11)}$$

Taking the responding matrixes to above equation, then Equation (8) can be can be achieved.

Appendix C

Table A1. Three-phase Four-wire Split Capacitor Grid-connected Inverter Parameters.

Symbol	Parameter	Value
U_s	Rated voltage	380 V
P_n	Rated power	30 kW
f_1	Fundamental frequency	50 Hz
f_s	Switching frequency	5 kHz
L_f	Filter inductance	3 mH
R_{Lf}	parasitic resistance of filter inductance	0.02 Ω
L_g	Grid inductance	1 mH
R_{Lga}	parasitic resistance of Grid inductance	0.02 Ω
k_{pp}	Proportional gain of PLL controller	0.16
k_{pi}	Integral gain of PLL controller	0.25
k_{dip}	Proportional gain of *d*-axis current controller	1
k_{dii}	Integral gain of *d*-axis current controller	18
k_{qip}	Proportional gain of *q*-axis current controller	1
k_{qii}	Integral gain of *q*-axis current controller	18
k_{0ip}	Proportional gain of *zero*-axis current controller	3
k_{0ii}	Integral gain of *zero*-axis current controller	54
k_{dcp}	proportional parameter of DC voltage balance PI controller	2.1
k_{dci}	integral parameter of DC voltage balance PI controller	4.2

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