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Compact Thirteen-Level Inverter for PV Applications

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Abstract: In renewable energy source applications, multilevel inverters with lower power components have become more popular in recent decades. This work exhibits a novel topology for high-quality output in PV applications, along with low-power switches and isolated dc sources. The core module of the suggested design may create a 13-level output waveform with two unequal voltage source values. The cascaded structure is intended to boost the voltage levels, and the related parameters are obtained analytically. The even and odd levels of voltage can be created natively without the usage of an additional H bridge circuit. Furthermore, the switches, gate driver circuits, dc sources, and standing voltage are fewer in number when compared to other recent topologies. Power losses and cost comparisons are calculated and given in monetary terms. This new research supports the idea that nearest level control (NLC) is used as a modulation scheme in the simulation modeling and experimental validation of the proposed topology.

Keywords: multilevel inverter; module; standing voltage; cascaded structure; reduced power switches

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1. Introduction

The power demand is rapidly increasing worldwide; renewable energy sources are inevitable due to their huge availability, environmental sustainability, low greenhouse emissions, and less maintenance expense [1–3]. Multilevel inverters (MLIs) have become an emerging alternative power conditioning device in photovoltaic (PV) generation, adjustable speed drives, active power filters, uninterruptible power supplies (UPS), electric vehicle, medium-voltage industrial applications, etc. The quality output waveform, fewer harmonic contents, low voltage stress on the switches, better electromagnetic interferences, and high efficiency are some of the elegant features of MLIs compared to the two-level inverters [4,5]. The famous multilevel inverters, named NPC, FC, and CHB, have been commercially established and extensively used in medium-voltage power conversion applications for the last few decades. These MLIs need many active switches, clamping diodes, flying capacitors, and other devices to synthesize an increased output voltage level, which makes the overall system complex and expensive [6,7]. Nevertheless, the CHB topology is highly recommended for PV applications due to its modular structure, compact design, and isolated dc source configuration. On the other hand, the cascaded MLIs may be expanded to provide a wider variety of voltage levels while using fewer basic units and can be designed in symmetric or asymmetric architecture depending on the magnitude of dc sources used in each unit. The magnitude of dc sources is the same in symmetric topology and different in asymmetric topology. However, the voltage level not only increases the required number of power devices but also the voltage stress. Therefore, researchers have developed new versions of cascaded MLI for higher voltage levels through the use of reduced power components such as switches, gate drivers, and isolated dc sources. A new MLI topology is proposed with basic units connected in series, in which each unit consists of dc sources and two switches. In order to increase the number of voltage

levels, a cascaded structure is developed, and the dc source values are determined in the geometric progression method with a power of two or three [8,9]. However, the trinary source configuration creates more voltage levels, and the additional cascaded units increase the power components and installation space. To assess the suitable number of cascaded units, an optimal scheme is introduced in two different approaches such as maximizing the voltage level with constant power components and minimizing the voltage stress for higher voltage levels [10]. The topologies [11–13] have presented a cascaded topology with several sub multilevel inverters. Even though it uses a lower number of switches, gate driver circuits, and dc sources, the sub multilevel inverter can generate a unidirectional multistep output waveform. In order to obtain the polarity change of the sub multilevel inverter output, a back end H-bridge circuit is connected, and its switches are capable of withstanding the sum of dc source value available in each unit [14]. Another attempt is made with the development of switched-capacitor topology, in which the combination of dc sources and capacitors is used in different voltage ratios to reduce the required dc sources. However, the topology produces a higher voltage level using the lowest number of isolated dc sources, and an additional control circuit is required for balancing the charge of the capacitors, which might complicate the circuit operation with high boost ratio capacitors [15]. In order to generate a higher voltage level without using the additional capacitor or isolated dc sources, the asymmetric topology is presented in [16,17]. These topologies require bidirectional switches and back-end H-bridge circuits to produce possible voltage levels in the output, which increases the high-voltage rating switches and other power components. Another new MLI is introduced as a modular-based structure to reduce the voltage stress of the switches because the topology generates positive and negative voltage levels without requiring an additional H-bridge circuit. However, it increases the voltage level along with the high-voltage stress on the switches, the component counts, and the bidirectional switches [18–21]. In [22], diode-based MLI is presented with reverse connected basic units in either side of packed H-bridge circuit, in which each basic unit consists of a single voltage source and diode. However, a switched diode topology is introduced with a packed U cell structure, in which each cell uses two dc-link capacitors and a diode that equally divides the isolated dc source voltage [23]. Although the switched diode topologies produce higher voltage levels, the required number of power diodes, switches, dc-link capacitors, and gate driver circuits is increased. In [24], two different structures are presented with ten switches and four asymmetric voltage sources to obtain all possible voltage levels, another topology is presented with ten switches and four symmetric voltage sources for higher voltage-level generation [25].

However, the presented cascaded topologies generate a higher number of voltage levels, and the required power components and input dc sources may increase the limitation of multilevel inverters in PV applications. Therefore, this study provides a novel MLI structure with some advantages:

1. Eight IGBTs are used for desired voltage-level generation.
2. Two input dc sources can produce 13-level voltage.
3. The maximum voltage stress of the switches is 6 $V_{DC.}$
4. Inherent polarity changer for ac voltage-level generation.
5. Two dc link capacitors are naturally balanced for input PV sources.
6. Low-switching-frequency modulation (NLC) is employed.

2. Proposed Module Configuration

The cascaded topology with an isolated dc source is a suitable design for PV application in the multilevel inverter family. In symmetric topology, some series-connected PV panels are required, but an asymmetric topology can produce a higher number of voltage levels with a fewer number of PV panels. The polarity changer unit is added at the end stage of cascaded inverters, whose switches produce more high-voltage stress than other switches. The proposed module (PM) is presented for PV application with a reduced num-

ber of PV panels; however, the PM can produce a bipolar voltage level without including a polarity changer unit as it reduces the voltage stress of the switches.

2.1. Asymmetric Configuration

Figure 1 shows the proposed module with a PV-fed configuration. This module consists of two PV sources (V_{p1}, V_{p2}) and eight switches, in which six switches (S_1, S_3, S_4, S'_1, S'_3, S'_4) have single IGBT with freewheeling diode and two switches (S_2, S'_2) have single IGBT but it does not include freewheeling diodes. However, the PM does not require any bidirectional switches. The magnitude of the two dc sources is different, and the V_{p2} is four times greater than the V_{p1} to operate the proposed topology as an asymmetric multilevel inverter. In other words, the PV sources are chosen as (1:4) ratio, in order to produce the desired output voltage level, and the proposed switching pattern is presented in Table 1. It is important to note that the pair switches (S_2, S'_2) should not conduct simultaneously to avoid the short circuit of the PV panels; similarly, the pair switches (S_1, S'_1), (S_3, S'_3), and (S_4, S'_4) conduct in a complementary manner. The conduction state of the switch is represented as '1'; the blocking state is represented as '0'; and the $V_{o,\,Max}$ is output voltage, which is obtained at each level. The dc-link capacitors (C_1, C'_1) are connected in series, and switches (S_2, S'_2) divide the voltage of PV source (V_{p1}) with an equal magnitude as V'_{c1} and $V_{c1} = V_{dc}$. Another terminal of these switches is connected to the positive and negative terminal of the PV source (V_{p2}). These switches can control the charging and discharging of the capacitor voltage with a proper switching combination, which can be achieved by using the natural balancing method.

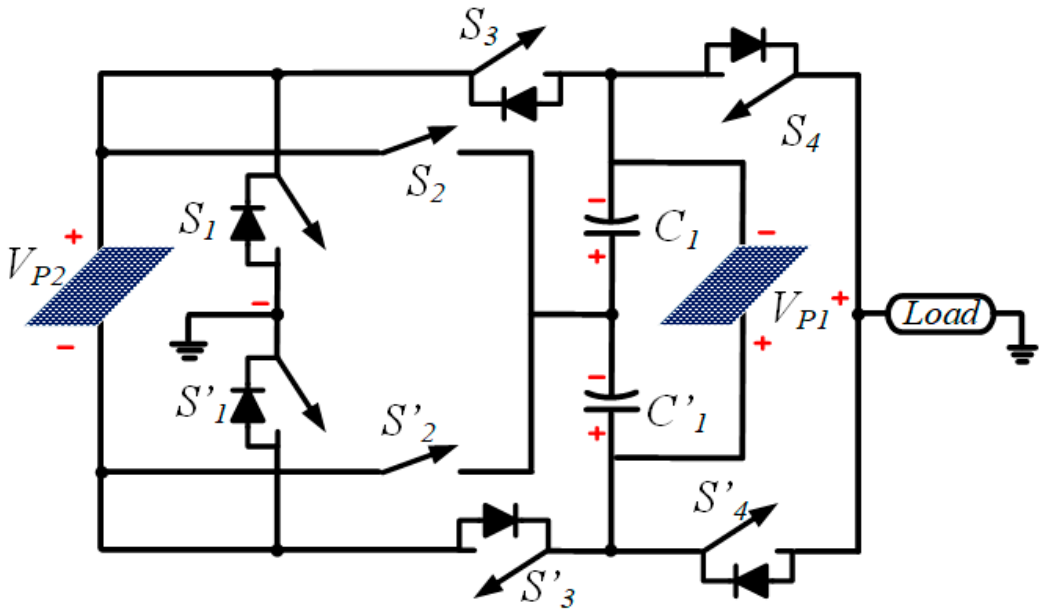


Figure 1. Circuit configuration of proposed module.

2.2. Mode of Conduction

The magnitude of dc sources is considered as $V_{p1} = 2\ V_{dc}$ and $V_{p2} = 4\ V_{dc}$, to generate a 13-level from the proposed topology. These sources can be established from PV sources and dc-link capacitors for possible voltage-level generation with different magnitudes. Figure 2a–g shows the various conduction modes of the proposed topology for positive and zero level generation. The conduction path is highlighted with pink color, and the corresponding output voltage is mentioned in the load terminal. In mode 1, the switches S'_1, S'_2, and S'_4 are turned on and other switches are turned off, a single dc source can provide the supply to the load and generate V_{dc} voltage level, and Figure 2a shows the current path. The second level ($2\ V_{dc}$) is developed with the conduction of switches S_1, S_3, and S'_4, with two equal magnitudes of dc sources, as shown in Figure 2b. At this level,

another dc source (4 V_{dc}) is included and subtracted with a dc-link voltage (V_{dc}) to produce the output voltage as 3 V_{dc} with the conduction of switches S'_1, S_2, and S_4.

Table 1. Switching scheme for 13-level generation.

Level	On Switches								Output Voltage ($V_{o,\,Max}$)	Each Voltage Level Value (V)
	S_1	S'_1	S_2	S'_2	S_3	S'_3	S_4	S'_4		
0	1	0	0	0	1	0	1	0	0	0 V
+1	1	0	1	0	0	0	0	1	$V_{c'1}$	$+V_{dc}$
+2	1	0	0	0	1	0	0	1	$V_{c'1}+V_{c1}$	+2 V_{dc}
+3	0	1	1	0	0	0	1	0	$V_{p2}-(V_{c'1}+V_{c1})$	+3 V_{dc}
+4	0	1	0	0	1	0	1	0	V_{p2}	+4 V_{dc}
+5	0	1	1	0	0	0	0	1	$V_{p2}-V_{c'1}$	+5 V_{dc}
+6	0	1	0	0	1	0	0	1	$V_{p2}+V_{c'1}+V_{c1}$	+6 V_{dc}
0	1	0	0	0	1	0	1	0	0	0 V
−1	0	1	0	1	0	1	1	0	$-V_{c1}$	$-V_{dc}$
−2	0	1	0	0	0	0	1	0	$-(V_{c'1}+V_{c1})$	−2 V_{dc}
−3	1	0	0	1	0	1	0	1	$-V_{p2}+V_{c'1}+V_{c1}$	−3 V_{dc}
−4	1	0	0	0	0	0	0	1	$-V_{p2}$	−4 V_{dc}
−5	1	0	0	1	0	1	1	0	$V_{c'1}-V_{c2}$	−5 V_{dc}
−6	1	0	0	0	0	0	1	0	$-(V_{p2}+V_{c'1}+V_{c1})$	−6 V_{dc}

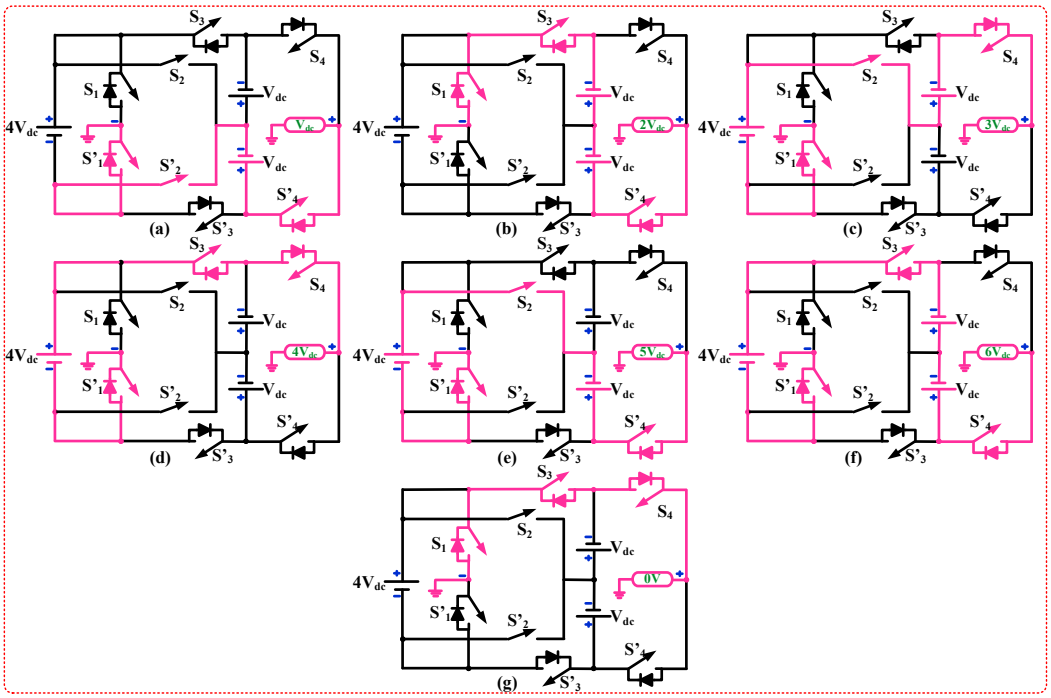


Figure 2. Various voltage-level generations of the proposed module. (**a**) V_{dc} level (**b**) 2 V_{dc} level (**c**) 3 V_{dc} level (**d**) 4 V_{dc} level (**e**) 5 V_{dc} level (**f**) 6 V_{dc} level (**g**) 0 level.

The fourth voltage level can be generated from a PV source (V_{P2}), and the switches S'_1, S_3, and S_4 can be turned on without adding dc-link capacitors. In Figure 2e, the switches S'_1, S_2, and S'_4 are turned on with the addition of two unequal magnitude dc sources; as a result, the voltage 5 V_{dc} is obtained in the output. All PV panels together can supply the load, and the switches S'_1, S_3, and S'_4 are turned on to achieve the maximum output level of the proposed module. Moreover, zero level is obtained with the conduction of either upper side switches (S_1, S_3, and S_4) or lower side switches (S'_1, S'_3, and S'_4), and no sources are included in this mode. Similarly, the negative voltage level can be generated based on the switching pattern as shown in Table 1. However, two or three switches are turned on for each voltage-level generation among eight switches, which is an added advantage of the proposed topology. Thus, each module is capable of fourteen operating modes and

the synthesis of thirteen voltage levels: 0, ±1 V_{dc}, ±2 V_{dc}, ±3 V_{dc}, ±4 V_{dc}, ±5 V_{dc} and ±6 V_{dc}. In output level generation, the maximum voltage stress of the switches is obtained as 6 V_{dc}. The maximum voltage stress should not be higher than the output voltage for any voltage-level generation.

2.3. Cascaded Structure for Proposed Module

Furthermore, to increase the voltage level, the proposed topology can be extended with the '*n*' number of cascaded modules, as shown in Figure 3. Each unit can be energized with two PV sources (V_{P11}, V_{P21}, V_{P12}, V_{P22} … , V_{P1n}, and V_{P2n}) and can generate output voltage (V_{O1}, V_{O2} … V_{On}). The maximum voltage ($V_{O,Max}$) of the proposed topology is the addition of individual output voltage of cascaded units, and the voltage level (N_{Level}) can be determined in general as '2 $V_{O,Max}$ + 1'. Then, other parameters such as a number of dc sources (N_{DC}), switches (N_S), and gate driver circuits (N_G) can be expressed in terms of a number of the cascaded module as '2*n*' and '8*n*', respectively. It is obvious that the proposed topology uses an equal number of switches and gate driver circuits and the voltage-level generation is based on the magnitude of dc sources' value.

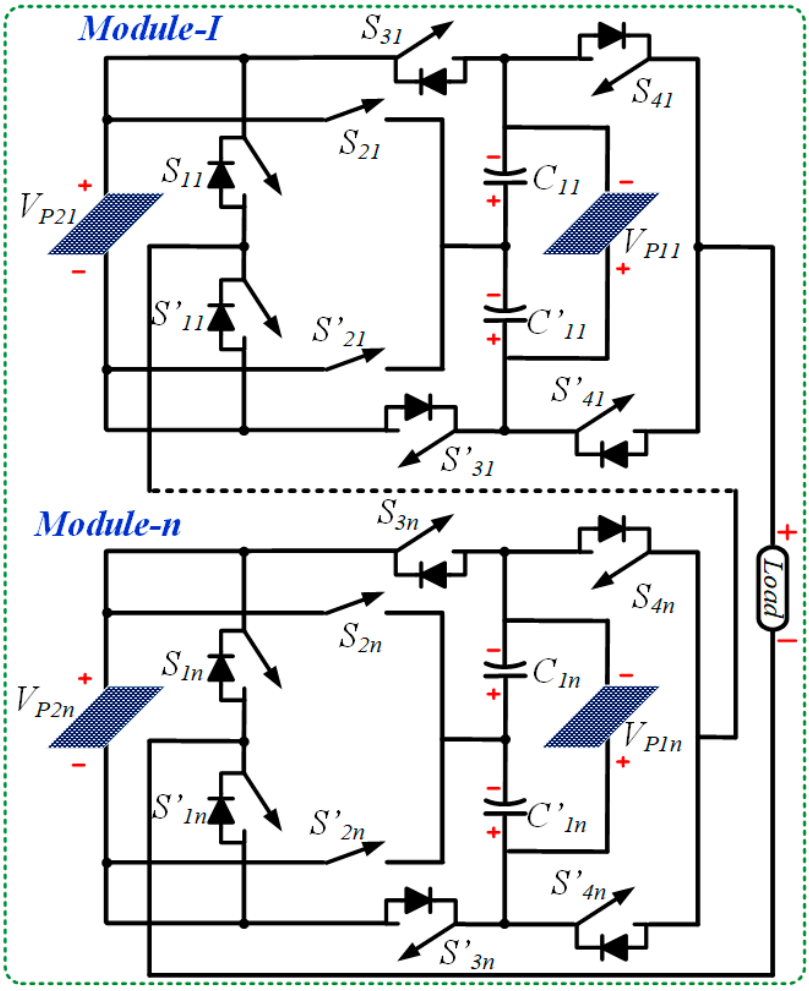


Figure 3. Cascaded structure of proposed topology with '*n*' module.

2.3.1. Determination of the Magnitude of PV Sources for Maximum Output Voltage Level

The output voltage level is determined based on the magnitude of the PV panel voltage. If the dc sources' value is equal, the output voltage level is obtained as

$$N_{Level} = 6n + 1 \quad (1)$$

According to symmetric dc source value, a more number of power components are required for the increased voltage-level generation. To reduce the number of power switches and dc sources, asymmetric dc source value is considered with the ratio of 1:2 as $V_{P11} = 2V_{dc}$, $V_{P12} = 4V_{dc}$, and the output voltage and voltage level are determined in the first unit as

$$V_{O1,Max} = V_{P11} + V_{P12} = 6V_{dc} \text{ and } N_{Level,1} = 13 \quad (2)$$

In the second unit, asymmetric PV source value is determined from the previous unit output voltage, and the output level can be obtained as '$N_{Level,2} = 13^2$'. In this way, the maximum output voltage can be generated in 'nth' cascaded unit with the PV source value of $V_{Pi1} = (2V_{Oi-1,Max} + 1) * V_{dc}$, $V_{Pi2} = 2 * V_{\mathrm{Pi1}}$, and the output voltage and level are determined in the 'nth' cascaded module as

$$V_{Oi,Max} = (V_{Oi-1,Max} + V_{Pi1} + V_{Pi2}) * V_{dc} \quad (3)$$

$$N_{Level,i} = 13^i \text{ where } i = 1,\ 2,\ 3 \ldots n \quad (4)$$

2.3.2. Calculation of Total Standing Voltage

In cascaded topology, a higher number of voltage levels can be generated with the addition of modules, but it is limited due to the voltage stress on the switches and the cost of the high-voltage semiconductor devices. The voltage stress states that off-state voltage appears on each switch, which can be represented for cascaded 'n' modules (V_{S1n}, $V_{S'1n}$), (V_{S2n}, $V_{S'2n}$), (V_{S3n}, $V_{S'3n}$), and (V_{S4n}, $V_{S'4n}$). In addition, the voltage stress is based on the dc sources connected with the switches, and it is equal for each pair of switches. It means that the voltage stress of switch pairs (V_{S2n}, $V_{S'2n}$) and (V_{S4n}, $V_{S'4n}$) is equal to its PV source value, and the switches (V_{S1n}, $V_{S'1n}$) withstand the dc-link voltage value. However, the voltage stress of the switches (V_{S3n}, $V_{S'3n}$) is the sum of the two available PV sources; the maximum voltage stress of the inverter may be equal to the output voltage. According to this, the voltage stress of the switches can be evaluated for 'n' cascaded units as

$$V_{S1n} = V_{S\prime 1n} = V_{P1n}/2,\ V_{S2n} = V_{S2\prime n} = V_{P2n},\ V_{S3n} = V_{S\prime 3n} = (V_{P1n} + V_{P2n}), V_{S4n} = V_{S\prime 4n} = V_{P2n} \quad (5)$$

The total standing voltage (V_T) of the inverter can be obtained with the sum of voltage stress on individual switches

$$V_T = 2\sum_{i=1}^{n} (V_{S1n} + V_{S2n} + V_{S3n} + V_{S4n}) * V_{dc} \quad (6)$$

$$\begin{aligned} V_T &= 2\sum_{i=1}^{n} \left(\frac{5V_{P1n}}{2} + 2V_{P2n}\right) * V_{dc} \\ V_T &= \left[\frac{13(N_{Level}-1)}{6}\right] * V_{dc} \end{aligned} \quad (7)$$

3. Comparison of the Proposed Topology with the Existing 13-Level Topologies

The features of multilevel inverters can be evaluated based on their structure, operation, and application. In this aspect, required number switches, gate drivers, dc sources, and total standing voltage are considered as key parameters for the performance assessment. However, multilevel inverters synthesize different voltage levels in a symmetric and asymmetric configuration; for a reasonable comparison, the 13-level proposed topology is examined with conventional and recent topologies [10–24] in a similar output-level operation.

Figure 4a shows the graphical representation of switches versus voltage level, and it is observed that the conventional NPC, FC, and CHB MLIs use an equal number of switches for any voltage-level generation, and four switches are required in each unit to increase the voltage level. However, the presented topology [22] needs fewer switches than other topologies, and also the proposed topology uses lower number switches than considered topologies for all voltage-level generation. In Figure 4b, the graph represents

the gate driver circuit in terms of voltage level. The topologies [12,15,24] use the same number of switches and gate driver circuits, but the remaining topologies use bidirectional switches that reduce the required gate driver circuit and increase the number of switches. On other hand, topologies [15,16] utilize diodes for power flow and level generation instead of switches and gate driver circuits. It is shown that the proposed topology does not have any additional diodes and bidirectional switches for all possible voltage-level generation; hence, this reduction of components is a remarkable advantage of the proposed topology, which makes it feasible for medium-voltage application. Another limitation of the cascaded multilevel inverter in terms of cost and size is the required dc sources for the PV application as compared in Figure 4c. The topologies [10,14] have a similar operation of symmetric CHB, which uses an equal number of dc sources for voltage-level generation. The topology [15] requires a lower number of dc sources than other topologies due to its asymmetric configuration, but it requires an additional number of dc-link capacitors for voltage sharing and level generation instead of isolated dc sources. A higher voltage level with reduced dc sources and capacitors is an effective improvement in the proposed topology, compared to conventional and other presented topologies.

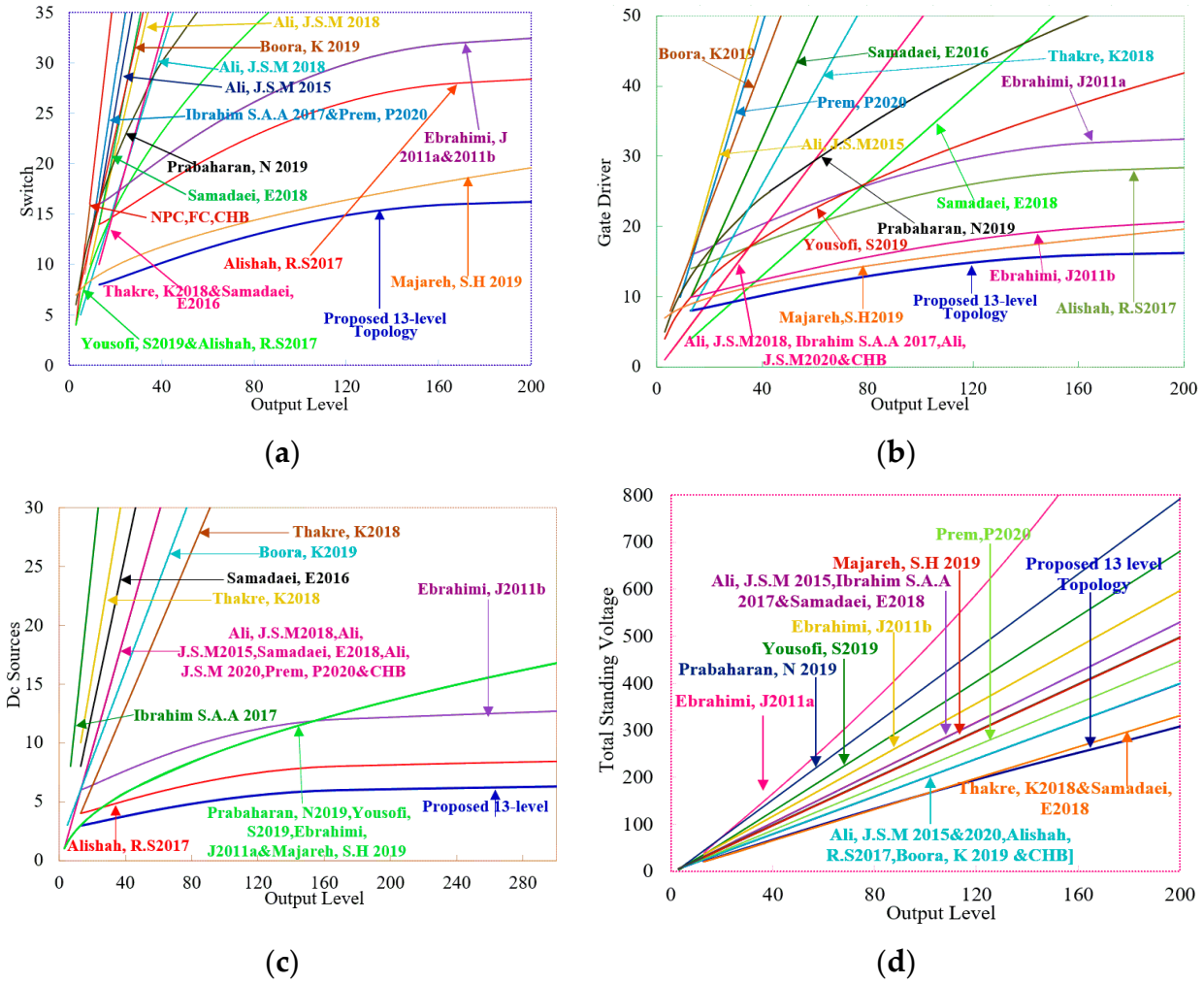


Figure 4. Comparison of performance parameters: (**a**) switch vs. output level, (**b**) gate driver vs. output level, (**c**) Dc sources vs. output level and (**d**) total standing voltage vs. output level.

Furthermore, as illustrated in Figure 4d, the total standing voltage of proposed and existing topologies is investigated for various voltage levels. The topologies [18,19] have lower standing voltage than other topologies that do not use H-bridge circuits such as [11–14,16,17] and packed H-bridge circuits in [15,22] for negative voltage-level genera-

tion. The presented topologies in [18,19] have a closed slope, with the proposed topology at the initial stage when it generates a higher voltage level; the proposed topology needs lower standing voltage than the remaining topologies. However, the proposed topology produces a higher number of voltage levels with reduced components than other topologies in the comparison, but the asymmetric source configuration requires the switches and heat sinks in different voltage ratings, which may increase the cost of the inverter. The cost of the switch rises as the number of high-voltage switches grows, but the suggested design includes two high-voltage switches in each unit. As a result, a cost comparison is presented for 13-level inverters with switches (N_S), gate drivers (N_G), dc sources (N_{DC}), dc-link capacitors (N_C), diodes (N_D), and per unit values of total standing voltage ($V_{TP \cdot U}$).

In order to consider the lower and higher current rating of the switches, the current coefficient (α) is (0.5 or 1.5) multiplied with the total standing voltage of the inverter, respectively, as given in (8). From the comparison, the proposed topology has a lower value of cost function (*C.F*) than the conventional and existing topologies, which is a remarkable advantage of the proposed topology. In Table 2, the parameters such as the number of switches, total utilization factor (*TUF*), switch utilization factor (*SUF*), and standing voltage are obtained with the ratio of the number of levels, which is also a lower value than other topologies. These features indicate the feasibility of the proposed topology for various medium-voltage operations such as PV application instead of the existing topologies.

$$CF = (N_S + N_C + N_G + \alpha.V_T p.u) \times N_{DC} \quad (8)$$

Table 2. Comparison of various parameters, which includes cost function for 13-level inverter topologies.

Ref	N_L	N_S	N_G	N_{DC}	N_D	N_C	*MSV*	V_T	$V_{TP \cdot U}$	*TUF*	*SUF*	*CF*		Polarity Changer
CHB	13	16	16	6	0	0	V_{dc}	16	2.7	1.2	1.2	15.4	16	Inherent
[10]	13	14	14	3	0	6	3 V_{dc}	26	4.3	2	1.1	8.3	8.8	Inherent
[11]	13	16	13	3	0	0	6 V_{dc}	45	7.5	3.5	1.2	7.6	8.4	H bridge
[12]	13	16	16	6	0	0	6 V_{dc}	36	6	2.8	1.2	16.2	17.5	H bridge
[13]	13	16	10	6	0	0	6 V_{dc}	39	6.5	3	1.2	13.5	15	H bridge
[14]	13	16	10	3	0	0	6 V_{dc}	36	6	2.8	1.2	6.7	7.4	H bridge
[15]	13	14	14	2	4	4	6 V_{dc}	30	5	2.3	1.1	5.9	6.3	Packed H bridge
[16]	13	18	16	3	2	4	6 V_{dc}	32	5.3	2.5	1.4	9.8	10.5	H bridge
[17]	13	12	10	3	0	0	6 V_{dc}	37	6.2	2.8	0.9	5.8	6.5	H bridge
[18]	13	10	8	4	0	0	6 V_{dc}	27	4.5	2.1	0.8	6.2	6.9	Inherent
[19]	13	10	8	4	0	0	5 V_{dc}	20	3.3	1.5	0.8	6.1	6.6	Inherent
[20]	13	14	9	2	0	2	6 V_{dc}	32	5.3	2.5	1.1	4.3	4.7	Inherent
[21]	13	16	16	6	0	0	6 V_{dc}	30	5	2.3	1.2	15.9	17.1	Inherent
[22]	13	9	9	3	3	0	6 V_{dc}	30	5	2.3	0.7	5.4	6	Packed H bridge
[23]	13	11	11	3	3	6	3 V_{dc}	26	4.3	2	0.8	7.7	8.2	Inherent
[24]	13	18	15	3	0	6	3 V_{dc}	27	4.5	2.1	1.4	9.5	10	Inherent
Proposed	13	8	8	2	0	2	4 V_{dc}	26	4.3	2	0.6	3.1	3.4	Inherent

4. Proposed Module with PV Configuration

A solar panel is a combination of PN junction diodes with a light-illuminating effect. When there is a solar light incident on the panel, the absorbed photon energy is converted into electrical energy. The magnitude of generated voltage (V_{pv}) is based on the irradiance level of sunlight (λ), atmospheric temperature (T), and potential energy of carriers (q). The schematic arrangement of the solar-fed proposed topology is shown in Figure 5. In Figure 6, the PV panel is presented with solar irradiation and equivalent circuit. The panels can be connected in series (N_S) and parallel (N_P), in order to increase the output voltage and current; Figure 6a shows the series-connected panels. A simple model of the PV panel is represented in Figure 6b, and a current source is connected with an antiparallel diode where the series (*Rs*) and parallel (*Rp*) resistance are included for practical consideration. In (9)–(11), I_{Ph} is a photon current as generated from solar energy, I_D is a diode current, I_P

is current flow through the shunt resistance, and I_O is the diode reverse saturation current. When the generated voltage is supplied to a load, the output current (I_{pv}) is drawn from the PV cell as deduced as

$$I_{Pv} = I_{ph} - I_D - I_P \tag{9}$$

$$I_D = I_o\left(\exp\left(\frac{qV_d}{aBT_C}\right) - 1\right) \tag{10}$$

where V_d—diode voltage, q—the electron charge in Columb, a—the ideality factor, B—the Boltzmann's constant, and T_C—the cell absolute temperature in Kelvin.

$$I_{Pv} = N_P\left[I_{Ph} - I_o\left(\exp^{q\left[\left(\frac{V_{Pv}}{N_S}\right)+\left(\frac{I_{Pv}}{N_P}\right)R_S\right]} - 1\right) - \frac{\left(\frac{V_{Pv}}{N_S}\right) + \left(\frac{I_{Pv}}{N_P}\right)R_S}{R_P}\right] \tag{11}$$

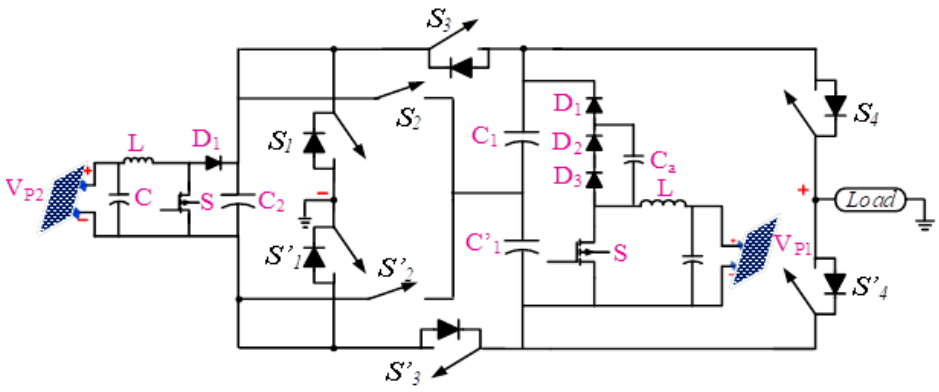


Figure 5. Schematic arrangement of PV sourced proposed module.

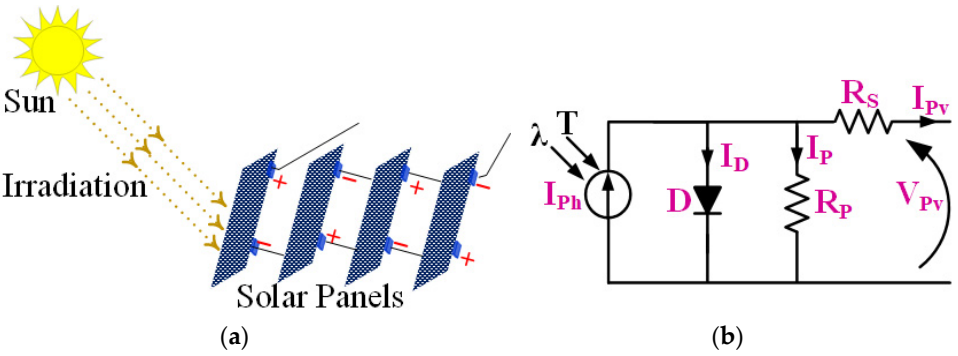


Figure 6. (**a**) Connection of solar panel and (**b**) equivalent circuit of solar panel.

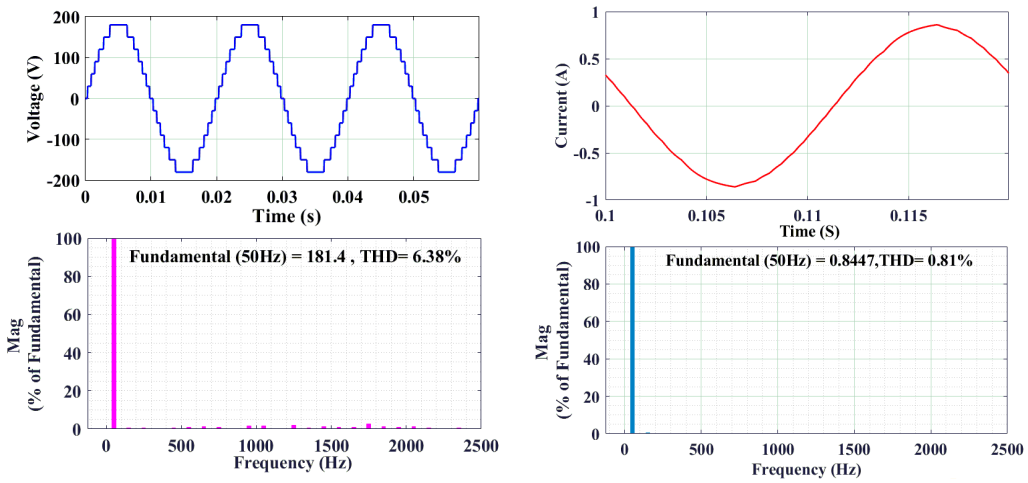
5. Results and Discussion

5.1. Simulation Validation

The switching schemes, output waveform, and power loss analysis of the proposed 13-level inverter are obtained with MATLAB/Simulink software. In MLI operation, the staircase output waveform is generated with proper commutation of switches, which is promising for different modulation techniques such as Pulse Width Modulation (PWM) or low-switching-frequency method. For higher voltage-level generation, fundamental frequency modulation is preferred; therefore, the proposed topology can implement the NLC method. The sinusoidal signal (50 Hz) is compared to the stepped waveform in order to create the gate pulse for appropriate level creation, according to Table 1. The magnitude of switching angle (θ_j) is determined for each cycle and given as follows:

$$\theta_j = \sin^{-1}\left(\frac{j - 0.5}{13}\right) \quad for\ j = 1, 2, \ldots 13 \tag{12}$$

Two PV sources are considered as V_{p1} = 60 V and V_{p2} = 120 V, and the peak value of the output voltage reaches 180 V for RL load value of 50 Ω and 100 mH, respectively. Figure 7a depicts the voltage waveform with its harmonic spectrum, whereas Figure 7b depicts the current waveform with its harmonic spectrum. The corresponding THD value of voltage and current waveforms is calculated from the Fast Fourier transform (FFT) analysis as 6.38% and 0.81%. The suggested topology's input and output parameters are then reported in Table 3. According to the recommended circuit diagram, the levels are generated as 0 V, 30 V, 60 V ... 120 V, 150 V, and 180 V. Then, the output current is drawn as 3.04 A for the given load values.



(**a**) (**b**)

Figure 7. Simulation output waveform with FFT analysis: (**a**) voltage and (**b**) current.

Table 3. Important parameters with simulation results.

Output Parameters	Simulation Results
Input voltage	V_{p1} = 60 V and V_{p2} = 120 V
Load value	R = 50 Ω, L = 100 mH
Maximum output voltage	180 V
Output current	3.04 A
Voltage THD	6.38%
Current THD	0.81%
Input power	548.762
Output power	534.5 W
Efficiency	97.4%

In order to verify the dynamic performance of the 13-level inverter, different modulation indexes and loading scenarios are considered, and the observed waveforms are presented in Figures 8 and 9, respectively. Figure 8 shows the output voltage and current waveform for the modulation indexes of 0.2 to 0.8 with an RL load for t = (0–2) s. It is observed from the figure that the output voltage levels are increased from level three to level 13. Then, the modulation index is varied from 0.2 to 0.4 at t = 0.3 s, where the voltage levels are increased from level three to level seven. At t = 0.6 s, the modulation index is adjusted as 0.6 and the output level is increased to level 11, and the output continuously reaches level 13 when the modulation index is 0.8. However, the modulation index value varies from 0.8 to 0.2, the symmetrical current and voltage waveform can be decreased from level 13 to level three. The simulation results of step load changes are presented in Figure 9. It indicates that the load value is considered as R = 50 Ω, L = 100 mH and R = 100 Ω, L = 200 mH, where the voltage waveform is uniform and produces level 13, but the current waveform is obtained with step variation at t = (0.1–0.2) s.

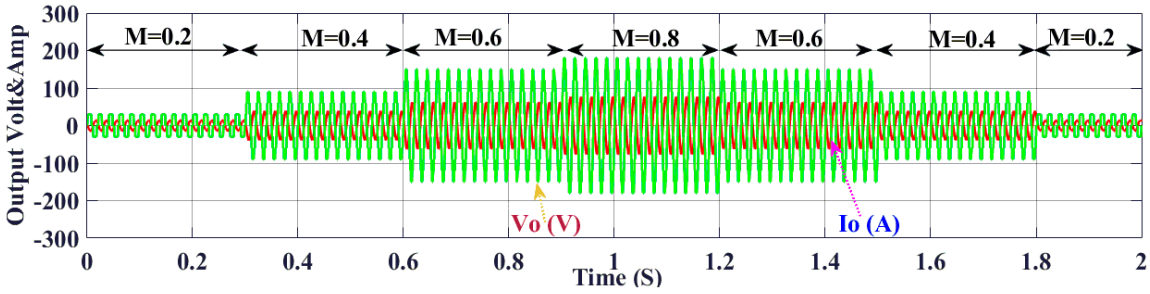


Figure 8. Simulation voltage and current waveform for different modulation indices.

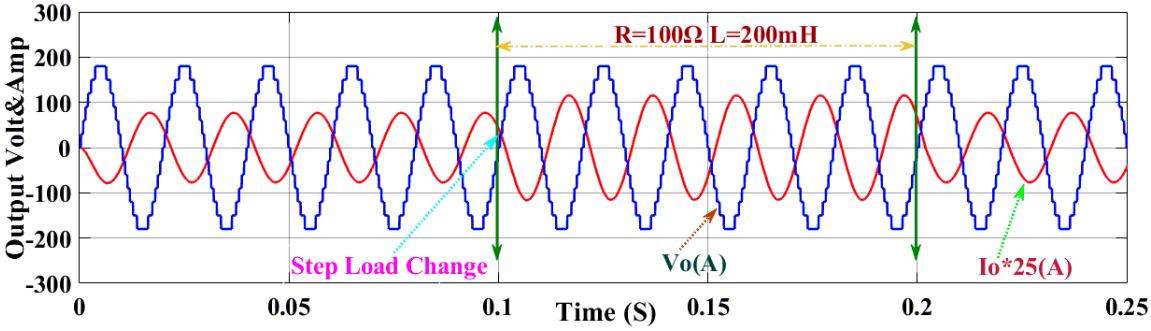


Figure 9. Simulation response of voltage and current waveform with step load change.

Moreover, the power loss of switches is determined for the given load value in the simulation study, and the results are plotted in Figure 10. The power loss is associated with the switching loss and conduction loss of the IGBT and diode present in the switches (S'_1, S_1 S'_3, S_3, S'_4, S_4), but the loss is calculated for IGBT alone for switches S_2 and S'_2 because they do not include the freewheeling diode. Accordingly, the efficiency is obtained as 97.5% for the output power of 0.5 kW with RL load.

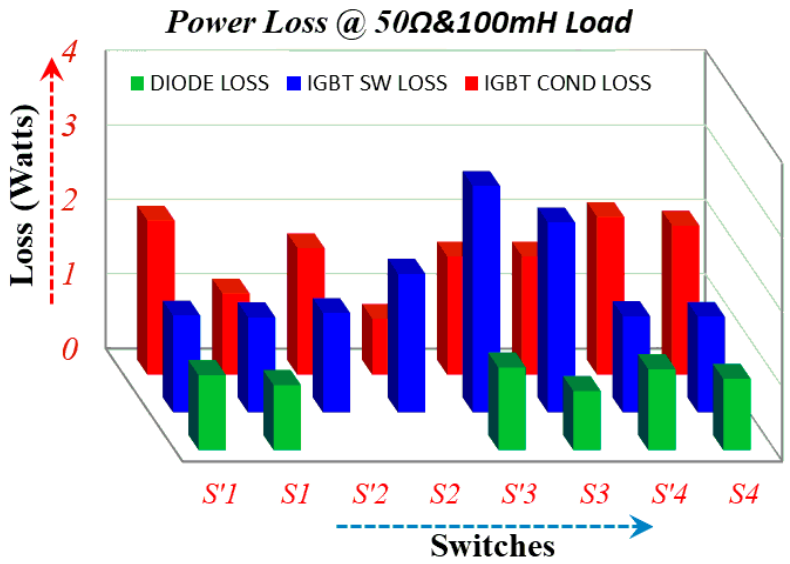


Figure 10. Simulation value of power loss calculation of switches.

5.2. Experimental Validation

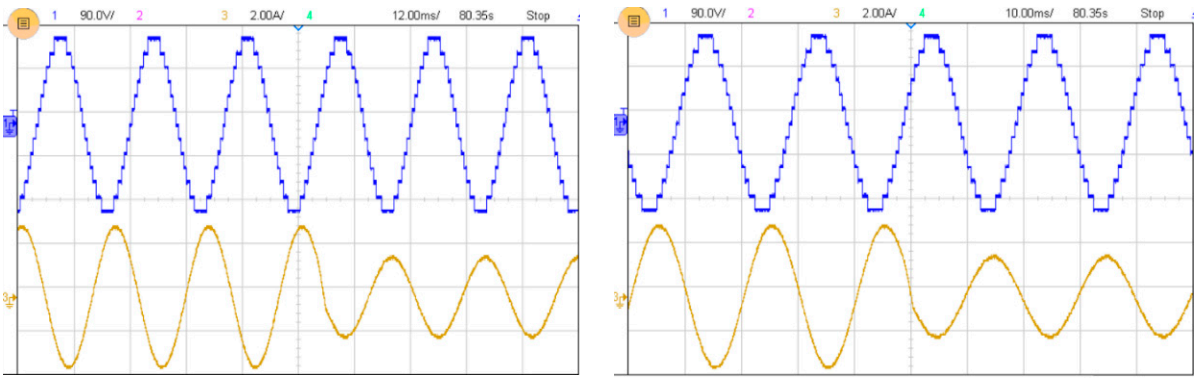
To confirm the simulation result of the proposed topology, an experimental setup is developed in a laboratory environment, as shown in Figure 11. For the experimental validation, the operating parameters are considered and depicted in Table 4. The circuit module consists of eight low-voltage IGBTs and gate driver circuits, which are implemented with

the proto type model of BUP400D and HCPL316J, respectively. The suitable gating pulses are generated with the FPGA Spartan XE3S250E controller for output level generation according to Table 1. The input voltage is given from the regulated power supplies (RPS) with the values of V_{p1} = 60 V and V_{p2} = 120 V. The maximum peak voltage is obtained for the load value of R = 50 Ω and L = 100 mH. The required output waveforms are captured using the DSOX3034T Oscilloscope with different loading conditions such as resistive, highly inductive, and balancing loads. For the configurations, the voltage and current waveforms are obtained from the experimental setup as given in Figures 12–15.

Figure 11. Photograph of laboratory experimental setup for proposed MLI.

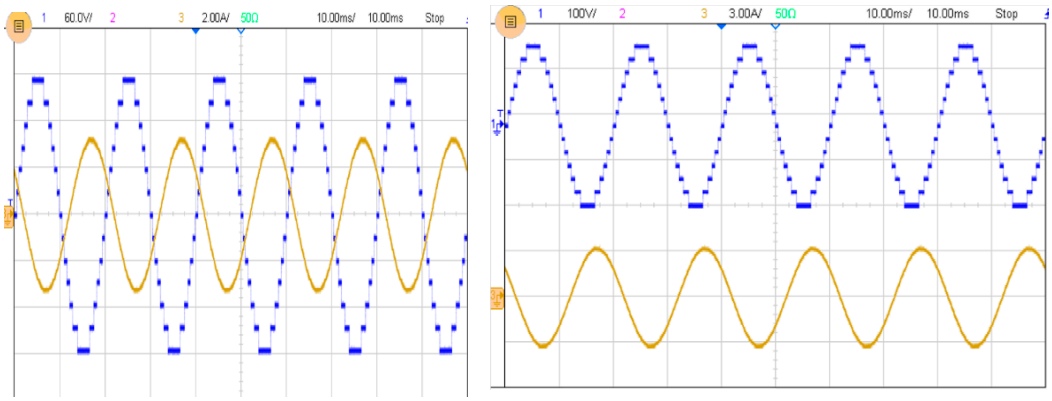
Table 4. Important parameters with experimental results.

Output Parameters	Simulation Results
Input voltage	V_{p1} = 60 V and V_{p2} = 120 V
Load values	R = 50 Ω, L = 100 mH to R = 100 Ω, L = 200 mH
IGBT	BUP400D
Gate driver circuit	HCPL316J
Maximum output voltage	180 V
Output current	3.08 A
Input power	550.762
Output power	532.5 W
Efficiency	95.4%



(**a**) (**b**)

Figure 12. The experimental value of output voltage and current waveform in the 13-level inverter (**a**) with balancing load and (**b**) with load changes.



(**a**) (**b**)

Figure 13. Experimental results (**a**) for highly inductive load and (**b**) zoomed view of load changes.

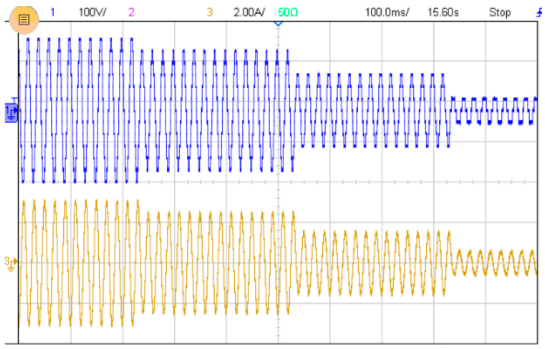
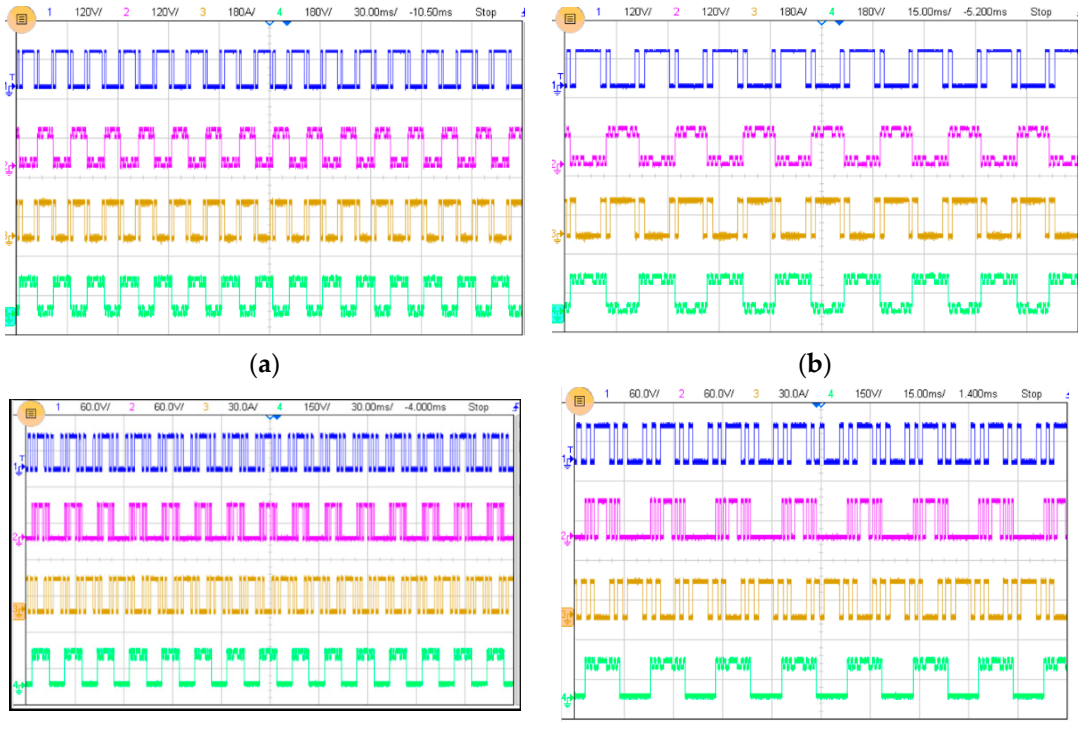


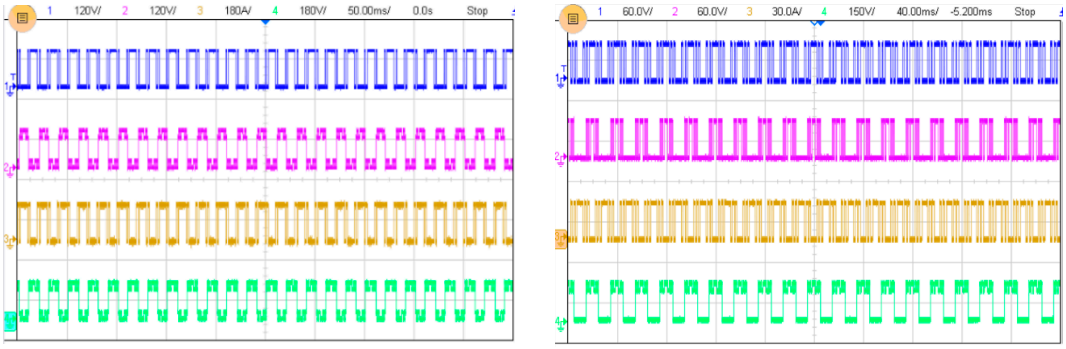
Figure 14. Experimental results of 13-level inverter voltage and current for continuous load changes.



(**a**) (**b**)

(**c**) (**d**)

Figure 15. *Cont.*



(**e**) (**f**)

Figure 15. Experimental blocking voltage across various switches (S) in 13-level inverter (**a**) S'_1, S_3, and S_4; (**b**) S_1, S'_4; (**c**) S_1, S_3, and S_4; (**d**) S'_1; (**e**) S_2; and (**f**) S'_2.

In Figure 12a, the output voltage and current waveform of the proposed topology are observed with the balancing load circuit. The effect of the load change on load voltage and current are indicated in Figure 12b. When the load value is changing from the R = 50 Ω, L = 100 mH to R = 100 Ω, and L = 200 mH, the output voltage waveform remains the same, and the load current is instantaneously changed at the initial time of load transition. However, the output current waveform is near the sinusoidal waveform, as shown in Figure 13a, and its zoomed view is depicted in Figure 13b.

Figure 14 shows that the output voltage levels have increased from three to thirteen. The modulation index is then increased from 0.2 to 0.4 at t = 0.3 s, by raising the voltage levels from three to seven. At t = 0.6 s, the modulation index is set to 0.6 and the output level is increased to level 11, and eventually the output level reaches level 13, when the modulation index is set to 0.8. However, the modulation index values vary from 0.8 to 0.2, and the symmetrical current and voltage waveform decrease from level 13 to level three. As illustrated in Figure 15a–f, the magnitude of the blocking voltage of the switches does not exceed the peak magnitude of 6 $V_{DC,}$ which shows that the low voltage switches can be used in the proposed topology for 13-level output generation.

6. Conclusions

In this paper, a novel cascaded MLI is proposed to produce a higher number of voltage levels with a reduced number of power components. This proposed module is designed with eight IGBTs, eight gate driver circuits, and two dc sources. The input PV sources are used with the voltage ratio of 1:2 to produce the 13-level output. Then, the required circuit parameters of the developed cascaded structure are evaluated, and their values are much lower than the recent topologies in the comparison study. Moreover, the simulation study is explored using MATLAB/Simulink software with FFT analysis and loss calculation under different loading scenarios. In order to verify the obtained simulation results, an experimental model is developed, and this research demonstrates that the feasibility of the proposed topology is suitable for PV application.

Author Contributions: A.V.P.: analysis, design, simulation, and hardware implementation of the proposed system; K.D.: comparison and validation of results; A.I.S.A.: formatting and English editing with grammar check. All authors have read and agreed to the published version of the manuscript.

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