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High Efficiency Transformerless Photovoltaic DC/AC Converter with Common Mode Leakage Current Elimination: Analysis and Implementation

Jorge Cardoso [1], Rodolfo Orosco [1], Nimrod Vazquez [1,*], Héctor López [1], Claudia Hernandez [1] and Joaquin Vaquero [2]

[1] Tecnológico Nacional de México/Instituto Tecnológico de Celaya, Celaya 38010, Mexico; d1803028@itcelaya.edu.mx (J.C.); rodolfo.orosco@itcelaya.edu.mx (R.O.); hector.lopez@itcelaya.edu.mx (H.L.); cvhg@ieee.org (C.H.)

[2] Área de Tecnología Electrónica, Universidad Rey Juan Carlos, 28933 Madrid, Spain; joaquin.vaquero@urjc.es

* Correspondence: n.vazquez@ieee.org; Tel.: +52-461-611-7575

Abstract: Photovoltaic (PV) electricity is widely used because of its positive environmental impact. To properly feed this energy into the grid, an electronic power converter, known as a PV inverter, is needed, which may or may not use a transformer. This article details the analysis and design of a transformerless photovoltaic inverter topology for grid-connected applications. This converter offers high efficiency, a low number of elements, and negligible leakage current, which makes it a good alternative for this application. The converter has been validated through an experimental prototype and compared with other topologies with similar characteristics.

Keywords: common-mode (CM); leakage current; photovoltaic systems; transformerless inverter

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1. Introduction

Currently, the use of renewable energy has gradually increased due to the environmental problems present nowadays [1]. One of the solutions to help care for the environment is the use of renewable energy, being photovoltaic (PV) energy one of the most used [2], which requires the use of power converters to use the energy produced by photovoltaic panels. These systems may or may not be connected to the AC grid [3].

For the use of PV modules as electrical power generation systems, a power converter is needed, known as a PV inverter, that has the function to produce an AC output voltage of controlled magnitude and frequency from a fixed or variable DC power source [4].

Galvanic isolation is a method of protection required in PV systems for both functional and safety purposes. It can be found on the DC side in the form of a high-frequency transformer, or on the AC grid side in the form of a large heavy AC transformer [5]. Both solutions offer personal safety and functional advantages for the PV inverter and the grid, but the efficiency of the entire system is diminished due to its losses. If the transformer is omitted, the efficiency of the entire PV system can be increased by an extra 1% to 2% [6]. However, when a transformer is not employed, there is no galvanic isolation between the grid and the PV modules, which may produce a leakage current that flows through the parasitic capacitors, which is illustrated in Figure 1 [7–9].

Leakage current results in problems including low system efficiency, output current distortion, electromagnetic interference (EMI), safety issues, and eventually shortens the life of the PV module [10]. This current can be avoided, or at least limited, by considering techniques to keep the total common-mode voltage (V_{CM}) unchanged. These techniques can be used individually or in combination with others [11,12].

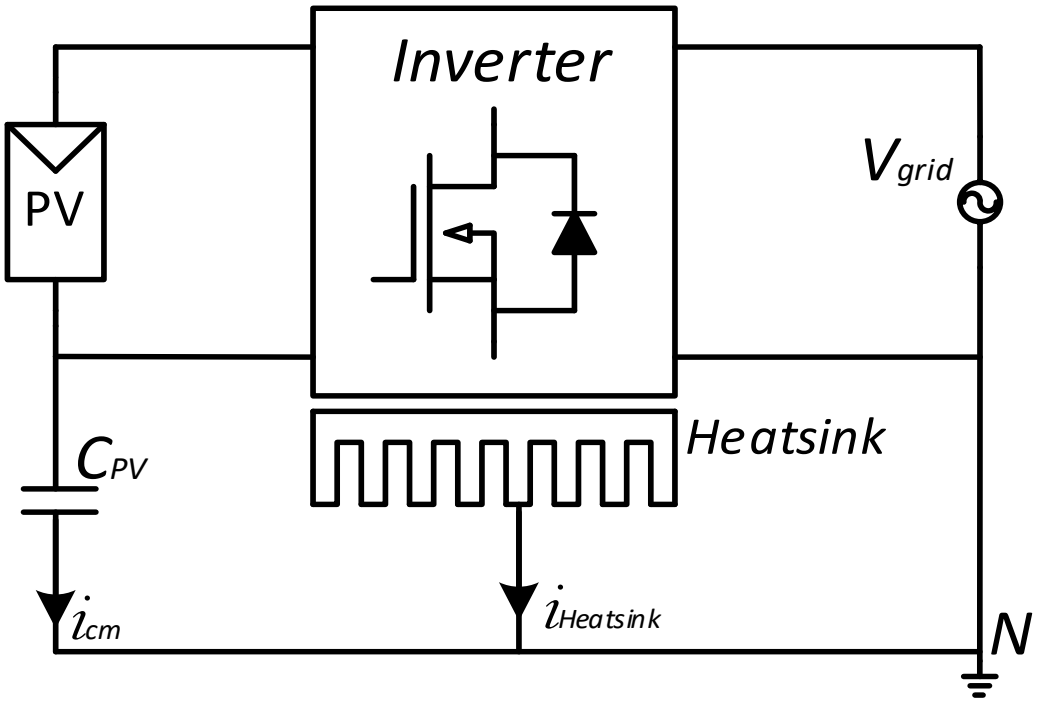

Figure 1. Leakage current in a photovoltaic system.

Sometimes the magnitude of the leakage current can exceed the permissible values, such as 300 mA stated in the German VDE 0126-1-1 grid standard, due to the variable behavior of the parasitic capacitance depending on the atmospheric conditions [13].

Many solutions have been proposed to reduce the leakage current. They can be classified into four types [7,14–22]. The first one is using bipolar SPWM modulation, which reduces the leakage current by not generating variations in V_{CM} [7]; the second technique is based on the disconnection of the PV modules from the grid when V_{CM} varies [14–18]; the third technique, instead of disconnecting the PV modules upon variations of V_{CM}, connect them to the mean voltage of the input voltage through a capacitive divider [7,19,20]. The last technique clamps the PV module negative terminal to the neutral point of the grid [16,21,22].

The latter technique results in the so-called common-mode topologies, offering good characteristics since the leakage current is theoretically eliminated. Different topologies have been proposed. In [21], the charge pump concept is employed, resulting in a topology with four active elements, two diodes, and two additional capacitors, in which always two or more devices are conducting at the same time, penalizing the efficiency. On the other hand, [15] proposes a variation of the flying inductor topology, which has a low semiconductor count; however, it also includes two devices that are always conducting at the same time. In [22], they propose a common-mode topology to eliminate the leakage current problem in addition to having high efficiency, however, no experimental results were provided.

In this paper, a variation of the topology seen in [22] is presented, which offers a low number of active elements in each mode of operation, resulting in improved efficiency, but keeping the common-mode connection and then theoretically eliminating the leakage current. The converter is composed of five switches and a capacitor additional to an LCL output filter. High efficiency is achieved due to low conduction losses, while no leakage current is obtained through the common-mode strategy, and low current harmonic distortion is achieved (% THD).

The paper is organized as follows: in Section 2, the operation principle of the topology is presented, as well as its dynamic equations; in Section 3, the design methodology is presented, both for the topology and the filter used; in Section 4, the control strategy

is discussed; in Section 5, the experimental results obtained are illustrated; in Section 6, the topology is compared against other existing topologies; and finally, in Section 7, a conclusion of the work is given.

2. Studied Inverter

To reduce the leakage current in grid-connected PV systems and improve efficiency, a transformerless PV inverter is analyzed and designed. The topology is shown in Figure 2. The scheme considers a direct connection between the negative terminal of the PV module and the neutral of the AC grid, this is keeping the common-mode voltage V_{cm} constant, thus reducing the possibility of leakage currents appearing.

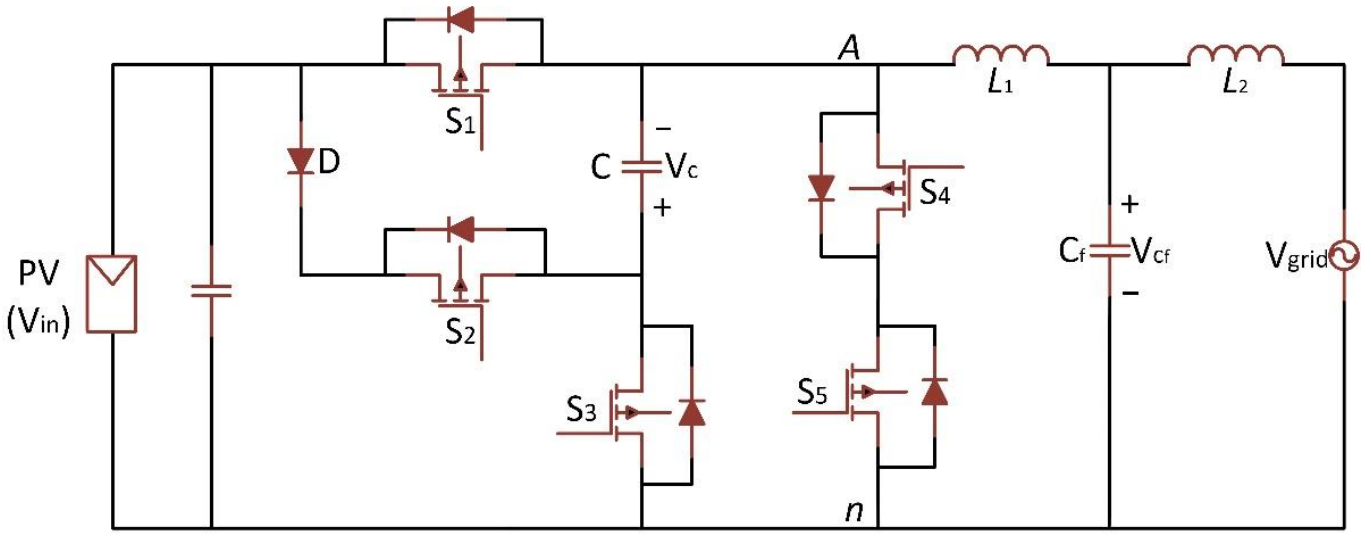

Figure 2. Studied transformerless inverter topology.

It can be seen in Figure 2 that the topology consists of: five switches (MOSFETs), in which S_4 and S_5 are in anti-series configuration; one diode (D), which prevents misconduction; a capacitor (C) which will provide the negative output voltage; and an output filter (LCL). The converter has switching states in which only one device is conducting, then the efficiency is improved by reducing the conduction losses. The operating principle is discussed in the next lines.

2.1. Operating Principles and Topology Modeling

The switching strategy and working principle of the topology are discussed in this section. The switching scheme of the inverter is illustrated in Figure 3. A unipolar sinusoidal pulse width modulation (SPWM) is employed [14,23,24]. This SPWM modulation compares a carrier signal against two modulating signals. Even though the unipolar SPWM modulations generate the necessary levels to charge and discharge the capacitor C, the bipolar modulation could not permit to charge the capacitor C, which prevents its use in this topology.

Figure 3 also shows the inverter control signals (P, Q, and R), the signals of each switch (S_1, S_2, S_3, S_4, and S_5), the voltage node signal (V_{An}), and finally, the operating mode that determines each level in the output V_{An}, all represented at a low frequency.

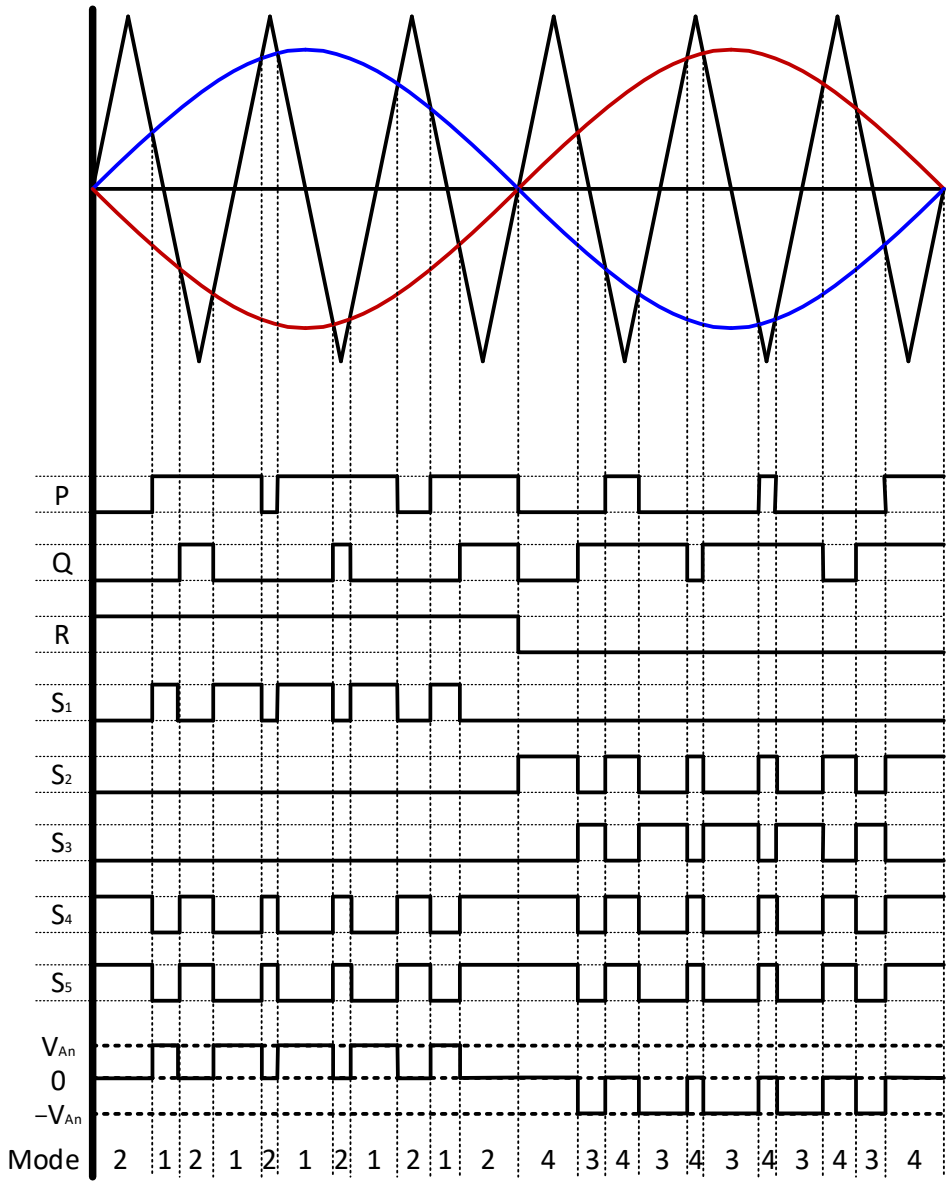

Figure 3. Ideal waveforms of the inverter with a unipolar SPWM.

Through the control signals P and Q, the level of the V_{An} signal can be inferred; when signals P and Q are equal, zero level is generated for signal V_{An}. When signals P and Q are different, signal V_{An} can be positive or negative, depending on the positive or negative half-cycle of the AC grid (determined by control signal R).

It can be seen that the control signals for the switches S_1, S_2, and S_3 commute in a hybrid way, only during one half-cycle, while the switches S_4 and S_5 operate at high frequency. This allows a reduction in switching losses since only two devices are operating at this high frequency during the whole time, achieving better efficiency in the system. Also notice that there are two switching states in which only one device is conducting instead of two as other topologies usually do, reducing the conduction losses.

The different switching states of the inverter are displayed in Figure 4a–d. For the explanation of the modes of operation, it is assumed that all active and passive elements are ideal devices.

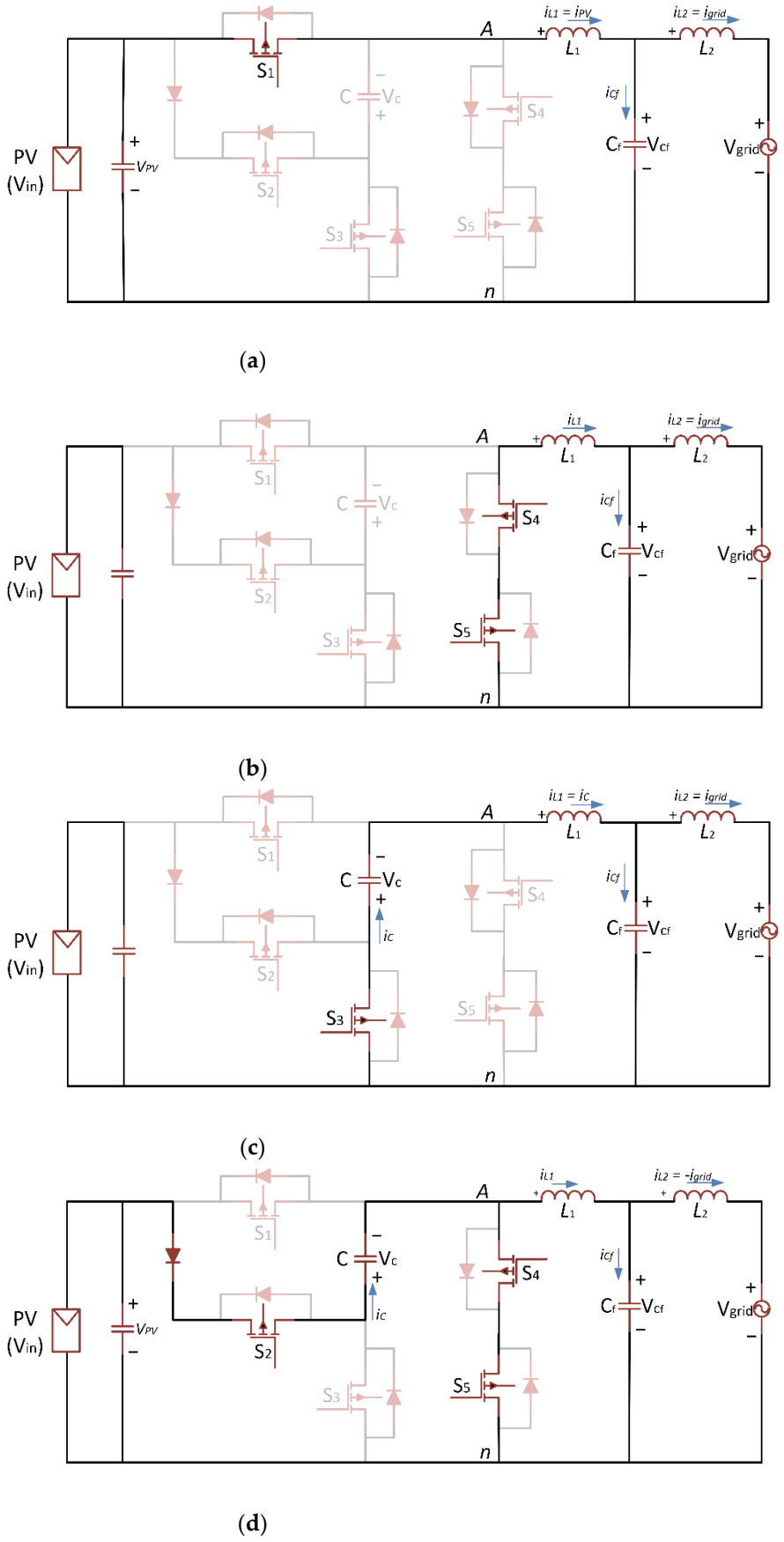

Figure 4. Switching states of the proposed transformerless inverter: (**a**) Mode 1, (**b**) Mode 2, (**c**) Mode 3, (**d**) Mode 4.

Mode 1 (S_1 is ON, and S_2, S_3, S_4, and S_5 are OFF). This mode generates the voltage for the positive half-cycle (V_{PV}), and the capacitor voltage V_C remains unchanged. The voltage level before the filter (V_{An}) in this mode is equal to V_{PV}. The state equations for this mode are:

$$\frac{d}{dt}v_C = 0 \tag{1}$$

$$\frac{d}{dt}v_{Cf} = \frac{i_{L1} - i_{grid}}{C_f} \tag{2}$$

$$\frac{d}{dt}i_{L1} = \frac{v_{PV} - v_{Cf}}{L_1} \tag{3}$$

$$\frac{d}{dt}i_{L2} = \frac{v_{Cf} - v_{grid}}{L_2} \tag{4}$$

where:

$C \rightarrow$ The capacitance of the capacitor C
$C_f \rightarrow$ LCL Filter Capacitance
$L_1 \rightarrow$ The inductance of the filter inductor one
$L_2 \rightarrow$ The inductance of the filter inductor two
$i_{L1} \rightarrow$ The current of filter inductor one
$i_{L2} \rightarrow$ The current of filter inductor two
$i_{PV} \rightarrow$ The output current of the PV inverter
$i_{grid} \rightarrow$ The grid current
$v_C \rightarrow$ The voltage of the inverter capacitor
$v_{Cf} \rightarrow$ The voltage of the filter capacitor
$v_{PV} \rightarrow$ The voltage of the PV inverter before the LCL filter
$v_{grid} \rightarrow$ The grid voltage

Mode 2 (S_4 and S_5 are ON, and S_1, S_2, and S_3 are OFF). A zero voltage is produced in the output voltage V_{An}, this mode operates in the positive half-cycle of the output voltage. The state equations for this mode are (1), (2), (4) and:

$$\frac{d}{dt}i_{L1} = -\frac{v_{Cf}}{L_1} \tag{5}$$

Mode 3 (S_3 is ON, and S_1, S_2, S_4, and S_5 are OFF). The voltage for the negative half-cycle is generated in this mode, and the capacitor (C) provides the energy. In this mode, the PV module is disconnected. The state equations now are (2), (4) and:

$$\frac{d}{dt}v_C = \frac{i_{L1}}{C} \tag{6}$$

$$\frac{d}{dt}i_{L1} = -\frac{v_C + v_{Cf}}{L_1} \tag{7}$$

Mode 4 (S_2, S_4, and S_5 are ON, and S_1 and S_3 are OFF). Switches S_4 and S_5 generate a zero voltage in the output voltage V_{An}. while the capacitor (C) is charged through S_2. The capacitor charges in a short time, then the capacitor stops conducting current through it so that switches S_4 and S_5 are the only ones that remain active. This allows a reduction in conduction losses in the topology.

As in this stage the capacitor must be charged (mode 4), some non-idealities for the devices must be considered, adding in series to the capacitor C a resistance R_{eq} equivalent to the sum of all the parasitic resistances of each element. The equations for this mode are (2), (4), (5) and:

$$\frac{d}{dt}v_C = \frac{v_{PV} - v_D - v_C}{R_{eq}C} \tag{8}$$

where the equivalent resistance, R_{eq}, is described by:

$$R_{eq} = 3R_{DS(ON)} \tag{9}$$

where:

$v_D \rightarrow$ Diode forward voltage

$R_{DS(ON)} \rightarrow$ MOSFET on resistor

The four switching states of the proposed inverter are summarized in Table 1, along with other aspects related to the switching state.

Table 1. Switching states.

State	*Switching States*					*Voltages of Interest*	
	S_1	S_2	S_3	S_4	S_5	V_C [V]	*Inverter output [V]*
1	***ON***	*OFF*	*OFF*	*OFF*	*OFF*	*Without changes*	V_{PV}
2	*OFF*	*OFF*	*OFF*	***ON***	***ON***	*Without changes*	*Zero*
3	*OFF*	*OFF*	***ON***	*OFF*	*OFF*	*Discharge*	$-V_C = -V_{PV}$
4	*OFF*	***ON***	*OFF*	***ON***	***ON***	*Charge*	*Zero*

Since the topology has a four-quadrant switch (S_4 and S_5), it is necessary to carry out a commutation following the four-step rule, performing a combination of blanking times and overlapping times [25].

It is important to mention that a switching sequence must be followed during the transitions between switching states. This is since a four-quadrant switch is employed (S_4 and S_5). This depends on the operating mode, for example:

In the positive half cycle (R = 1), and a change from operation mode 1 ($P \neq Q$) to 2 ($P = Q$), follow the following switching sequence must be followed:

- At first S_4 = 1;
- Then S_1 = 0;
- To end S_5 = 1.

To change from operating mode 2 to mode 1, the sequence must be carried out in the opposite direction.

On the other hand, when the negative half-cycle (R = 0) happens, and a change from operating mode 3 ($P \neq Q$) to 4 ($P = Q$), the following switching sequence must be followed:

- Initially S_5 = 1;
- Then S_3 = 0;
- To end $S_2 = S_4$ = 1.

To change from operating mode 4 to mode 3, the sequence must be carried out in the opposite direction.

The sequence of the switches is illustrated below in Figure 5, all represented at a low frequency.

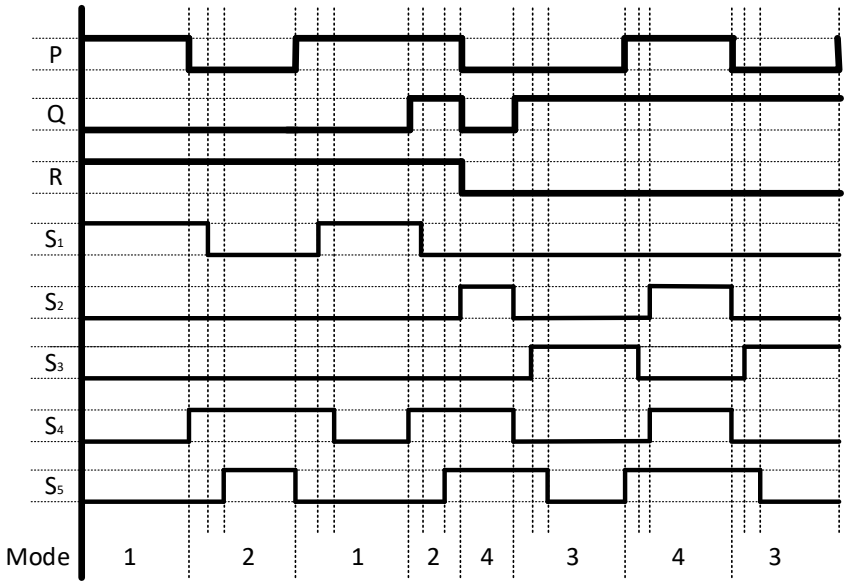

Figure 5. Waveforms with the four-step rule.

3. Topology Design

The design criteria for the different components of the converter are detailed in this section. To properly operate the topology, a unipolar SPWM modulation is carried out as already discussed in Section 2 [26–28]. Considering the above, we proceed to calculate the passive elements of the converter.

3.1. Capacitor C

It is desirable to have capacitor *C* as small as possible, but large enough to store energy and maintain a constant voltage to produce the negative level of the corresponding half-cycle. The positive half-cycle does not use the capacitor *C*.

The design was made considering the worst case, corresponding to a change from mode 3 to mode 4, in which the capacitor discharges for a longer time (Figure 6, in red).

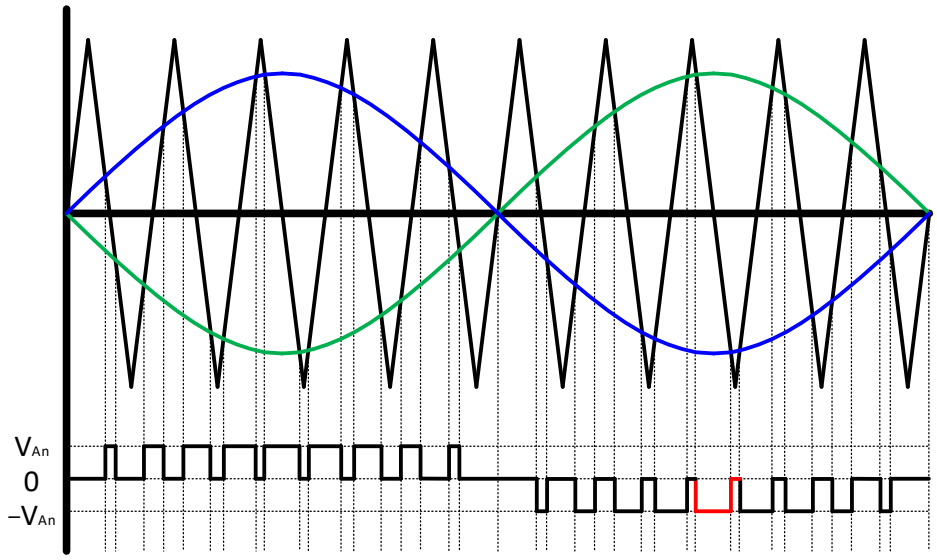

Figure 6. Double-frequency SPWM and V_{An} with worst-case for V_C.

The next equation determines the behavior of the capacitance, which is derived from Equation (6):

$$C_3 = \frac{i_{L1}\Delta t_3}{\Delta v_C} \tag{10}$$

where Δt_3 is the operating time of the mode 3 subcircuit.

Considering an RMS current of i_{L1} = 2.8 A, a modulation index of 0.75; a switching frequency of 30 kHz, and ΔV_C = 12 V (5% of V_C), results in capacitance of approximately of 5 µF.

3.2. LCL Filter

The LCL filter has the particularity of reducing the switching frequency ripple, having a good reduction of the total harmonic distortion (THD) and greatly reducing the emission of conducted electromagnetic interference (EMI) [29]. The LCL filter has better results in THD than an L or LC filter, as well as being of a smaller implementation volume and therefore a higher energy density, contributes to the useful life of the inverter, allowing a lower probability of failures in the devices in constant use [30].

For these reasons, the LCL filter has been chosen and has been designed to provide third-order filtering due to its 60 dB/decade attenuation. The filter ensures high power quality by eliminating voltage and current harmonics, which is composed of two inductors (L_{f1} and L_{f2}) and a capacitor (C_f); the resonance frequency (f_{res}) of the LCL filter is given as [31,32]:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_{f1} + L_{f2}}{L_{f1} \cdot L_{f2} \cdot C_f}} \tag{11}$$

The resonance frequency is selected between [30].

$$10 f_g < f_{res} < 0.5 f_s \tag{12}$$

where f_g is the system output frequency and f_s is the inverter switching frequency.

The base impedance (Z_b) and base capacitance (C_b) are expressed by [31,33]:

$$Z_b = \frac{{V_{orms}}^2}{P} \tag{13}$$

$$C_b = \frac{1}{2 \cdot \pi \cdot f_g \cdot Z_b} \tag{14}$$

where V_{orms} is the root mean square (RMS) of the system output voltage (V_{grid}).

The filter capacitor is calculated with:

$$C_f \leq 0.05 C_b \tag{15}$$

The first inductor is given by [33]:

$$L_{f1} = \frac{V_{PV}}{6 \cdot f_s \cdot \Delta I_{\max}} \tag{16}$$

where V_{PV} is the inverter input voltage.

The maximum current ripple ($\Delta I_{\max}$) of the output inverter is obtained with:

$$\Delta I_{\max} = 0.1 \frac{P\sqrt{2}}{V_{orms}} \tag{17}$$

The second inductor is expressed by:

$$L_{f2} = 0.6 \cdot L_{f1} \tag{18}$$

The designed LCL filter parameters are given in Table 2.

Table 2. Filter Parameters.

System Parameter	Values
System output frequency, f_g	60 Hz
Inverter switching frequency, f_s	30 kHz
Inverter input voltage DC, V_{PV}	240 V
System output voltage (RMS), V_{orms}	170 V
System Power, P	700 W
LCL filter and Internal Capacitor	**Values**
Internal capacitor, C	5 µF
Inverter side inductor, L_{f1}	2.36 mH
Load side inductor, L_{f2}	1.42 mH
Filter capacitance, C_f	3.13 µF
Cut off frequency, f_{res}	3 kHz

3.3. Semiconductors and Sensors

According to the values of Table 2, the MUR860 was chosen as the power diode for its peak voltage and peak current values, 600 V and 16 A respectively, fast recovery time (75 ns), and low forward voltage (1.5 V) [34].

C3M0065090D was chosen as silicon carbide (SiC) MOSFET, which has a drain-source voltage of 900 V, a maximum gate-source voltage of 15 V, a drain current of 36 A, a drain-source on-state resistance of 65 mΩ, and a rise and fall time of 11 ns and 9 ns respectively [35].

The current sensor used is the LA 25-NP, which is a hall effect sensor that operates using a variable transformer depending on the configuration of its pins [36].

The voltage sensor used is the LV 25-P, which is also a hall effect sensor that senses the voltage through a current relationship using Ohm's law. An external resistor is necessary to obtain a nominal current of 10 mA [37].

Both sensors need a current to voltage conversion stage because the transducer output is in current. After that, a conditioning stage is used, which is recommended to match impedances with the following stage, which usually is the digital stage.

4. Control Strategy

In this section, the controller employed is described in detail. A current control loop is employed, but also other circuitries.

4.1. Combinational Logic Circuit

As mentioned in Section 2.1, a unipolar SPWM was used, where two symmetrical sinusoidal signals are compared against a triangular carrier signal, as illustrated in Figure 3. When comparing the blue sinusoidal signal of Figure 3 against the triangular signal, control signal P is obtained; while comparing the symmetrical sinusoidal signal (the red one in Figure 3) against the triangular signal, results in the control signal Q. The control signal R indicates the polarity of the positive and negative half-cycle of the sinusoidal signal.

A combinational logic circuit is employed to determine the activating signals of the switches. The truth tables for each switch are shown in Figure 7.

R	P Q: 00	01	11	10
0	0	0	0	0
1	0	0	0	1

(**a**)

R	P Q: 00	01	11	10
0	1	0	1	0
1	0	0	0	0

(**b**)

R	P Q: 00	01	11	10
0	0	1	0	0
1	0	0	0	0

(**c**)

R	P Q: 00	01	11	10
0	1	0	1	0
1	1	0	1	0

(**d**)

Figure 7. Truth table of the control signals of the switches (**a**) switching logic for S1: $S_1 = P\overline{Q}R$; (**b**) switching logic for S_2: $S_2 = \overline{R}\left(PQ + \overline{PQ}\right)$; (**c**) switching logic for S_3: $S_3 = \overline{P}Q\overline{R}$; (**d**) switching logic for S_4 and S_5: $S_4 = PQ + \overline{PQ}$.

4.2. Controller Stage

The control strategy employed is a Proportional-Resonant (PR) [38], as shown in Figure 8. The proportional-resonant (PR) controller is widely used in grid-connected voltage-source converters [39] because it offers good accuracy and a considerably fast speed when tracking sinusoidal signals in steady state compared to other control strategies [40].

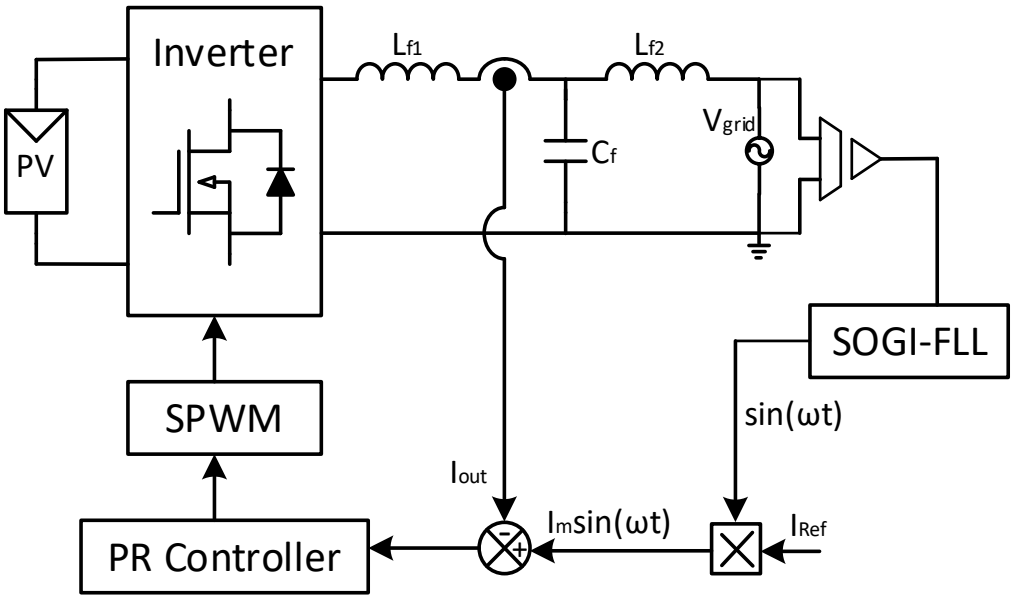

Figure 8. Control diagram for the inverter topology.

This PR controller must be synchronized with the AC grid, which is achieved using a SOGI-FLL. Its dynamic response depends mainly on an appropriate selection of the parameters p and k, where p is the FLL gain and k is the SOGI gain [41]. The block diagram of the SOGI-FLL controller is shown in Figure 9.

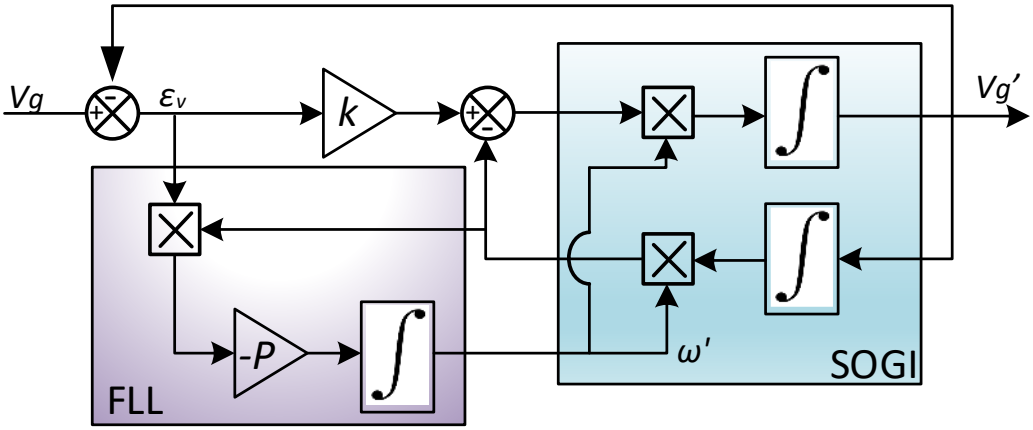

Figure 9. Block diagram of SOGI-FLL controller.

The proposed values for k and p were 2 and 1, respectively.

On the other hand, the transfer function of the proportional-resonant (PR) controller is:

$$H_{PR} = K_p + \frac{K_i s}{s^2 + \omega_0{}^2} \tag{19}$$

Equation (19) can be seen to be an ideal PR controller which achieves infinite gain at the AC frequency $\omega_{0,}$ where $\omega_0 = 2\pi f_g$ is the resonant frequency and K_p and K_i represent proportional and resonant gains respectively. K_p mainly determines the bandwidth and the phase and gain margins of the system, while K_i can be tuned for shifting the magnitude response vertically [42]. The block diagram of the PR controller loop is shown in Figure 10. In this case, the value for ω_0 = es 376.9911 rad/s, for K_p and K_i are equal to 1.2 and 22, respectively.

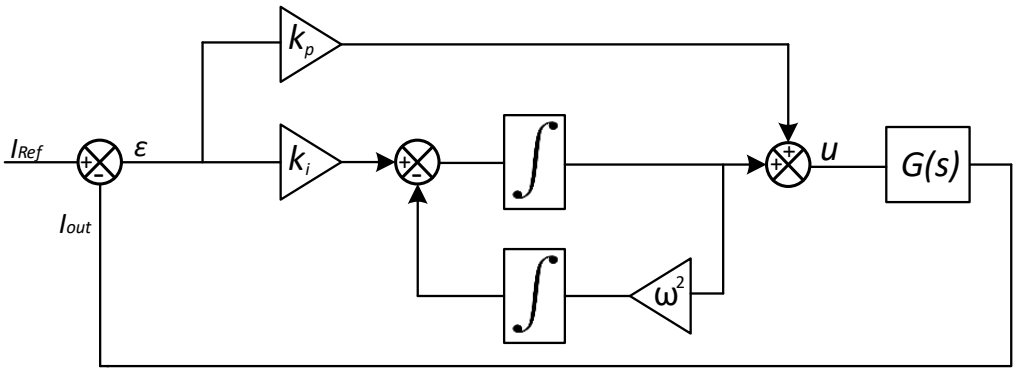

Figure 10. Block diagram of PR controller.

Output current and voltage are obtained by the LA25-NP and LV25-P sensors, respectively, as mentioned in Section 3.3, which provide the necessary signals for the SOGI-FLL control as well as the PR control.

The SOGI-FLL control as the PR control has been programmed in the LabView 2015b platform, and downloaded in the National Instrument GPIC board hardware, which has a sampling frequency of 100,000 samples per second.

This limits the execution time of each block to 10µs, having an integration step of 0.0037699s for each integral within the SOGI-FLL controller and the PR controller.

5. Simulated and Experimental Results

To verify the operation of the controller and topology, PSIM simulations were made and an experimental prototype was built. Several tests were carried out. Parameters for

the simulation and experimental system are shown in Table 3. The photograph of the experimental prototype is shown in Figure 11.

Table 3. Parameters used for the simulation of the proposed topology.

System Parameter	Values
System output frequency, f_g	60 Hz
Inverter switching frequency, f_s	30 kHz
Inverter input voltage DC, V_{PV}	240 V
System output voltage (RMS), V_{orms}	170 V
System Power, P	300 W
LCL filter and Internal Capacitor	**Values**
Internal capacitor, C	5 µF
Inverter side inductor, L_{f1}	2.36 mH
Load side inductor, L_{f2}	1.42 mH
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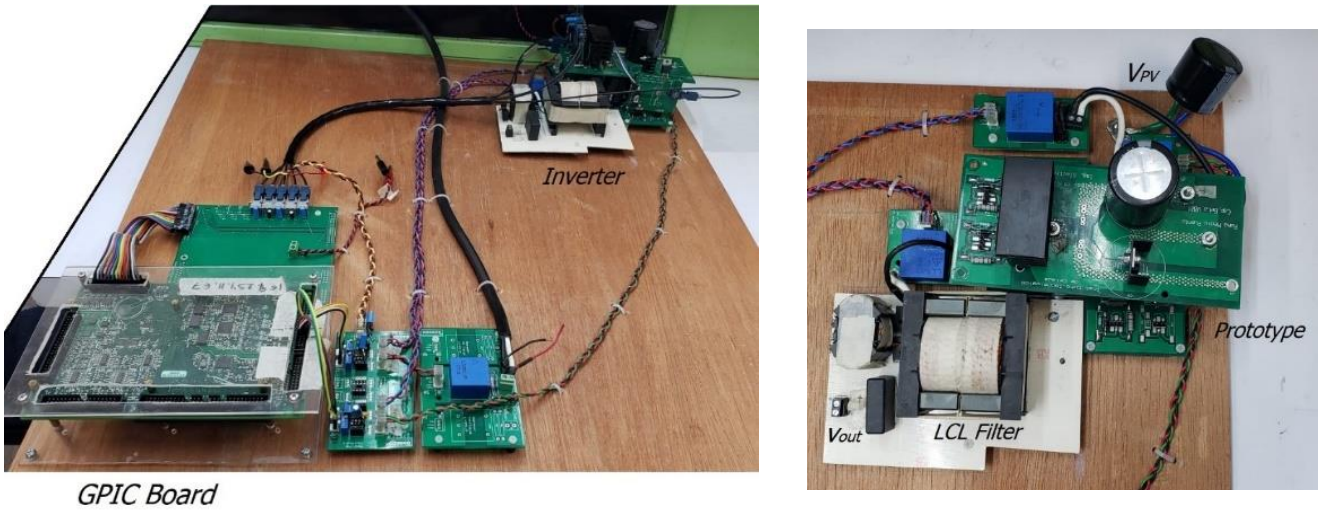

(**a**) (**b**)

Figure 11. Experimental setup for the proposed inverter. (**a**) Inverter with measurement equipment and GPIC board, (**b**) inverter with LCL filter.

For the experiments, the AC grid was replaced by a programmable AC Source Agilent 6812B, and the PV was replaced by a PV panel simulator Keysight N8937 APV. The equivalent parasitic capacitor between the negative terminal of the DC bus and the ground was replaced by an external capacitor. As mentioned in the previous section, the controller was implemented in a National Instrument GPIC board which can be seen in Figure 11a.

All the tests were carried out over 1 year in which the topology was operating daily for a minimum of 1 h and a maximum of 3 h without presenting any problem in its operation.

The first test was to obtain the steady-state waveforms. The voltage and current signals after the LCL filter are obtained, as well as the signal V_{An}. As it can be observed, all signals are in phase with V_{grid}. This is illustrated in Figure 12a,b, for simulation and experimental results, respectively.

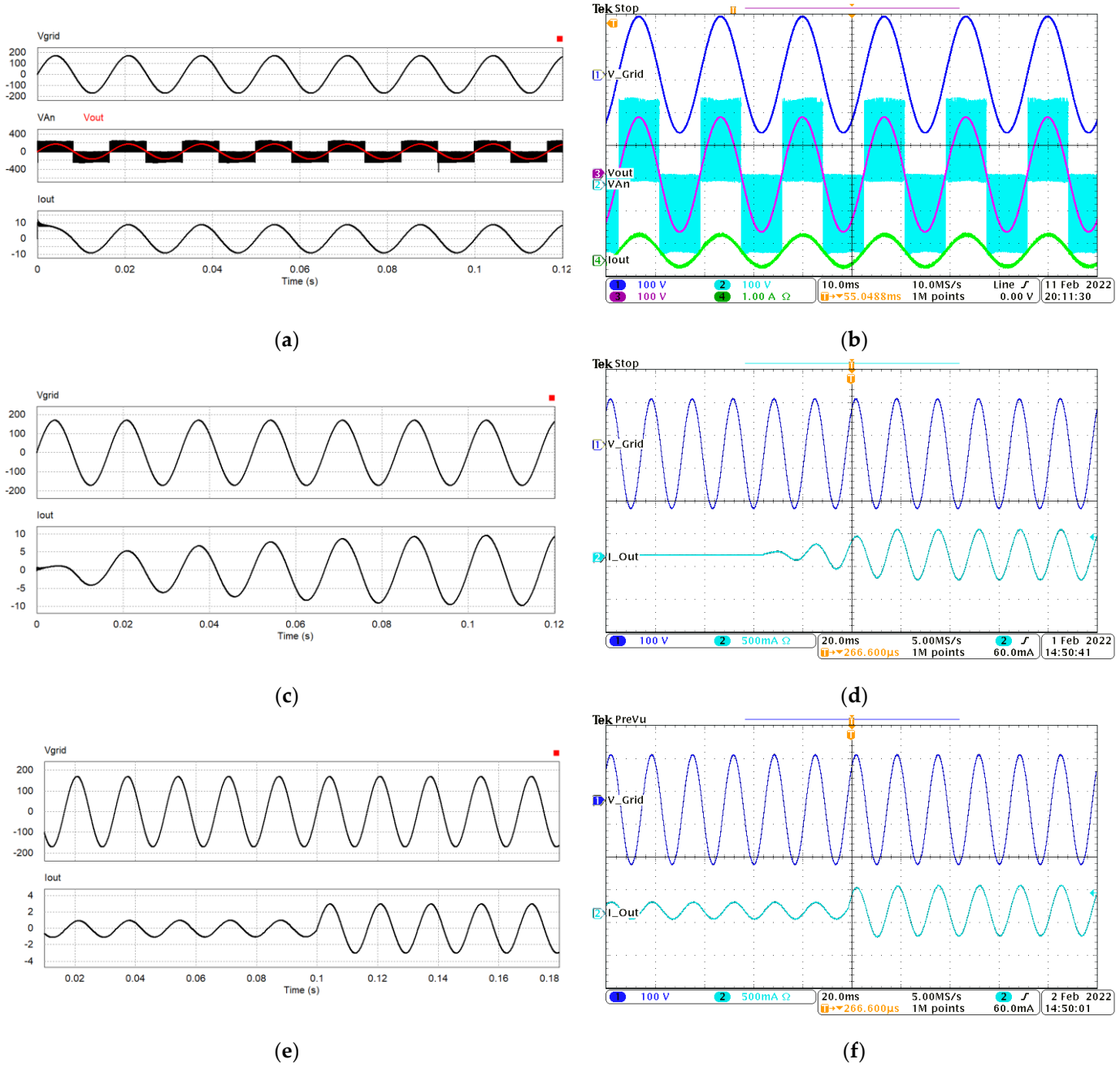

Figure 12. Simulated and experimental results. (**a**) Simulated waveforms V_{grid}, V_{An}, $V_{out,}$ and i_{out}. (**b**) Experimental waveforms V_{grid}, V_{An}, V_{out}, and i_{out}. (**c**) Simulated waveforms V_{grid} and i_{out}. (**d**) Experimental waveforms V_{grid}, and i_{out}. (**e**) Simulated waveforms V_{out} and i_{out}. (**f**) Experimental waveforms V_{out} and i_{out}.

The second test illustrates the implemented soft start. It is graphed the output current and the grid voltage. It can be observed that around three cycles were taken to reach the steady state, once it started the system. This is observed in Figure 12c,d, for simulation and experimental results, respectively.

As the third test, an amplitude variation of the current reference was made. As can be observed in Figure 12e,f (simulation and experiment, respectively), the system has a good dynamic response.

As a fourth test, the inverter was tested with an RL load of 50 Ω and 50 mH, given by Chroma programmable AC/DC Electronic Load model 63802, the output voltage and current signal are illustrated below in Figure 13, it is clear that there is a phase lag

between the signals generating reactive power, the converter operates properly and no effect on it appears.

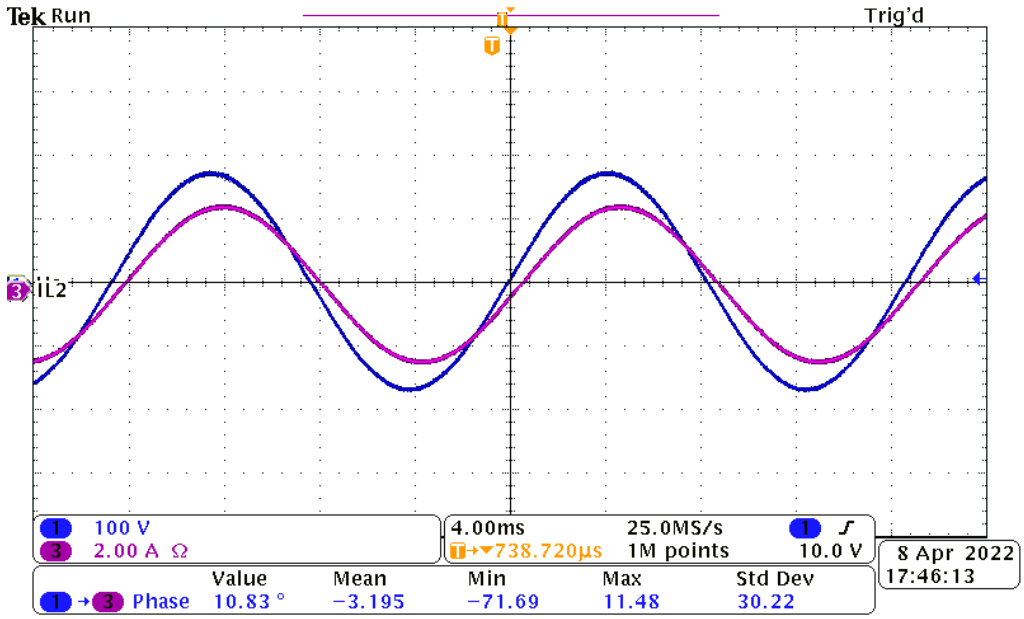

Figure 13. Output voltage and current signals under inductive load.

In Figure 14, the V_{An} signal and the measured leakage current are illustrated. One can observe that the current is less than 10 mA, fully complying with the VDE 0126-1-1 standard, which indicates that the leakage current must be less than 300 mA.

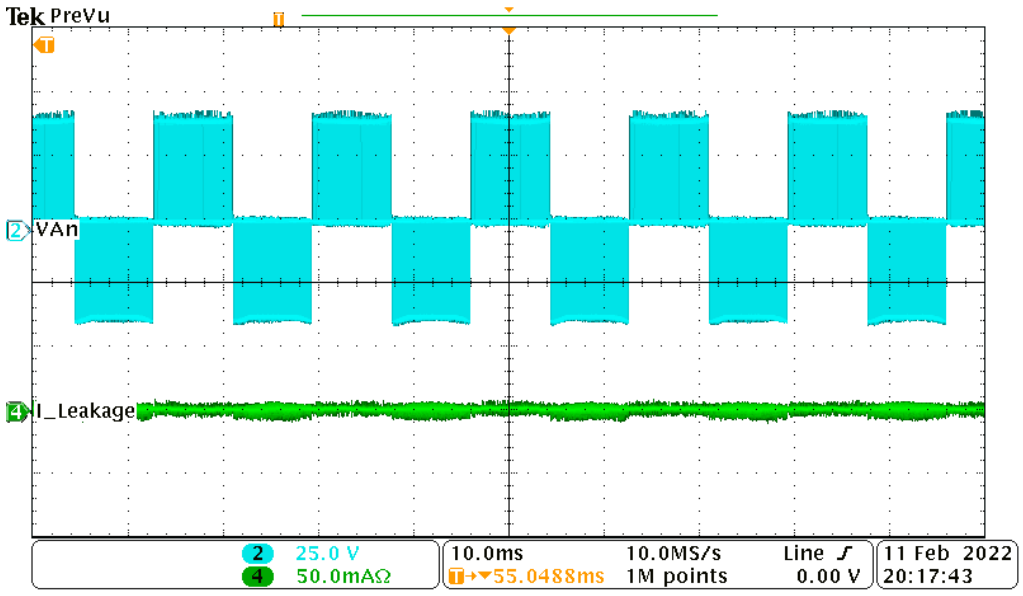

Figure 14. V_{An} and Leakage current.

Once these tests were carried out, the efficiency and the THD at different powers were obtained. Maximum efficiency of 98.2% was achieved at the nominal power of 300 W. However, a sweep of efficiencies was carried out at different percentages of power with respect to the nominal power that allows us to calculate the CEC and EE efficiencies [14,43],

through the Equations (20) and (21), which are 96.973% and 96.227%, respectively. All efficiencies were obtained using Chroma Digital Power Meter 66,204 device.

$$Ef_{EE} = 0.03Ef_{5\%} + 0.06Ef_{10\%} + 0.13Ef_{20\%} + 0.1Ef_{30\%} + 0.48Ef_{50\%} + 0.2Ef_{100\%} \quad (20)$$

$$Ef_{EE} = 0.04Ef_{10\%} + 0.05Ef_{20\%} + 0.12Ef_{30\%} + 0.21Ef_{50\%} + 0.53Ef_{75\%} + 0.05Ef_{100\%} \quad (21)$$

where the percentage that each efficiency has corresponds to the value of the efficiency obtained at that percentage of the power with respect to the nominal value of power [44].

THD measurements of the output current of the topology were made also at different powers using a Fluke1735 device, the same as in the analysis of efficiencies, the THD at 300 W resulted in a THD value of 0.1%, while in the worst of the conditions at 15 W with a value of 0.9% was obtained, in all cases the THD value measured is lower than the IEEE 1547 standard [45]. Figure 15 illustrates the efficiency and the THD.

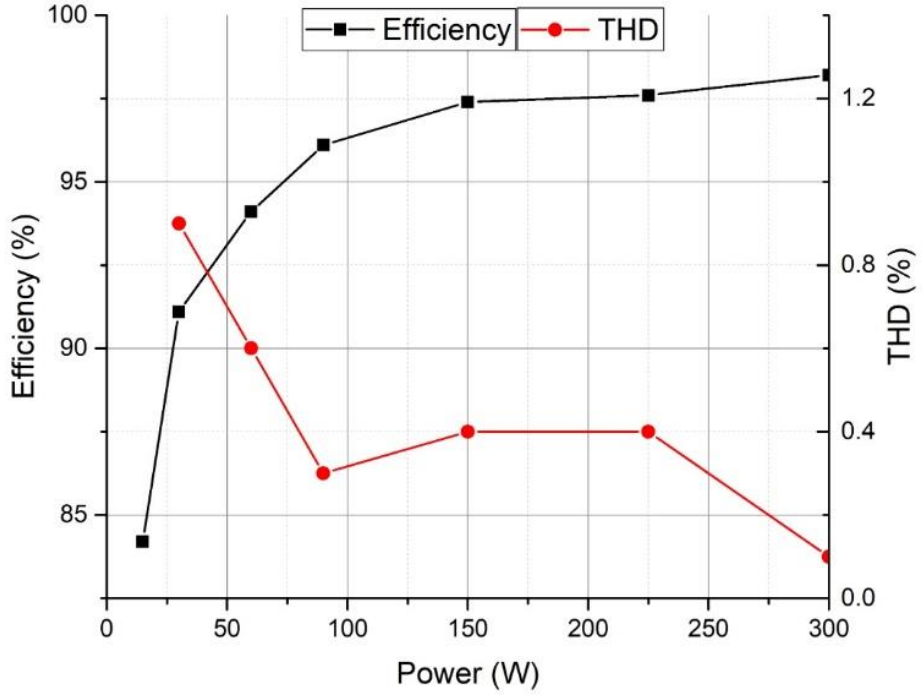

Figure 15. Steady-state performance: efficiency and THD.

The useful life of the system will depend on the useful life of each element separately, which are affected by different factors, such as the environment where it operates, the temperature, the implementation and operation parameters [46]. The devices that present the highest percentage of failures found in the proposed topology are MOSFETs, followed by diodes [30,46]. Table 4 shows the percentage of failures in 1000 h of use for the various elements [47]:

Table 4. Some typical component failure rates (% per 1000 h).

Component	% per 1000 h
Capacitors	0.01
Inductors	0.05
Transistors	0.01–0.1
Diodes	0.05

The useful life of an inverter varies depending on the factors mentioned, as well as the number of elements that the topology contains and the stress to which they are subjected, and to a large extent the THD that the topology presents. In general, the useful life of

the inverter system can be guaranteed in 10^6 h, where the active components (MOSFETs) feature the highest failure probability among the elements in the topology [46].

Based on this, temperature measurements in degrees Celsius were made on the components within the topology every minute for 1 h, when temperatures have already stabilized (Figure 16). The converter was operating at 300 W.

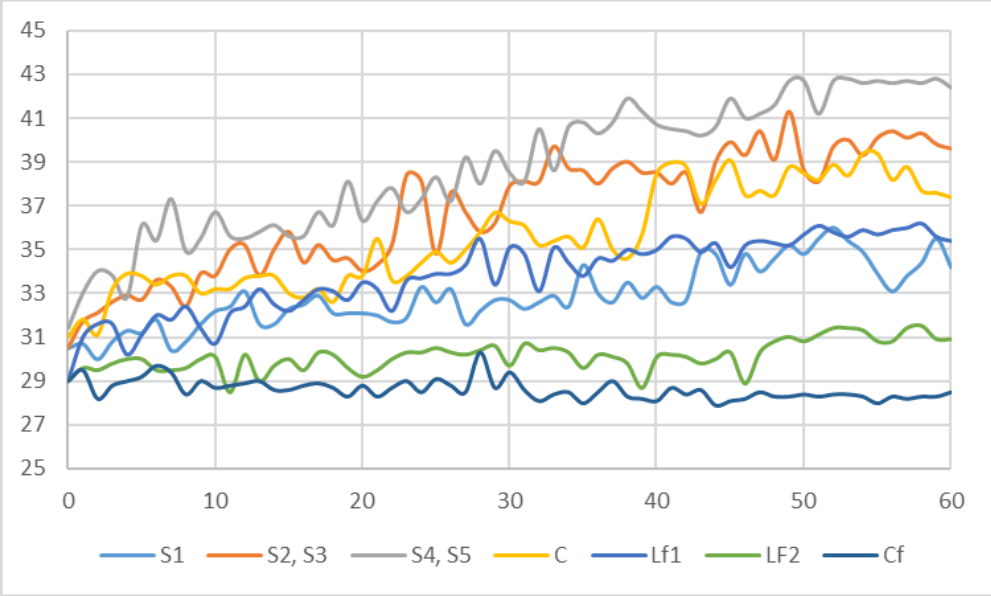

Figure 16. Temperature of each component as a function of time (min).

The temperature measurement was carried out on each of the devices utilizing digital thermometers. The average, minimum, and maximum increase of the temperature value of each device is shown below in Table 5, with which, in support of Figure 16, it can be concluded that the device that could present failures first would be MOSFETs S_4 and S_5.

Table 5. Average, maximum, and minimum temperature in degrees Celsius.

	Average	Maximum	Minimum	Increase
S_1	32.89	36	30	6
S_2, S_3	36.82	41.3	30.5	10.8
S_4, S_5	38.75	42.8	31.4	11.4
C	35.57	39.4	31	8.4
L_{f1}	33.85	36.2	29	7.2
L_{f2}	30.14	31.5	28.5	3
C_f	28.62	30.3	27.9	2.4

It must be considered that these temperatures contemplate the temperature of the environment at the moment of being measured, which at the beginning of the measurement was 29 °C and at the end of the test it was 26 °C.

6. Comparison with Other Schemes

Several characteristics of the converter have been compared with other topologies (Table 6), where, in addition to comparing in terms of efficiency, THD and leakage current, the number of devices used has also been compared; these include semiconductor devices and also internal passive devices in each inverter, and the elements that are used in the proposed filter in each topology, since they directly affect the THD, the efficiency and the lifetime of each one of them.

Table 6. Comparison with other schemes.

Topology	Semiconductor Devices		Passive Elements		Filter		Semiconductors Operating at the Same Time		Leakage Current [mA]	Maximum Efficiency [%]	THD [%]
	Switches	Diodes	C	L	C	L	Minimum	Maximum			
Proposed inverter	5	1	1	0	1	2	1	3	≈0	98.2 @ 300 VA	0.1
HBVS [7]	5	1	1	2	1	2	3	3	<77	94.5 @ 1 kVA	11.6
H6 DC side [14]	6	0	2	0	1	2	2	4	<200	95.9 @ 300 VA	2.54
CH6 [15]	6	0	0	2	1	2	2	3	<140	NM @ 720 VA	3.77
Topology in [16]	5	0	2	1	1	1	2	2	≈0	92.5 @ 200 VA	–
qZSI Modified [17]	6	3	2	2	1	2	3	7	≈0	91.4 @ 500 kVA	6.2
Heric parallel AC switch [18]	6	2	0	0	1	2	2	2	<20	98.7% @ 9 kVA	–
Heric back-to-back [18]	6	0	0	0	1	2	2	2	<20	97.5%@ 9 kVA	–
H5 [18]	5	0	0	0	1	2	2	3	<35	98.1 @ 300 VA	–
H6 [18]	6	2	0	0	1	2	2	4	<40	96.35 @ 200 VA	–
Hybrid bridge [19]	6	2	1	0	1	2	2	3	<17.4	94.75 @ 1 kVA	–
H5-D [20]	5	1	2	0	0	2	3	3	≈60	96 @ 650 VA	–
S4 Topology [21]	4	2	3	0	1	1	1	3	≈0	97.2 @ 500 VA	2.1
Inverter in [22]	5	1	1	1	1	1	1	3	≈0	–	0.14

In terms of efficiency, a good value is achieved. The efficiency depends on the switching and conduction losses. This proposal has low conduction losses due to the reduction of active semiconductors in each operation mode. A single semiconductor is turned on in two of the operating modes. In Table 6 the number of semiconductors operating at the same time for each topology is indicated. The proposed topology, as in [21,22], only uses one semiconductor used in an operation mode, while the others consider more elements, penalizing efficiency, except for the HERIC parallel AC switch topology [18] which presents better efficiency. However, the analyzed topology is expected to improve its efficiency at higher power, matching or surpassing also the HERIC parallel AC switch topology [18]. It is worth mentioning that [18] is a review with the maximum efficiency reported for each topology so far according to the reference.

In addition, a low THD was obtained compared to other topologies.

The leakage current was also considered. Considering that this proposal is a common mode converter, the leakage current is close to zero. Not all the topologies eliminate it, some of them only reduce it, as is the case of [7,14,15,18–20]. All the topologies presented in [17] do not manage to eliminate the leakage current in its entirety.

Regarding the number of semiconductor devices, only the topology presented in [16] and the H5 topology [18] use fewer components than the proposed topology. However, the topology in [16] has one extra passive element. The topologies in [7,14,15,20–22] have the same number of semiconductors, however, the number of passive elements in each of them is greater than in the proposed topology, except [22]. However, that work does not address many details concerning the analysis and calculation of the elements, and no experiments were provided. The topologies reported in [17,19] have a higher number of semiconductors than the proposed topology.

The main difference with [22] is the filter used, which improves the results obtained by reducing THD and EMI, which would extend the life of the system, and a better power density is obtained.

7. Conclusions

A topology for transformerless PV inverters is analyzed and experimentally evaluated in this paper, which can effectively suppress the leakage current, but also have high

efficiency due to the reduced conduction losses. The topology comprises five switches and a diode, with only one semiconductor operating during two of the operating modes. The LCL output filter increases efficiency, lifetime, THD and EMI reduction of the converter.

The results obtained verify the operation of the topology, where a zero-leakage current is measured, complying with the VDE 0126-1-1 standard where it must be less than 300 mA.

An efficiency study was performed, having a maximum efficiency of 98.2% at a power of 300 VA. In the same way, a very low THD was obtained, 0.1% in the best of cases and 0.9% for the worst.

A temperature measurement of the devices used in the implementation over an hour of operation without interruptions at nominal value was made, as well as an estimation of failures for the useful life of the system was given.

Simulation and experimental results allow validating the operation of the converter and the controller, resulting in a good choice for single-phase transformerless PV inverters due to its simplicity and practicality.

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