energies

MDPI

Article

A Reconfigurable Fault-Tolerant PV Inverter via Integrating HERIC and H5 Topologies

Hossein Khoun Jahan [1], Nima Abdolmaleki [2], Mohammad Ahmadpour [1], Jianfei Chen [3], Caisheng Wang [2,*], Mehdi Abapour [1] and Frede Blaabjerg [4]

[1] Electrical and Computer Engineering Department, University of Tabriz, Tabriz 51666, Iran; hosseinkhounjahan@yahoo.com (H.K.J.); mahmadpour@tabrizu.ac.ir (M.A.); abapour@tabrizu.ac.ir (M.A.)
[2] Electrical and Computer Engineering Department, Wayne State University, Detroit, MI 48202, USA; nima.maleki@wayne.edu
[3] School of Electrical Engineering and Automation, Wuhan University, Wuhan 430072, China; jianfei@whu.edu.cn
[4] Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark; fbl@et.aau.dk
* Correspondence: cwang@wayne.edu

Abstract: Solar energy is prevalent in many applications, therefore, the reliability of solar energy systems has become an important topic for research communities and industry. High reliability and fault-tolerant capability are particularly vital for the solar energy systems that are mission-critical and/or inaccessible to affordable maintenance. In order to enhance the reliability of a grid-tied PV system, a fault-tolerant Photovoltaic (PV) inverter, termed Integrated Fault-Tolerant PV Inverter (IFTPVI), is proposed in this paper. The IFTPVI is based on the Highly Efficient and Reliable Inverter Concept (HERIC) and H5 inverters that are both popular and commercialized transformerless inverters in grid-tied PV applications. The IFTPVI can tolerate both open-circuit (OC) and short-circuit (SC) faults while maintaining the same voltage and current levels. The system description, reliability analysis, simulation in Matlab/Simulink 2018, and experimental results are provided to verify the feasibility and viability of the proposed inverter topology.

Keywords: PV inverter; fault-tolerant; reconfiguration; grid-tied PV system; open-and-short-circuit faults

Citation: Khoun Jahan, H.; Abdolmaleki, N.; Ahmadpour, M.; Chen, J.; Wang, C.; Abapour, M.; Blaabjerg, F. A Reconfigurable Fault-Tolerant PV Inverter via Integrating HERIC and H5 Topologies. *Energies* **2022**, *15*, 3403. https://doi.org/10.3390/en15093403

Academic Editors: Federico Barrero and Rui Esteves Araújo

Received: 10 March 2022
Accepted: 29 April 2022
Published: 6 May 2022

1. Introduction

Renewable energy systems such as solar and wind energy systems have been increasing rapidly in both industry and residential applications worldwide. Among the renewable energy systems, PV based energy generation systems stand out for being clean and quiet without rotating parts and having a reliable operation. The International Energy Agency-Photovoltaic Power Systems Program (IEA-PVPS) 2021 report shows that global PV capacity reached a milestone of 200 GW in 2015. Approximately, 140 GW of PV systems have been installed in 2020, and the total worldwide PV capacity by the end of 2020 reached well above 750 GW [1]. The records suggest that solar energy exploitation has been increasing remarkably in recent years.

PV systems require inverters to interface the PV panels to the loads and/or the grid. The PV inverters are categorized into isolated and non-isolated types. Isolated inverters use transformers in dc and/or ac sides to provide galvanic isolation, so they block the leakage current in the panel, avoid voltage shock, and guarantee the safety. However, non-isolated transformerless inverters are at the center of attention in residential and medium power applications as they offer higher power densities and efficiency as well as lower weight and cost [2–7]. The Voltage Source Inverters (VSIs) are most attractive compared to their Current-Source counterparts due to better power densities, efficiency, and lower cost [8]. Numerous single-phase transformerless inverters for PV applications have been introduced in the literature, and efforts have been made to catalog and review these topologies [8–12].

The improvements in size, weight, and cost that transformerless PV inverters provide come at the cost of losing isolation and suffering from higher common-mode currents in the system. A group of transformerless PV inverters, categorized as H-bridge-based in [8], imitate isolated inverters to some degrees and provide partial isolation through decoupling the dc side from the ac side by the use of switches. The HERIC and H5 inverters are two examples of this family and have been successfully commercialized [13,14]. The HERIC and H5, respectively, use two switches on the ac side and one switch on the dc side to decouple the dc side from the ac side during a zero-voltage state. This decoupling prevents the current flow to the dc side during the current freewheeling period and effectively reduces the common-mode current, electromagnetic interference (EMI), total harmonic distortion (THD), and the output filter size.

High reliability and fault-tolerant capability are important for mission-critical PV systems such as those on a space station and for the applications that have no access to affordable maintenance. For example, the need for highly reliable power converters in remote areas is pressing, since a fault in these systems may result in highly expensive or catastrophic system malfunctions. Therefore, the reliability in such applications is given a much higher priority than the overall cost of the system [15] as the maintenance might prove to be difficult to carry out, if not impossible. Even though faults might occur in both PV arrays and inverters, it is reported in the literature that inverters are the most prone-to-failure parts of PV systems [16,17]. For instance, the Mean Time Between Repairs (MTBR) is guaranteed to be more than 20 years for modern PV arrays, while this parameter can drop as low as 2 years for an inverter [18,19]. Consequently, a number of fault-tolerant PV inverter topologies have been developed in the literature as efforts to mitigate the reliability concerns associated with PV systems [18,20–25]. A spare-inverter approach was proposed for multi-inverter systems so that the additional inverter can replace the faulty inverter until it is repaired [18]. This method, while applicable to multi-inverter PV systems, may not be very efficient when the PV system only consists of a single inverter as it significantly increases the costs of power converter implementation. The issue of using spare inverter versus using a fault-tolerant inverter to enhance reliability needs further investigation that is out of the scope of the present work. The method presented in [20] adds four TRIACs to an H-bridge in order to provide it with fault tolerance and reconfiguration capabilities. The use of TRIACs adds to the complexity of driver circuits, and their low immunity to dv/dt calls for additional dv/dt filter, which increases the cost and size of the circuit. There are also fault-tolerant methods for multilevel PV inverters that are not applicable to two or three-level single-phase PV inverter systems [21–25]. Hence, there is still a great need for studying fault-tolerant PV inverters to further enhance reliability and alleviate common-mode currents. The common-mode current in grid-tied PV systems has a direct relation with the capacitance of the stray capacitor of the PV panel and switching frequency [26,27].

To address this challenge, a new single-phase fault-tolerant PV inverter is proposed in this paper. The proposed inverter, called Integrated Fault-tolerant PV Inverter (IFTPVI), uses a redundant switch-leg, a fault-managing unit (FMU), and three electromechanical relays. In normal operation, the IFTPVI is in the form of a HERIC inverter. Under a faulty condition, the redundant switch-leg replaces the faulty switch-leg. If the bidirectional switch fails, the IFTPVI is reconfigured, and it takes the shape of an H5. All the mentioned actions are handled by electromechanical relays.

The rest of this paper is organized as follows: the configuration of the proposed inverter is defined in Section 2 where the healthy and faulty conditions are discussed in detail. The fault diagnosis and elimination algorithm are given in Section 3, which also illustrates different parts of the proposed fault tolerant structure. The reliability evaluation and Mean Time to Failure (MTTF) analysis are provided in Section 4. In this section, the reliabilities and the MTTFs of the HERIC, H5 and the proposed inverter are thoroughly investigated. The numerical results and comparisons for reliability and MTTF analysis are

given in Section 5, and the simulation and experimental results are provided in Section 6. Finally, the overall work is concluded in Section 7.

2. Topology and Operation Principle of the IFTPVI

2.1. The HERIC and H5 Inverter Topologies

Since the IFTPVI is implemented through the integration of the HERIC and H5 inverters, the topologies of these two inverters are displayed in Figure 1a,b for quick reference. As shown in Figure 1a, the HERIC decouples the ac and dc sides during the zero-voltage state by opening the four switches in the H-bridge and closing S_b. The H5 achieves the same goal by opening S_5 and closing the upper or lower switches in H-bridge during a zero-voltage state.

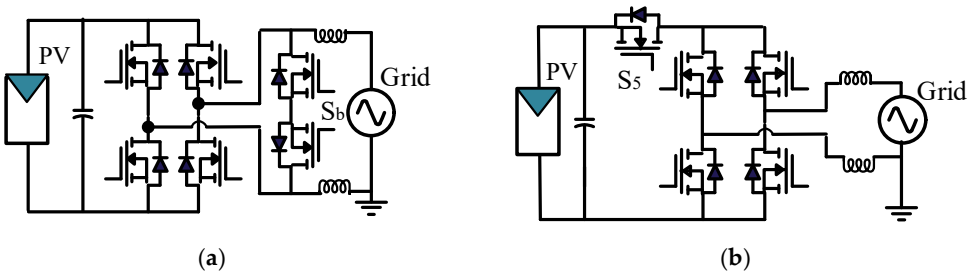


Figure 1. Conventional grid-connected PV inverters (**a**) HERIC [15] (**b**) H5 [16].

2.2. The Proposed Fault-Tolerant PV Inverter Topology

The proposed fault-tolerant PV inverter is shown in Figure 2. In this topology, one reserve switch-leg (Leg_R), which is synthesized using two semiconductor switches (S_{r1} and S_{r2}), and three electromechanical relays (R_1, R_2, and R_3) are used to provide the HERIC inverter with the fault-tolerance and reconfiguration abilities in case of Short-Circuit (SC) and Open-Circuit (OC) faults. The FMU is used to diagnose the fault and drive the relays to reconfigure the inverter. As shown in Figure 2, each relay has two metal-ware contacts that are used to remove the faulty part and insert the reserve part into the circuit. Different operation modes are described in the forthcoming subsections. For more clarity of discussion in these subsections, some of the labels shown in Figure 2 are not displayed in Figures 3–5.

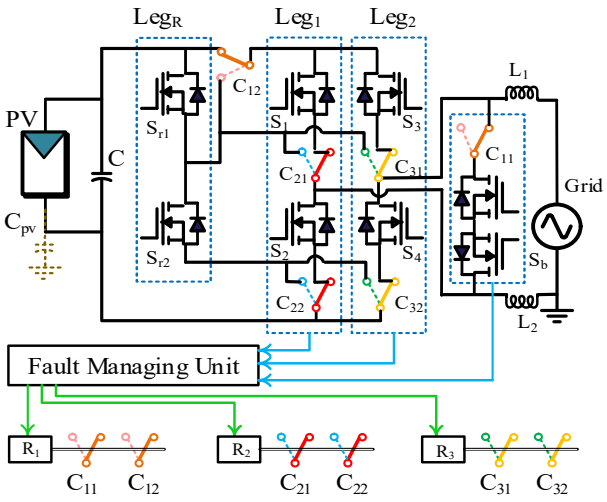


Figure 2. The proposed integrated fault tolerant PV inverter (IFTPVI).

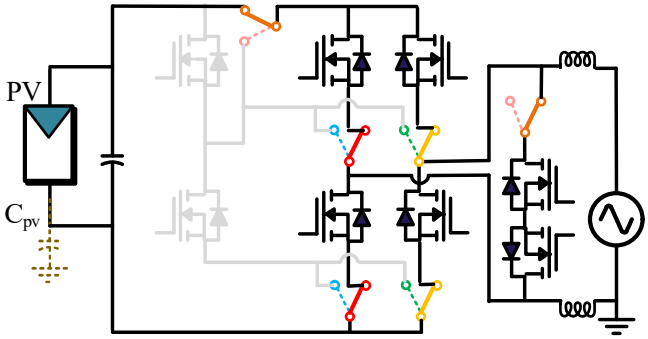
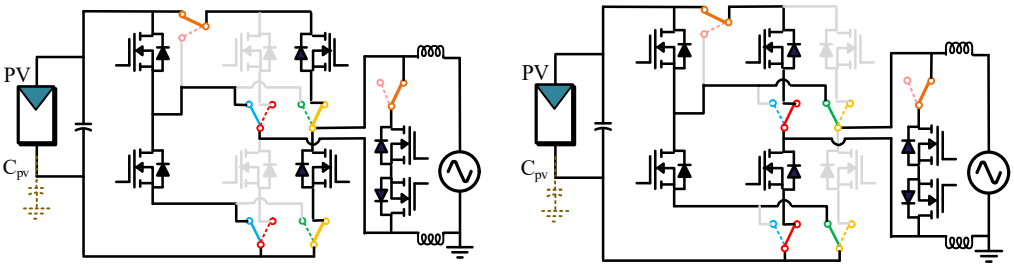


Figure 3. Configuration in the healthy mode of the IFTPVI.



(**a**) (**b**)

Figure 4. Configuration after a fault in one of the legs. (**a**) Configuration after a fault in Leg_1, and (**b**) configuration after a fault in Leg_2.

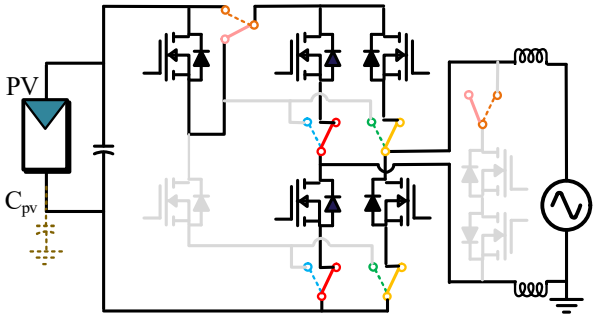


Figure 5. Configuration after a fault in S_b.

2.3. Healthy Operation Mode

Assuming the initial condition to be a healthy mode, the converter operates as a HERIC inverter, which is shown in Figure 3. In the healthy mode, the reserve switch-leg is inactive. While operating as the HERIC inverter, a bidirectional switch (S_b) is used to create the zero-voltage state at the output to reduce dv/dt, EMI, power losses, and filter size. During the zero-voltage state, the dc and ac sides are decoupled through S_1, S_2, S_3, and S_4 to reduce the common-mode current.

2.4. Faulty Modes

The faulty mode begins once a short-circuit or open-circuit fault is detected through the FMU. If the fault occurs in one of the switch-legs (Leg_1 or Leg_2 in Figure 2), depending on the location of the faulty switch, the corresponding relay (R_2 for Leg_1 and R_3 for Leg_2) contacts disconnect the faulty leg and replace it with the reserve leg so that the inverter resumes operation as a HERIC inverter with the same input and output characteristics. Figure 4a shows the reconfiguration of the proposed inverter before and after a fault in Leg_1. Similarly, Figure 4b shows the configuration after a fault in Leg_2.

In the case that the fault occurs in the bidirectional switch (S_b), relay R_1 will be activated so that S_b is disconnected from the circuit and S_{r1} joins the circuit. In other words, the inverter is reassembled as an H5 inverter in this condition, as displayed in Figure 5. While operating in the H5 mode, S_{r1} decouples the dc side from the ac side under the zero-voltage state to mitigate the common-mode current. While the efficiency might be slightly lower, the inverter would still be able to maintain the same operating characteristics and the same output voltage and current as of the pre-fault condition.

It is noteworthy that the maximum switch voltage stress of the IFTPVI in any operation mode is equal to the input voltage (PV voltage), which is the same as the maximum voltage stress in the conventional HERIC and H5 inverters.

3. Fault-Tolerant Structure of IFTPVI

The main parts of the fault-tolerant structure in the proposed topology are the FMU and electromechanical relays. The operation principle of the FMU and the relays are defined in this section.

3.1. Fault Managing Unit (FMU) and Fault Diagnosing Strategy

In order to implement the FMU and diagnose the fault, three current sensors are needed to sense the instantaneous currents of Leg_1, Leg_2 and the bidirectional switch (S_b), as indicated by *Ia*, *Ib*, and *Ic*, accordingly, in Figure 6. The fault is diagnosed through the procedure displayed in the flow-chart of Figure 7. According to this flow-chart, the FMU processes the measured currents along with the switching patterns for every switching period. The currents that each switching pattern should cause to flow in each leg during the normal operation are known. These values can only be equal to the output current or zero under normal conditions. The possible switching patterns and currents under healthy and faulty modes are summarized in Table 1 (in this table, "1" and "0" indicate the on and off states of the switches, respectively). In the case that one of the currents does not match the switching pattern, the FMU diagnoses the fault and locates the faulty section. As the faulty section is located, the FMU commands the associated relay R_1, R_2, or R_3 for faults in the bidirectional switch, Leg_1, or Leg_2, respectively. The relay corresponding to the faulty switch decouples the faulty section and adds the respective reserve element (or elements) to the circuit. Once the reconfiguration is successfully accomplished, new switching patterns are provided to the reconfigured configuration.

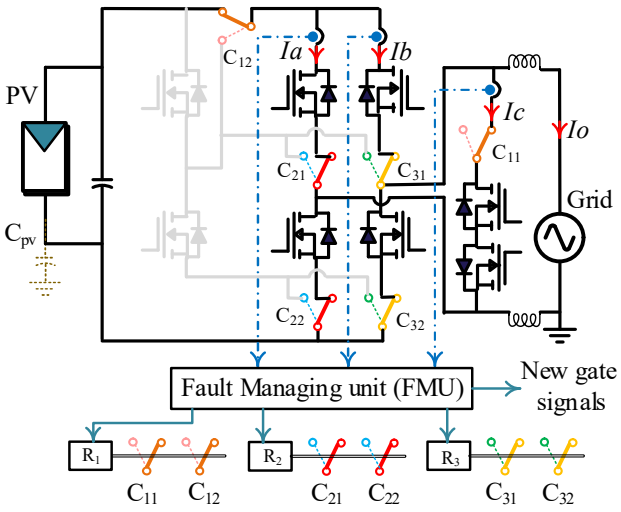


Figure 6. Fault managing unit of IFTPVI.

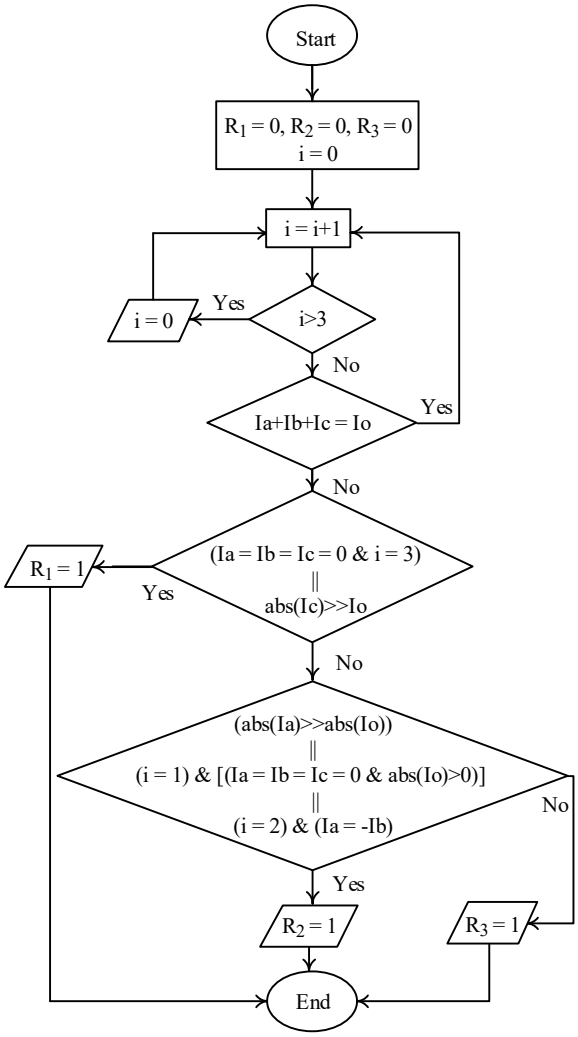


Figure 7. Fault diagnosing and reconfiguration flowchart.

Table 1. Operation modes of the proposed fault tolerant inverter.

Operation Modes		Switching Pattern of the Switches S_1, S_2, S_3, S_4, S_b	Current in Legs *Ia*	*Ib*	*Ic*	Io
Healthy Mode		10010	I	0	0	−I
		00001	0	0	I	−I
		01100	0	I	0	I
Faulty modes (faulty switch identification)	OC in Leg_1	10010	0	0	0	I
	OC in Leg_2	10010	I	−I	0	I
	SC in Leg_1	10010	>I	0	0	I
	SC in Leg_2	10010	I	>I	0	I
	SC in S_b	10010	>I	0	>I	I
	OC in S_b	00001	0	0	0	0
	OC in Leg_1	01100	−I	I	0	I
	OC in Leg_2	01100	0	0	0	I
	SC in Leg_1	01100	>I	0	0	I
	SC in Leg_2	01100	I	>I	0	I
	SC in S_b	01100	0	>I	>I	I

3.2. Electromechanical Relay

Each of the electromechanical relays in the IFTPVI consists of two normal-open (NO) and two normal-close (NC) metal-ware contacts. Figure 8 shows the structure of the electromechanical relay used in IFTPVI. Since the electromechanical relays in the proposed

inverter experience only one switching action, the slow characteristic of these relays is not important. However, the robustness of the structure is of great importance because they are to enhance reliability. Referring to Figure 2, it is seen that the normal-open conductors of the relays isolate the reserve switches from the circuit and avoid having voltage stresses across those switches during the healthy mode. Minimizing the voltage stress on reserve switches is very important since the voltage stress across the reserve switches could damage them before they enter the circuit operation.

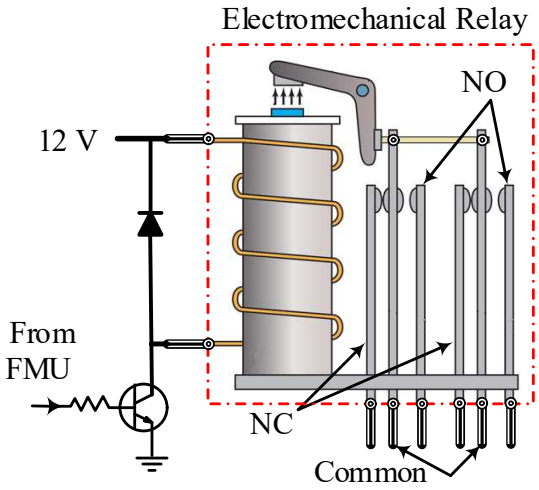


Figure 8. Electromechanical relay.

4. Reliability and MTTF Analysis

One of the most prominent techniques among many analytical techniques [28] for reliability analysis and evaluation is the Markov chain approach. The Markov method is applicable to the memoryless stationary systems.

As stated in [29–31], the lifetime of a power electronic element can be divided into three periods. The first period, often referred to as the debugging phase, is the period that device is most likely to fail in and consequently has high failure rate due to manufacturing errors, improper design or errors occurring due to the operator. The hazard rate in this phase decreases with time. The debugging phase may be short or non-existent for power electronic converters. The second period is referred to as normal operating phase. The hazard rate in this period is almost constant and failures occur by chance. This phase is the only phase in which the exponential distribution is valid. The third phase is termed as fatigue phase in which the hazard rate accelerates with time.

In order to figure out the reliability of an inverter, a Markov chain model of the inverter can be developed. Then, the transition rates of the model should be extracted using the failure rates of the utilized components. Additionally, the differential equations corresponding to the probability of the system being in operational states in the Markov chain model are needed. Finally, the Mean Time to Failure (MTTF) and the reliability of the inverter, which is the sum of the time-dependent probabilities of the operating states in the Markov chain, are calculated. In the following subsections, the reliability analysis of the conventional HERIC and H5 inverter along with the proposed fault-tolerant PV inverter topology is presented.

4.1. Reliability of the Conventional HERIC and H5 Inverter

The conventional HERIC and H5 inverters are both two-state systems [30]. The Markov chain model for these two inverters is shown in Figure 9, where State I is the Up state (operating state) and State II is the Down state (failed or absorbing state).

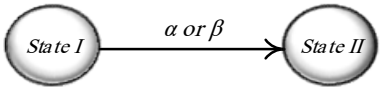


Figure 9. Markov chain model for the conventional HERIC and H5 Inverters.

For the sake of obtaining a more realistic model, the PV panels parallel capacitors C are also taken into consideration as shown in Figure 2. The Markov chain model transition rates of the HERIC (α) and H5 (β) inverters are, respectively, given as

$$\alpha = 6\Lambda_{sw_{HERIC}} + 6\Lambda_{D_{HERIC}} + \Lambda_C \tag{1}$$

$$\beta = 5\Lambda_{sw_{H5}} + 5\Lambda_{D_{H5}} + \Lambda_C \tag{2}$$

where, Λ_{SW}, Λ_D, and Λ_C represent the failure rates of switch, diode, and dc link capacitor, respectively. For the sake of brevity, the devices are all assumed to be in their normal operating phase. Therefore, their reliabilities can be described with exponential distributions [29].

In the initial state, both HERIC and H5 converters are assumed to begin operation in healthy condition. Thus, the initial condition matrix is

$$P(0) = [1\ 0] \tag{3}$$

The Up states time-dependent probabilities for HERIC and H5 are, respectively, given as Equations (4) and (5).

$$\frac{d}{dt}\left[P_{1_{HERIC}}(t) \quad P_{2_{HERIC}}(t)\right] = \left[P_{1_{HERIC}}(t) \quad P_{2_{HERIC}}(t)\right]\begin{bmatrix} -\alpha & \alpha \\ 0 & 0 \end{bmatrix} \tag{4}$$

$$\frac{d}{dt}\left[P_{1_{H5}}(t) \quad P_{2_{H5}}(t)\right] = \left[P_{1_{H5}}(t) \quad P_{2_{H5}}(t)\right]\begin{bmatrix} -\beta & \beta \\ 0 & 0 \end{bmatrix} \tag{5}$$

Referring to Equations (1)–(5), the reliabilities of the conventional HERIC and H5 are obtained as

$$P_{1_{HERIC}}(t) = R_{HERIC}(t) = e^{-\alpha t} \tag{6}$$

$$P_{1_{H5}}(t) = R_{H5}(t) = e^{-\beta t} \tag{7}$$

4.2. Reliability of the Proposed Fault-Tolerant Topology

The proposed fault-tolerant PV inverter can keep operating regardless of any kind of fault (OC or SC) in any of its semiconductor switches. The Markov chain model for IFTPVI is displayed in Figure 10. State I is the healthy state, all elements and switches of the converters are healthy and operational. In State II, one of the H-bridge switches in the initial HERIC configuration has failed and its corresponding leg was replaced with the reserve leg. Furthermore, State III represents the situation in which one of the two switches in the bidirectional switch has failed and therefore, was replaced by S_{r1}. Finally, State IV is the absorbing state. Once the converter enters the absorbing state, it can no longer operate with the original characteristics or cannot operate at all. States I–III are referred to as Up states as the converter maintains normal operation in those states. Oppositely, State IV is known as the Down state since the converter in this state is considered failed.

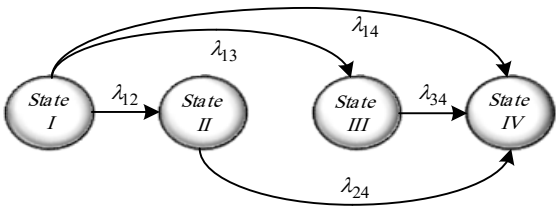


Figure 10. Markov Model for the IFTPVI (the proposed inverter topology).

The transition rates for the Markov chain model given in Figure 10 are

$$\lambda_{12} = 4\left(\Lambda_{sw_{HERIC}} + \Lambda_{D_{HERIC}}\right)P_r \tag{8}$$

$$\lambda_{13} = 2\left(\Lambda_{sw_{HERIC}} + \Lambda_{D_{HERIC}}\right)P_r \tag{9}$$

$$\lambda_{14} = 6\left(\Lambda_{sw_{HERIC}} + \Lambda_{D_{HERIC}}\right)(1 - P_r) + \Lambda_C \tag{10}$$

$$\lambda_{24} = 6\left(\Lambda'_{sw_{HERIC}} + \Lambda'_{D_{HERIC}}\right) + \Lambda_C \tag{11}$$

$$\lambda_{34} = 5\left(\Lambda'_{sw_{H5}} + \Lambda'_{D_{H5}}\right) + \Lambda_C \tag{12}$$

where $\Lambda'_{sw_{HERIC/H5}}$ and $\Lambda'_{D_{HERIC/H5}}$ are, respectively, failure rates of switch and diode for IFTPVI after a fault has occurred, the converter is reconfigured and is operating as HERIC or H5. λ_{ij} is the transition rate from state i to state j in the Markov chain model of IFTPVI shown in Figure 10. P_r is the probability of successful operation of the relay to remove the faulty part and to replace it by the reserve one. The failure rate of relays is a function of the number of on/off cycles. Thus, if a relay is switched only once in its lifespan, which is the case in IFTPVI, its hazard rate can be assumed to be zero [32]. Therefore, it is assumed that once the relay is turned on, it will keep up the proper operation. In this reliability analysis, the value of P_r is assumed 0.98 instead of 1 in order to have a more realistic analysis [28,31]. The maximum contact resistance for Omron MM series electromechanical power relays is 25 mΩ. These small relay contact resistances have a minuscule effect on the current and losses and, therefore, are ignored in the failure rate analysis. It is also worth noting that internal resistances of the reserve switches are assumed to be 5% higher than the main switches. This assumption is made in order to have a more realistic analysis by considering the component variations to a degree and to make sure that state I and state II of the Markov chain model in Figure 10, which respectively correspond to IFTPVI operating as HERIC pre-fault and post-fault, would not be rendered identical due to the above simplifications.

Each state change corresponds to the occurrence of a fault in the PV inverter. The IFTPVI can tolerate an SC or OC fault in any of the semiconductor switches as long as the corresponding relay functions properly after the fault is detected through the FMU. Consequently, if a fault occurs while IFTPVI is in State I and the relay responsible for bypassing and replacing the faulty switch fails to switch correctly, the inverter will cease to operate and moves to the State IV, the absorbing state in the IFTPVI Markov chain model. After the first fault has already occurred and the system is reconfigured once, the other two scenarios to enter the absorbing state are the occurrence of a second fault in any of the switches and the dc link capacitor failure. Therefore, the capacitor failure rate should be taken into account in the transition rates. The system is considered initially operational; and thus, all the assumptions in Section 4. A are valid here as well. The initial condition matrix is given as

$$P(0) = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix} \tag{13}$$

The time-dependent probabilities for each of the states are determined using Equations (8)–(14).

$$\begin{aligned} \tfrac{d}{dt}[P_1(t)\ \ P_2(t)\ \ \ldots\ P_4(t)] &= [P_1(t)\ \ P_2(t)\ \ \ldots\ P_4(t)] \\ \times &\begin{bmatrix} -(\lambda_{12}+\lambda_{13}+\lambda_{14}) & \lambda_{12} & \lambda_{13} & \lambda_{14} \\ 0 & -\lambda_{24} & 0 & \lambda_{24} \\ 0 & 0 & -\lambda_{34} & \lambda_{34} \\ 0 & 0 & 0 & 0 \end{bmatrix} \end{aligned} \tag{14}$$

As discussed, the (Up) state probabilities in the Markov model in Figure 10 are P_1, P_2, and P_3. Therefore, the reliability of the proposed fault-tolerant PV inverter is obtained as

$$R(t) = P_1(t) + P_2(t) + P_3(t) = \sum_{j=1}^{3} P_j(t) \tag{15}$$

Solving the differential equations in Equation (14) yields the time-dependent probabilities of the operating (Up) states as

$$P_1(t) = e^{-(\lambda_{12}+\lambda_{13}+\lambda_{14})t} \tag{16}$$

$$P_2(t) = \frac{\lambda_{12}}{\lambda_{12}+\lambda_{13}+\lambda_{14}-\lambda_{24}}\left[-e^{-(\lambda_{12}+\lambda_{13}+\lambda_{14})t} + e^{-\lambda_{24}t}\right] \tag{17}$$

$$P_3(t) = \frac{\lambda_{13}}{\lambda_{12}+\lambda_{13}+\lambda_{14}-\lambda_{34}}\left[-e^{-(\lambda_{12}+\lambda_{13}+\lambda_{14})t} + e^{-\lambda_{34}t}\right] \tag{18}$$

4.3. MTTF Analysis of the IFTPVI, HERIC and H5 Inverters

Using the coefficient matrices in Equations (4), (5), and (14), the stochastic transitional probability matrix P can be defined [29] for the HERIC, H5, and IFTPVI. In matrix P, each element P_{ij} corresponds to the probability of transition to state j after being in state i for a non-zero time interval.

$$P_{HERIC} = \begin{bmatrix} 1-\alpha & \alpha \\ 0 & 1 \end{bmatrix} \tag{19}$$

$$P_{H5} = \begin{bmatrix} 1-\beta & \beta \\ 0 & 1 \end{bmatrix} \tag{20}$$

$$P_{IFTPVI} = \begin{bmatrix} 1-(\lambda_{12}+\lambda_{13}+\lambda_{14}) & \lambda_{12} & \lambda_{13} & \lambda_{14} \\ 0 & 1-\lambda_{24} & 0 & \lambda_{24} \\ 0 & 0 & 1-\lambda_{34} & \lambda_{34} \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{21}$$

The truncated stochastic transitional probability matrix Q can be obtained by omitting the row and column associated with the absorbing state in the stochastic transitional probability matrices given in Equations (19)–(21). The absorbing state for HERIC and H5 is State II, and the absorbing state for IFTPVI is State IV. Therefore, their corresponding truncated stochastic transitional probability matrices are

$$Q_{HERIC} = [1-\alpha] \tag{22}$$

$$Q_{H5} = [1-\beta] \tag{23}$$

$$Q_{IFTPVI} = \begin{bmatrix} 1-(\lambda_{12}+\lambda_{13}+\lambda_{14}) & \lambda_{12} & \lambda_{13} \\ 0 & 1-\lambda_{24} & 0 \\ 0 & 0 & 1-\lambda_{34} \end{bmatrix} \tag{24}$$

The MTTF can be defined as the average time passed before the converter enters the absorbing state, and can be calculated either by the integration of reliability over the time from the starting point of converter operation to infinity or by using the stochastic transitional probability matrix method. The latter obtains the MTTF through inversion of the matrix produced by subtraction of the truncated matrix Q from the corresponding identity matrix [29]. The MTTF matrix (M) of the HERIC and H5 inverters are, accordingly, calculated as

$$MTTF_{HERIC} = M_{HERIC} = \int_0^\infty R_{HERIC}(t)dt = [I - Q_{HERIC}]^{-1} = \frac{1}{\alpha} \tag{25}$$

$$MTTF_{H5} = M_{H5} = \int_0^\infty R_{H5}(t)dt = [I - Q_{H5}]^{-1} = \frac{1}{\beta} \tag{26}$$

For of the sake of brevity, the stochastic transitional probability matrix method is used calculating MTTF matrix (M) for the IFTPVI.

$$M_{IFTPVI} = [I - Q_{IFTPVI}]^{-1} = \begin{bmatrix} \frac{1}{\lambda_{12}+\lambda_{13}+\lambda_{14}} & \frac{\lambda_{12}}{\lambda_{24}(\lambda_{12}+\lambda_{13}+\lambda_{14})} & \frac{\lambda_{13}}{\lambda_{34}(\lambda_{12}+\lambda_{13}+\lambda_{14})} \\ 0 & \frac{1}{\lambda_{24}} & 0 \\ 0 & 0 & \frac{1}{\lambda_{34}} \end{bmatrix} \quad (27)$$

In the matrix M, M_{pq} indicates the average number of hours spent in state q given that the system began operation from state p [29]. Consequently, the MTTF for the IFTPVI is obtained as

$$MTTF_{IFTPVI} = M_{11} + M_{12} + M_{13} \quad (28)$$

It is the sum of the average number of hours spent in each of the Up States (I–III) given that the converter begins operation in State I, the healthy state.

4.4. Failure Rate Analysis

Failure rate analysis is necessary to obtain the numerical results of reliability and MTTF of the converter. The method reported in [30] is used to calculate the failure rates of the power electronic circuit components. Even though the approach in [30] is criticized from a different point of view [31], it is still used to compare relative MTTF ameliorations [32]. According to [30], the failure rates of the power electronic elements can be estimated using Equation (29).

$$\Lambda_{component} = \Lambda_b \prod_{j=1}^{n} \pi_j \left(\text{failure}/10^6 \text{ h}\right) \quad (29)$$

where $\Lambda_{component}$, Λ_b, and π_j are, respectively, the failure rate of a component, the component basic failure rate, and the special factors that affect the failure rate of the component. These factors may vary for different circuit components. The factors affecting the considered power electronic components in this work are given in Table 2 [30].

Table 2. Factors Affecting the Failure Rates.

Factor	Definition
π_s	Electrical stress factor $(\pi_S) = V_S^{2.43}$, voltage stress factor $(V_s) = \frac{V_{applied}}{V_{rated}}$
π_c	Contact contraction factor–takes the values of 1 and 2 for metallurgically-bonded and non-metallurgically-bonded diodes.
π_Q	Quality factor = 1 [33]
π_E	Environment factor–takes different values based on the operation environment, for instance, space, ground, etc. For ground operation $\pi_E = 1$.
π_A	Application factor–depends on operation power.
π_V	Capacitor electrical stress factor. $\pi_V = [\left(\frac{\frac{V_{C_A}}{V_{C_{rated}}}}{0.5}\right)^3 + 1]$ where V_{C_A} and $V_{C_{rated}}$ are maximum applied voltage and the rated voltage, respectively.
π_{Cap}	Capacitor factor–depends on the materials used in the capacitor. For exam-ple, the Dielectric for an electrolytic capacitor: $\pi_{cap} = 0.34C^{0.18}$ where C is the nominal capacitance.
π_T	factors in the temperature on failure rates. π_T is a function of junction temperature in the case of MOSFETs and diodes.

Equations (30)–(32) provide the formula to calculate the π_T for diodes, MOSFETs, and capacitors, respectively [30].

$$\pi_{T_D} = exp[-3091\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)] \quad (30)$$

$$\pi_{T_M} = exp[-1925\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)] \tag{31}$$

$$\pi_{T_C} = exp[-5.09\left(\frac{T_a + 273}{353}\right)^5] \tag{32}$$

where T_a is the ambient temperature, which is assumed to be 25 °C. Moreover, T_j (°C) is the junction temperature of the MOSFET or diode and it is calculated as

$$T_j = T_a + \theta_{ca} P_l + \theta_{jc} P_l \tag{33}$$

where θ_{ca}, θ_{jc}, and P_l are the case to ambient thermal resistance (°C/W), junction to case thermal resistance (°C/W), and power losses (W), respectively. Other factors affecting failure rates are given in Table 3.

Table 3. Effective Factors on Components Failure Rates.

Components	Effective Factors (π_j)
Diode	$\pi_T.\pi_S.\pi_C.\pi_Q.\pi_E$
MOSFET	$\pi_T.\ \pi_A.\pi_Q.\pi_E$
Capacitor	$\pi_T.\pi_V.\pi_{Cap}.\pi_Q.\pi_E$

According to [34], the conduction power loss of a MOSFET and a diode can be calculated using the electrical models as shown in Figure 11.

Figure 11. MOSFET and diode power loss models in the on-state.

Where V_T and V_F are MOSFET threshold voltage and diode forward voltage; and $R_{DS_{on}}$ and $R_{d_{on}}$ are the MOSFET and diode on-state resistances, respectively. The aforementioned parameters are to be extracted from the component datasheets. Equations (34) and (35) respectively show the average power losses of the diode and MOSFET [30–39]:

$$P_{D_l} = \frac{1}{T}[\int_0^T (R_{d_{on}} \cdot i_S^2(t) + V_F \cdot i_S(t))dt] \tag{34}$$

$$P_{sw_l} = P_C + P_S = \frac{1}{T}[\int_0^T (R_{DS_{on}} \cdot i_S^2(t) + V_T \cdot i_S(t))dt] + [C_{oss} f_s V_{DS}^2] \tag{35}$$

where i_S, P_C, P_S, C_{oss}, f_s and V_{DS} are the instantaneous MOSFET or diode current, average conduction losses, average switching losses, MOSFET output capacitance, switching frequency, and the applied Drain-Source voltage, respectively. The conduction losses are calculated as the average losses in MOSFET or diode caused by their on-state voltage and internal resistance. The MOSFET average switching loss is calculated by the second term in Equation (35) [30–39], and the diode switching loss is ignored due to its small value.

5. Numerical Results and Comparison

5.1. Numerical Results

In this section, the numerical values of the reliability and MTTF of the HERIC and H5 inverters are compared with those of the IFTPVI. Furthermore, a comparison study is conducted to demonstrate the enhanced reliability of the proposed fault-tolerant technique. The simulation parameters are given in Table 4. A power factor of 0.87 was selected since

most PV inverters operate with a power factor of close to unity. Table 5 provides the values of the parameters introduced in Tables 2 and 3 and Equations (29)–(35), which are required for calculating power electronic circuit components failure rates and, in turn, obtaining the numerical values of Markov chain models transition rates, reliabilities, and MTTFs of the HERIC, H5, and IFTPVI. The values in Table 5 are extracted from [30] and the components' datasheets. In case of using other types of semiconductor switches, diodes, or capacitors, their corresponding Table 5 parameters can be extracted from [30].

Table 4. Circuit Parameters for Simulation.

Parameter	Description	Value
$V_{o_{RMS}}$	Peak load voltage	320 (V)
P_o	Load power	2 (kW) and 1.1 (kVar)
P.F.	Power factor (lagging)	0.87
$R_{DS_{on}}$	MOSFET on-state resistance	40 (mΩ)
$R_{d_{on}}$	Diode on-state resistance	0.1 (mΩ)
V_T	MOSFET threshold voltage	1.2 (V)
V_F	Diode forward voltage	1.2 (V)
V_{dc}	PV voltage	350 (V)
f_s	Switching frequency	25 (kHz)
C	Parallel capacitor of PV panel	470 (μF)
C_{oss}	MOSFET parasitic output capacitance	720 (PF)
V_c^{rated}	PV panel capacitor rated voltage	450 (V)

Table 5. Numerical Values Necessary for Calculation of Effective Parameters on Failure Rates.

Parameter	Description	Value
λ_b	Basic failure rate of diode	0.003 (failure/10^6 h)
	Basic failure rate of MOSFET	0.012 (failure/10^6 h)
	Basic failure rate of capacitor	0.0012 (failure/10^6 h)
π_c	Contact contraction factor	1
π_Q	Quality factor	1
π_E	Environment factor	1
π_A	Application factor	10
T_a	Ambient temperature	25 (°C)
θ_{ca}	MOSFET case to ambient temperature	40 ($\frac{°C}{W}$)
	Diode case to ambient temperature	60 ($\frac{°C}{W}$)
θ_{jc}	MOSFET junction to case temperature	0.65 ($\frac{°C}{W}$)
	Diode junction to case temperature	2 ($\frac{°C}{W}$)

Table 6 presents the numerical values of temperature factor π_T for MOSFETs, diodes, and capacitors as well as other factors that require calculation for obtaining the power electronic circuit components failure rates. The values in this table are extracted using Table 2, Equations (30)–(32), and the simulation results obtained using Matlab Simulink™. Table 7 provides the components failure rates for conventional HERIC and H5, and IFTPVI. These failure rates are calculated using the data given in Tables 2–6. For the purpose of simplification, the effect of heat sinks on losses are not taken into account in the reliabilities evaluations and comparisons.

Table 6. Numerical Values Necessary for Effective Parameters on Failure Rates.

Component & Parameters	MOSFET and Parallel Diode				Capacitor		
	P_l (W) (Average Loss for One MOSFET and Its Parallel Diode)	$\pi_{TMOSFET}$	π_S	π_{TDiode}	π_{Cap}	π_V	$\pi_{TCapacitor}$
HERIC or IFTPVI operating as HERIC before fault	6.5400	17.6800	0.4203	2.3668	0.0856	4.7641	8.8672
H5	9.3400	37.0507	0.4203	1.0894	0.0856	4.7641	8.8672
IFTPVI operating as HERIC after fault	6.5700	17.8244	0.4203	0.9948	0.0856	4.7641	8.8672
IFTPVI operating as H5 after fault	9.4400	37.6867	0.4203	1.0894	0.0856	4.7641	8.8672

Table 7. Numerical Values for Components Failure Rates in HERIC, H5, and IFTPVI.

Component & Parameters	MOSFET				Diode				Capacitor
	$\Lambda_{sw_{HERIC}}$	$\Lambda_{sw_{H5}}$	$\Lambda'_{sw_{HERIC}}$	$\Lambda'_{sw_{H5}}$	$\Lambda_{D_{HERIC}}$	$\Lambda_{D_{H5}}$	$\Lambda'_{D_{HERIC}}$	$\Lambda'_{D_{H5}}$	Λ_C
Values	2.1216	4.4461	2.1389	4.5224	0.0030	0.0014	0.0030	0.0014	0.0043

The numerical values for the transition rates in the Markov chain models of the HERIC, H5, and the IFTPVI, shown in Figures 9 and 10, are provided in Table 8. The values in the aforementioned table are obtained using Equations (1), (2) and (8)–(12), and the circuit components failure rates given in Table 7.

Table 8. Numerical Values for the Transition Rates in Markov Chain Models of HERIC, H5, and IFTPVI.

Chain	Numerical Value (Failure/10^6 h)
α (HERIC)	12.7518
β (H5)	22.2416
λ_{12}	8.3284
λ_{13}	4.1642
λ_{14}	0.2593
λ_{24}	12.8557
λ_{34}	22.6233

5.2. Comparison

In order to do a comprehensive evaluation, the IFTPVI is compared with the HERIC and H5 inverters. Table 9 provides a comparison of the reliabilities and MTTFs among the aforementioned topologies. The reliabilities in this table are calculated by inserting the transition rates values obtained in Table 8 and inserting them into Equations (6), (7) and (15)–(18). Moreover, insertion of transition rates in Table 8 in Equations (25)–(28) yields the MTTFs for the conventional HERIC, conventional H5, and IFTPVI, all of which are provided in Table 9.

Table 9. Comparison of Fault-Tolerant Techniques.

Topology	IFTPVI	HERIC	H5
Reliability	$81.5744e^{-12.7518t}$ $-80.1526e^{-12.8557t}$ $-0.4218e^{-22.6233t}$	$e^{-12.7518t}$	$e^{-22.2416t}$
MTTF	0.1437×10^6 h	0.0784×10^6 h	0.0450×10^6 h

As it is seen in Table 9, the IFTPVI has the highest reliability and the longest MTTF. It should be noted that time t in the reliability expressions in the table has a unit of 10^6 h. A graphic study of the reliabilities for the IFTPVI, HERIC and H5 inverters is provided in Figure 12 to achieve a more in-depth and further detailed comparison.

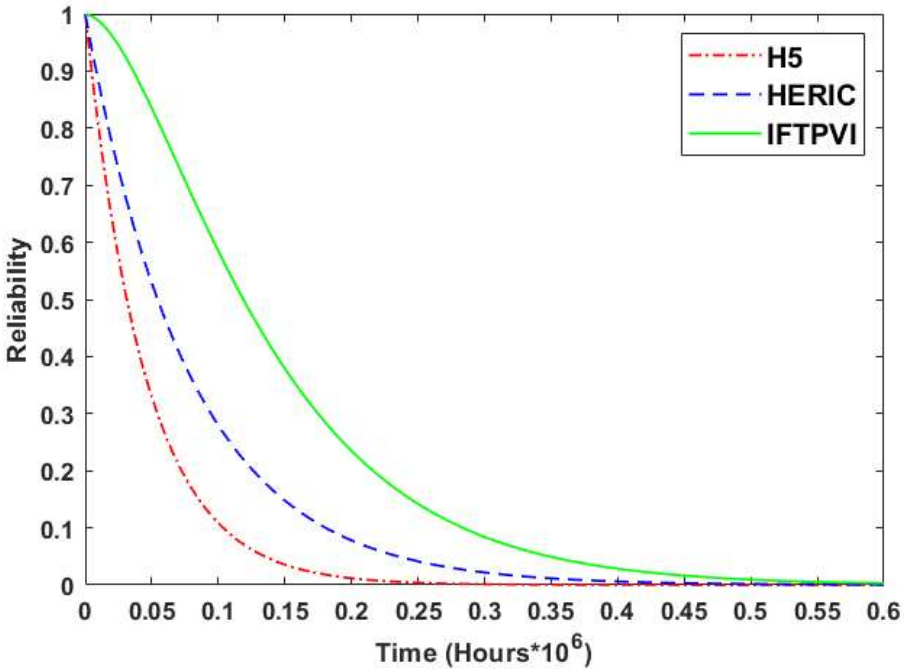


Figure 12. Reliability comparison of the IFTPVI versus the conventional HERIC and H5 inverters.

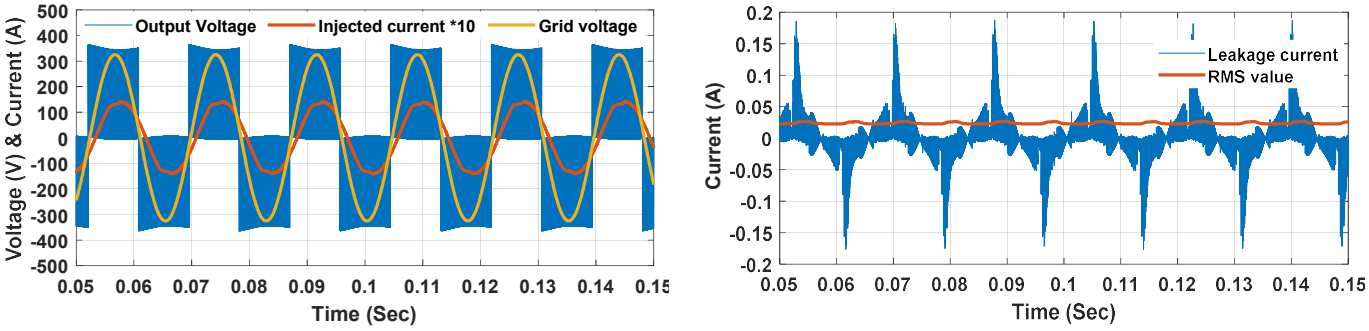
6. Simulation and Experimental Results

6.1. Simulation Results

The performance of the ITFPVI is first investigated by the simulation studies in Matlab/Simulink™ under the grid-tied condition. In the simulation model, the input voltage is a dc voltage of 350 V, and the RMS value and the frequency of the grid are 220 V and 50 Hz, respectively. Two inductor filters with 4.2 and 4 mH are used to interface the inverter to the grid since the filter inductors rarely have exactly the same inductances in practical applications. The switches are assumed to be IRFP450, and the switching frequency and parasitic capacitor are assumed to be 25 kHz and 300 nF, respectively.

In order to investigate the performance under different faulty conditions, three scenarios are considered. In the first scenario, the performance of the IFTPVI is evaluated under the healthy operation mode. In the second scenario, the fault occurs in one of the legs. In the last scenario, the reconfiguration of the inverter from HERIC to H5 is scrutinized when the fault occurs in the bidirectional switch (S_b).

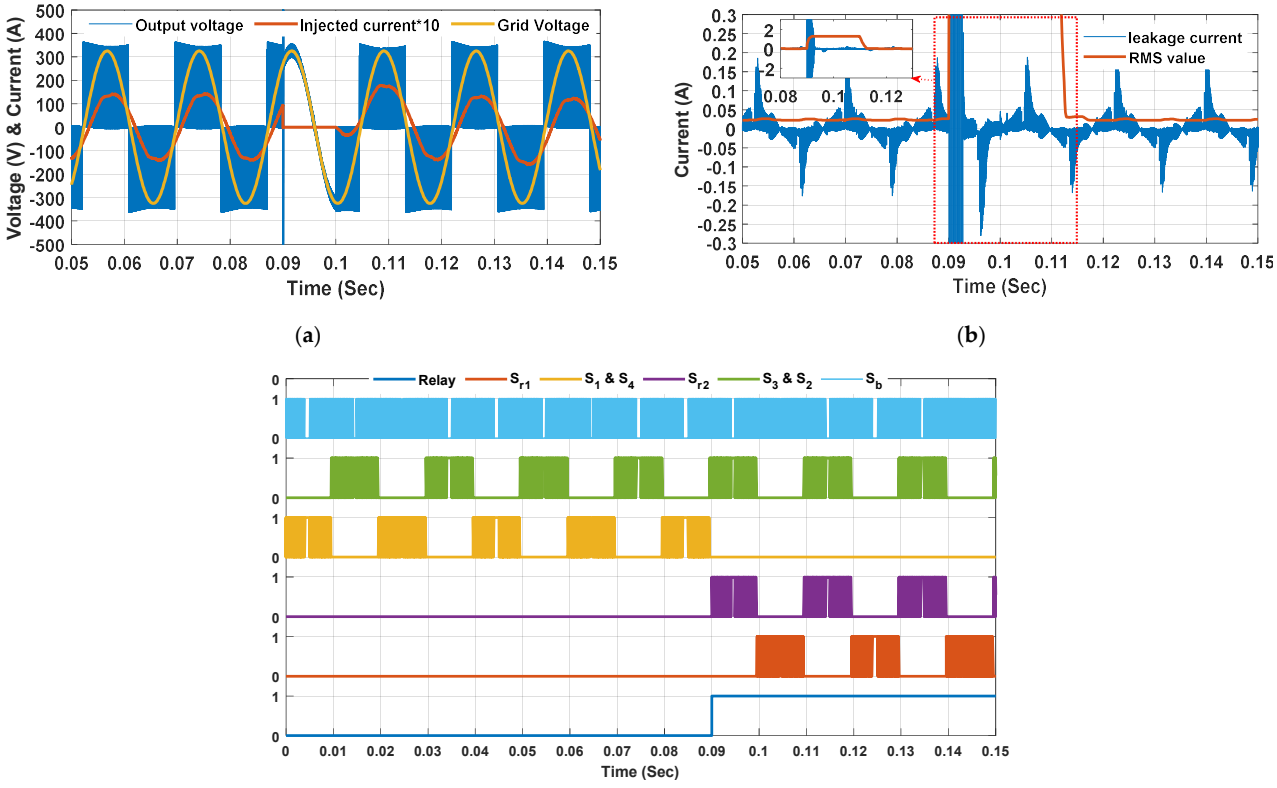
In order to investigate the performance of the inverter, 2 kW active and 1.1 kVar reactive powers are injected into the grid. The output voltage and injected current under the mentioned conditions are displayed in Figure 13a. Furthermore, the leakage current (common mode current) under the mentioned condition is shown in Figure 13b. The root mean square (RMS) value of the common mode current is about 20 mA, which is below the rated value. It is to be mentioned that according to VDE-AR-N-4105 standard the rated value should be below 300 mA [40–42].



(**a**) (**b**)

Figure 13. Normal operation of IFTPVI, (**a**) output voltage, injected current and grid voltage; and (**b**) leakage current.

Since the configuration of the inverter after the fault in the first or second leg is the same, only the fault in the first leg is investigated. The output voltage of the inverter before and after the fault is shown in Figure 14a. As it can be seen in this figure, during the reconfiguration process that takes about 10 ms, the output voltage becomes zero, and the output current is interrupted. However, after the reconfiguration, the control unit resumes the normal operation of the inverter. The leakage current under this condition is shown in Figure 14b. As shown in the figure, during the reconfiguration the leakage current reaches 2 A. Since this reconfiguration takes place once in the life span of the inverter, this value of the current is not important as long as it does not exceed the maximum current value. Figure 14c shows the switches and relay signal before and after fault.



(**a**) (**b**)

(**c**)

Figure 14. Performance when a fault occurs in one of the legs, (**a**) output voltage, injected current and grid voltage, (**b**) leakage current; and (**c**) switching and relay signals.

The other case is that the fault occurs in the bidirectional switch. Under this condition, the inverter should be reconfigured from the HERIC to H5. Since the HERIC inverter offers slightly higher efficiency compared to the H5, the efficiency will slightly decrease after the fault occurred in the bidirectional switch. The output voltage and current before and after the fault in the bidirectional switch are shown in Figure 15a. It is worth mentioning that the metal contacts of the electromechanical relays have almost zero resistance, and the relays will not affect efficiency. The leakage current before and after the reconfiguration is shown in Figure 15b. Comparing Figure 15b with Figure 14b shows that the H5 configuration causes a higher leakage current. Nevertheless, the common-mode current in both configurations is below the required threshold value. Figure 15c shows the switches and relay signal before and after fault.

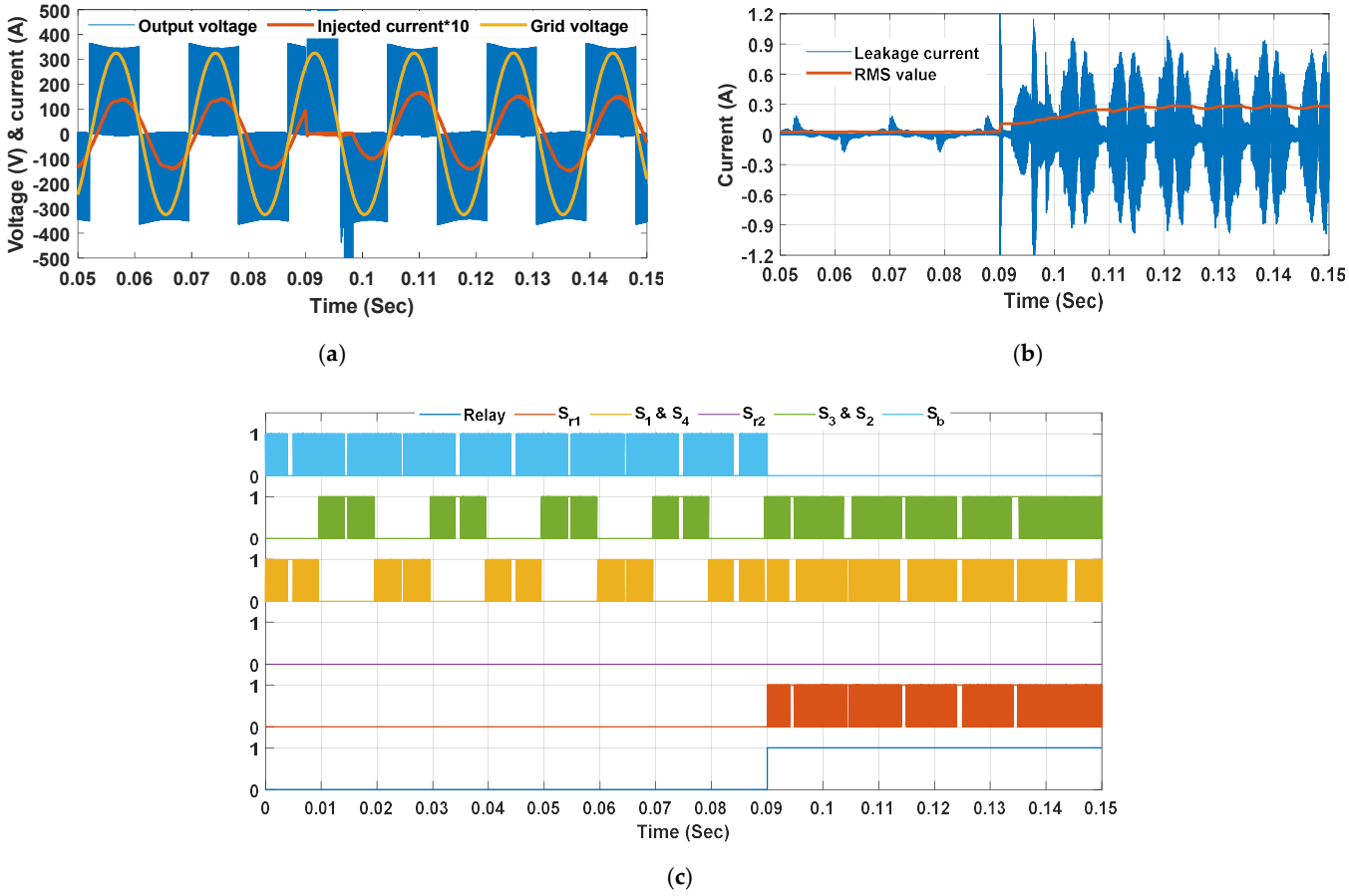


Figure 15. Performance when the bidirectional switch fails, (**a**) output voltage, injected current and grid voltage, (**b**) leakage current, (**c**) switching and relay signals.

In order to investigate the effect of the value of the load current on the leakage current, a load change is applied at the 0.2 s. The output voltage, injected current, and output voltage of the converter are shown in Figure 16a. The switching signals and relay command are shown in Figure 16b. Further, the leakage current under the mentioned condition is shown is Figure 16c. As seen in this figure, the value of the load current has no effect of the common-mode current (leakage current). This is because the leakage current depends on the capacitance of the parasitic capacitor, topology of utilized inverter, turn-on and turn-off speed, and voltage oscillation across the parasitic capacitor.

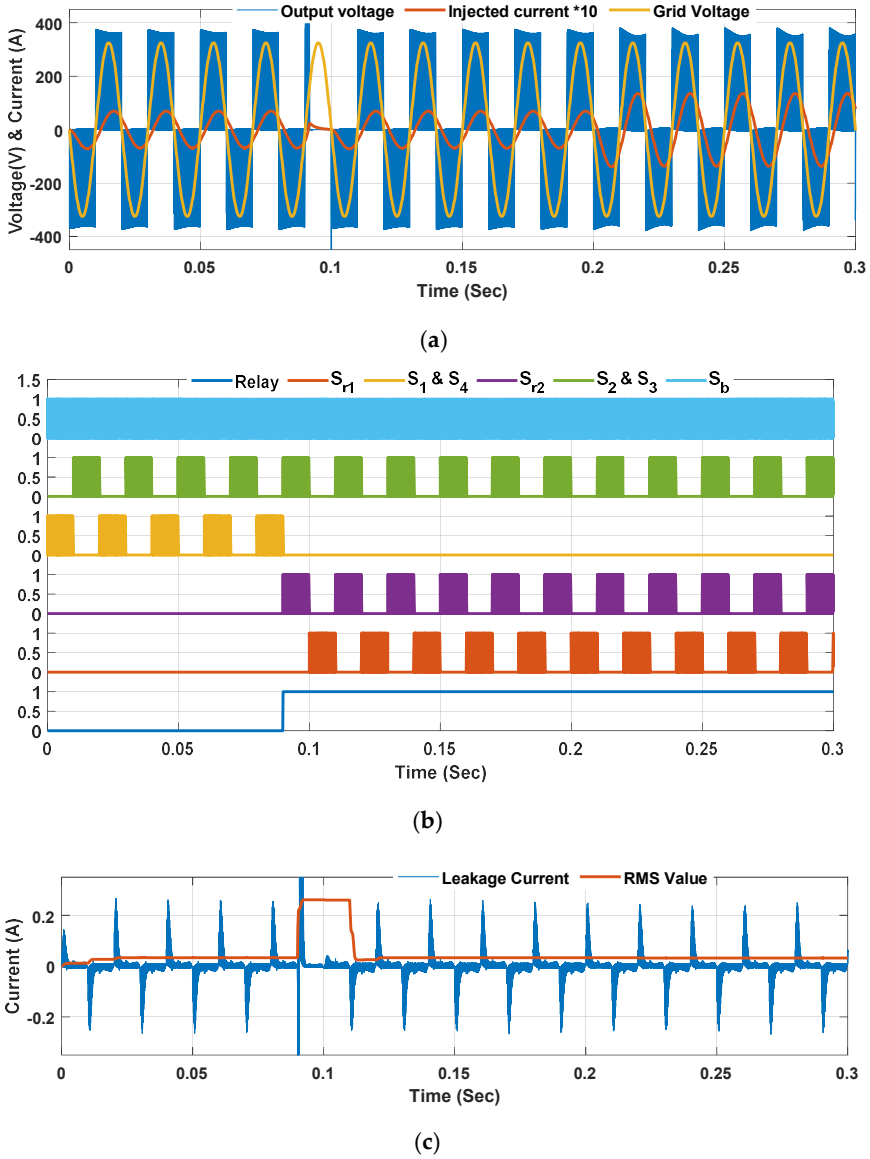


Figure 16. Performance when a fault occurs in one of the legs with the load change, (**a**) output voltage, injected current and grid voltage, (**b**) switching and relay signals; and (**c**) leakage current.

6.2. Experimental Results

In order to further prove the feasibility and viability of the proposed inverter topology, a laboratory-scaled prototype has been developed. The prototype is displayed in Figure 17, and its components' characteristics are listed in Table 10.

Table 10. Characteristics of the Prototype.

Switches	IRFP450
Gate-Driver	TLP 250
Relay	Omron
Processor	DSP F28335
Electrometrical Relays	Finder
Input Dc Voltage	350 V
Load	1.6 kW with PF = 0.87
Switching Frequency	5 kHz
Output Frequency	50 Hz

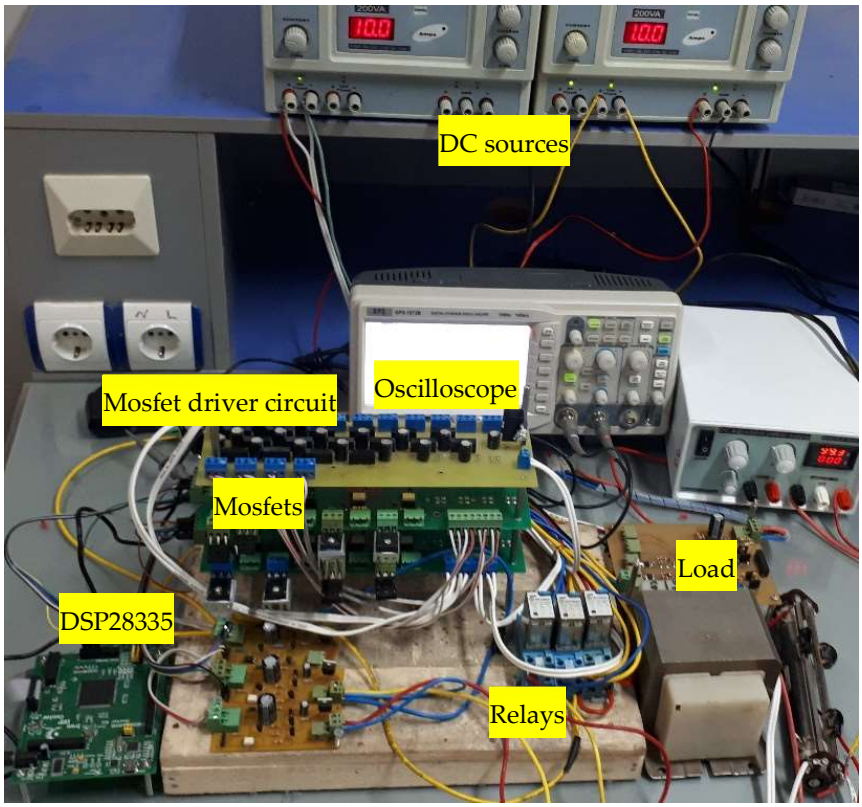
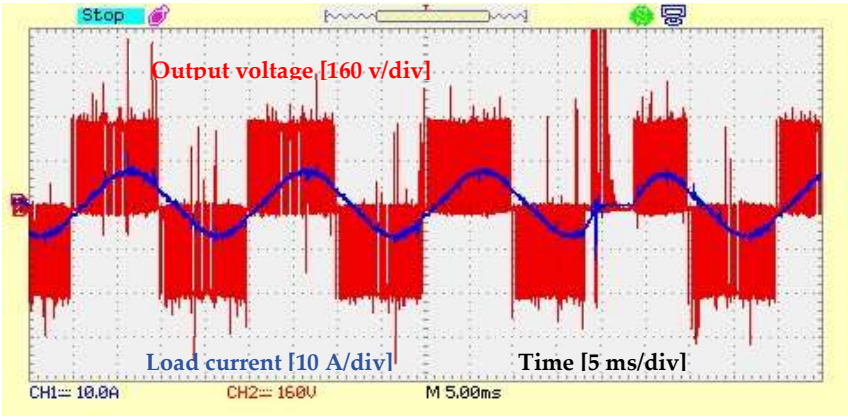


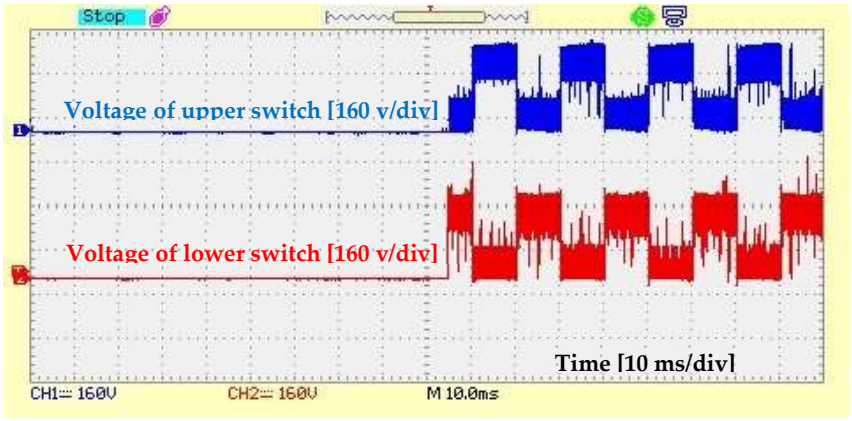
Figure 17. Laboratory Prototype.

Since the results of the fault in the first and second legs are the same, only the fault in the first leg is given here. In this test, a fault is exerted on one of the switches in the first leg. In order to remove the faulty part, the corresponding relay turns on. The result of this test is shown in Figure 18a. As it is shown in this figure, the relay has successfully removed the faulty section and replaced it with the reserve leg. This action takes about 4 ms, which is a very short interval and can be neglected as it happens once in the inverter lifespan. Additionally, the voltages across the reserve switches before and after fault are shown in Figure 18b. As it is shown in Figure 18b, the voltage across the reserve switches is zero as they are in the floating state during the reserve mode. As the fault takes place and the switches join the active part, the input voltage appears across them. It is worthy to mention that since the reserve switches experience no voltage stress during the reserve time they are assumed to be healthy before becoming active.

Moreover, in order to investigate the reaction of the IFTPVI in the presence of a fault in the bidirectional switch, a fault is applied to the switch. As it was explained previously, under this condition, the IFTPVI should maintain the pre-fault operation characteristics by reconfiguring from the HERIC to H5 configuration. To do so, the corresponding relay R_1 should remove the bidirectional switch and add the upper switch of the reserve leg into the circuit. The output voltage and load current under the mentioned condition are shown in Figure 19a. As shown in the figure, the reconfiguration process takes almost 13 ms, which is short enough to be neglected. Furthermore, the voltages of the reserve switches are shown in Figure 19b. It is observed that the voltage stress of the unused reserve switch in this scenario remains the same. Since the mentioned switch is used as the fifth switch of the H5, it experiences one third of the input voltage as shown in Figure 19b. It is to be noted that the lower reserve switch experiences no voltage stress, as seen in Figure 19b.

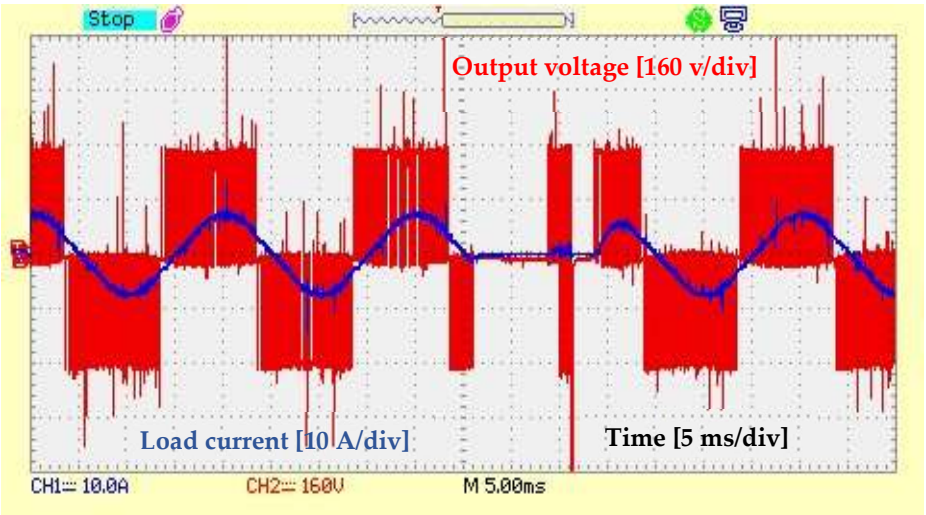


(**a**)



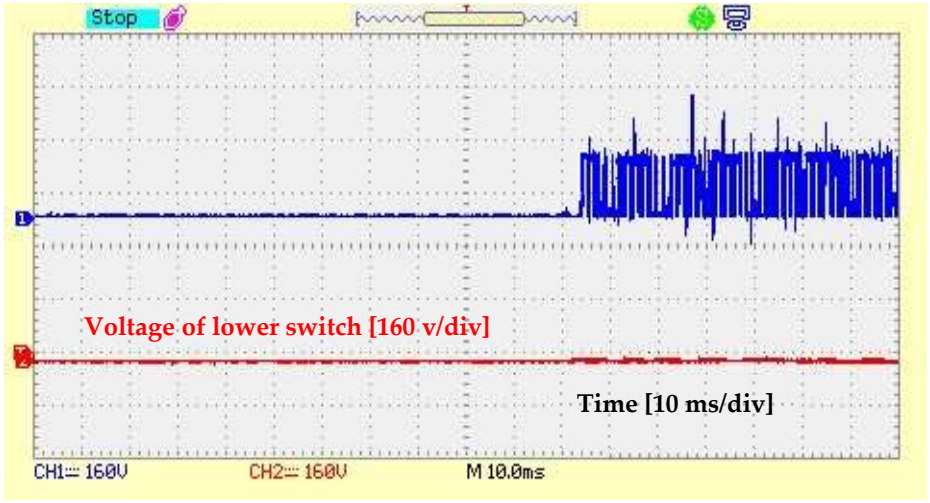
(**b**)

Figure 18. Performance measures of the proposed IFTPVI topology in the presence of a fault in the first leg; (**a**) output voltage and load current, and (**b**) voltage stresses of the reserve switches.



(**a**)

Figure 19. *Cont.*



(**b**)

Figure 19. Performance measures of the proposed topology when reconfiguring from HERIC to H5; (**a**) output voltage and load current, and (**b**) voltage stresses of the reserve switches.

7. Conclusions

In this paper, a fault-tolerant PV inverter has been proposed by effectively integrating a HERIC inverter, an H5 inverter, a reserve switch leg (half-bridge), and three electromechanical relays. The proposed inverter operates as a HERIC inverter under the normal condition. In the case when a fault occurs in any of the main legs, the corresponding relay removes the faulty leg and connects the reserve leg into the circuit so that the inverter keeps operating like the pre-fault configuration. If the fault occurs in the bidirectional switch, the corresponding relay reconfigures the inverter from HERIC to H5. In addition, a fault diagnosis method has been developed to identify and locate faults. The reliability analysis has been carried out to theoretically prove the reliability enhancement of the proposed topology. Furthermore, the simulation and experimental results have further verified the effectiveness and performance of the proposed PV inverter topology and successful reconfigurations of the inverter under different conditions.

Author Contributions: Conceptualization, H.K.J. and N.A.; methodology, N.A. and H.K.J.; writing—original draft preparation, N.A., H.K.J. and J.C.; investigation, H.K.J., N.A. and M.A. (Mohammad Ahmadpour); resources, C.W. and M.A. (Mehdi Abapour); writing—review and editing, C.W., F.B. and M.A. (Mehdi Abapour); visualization, H.K.J. and N.A.; supervision, C.W., M.A. (Mehdi Abapour) and F.B.; funding acquisition, C.W. and M.A. (Mehdi Abapour). All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Not Applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Brunisholz, M. IEA PVPS Annual Report 2021. In *International Energy Agency Photovoltaic Power Systems Technology Collaboration Programme (IEA PVPS TCP)*; International Energy Agency: Paris, France, 2021. Available online: https://iea-pvps.org/wp-content/uploads/2022/03/IEA-PVPS_Annual_Report_2021.pdf (accessed on 9 March 2022).
2. Li, H.; Zeng, Y.; Zhang, B.; Zheng, T.Q.; Hao, R.; Yang, Z. An Improved H5 Topology with Low Common-Mode Current for Transformerless PV Grid-Connected Inverter. *IEEE Trans. Power Electron.* **2019**, *34*, 1254–1265. [CrossRef]
3. Meraj, M.; Rahman, S.; Iqbal, A.; Ben-Brahim, L. Common Mode Voltage Reduction in a Single-Phase Quasi Z-Source Inverter for Transformerless Grid-Connected Solar PV Applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *7*, 1352–1363. [CrossRef]
4. Guo, X.; Yang, Y.; He, R.; Wang, B.; Blaabjerg, F. Transformerless Z-Source Four-Leg PV Inverter With Leakage Current Reduction. *IEEE Trans. Power Electron.* **2019**, *34*, 4343–4352. [CrossRef]

5. Liao, Z.; Cao, C.; Qiu, D.; Xu, C. Single-Phase Common-Ground-Type Transformerless PV Grid-Connected Inverters. *IEEE Access* **2019**, *7*, 63277–63287. [CrossRef]
6. Akpinar, E.; Balıkcı, A.; Durbaba, E.; Azizoglu, B.T. Single-Phase Transformerless Photovoltaic Inverter With Suppressing Resonance in Improved H6. *IEEE Trans. Power Electron.* **2019**, *34*, 8304–8316. [CrossRef]
7. Siwakoti, Y.P.; Blaabjerg, F. Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems. *IEEE Trans. Ind. Electron.* **2018**, *65*, 2100–2111. [CrossRef]
8. Khan, N.H.; Forouzesh, M.; Siwakoti, Y.P.; Li, L.; Kerekes, T.; Blaabjerg, F. Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems: A Comparative Review. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *8*, 805–835. [CrossRef]
9. Li, W.; Gu, Y.; Luo, H.; Cui, W.; He, X.; Xia, C. Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4537–4551. [CrossRef]
10. Meneses, D.; Blaabjerg, F.; García, O.; Cobos, J.A. Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application. *IEEE Trans. Power Electron.* **2013**, *28*, 2649–2663. [CrossRef]
11. Zeb, K.; Khan, I.; Din, W.U.; Khan, M.A.; Sathishkumar, P.; Busarello, T.D.C.; Ahmad, I.; Kim, H.J. Review on Recent Advances and Future Trends of Transformerless Inverter Structures for Single Phase Grid-Connected Photovoltaic Systems. *Energies* **2018**, *11*, 1968. [CrossRef]
12. Zeb, K.; Islam, S.U.; Uddin, W.; Khan, I.; Khan, M.; Ali, S.; Busarello, T.; Kim, H.J. An Overview of Transformerless Inverters for Grid Connected Photovoltaic System. In Proceedings of the International Conference on Computing, Electronic and Electrical Engineering (ICE Cube), Quetta, Pakistan, 12–13 November 2018; pp. 1–6. [CrossRef]
13. Schmidt, H.; Siedle, C.; Ketterer, J. DC/AC Converter to Convert Direct Electric Voltage into Alternating Voltage or into Alternating Current. U.S. Patent No. 7,046,534, 16 May 2006.
14. Victor, M.; Greizer, F.; Bremicker, S.; Hübler, U. Method of Converting a Direct Current Voltage from a Source of Direct Current Voltage, more Specifically from a Photovoltaic Source of Direct Current Voltage, into a Alternating Current Voltage. U.S. Patent No. 7,411,802, 8 August 2008.
15. Ristow, A.; Begovic, M.; Pregelj, A.; Rohatgi, A. Development of a Methodology for Improving Photovoltaic Inverter Reliability. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2581–2592. [CrossRef]
16. Bazzi, A.M.; Kim, K.A.; Johnson, B.B.; Krein, P.T.; Dominguez-García, A. Fault impacts on solar power unit reliability. In Proceedings of the 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 6–11 March 2011; pp. 1223–1231.
17. Maghraby, H.A.M.; Shwehdi, M.H.; Al-Bassam, G.K. Probabilistic assessment of photovoltaic (PV) generation systems. *IEEE Trans. Power Syst.* **2002**, *17*, 205–208. [CrossRef]
18. Omaña, M.; Fiore, A.; Mongitore, M.; Metra, C. Fault-Tolerant Inverters for Reliable Photovoltaic Systems. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2019**, *27*, 20–28. [CrossRef]
19. Obeidat, F.; Shuttleworth, R. PV inverters reliability prediction. *World Appl. Sci. J.* **2017**, *35*, 275–287.
20. Kumar, V.V.S.P.; Fernandes, B.G. A Fault-Tolerant Single-Phase Grid-Connected Inverter Topology With Enhanced Reliability for Solar PV Applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2017**, *5*, 1254–1262. [CrossRef]
21. Nallamekala, K.; Dandabatthina, S.; Tella, V.K. A novel fault tolerant 21-level inverter configuration for PV applications. In Proceedings of the 2017 International Conference on Circuit, Power and Computing Technologies (ICCPCT), Kollam, India, 20–21 April 2017; pp. 1–7.
22. Roopa, K.; Jugge, P.; Kalyani, S.T. A new 15-level inverter configuration with fault tolerant capability for PV applications. In Proceedings of the 2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), Chennai, India, 21–22 September 2017; pp. 1830–1835.
23. Madhukar Rao, A.; Sahoo, M.; Sivakumar, K. A three phase five-level inverter with fault tolerant and energy balancing capability for photovoltaic applications. In Proceedings of the 2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Trivandrum, India, 14–17 December 2016; pp. 1–5.
24. Rao, A.M.; Sivakumar, K. Five level single phase inverter scheme with fault tolerance for islanded photovoltaic applications. In Proceedings of the 2015 7th International Conference on Information Technology and Electrical Engineering (ICITEE), Chiang Mai, Thailand, 29–30 October 2015; pp. 194–199.
25. Madhukar Rao, A.; Sivakumar, K. A Fault-Tolerant Single-Phase Five-Level Inverter for Grid-Independent PV Systems. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7569–7577.
26. Jahan, H.K. A New Transformerless Inverter With Leakage Current Limiting and Voltage Boosting Capabilities for Grid-Connected PV Applications. *IEEE Trans. Ind. Electron.* **2020**, *67*, 10542–10551. [CrossRef]
27. Jahan, H.K.; Abapour, M. Switched-Capacitor-Based Multilevel Inverter for Grid-Connected Photovoltaic Application. *IEEE Trans. Power Electron.* **2021**, *36*, 10317–10329. [CrossRef]
28. Liu, M.; Li, W.; Wang, C.; Billinton, R.; Yu, J. Reliability evaluation of a tidal power generation system considering tidal current speeds. *IEEE Trans. Power Syst.* **2016**, *31*, 3179–3188. [CrossRef]
29. Billinton, R.; Allan, R.N. *Reliability Evaluation of Engineering Systems*; Springer: New York, NY, USA, 1983.
30. *MIL-HBDK-217 Military Handbook: Reliability Prediction of Electronic Equipment*; Department of Defense: Washington, DC, USA, 1990.

31. Khosroshahi, A.E.; Abapour, M.; Sabahi, M. Reliability Evaluation of Conventional and Interleaved DC–DC Boost Converters. *IEEE Trans. Power Electron.* **2015**, *30*, 5821–5828. [CrossRef]
32. Liu, M.; Li, W.; Wang, C.; Polis, M.P.; Wang, L.Y.; Li, J. Reliability Evaluation of Large Scale Battery Energy Storage Systems. *IEEE Trans. Smart Grid* **2017**, *8*, 2733–2743. [CrossRef]
33. *MIL-S-19500/477*; Revision B, Military and Government Specs & Standards. Naval Publications and Form Center (NPFC): Tokyo, Japan, 1994.
34. Graovac, D.; Pürschel, M.; Kiep, A. *MOSFET Power Losses Calculation Using the Data-Sheet Parameters*; Infineon: Neubiberg, Germany, 2006; Available online: https://www.scribd.com/document/34308439/MOSFET-Power-Losses-Calculation-Using-the-Data-Sheet-Parameters (accessed on 9 March 2022).
35. Jahan, H.K.; Panahandeh, F.; Abapour, M.; Tohidi, S. Reconfigurable Multilevel Inverter With Fault-Tolerant Ability. *IEEE Trans. Power Electron.* **2018**, *33*, 7880–7893. [CrossRef]
36. Rausand, M.; Hoyland, A. *System Reliability Theory: Models, Statistical Methods, and Applications*; Wiley: Hoboken, NJ, USA, 2004; Volume 396.
37. *Engineers Relay Handbook*, 5th ed.; Relay and Switch Industry Association (RSIA): Arlington, VA, USA, 1996.
38. Dhople, S.V.; Davoudi, A.; Domínguez-García, A.D.; Chapman, P.L. A Unified Approach to Reliability Assessment of Multiphase DC–DC Converters in Photovoltaic Energy Conversion Systems. *IEEE Trans. Power Electron.* **2012**, *27*, 739–751. [CrossRef]
39. Haji-Esmaeili, M.M.; Naseri, M.; Khoun-Jahan, H.; Abapour, M. Fault-tolerant structure for cascaded H-bridge multilevel inverter and reliability evaluation. *IET Power Electron.* **2017**, *10*, 59–70. [CrossRef]
40. *VDE-AR-N 4105: Power Generation Systems Connected to the Low-Voltage Distribution Network—Technical Minimum Requirements for the Connection to and Parallel Operation with Low-Voltage Distribution Networks*; VDE Association for Electrical, Electronic & Information Technologies: Frankfurt am Main, Germany, 2011.
41. Panigrahi, R.; Mishra, S.K.; Srivastava, S.C. Grid Integration of Small-Scale Photovoltaic Systems-A Review. In Proceedings of the 2018 IEEE Industry Applications Society Annual Meeting (IAS), Portland, OR, USA, 23–27 September 2018; pp. 1–8. [CrossRef]
42. Kerekes, T.; Séra, D.; Máthé, L. Leakage current measurement in transformerless PV inverters. In Proceedings of the 2012 13th International Conference on Optimization of Electrical and Electronic Equipment (OPTIM), Brasov, Romania, 24–26 May 2012; pp. 887–892.