energies

MDPI

Review

Comprehensive Study on Reduced DC Source Count: Multilevel Inverters and Its Design Topologies

Kommoju Naga Durga Veera Sai Eswar [1], Mohan Arun Noyal Doss [1,*], Pradeep Vishnuram [1], Ali Selim [2], Mohit Bajaj [3,4], Hossam Kotb [5] and Salah Kamel [2,6,*]

1 Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Kattankulathur, Chennai 603203, India
2 Electrical Engineering Department, Faculty of Engineering, Aswan University, Aswan 81542, Egypt
3 Department of Electrical Engineering, Graphic Era (Deemed to be University), Dehradun 248002, India
4 Graphic Era Hill University, Dehradun 248002, India
5 Department of Electrical Power and Machines, Faculty of Engineering, Alexandria University, Alexandria 21544, Egypt
6 Applied Science Research Center, Applied Science Private University, Amman 11931, Jordan
* Correspondence: arunnoyal@gmail.com (M.A.N.D.); skamel@aswu.edu.eg (S.K.)

Abstract: Due to cutting-edge innovations in industry and academia, research is more centered around multilevel inverters (MLIs), which play a significant role in different high/medium voltage and high-power applications when contrasted with traditional inverters. Relative analysis of the reduced DC source count and switch inverter topologies highlight its significant benefits, which include control complexity, switch count, source count, reliability, efficiency, cost, voltage stress, total harmonic distortion (THD), and power quality. When switched-capacitor technology is deployed, it is seen that with the assistance of 14 switches, a 53 level result is accomplished, and the THD is just around 1.41%, which is kept up with as per the IEEE 519-2014 norms. Whenever cascaded MLI topology is employed, the inversion efficiency is more prominent, and is about 99.06%. Hence, this review focuses on a few of the late-evolved MLIs utilized, and the benefits and drawbacks for different topologies are examined. To assist with current modern research in this field and the decision of the proper inverter for various applications, a novel topology of an MLI can be planned later on. Different setups of MLIs have been exhaustively covered and reviewed.

Keywords: multilevel inverter (MLI); reduced component count; asymmetrical; pulse width modulation (PWM); photovoltaic (PV) systems; electric vehicles (EV)

Citation: Eswar, K.N.D.V.S.; Doss, M.A.N.; Vishnuram, P.; Selim, A.; Bajaj, M.; Kotb, H.; Kamel, S. Comprehensive Study on Reduced DC Source Count: Multilevel Inverters and Its Design Topologies. *Energies* **2023**, *16*, 18. https://doi.org/10.3390/en16010018

Academic Editors: Jagabar Sathik Mohammed and Yam P. Siwakoti

Received: 14 October 2022
Revised: 26 November 2022
Accepted: 9 December 2022
Published: 20 December 2022

1. Introduction

Because of the rise in population, and enterprises and to fulfill everyday needs, power generation has received enormous interest. To deliver electrical energy, many power plants have been entrenched for years. A total of 75% of the energy in India is created by of thermal power stations, which use fossil fuels and coal. Thus, it brings about an expansion in the carbon levels. This has a tremendous effect on atmospheric climatic conditions, which are changing daily. Utilizing environmentally friendly power from renewable energy conventional sources (RECS), predominantly solar and wind, creates a lot of interest in power generation in recent research. This will likewise build a more extensive scope of utilization in power electronics and power system regions, rather than a huge reliance on changing climatic circumstances [1]. The objective of this paper is to change one type of energy over to another form, either by a rectification or an inversion process. Essentially, a traditional voltage-fed inverter is utilized, which can create two-levels of voltage. The terms MLI was first used with the advent of the three-level converter in the late 20th century. Since multilevel inverters have more levels than standard versions, their power rating has improved, while their device count has decreased [2]. Buck-boost and Q-ZSIs-type

operations are more efficient compared to ordinary VSIs and CSIs [3]. In [4], the author discussed the main characteristic of the proposed interconnection system: it can provide power to the load even though one of its converters is under maintenance. To obtain a high voltage gain with less voltage stress on the switches, the cells are coupled in parallel for the LV bus, and in series for the HV bus.

For higher applications and high-power evaluations, MLIs are employed. An MLI is a setup in which the different variations of powered electronic devices are arranged and worked together with DC-connected voltages to deliver more significant levels of the waveform at the output side [5]. MLIs are liked because of their intrinsic benefits, for example, low switching pressure, low dv/dt rating across the switches, reliability, lower cost, reduced complexity, improved THD, and superior efficiency when used in applications [6]. For the most part, DC–DC gain converters are put into use for higher power applications, for example, solar PV systems, fuel cells, high discharge lights, electric power trains, high power density devices, induction engine drives, UPS, X-ray beams, medical equipment, auto applications, and so forth.

MLIs assume a significant role in renewable energy (RE) applications as well as in electric vehicles. As a result, MLIs employ advanced power semiconductor devices to develop a stepped waveform that seems to be near to a sine waveform. It is the ideal choice for generating vast output, mostly in SPV applications [7]. A novel hybrid MLI topology that integrates the concepts of hybrid and asymmetrical behavior is presented in work in [8]. The smaller number of devices and sources makes the architecture possible for applications linked to solar PV and motor drives. Authors in [9] developed a new MLI with symmetric and asymmetric structures, presented in this study. Asymmetric topologies employ a minimum switch count, while symmetric topologies demand equal DC source values. However, the switches in both structures experience multiple blocking voltages, lowering the losses. The author of the work [10] developed an MLI by employing stacked capacitors for three-phase four-wire grid supply systems. With inherent advantages such as high-power density, reliability in extended temperatures, and stable drop characteristics, it lacks in its cost for high voltage applications. The essential concept in EV works as such: it contains the battery which is fed to the inverter, followed by the motor, where it relies upon the sort of vehicle. This vital role is performed by the inverter alongside the controller [11]. By changing the duty cycles of the employed inverter, the result output can be controlled. Inverters likewise have a rise and impact in EV charging systems; they can either be a wired or a wireless system. Along these lines, different MLIs are planned by their applications [12]. A large portion of the EV's innovation is coordinated with the RES. This can be valuable for suitable systems while working in V2G operations, where the power flow ought to be bi-directional. These are additionally used to further develop the battery life, state of charge (SOC), and state of discharge (SOD).

The hybrid form of the MLI is another category. It typically consists of two sections. The staircase voltage is created in unidirectional polarity in the first section, referred to as level generation [13]. This is accomplished by combining the DC sources in a specific way to flip between levels. The second step involves switching the polarity, which results in a voltage across the positive and negative load. For this, an H-bridge inverter is typically employed [14]. In [15], the author referred to the DC voltage sources in this topology that can be linked in series to create all the additive combinations.

Additionally, they can be linked in parallel, increasing the required output voltage and current flexibility. The author referred to it as a switched series/parallel sources (SSPS) MLI. Series connected switching sources (SCSS) are a different architecture that has been discussed. In this work [16], a novel idea for generating new converter topologies and output voltage waveforms has the advantage of low harmonic content. The converter employs two orthogonal space vectors. The basic idea is founded on being able to produce 133 distinct output space vectors and to allow for stepwise RMS output voltage adjustment.

Classification of MLIs: Fundamentally, ordinary MLIs are characterized into three classifications, represented in Figure 1: the diode clamped (DC-MLI), the flying capacitor

type (FC-MLI), and the cascaded H-bridge type inverter (CHB-MLI). These are called classical inverters, where this kind of arrangement finds a use for switches that are straight forward and that correspond to their generating levels, resulting in complexity in the system [5]. Further arrangements are made for diminishing the switch count and making the structure a complex-free operation. Table 1 represents the merits and demerits of the classified topologies [6]. DC-MLI uses fewer DC voltage sources. However, it performs numerous tasks such as fault-tolerant analysis, is simple to use, and is essential in development. Yet because the available power is halved on the output side, it cannot be applied in high-voltage applications. In [11], FC-MLI shows many benefits. For example, a lower number of devices, and energy can be created by the power-dense capacitors for obtaining ripple-free voltage and the multiplying effect [11].

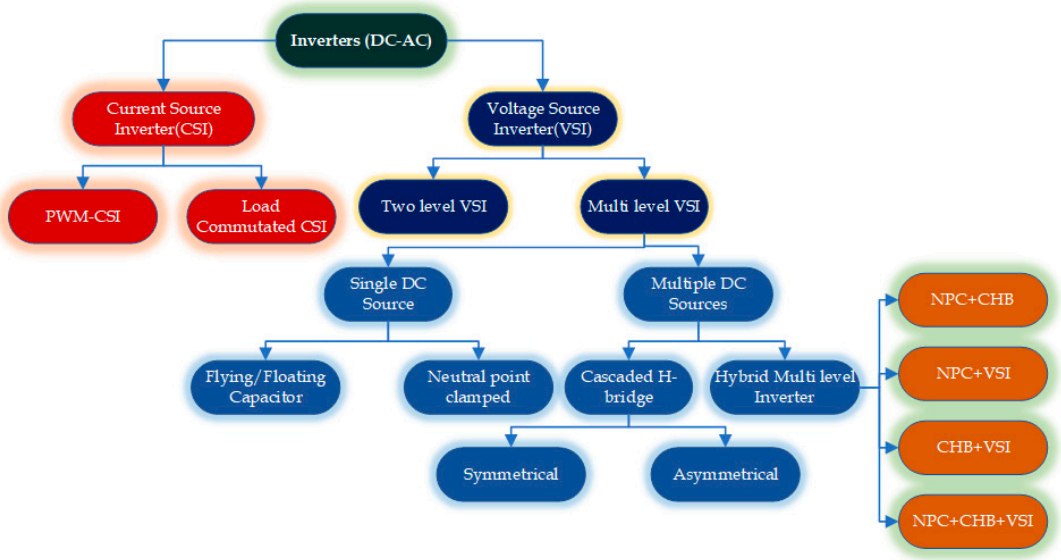

Figure 1. Classification of MLI.

CHB-MLI are classified into symmetrical and asymmetrical arrangements. To create a higher level of voltage, symmetrical arrangement is preferred, where the voltage of the DC source accommodated with each circuit is the same. Various magnitudes of voltage are given for creating asymmetrical configurations [17]. SC-MLI topology is created using available advantages in the cascaded and neutral point clamped MLIs, such as the low use of capacitors, switches, and diodes. It offers many benefits, such as boosting the output power and balancing the capacitor voltage.

Based on the preceding development in presumed converters, this review article makes an effort by providing an in-depth survey of all deduced converters currently used in the field of power semiconductor research. The following is a list of the review article's undertakings: (1) An overview of various determined converters is given, along with a discussion of how they differ from traditional converters. (2) Control methods used to operate the switches of the inferred converters are thoroughly explained.

The article is organized into four sections. The introduction and conclusion were explained better in Sections 1 and 4. A survey of various inferred converters is clarified, along with their operation and application point of view in Section 2. Section 3 clarifies various types of controllers exploits for working the inferred converters.

Table 1. Pros and Cons regarding different Multilevel Inverters.

Types of MLI Configurations	Pros	Cons
Diode clamped [18–23]	✓ They are used for rectification processes. ✓ It tends to be deployed for high switching frequencies; therefore, switching operation is improved. ✓ Capacitors can be charged with few input sources. ✓ The method to control the circuit is straightforward. ✓ Limited DC sources are required. ✓ They are used for fault-tolerant operations.	✓ It is challenging to balance the voltage in the circuit. ✓ The switches present in the circuit share unequal voltages. ✓ If there is a high output voltage level requirement, the number of diodes should be increased, i.e., no. of levels directly proportional to diodes. ✓ Even if a high input source voltage is given, the output voltage is halved due to the diode losses present in the circuit.
FC MLI [19,20,23–26]	✓ Reduction in input DC components. ✓ The level of the capacitor voltage is balanced. ✓ The diode requirement is zero. ✓ The flow of power can be controlled easily ✓ Harmonics are reduced abruptly, with no need for extra usage of filters. ✓ Transformer-less operation for high levels	✓ The rating of the capacitor should be high. ✓ The voltage balancing circuit, which is designed for the capacitor, is more complex. ✓ Monitoring each capacitor voltage is difficult. ✓ Losses are greater while transmitting real power. ✓ Designing the circuit is more costly. ✓ The estimation of pre-charging time is more complicated.
CHB-MLI [22,24,25,27,28]	✓ Due to the absence of diodes and capacitors, there is a huge reduction in the circuit component ✓ Easy to design and control. ✓ Voltage levels can be extended according to the required value. ✓ In the cascaded H-bridge case, MLI bi-directional switches employed are fewer in number and operated for only particular levels. Therefore, stress is low across the switch. ✓ Symmetrical and asymmetrical sources can be employed in both operations. ✓ Electric shocks are prevented due to isolation in the circuit	✓ The output voltage is significantly lower. ✓ To drive the circuits, more gating circuits are required. ✓ This can be used only for specific applications where a separate DC source is needed. ✓ To obtain the maximum output, more DC sources are required. ✓ When the bi-directional switch is employed for multiple levels for continuous operation, switch stress increases further, leading to switching losses and a reduction in efficiency ✓ Complexity in the circuit, especially in asymmetrical configuration. ✓ Cost is more in the case of asymmetrical operation. ✓ Different ratings of switches are needed for the configuration.

2. Review of Derived Converters, Operation, and Applications

Since the utilization of multilevel inverters over the last many years, numerous alterations in the inverters have been performed with the usage of power electronic devices. For expanding the voltage levels in the inverter, the quantity of the switch count, the source count, and the components helped increase the circuit activity. This outcome results in different factors, such as increasing the circuit's complexity, increasing the weight and cost, stress across the switches, electromagnetic compatibility (EMC) and electromagnetic interference (EMI) issues, THD, and losses in the circuit. At long last, this prompts a decline in efficiency and impacts the nature of the power on the grid utilities/distribution systems. To decrease the previously mentioned drawbacks, the paper investigates the various topologies and their operation with the decreased part count. Right off the bat, in

the year 1993, a decreased switch count was presented. For evaluating the operations of various topologies, asymmetrical and symmetrical arrangements are considered [11]. The main drawback of using a switched-capacitor is that it can produce only 5, 7, and 11 levels. Subsequently, planning an SC-MLI for more generating levels is a difficult task [28]. Due to the advantage of high switching operations and high voltage ratings, IGBT/MOSFET are used. Recently, wide band gap (WBG) semiconductors are also performing the operations for generating high levels. These also have low thermal conductivity and are highly stable during operation.

2.1. Operation of Derived Converters Based on DC Source Count

For easy understanding, Table 2 is framed, and the analysis of the derived converters is taken with respect to their DC source counts.

Table 2. Comparative analysis for different converters representing their switch counts, diodes, capacitors, inductors, DC source counts, number of levels generated, efficiency, THD, algorithm/controller used, and their applications.

Ref No	N_s	N_d	N_{cap}/N_{ind}	N_{dc}	N_l	Efficiency in (%)	THD	Algorithm/Controller Used	Application
[29]	14	3	3	3	53	94.21	1.41	P&O	SPV & EV
[30]	12	0	0	6	35	> 93	1.90	FFS	Low and Medium power factor loads
[31]	9	2	0	5	23	93.06	As per IEEE standards	FFS	Industrial Applications
[32]	10	0	0	3	21	94.02	3.49	P&O-based MPPT technique is used	SPV Energy Systems
[15]	9	3	7	6	17	98.05	3.88	SHE-PWM	RES
	11	3	7	6	19			PD-PWM	
[33]	10	0	0	3	15	99.01	As per IEEE standards <5%	FFS and SF are used	Medium and High-power voltage applications
	12	0	0	4	25				
[34]	6	2	4/4	2	Higher level of Voltages (19 times greater than input)	91	As per IEEE standards <5%	Double-input high DC–DC topology is employed	MPPT-based low and medium power applications and Regenerative braking in EV's
[35]	10	4	4	6	17	93.02	2.57	SHE-PWM	PV Systems
[36]	10	0	0	3	15	>90	3.50	Hybrid Modulation	High-Speed switching devices
[37]	10	10	0	3	13	99.06	6.60	FFS	SPV/RES
[38]	12	4	4	1	13	95.29	5.74	FFS and HFS Control loop techniques	RES
[39]	16	2	4	2	13	94.18	3.26	FFS and HFS control technique is used along with SHE	SPV systems and drives
[40]	9	5	0	5	11	>96	<4	Multi-carrier level shifted PWM strategy with phase disposition	Photo Voltaic systems

Ns—Number of sources, Nd—Number of diodes, Ncap/Nind—Number of capacitors/inductors used, Ndc—Number of DC sources, Nl—Number of levels generated in topology.

2.1.1. Using Six DC Sources

In [41], for *six* DC sources, the existing topology proposes 13-levels. In [42–44], the use of switches and the gate driver circuits are larger in number for a low level of steps in the output. This additionally causes the weight, size, and cost of the system to be more complicated. To avoid the disadvantages mentioned above, [30] created a structure that has eight unidirectional switches $(T1,\ T2,\ T3,\ T4,\ L2,\ R2,\ Su\ and\ Sd)$, among which four are bidirectional $(L1, R1, T5\ and\ T6)$, which are shown in Figure 2.

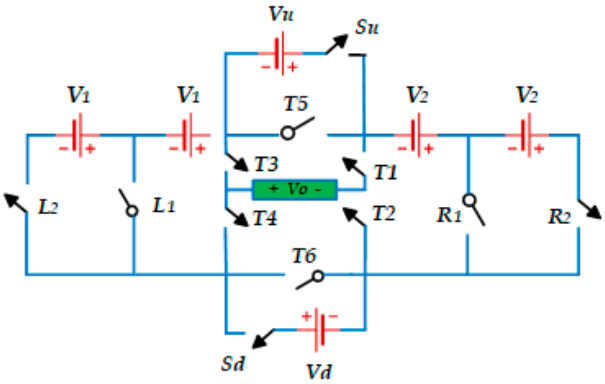

Figure 2. 35−Level MLI.

To create the positive, negative, and zero levels, the switches rely upon the DC sources. The DC sources are chosen as upper and lower sources, where $Vu = Vd = Vdc$. In Figure 2, it may be seen that the left leg creates $V1 = Vdc$, and the sources in the right leg create $V2 = 6Vdc$. If the connections are made in this manner, we can generate 35 levels: 17 levels on the positive side and 17 on the negative side, and zero levels where the expense and size of the structure are diminished.

In [45,46], the authors involved discrete diodes in the circuit, which resulted in a more typical structure when contrasted with the traditional structure, topologies need just a few DC sources. In [47,48], they considered U-packed cells and the series connected switched capacitors. In any case, these have a few downsides, as it uses several part counts for producing the minimum output level. With a similar switch count, the proposed [15] topology creates more levels. It further includes a reduced switch H-bridge (RSHB) and LDC. The RSHB MLI profits with few units coupled to the H-bridge, where an H-bridge contains one switch and diode with two DC sources. By utilizing several units over and over in the circuit, for example, $(1,\ 2,\ \ldots.n)$, it can produce $2n + 3$ levels at the output. Switches and diodes in the circuit cannot be conducted all the while. On the other side, we consider, for one unit, the resulting voltage will be Vdc/n when the switch Sn is in OFF, where $(Vcr1, Vcr2, \ldots.Vcrn = Vdc)$. When the switch Sn is turned ON, the result (Vrn) will be $(Vdc + Vdc/n)$, where, $(Vcr1/n, Vcr2/n, \ldots.Vcrn/n = Vdc)$. In the proposed structure 1 from Figure 3a, it may be seen that PS2 has an LDC module which includes two switches (K1 and K2) and one capacitor (C). The two switches ought to be turned on alternatively to avoid heavy short circuits. In reference [32], to prevent the source from short-circuiting, the switches K1 and K2 in LDC1 should turn ON alternatingly. Additionally, K1 and K2 primarily function in the cycle's positive and negative halves, respectively. It is feasible to almost double the number of levels compared to the output produced by the RSHB MLI with just two more switches. Equivalent equations are (1)–(4) for the number of levels, sources/capacitors, and switches. The corresponding expressions are [32]:

$$\text{Number of switch count } (Nsw) = n + 6 \tag{1}$$

$$\text{Number of discrete diodes } (Ndd) = n \tag{2}$$

$$\text{Number of DC sources/capacitors } (N_{dcs}) = 2n + 1 \tag{3}$$

$$\text{Number of levels } (N_l) = 4n + 5 \tag{4}$$

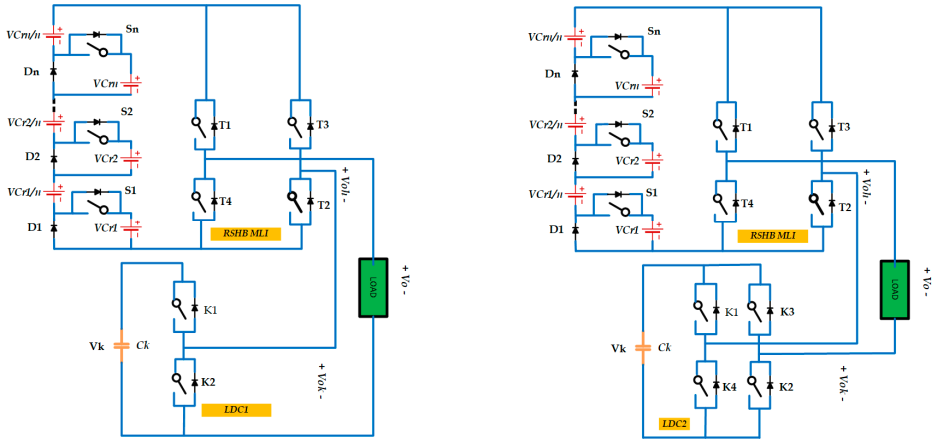

Figure 3. (**a**) 19−Level MLI; (**b**) 17−Level MLI.

In the proposed structure 2 from Figure 3b, it tends to be seen that the PS2 has an LDC module that involves four switches (K1, K2, K3 *and* K4) which are only a full H-bridge. The activity is the same as that of construction 1, yet in this, (K1 *and* K3) will be worked for the positive half cycle and (K2 *and* K4) will be worked for the negative half cycle. Generalized expressions for determining the component count in the PS2 are given as follows [32]:

$$\text{Number of switch count } (N_{sw}) = n + 8 \tag{5}$$

$$\text{Number of discrete diodes } (N_{dd}) = n \tag{6}$$

$$\text{Number of DC sources/capacitors } (N_{dcs}) = 2n + 1 \tag{7}$$

$$\text{Number of levels } (N_l) = 4n + 7 \tag{8}$$

When contrasted with [49–52], the proposed [53] Figure 4 does not need an H-bridge even if it can create more levels; ($two\ 2Vdc$, $3vdc$, $and\ one\ 0.5Vdc$) are given as input DC sources. ($Sa1$, $Sb1$, $Sc1$, $Sd1$) are the switches used to produce various levels of voltage for the result, which are implemented for boosting the voltage level. By providing complimentary switching operations, ($Ha1$, $Hb1\prime$) works during the positive half cycle and ($Hc1$, $Hd1\prime$) works during the negative half cycle. The switch voltage stress is limited by operating this way. The designed circuit is useful to lessen the total blocking voltage (TBV), and the overall performance of the ACCM MLI is improved successfully. The conduction and switching losses are all well determined, and they fundamentally rely upon the switching operation of the circuit.

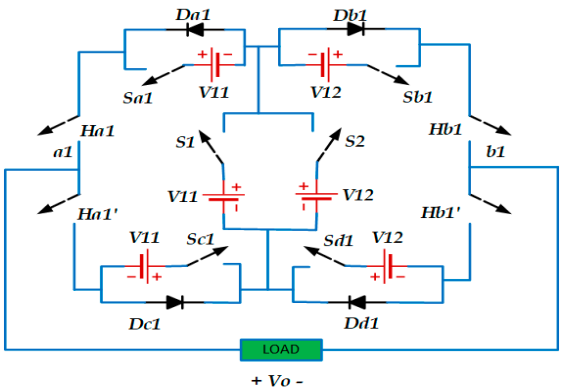

Figure 4. 17−Level MLI.

2.1.2. Using Five DC Sources

In [46,54–57], more DC sources with different magnitudes are chosen. In [56], the switches chosen were additionally more in number. The proposed [31] structure diminishes all of the disadvantages mentioned in the previous topologies. The design is made with a T-type and half-bridge inverter. An adjusted design was created, which is displayed in Figure 5. Out of nine, eight switching devices, named $S1, S1', S2, S2', T1, T1', T2, T2'$, which are unidirectional, and switch $S3$ is unidirectional. The DC source sizes are unique and named as $(V1 = V2,\ V3, V4 = V5)$. Because of the decreased switch count and the DC source, the blocking voltage is an additional benefit.

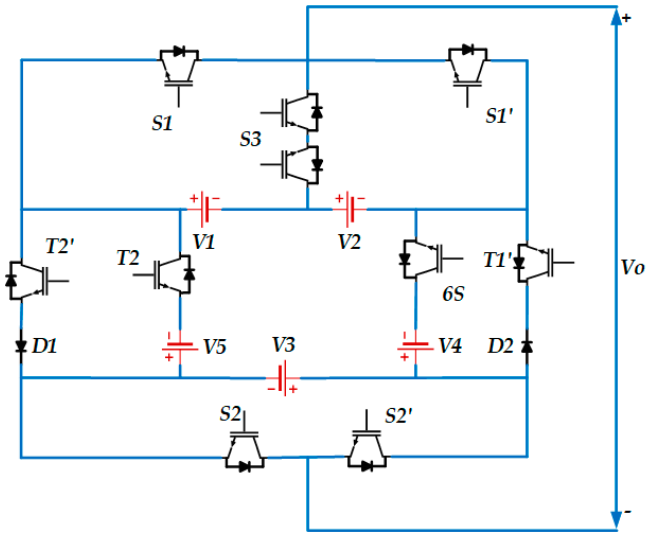

Figure 5. 23−Level MLI.

In [58–60], because of the adjustment of the temperature and irradiance in the created PV system, it brings about the open circuit voltages and the short circuit currents. By involving the MPPT controller in [40], this can be avoided. The converter configuration is kept up with stability even in disturbed load conditions. The designed topology is the change of the cascaded half-bridge MLI. The DC sources in Figure 6 are symmetrical where all the voltage sources are equivalent $V1 = V2 = V3 = V4 = V5 = Vdc$. For the level-generating part, the switches $(S1 - S5)$ are alike, and for the polarity part $(S6 - S9)$ are utilized in the H-bridge structure, where both operate at switching frequencies.

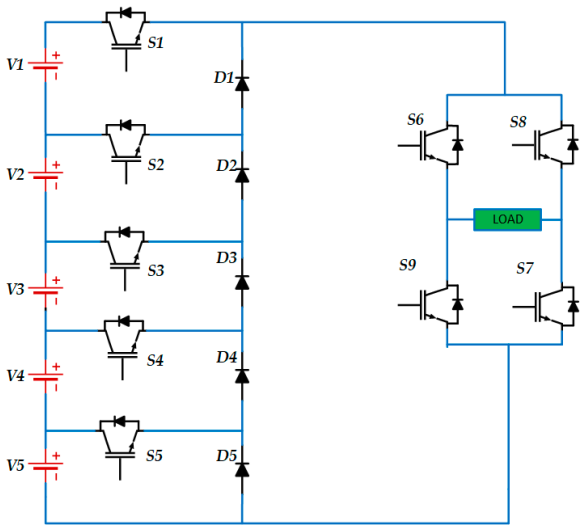

Figure 6. 11−Level MLI.

Modulation index (ma) for the reduced switch count is given by Equation (9), referred from [40], where Vm represents the amplitude of reference and Vcr represents the amplitude of carrier wave, and m relates to the number of levels

$$m_a = \left(\frac{2V_m}{V_{cr}(\mathrm{m}-1)} \right) \tag{9}$$

2.1.3. Using Four DC Sources

In [61], the construction works with 12 switches and creates a 17-level. When contrasted with [62], the TSV is kept up at 78. Cost and conversion efficiency are additionally an issue. For a similar switch count, the proposed topology [33] creates 25 levels, and the TSV is additionally 60. Reduced switching loss and cost are the main principles and advantages. Switches $(S1 - S8)$ are unidirectional and one bidirectional switch $(S9)$ is available in the circuit. Switches $(S1 - S2)$, $(S3 - S4)$, $(S5 - S6)$, $(S7 - S8)$ are paired in a complementary manner to avoid short circuits. The designed Figure 7 can be worked in two setups. Possibly, it very well may be symmetrical/asymmetrical. To have the circuit in a symmetrical setup, the voltages $V1$ and $V2$ should be equivalent to Vdc $(V1 = V2 = Vdc)$. To acquire a similar circuit in the asymmetrical setup, the voltage magnitudes are different such that $(V1 = Vdc)$ and $(V2 = 3Vdc)$, thusly, the circuit performs. In a similar way to produce 25-level output, the structure needs to replace supply voltage source $V1$ with two configured voltage sources with the same magnitude. This is possible only with an asymmetrical configuration.

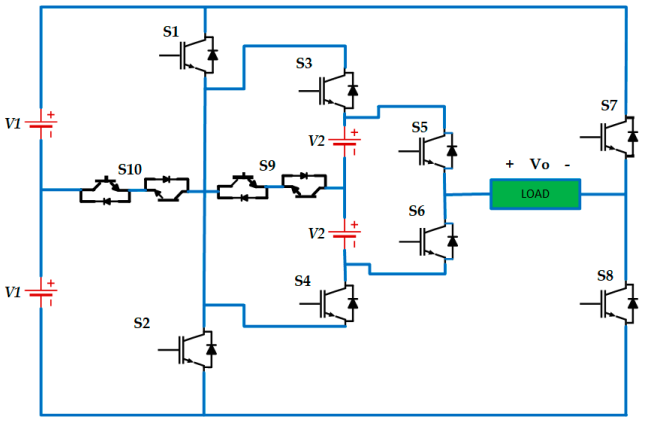

Figure 7. 25−Level MLI.

2.1.4. Using Three DC Sources

In [60], the part count per level and the TSV bring about a higher value. To further avoid the present circumstance in the MLIs, a new proposed [29] topology produces a 53-level result where a switched capacitor (SC) is placed at the front side alongside the H-bridge as shown in Figure 8. It boosts the voltage and makes the operation of capacitor charging and discharging simple. Utilizing many quantities of capacitors prompts an increment in the levels of the MLI. During ideal circumstances, capacitor C, which is at the front side of MLI, is charged to voltage $V1$ when it is associated with the corresponding DC source. Whenever the capacitor is made in series connection, it is discharged with regard to the load. At the point when the switch $S2$ is in conduction, the capacitor is charged for every half-cycle during $Vo = \pm Vc1$. During discharging mode, diode D and switch $S2$ will be in the OFF position. Capacitor C discharges while switch $S1$ is in conduction. The load currents are known with the help of $V1$ and $Vc1$ when it supplies energy to the load.

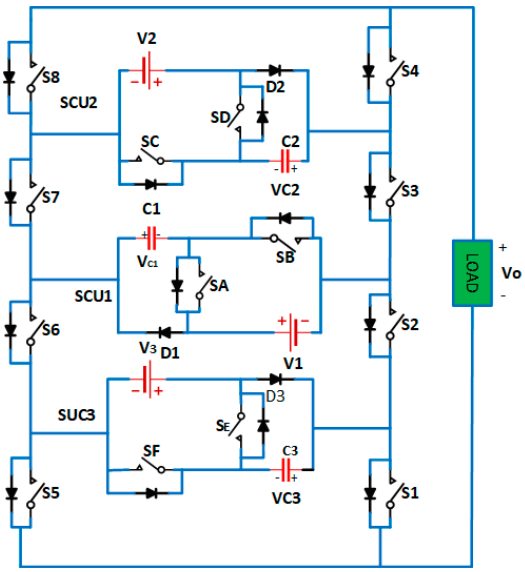

Figure 8. 53−Level MLI.

The cost factor relies upon many factors, for example, switch count, DC source count, total standing voltage (TSV), and the gate driver circuit. It is given by

$$\text{Cost Factor (C.F)} = (N_s + N_{dk} + N_d + N_c + \alpha TSVpu) \times n \tag{10}$$

In [45,60,63–67], more gate driver circuits, switches, and DC sources are used for generating the resulting level. Along these lines, the TSV and cost work is less. Mentioned in [32], a proposed structure decreases the part count without diodes, capacitors, and inductors. Another design has been created, which is displayed in Figure 9. $(V1, V2, V3)$ are utilized in this topology. Based on the switching operations, the output levels are obtained. Assuming the switching state is '1', it expresses that the switch is in conduction (ON state) and assuming that the switching state is '0' it implies that the switch is in (OFF) condition. To obtain the resulting voltage of 400 V, switches should be worked in various modes. Prior to that, voltages are opted based on a $1:2:7$ proportion. In this way, it produces a voltage level of 40 V, 80 V, 280 V individually. It obstructs every one of the undesirable voltages, therefore, the cost of the design is decreased.

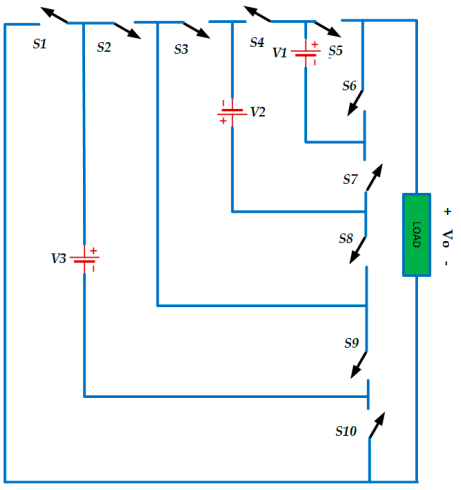

Figure 9. 21−Level MLI.

The total standing voltage is given by

$$TSV = 2(Vs1 + Vs3 + Vs5 + Vs7 + Vs9) \tag{11}$$

The current of 4 A is created at 400 V voltage level with the resistor value of 100 Ω. This topology has performed many tests with sudden disturbances for various loads, and it shows reliable results.

$$\text{Number of switches } (N_s) = 2n + 2 \tag{12}$$

$$\text{Number of voltage levels } (N_l) = 7 \times n \tag{13}$$

$$\text{Output voltage } (V_o) = 2n + 2 * Vdc \tag{14}$$

$$\text{Cost factor } (C.F) = (N_s + N_{dk} + N_d + N_c + \alpha TSVpu) \times n \tag{15}$$

where, (Ns) is the number of switches present in the circuit, and (Ndk) is the driving board circuit. (Nd) and (Nc) indicate the number of diodes and capacitors. (TSV) is the total standing voltage and (n) demonstrates the number of DC sources used.

Fundamentally, losses are two types, conduction loss and switching loss.

$$\text{Conduction loss } (P_{cl}) = \left[V_s + R_{si\beta}(t)\right] i(t) \tag{16}$$

Here (Vs) is the voltage drop, and (Rs) is the switch equivalent resistance.

In [65], the current design needs 28 and 36 switches for producing 11 and 15 levels. This shows the tremendous effect on design structure, and brings more conduction and switching losses. In [60], for the same hybrid topology, 16 switches are expected for the 15 level output. The proposed structure [36] employs a switched capacitor and an H-bridge circuit in the topology shown in Figure 10. It is apportioned into two sections. In the initial segment, it is a design with an H-bridge where the DC voltage is equivalent to Vo. Section 2 construction is an inverter where the voltage equivalents to Vk. The voltage source can utilise the example of exchanging capacitors. From this, we can comprehend that the simple switching circuit is placed in the front side (DC source) while $(Sa - 1 - San - 1)$ and $(Sb1 - Sbm - 1)$ are the operating switches that are associated in series. We can see that when Phase A is operated, switch $Sb1$ will be in ON state and the current passes through the switch, which brings about voltage $V1$. Consequently, it results $(Vab = V1)$. The switches $(Sa1\ and\ Sb1)$ will be in conduction mode, therefore the remaining switches are OFF. Voltages $(V1\ and\ V2)$ are in series outcomes of $Vab(Vab = V1 + V2)$. Later, switches $(Sa1\ and\ Sa2)$ are in ON state and different switches will be in OFF state, where the voltages $(V1\ and\ V3)$ are cascaded. This results in voltage as $(Vab = V1 + V2 + V3)$. For example, conventional topology uses 12 switches for 11 level output. The introduced topology is basic in structure, reliable, and efficient for power applications. In the alteration of the introduced topology, we can create 21 levels with just 12 switches when the proportion of $(Vo : Vk)$ is 1:3.

In [63,68,69], the device needs four DC sources for the 17-level. In [70,71], the MLI is designed by utilizing unidirectional switches. Hence, the gate driver circuit usage is greater. This outcome results in an expansion in part counts. The proposed design [37] uses just two DC sources and bi-directional switches, where just one gate driver circuit is put into service for the two bidirectional switches used in Figure 11. For voltage and current operations, unidirectional and bidirectional switches are utilized. Switches $(S1\ and\ S2)$, which are associated in the middle of the two-voltage source $V1$, need just one gate driver circuit. The voltage $V2$ is associated in the middle of the switch $(S3\ and\ S4)$, which changes the magnitude of operation. The modules associated in the circuit pairs are complementary switches $(S1 - S2)$, $(S3 - S4)$, $(S5 - S6)$, $(S7 - S8)$, which are not turned ON all the while. In the circuit, voltage sources are associated all the while, thus, it can further develop the voltage level.

$$\text{Total Standing Voltage is given by } TSV = \sum_{x=1}^{2k+4} Sx \tag{17}$$

The voltage Vx is the blocking voltage at switch Sx

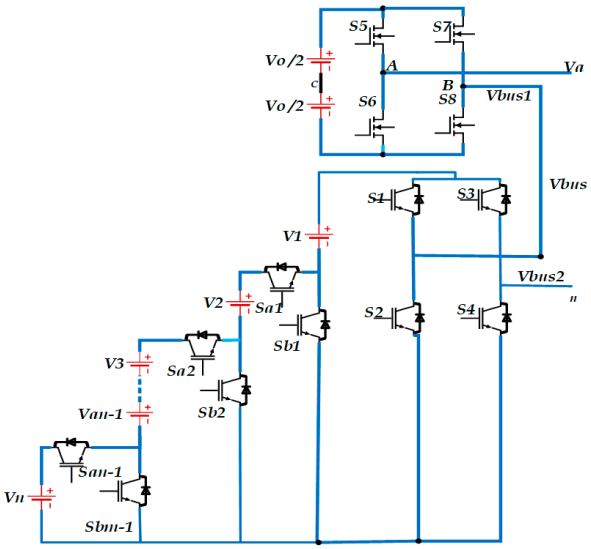

Figure 10. 15−Level MLI.

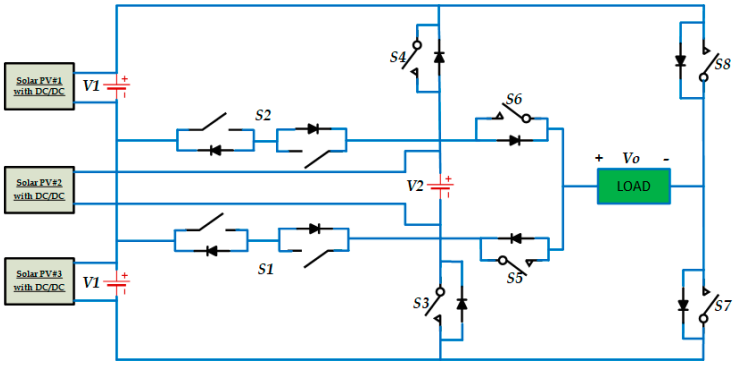

Figure 11. 13−Level MLI.

The reliability of the proposed structure is the major factor to be considered, and is calculated with the help of fault analysis.

2.1.5. Using Two DC Sources

In [71], the device generates fewer levels. In [72], it requires N DC sources for the N level. In [73–75], because of the presence of pulsating input currents, this is not appropriate for different applications. The proposed [34] structure has less conduction loss because of low diode counts, and has a higher gain value. Figure 12 involves non-coupled inductors $(L1a,\ L1b,\ L2a,\ L2b)$, capacitors $(C1, C2, Cm1, C0)$, switches $(T1,1,\ T1,2,\ T1,3\ , T2,1,\ T2,1,\ T2,2,\ Q\ )$, and diodes $(Dm1,\ D2)$, and presents a fundamental dual topology. Here in the circuit, two voltage sources are named $(V1)$ (either storable or non-storable) and $(V2)$. Assuming the voltage source $(V1)$ is storable, it can transfer energy or, in all likelihood, it can take from another source. At the point when the power flow is unidirectional, the component (Q) can be replaced by a diode. $Cm1$ is used to further develop the voltage gain of the converter. In this topology, peak inverse voltage (PIV) assumes an imperative part, where it shows the tremendous effect on the switches, and subsequently the cost of the system is decreased. To avoid this condition, another new quantity is carried out, i.e., $(NPIV)$, which is given by

$$NPIV = \left[\left(\frac{PIV}{V_o}\right)\right] \tag{18}$$

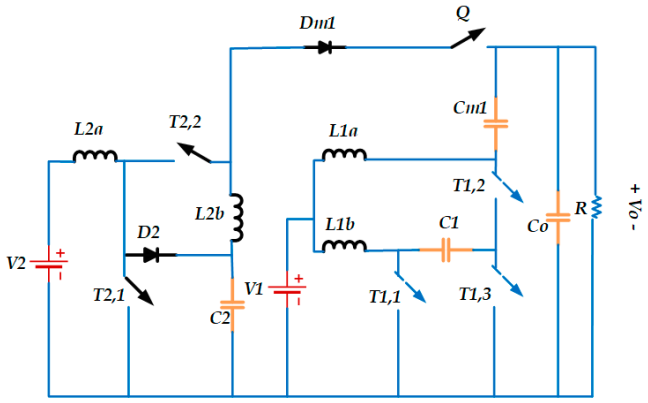

Figure 12. Dual Input Topology.

Ripple currents produced are due to inductors, which are directly proportional to the switching frequency. Further, this topology can be changed, and only 4n switches are utilized to create the higher level. This results in the output voltage being boosted to 19 times that of the input voltage. When contrasted with [76–87], the proposed topology [88,89] has a maximum efficiency of 99.06%. Unidirectional switches and DC sources accomplish the maximum output. Voltage DC sources are organized differently to obtain five-level results shown in Figure 13. The SKHI 10/12R gate driver circuit is connected to a heat sink, which lessens internal temperatures. Here 'E' represents the source voltage, Phases are represented with A, B, C. The switches in the Circuit are represented from (S1–S12) and finally 0 represents the reference/ground value.

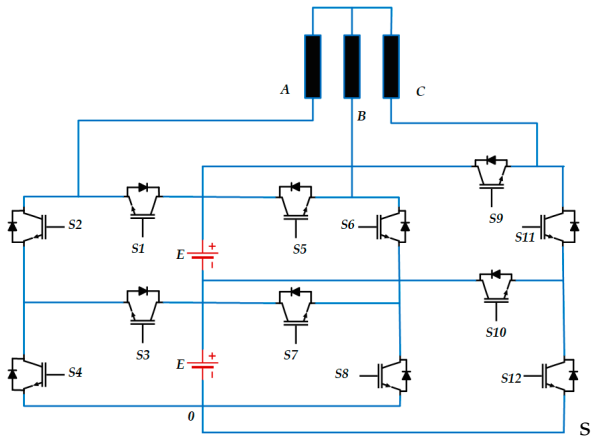

Figure 13. 5−Level MLI.

2.1.6. Using One DC Source

In [90–93] four capacitors find a use for a nine-level MLI. Because of the utilization of capacitors, inrush currents and voltage spikes across the diodes bring lower efficiency. Every one of the referenced drawbacks is changed in the [39], where it employs just three capacitors with one DC source. Figure 14 looks like an 'M'; thus, it is named an M-type switched capacitor MLI (MSCMLI). No H-bridge circuit is used. Out of 13, only 4 switches $(S10 - S13)$ will be operated once in the fundamental cycle, and the excess switches $(S6,\ S8,\ S9)$ will perform for the other method of operation. As such, the circuit will create all certain and negative levels in the result, which, accordingly, reduces the switching losses. The switches are matched to be integral $(S1 - S3)$ and $(S2 - S4)$ The level-1 is generated directly from the DC source and receives $(\pm Vdc)$, level-2 is obtained by adding the capacitor $(C1)$ that turns the switch $(S3)$ and receives the voltage $(\pm 2Vdc)$. The level-3 is delivered by adding the capacitors $(C1)$ and $(C2)$ and producing the $(\pm 3Vdc)$.

As such we can generate all levels. Where Pl represents the conduction loss, $Rint$ denotes for the internal resistance

$$\text{Conduction loss is given by } P_l = \frac{1}{2\pi}\int R_{int}\, I_c^2 d\omega t \tag{19}$$

$$\text{Total Standing Voltage is given by } TSV = \frac{TSV\ of\ all\ the\ indicidual\ switches}{peak\ value\ of\ output} \tag{20}$$

The cost factor is given by

$$CF = [N_{sw} + N_{dr} + N_d + N_c + \left(\delta * \frac{\text{TPSV}}{\text{Gain}}\right)](\frac{N_{dc}}{N_l}) \tag{21}$$

Nsw—defines the number of switches used in the topology, Ndr—states the number of gate driver circuits, $\frac{Ndc}{Nl}$, represents the number of DC sources ratio to that of the number of voltage levels generated, Nd and Nc belong to the number of diodes and capacitors employed in the circuit.

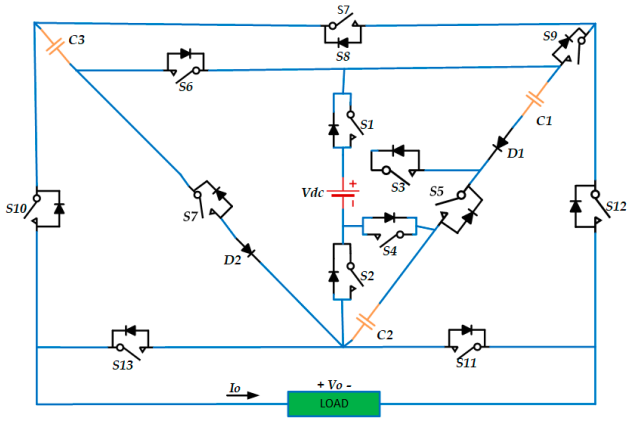

Figure 14. 13−Level MLI.

The switches used in the suggested structure [38] have only 10 switches compared to [94–97]. It engages just four self-capacitors, and every capacitor is boosted to three multiple times and generates higher levels with a short of one DC source, shown in Figure 15. In light of the switched capacitors, it is called cross-switched hybrid MLI, and is developed where the voltage is boosted to 1.5 times at the output side. The circuit is made with one DC source, with switches ranging from $(S1 - S12)$, diodes $(D1 - D4)$, and capacitors $(C1,\ C2,\ Cf1,\ Cf2)$. Here, we additionally have the complementary switch sets as $(S9, S10)$ and $(S11,\ S12)$. By utilising the series-parallel balancing rule, capacitors present in the circuit are self-charged to Vm. Switches $(S11\ and\ S12)$ have the voltage stress as $(2Vin)$; different switches will more often have voltage stress of just Vin. Capacitors $(C1\ and\ C2)$ have oneself charge capacity of Vin, and the excess capacitors $(Cf1\ and\ Cf2)$ have a value of $0.5Vin$. In the proposed CHI, the primary level of the positive half cycle is $(\pm 0.5Vin)$, which is acquired by subtracting $(Vcf1\ and\ Vin)$. Similarly, the negative half cycle the capacitor $C1$ is in charging mode up to $(-2Vin)$. The relevant equations for the respective circuit topology are stated in Equations (22)–(24). Where, f_s—is termed as the switching frequency, C_p—relates to parasitic capacitor at the blocking voltage V_B, and f_o defines the fundamental frequency

$$\text{Switching loss is given by } P_l = \frac{1}{2} f_s C_p V_B^2 \tag{22}$$

$$\text{Ripple loss is given by } P_r = \frac{1}{2} f_o C \Delta V_c^2 \tag{23}$$

$$\text{Ohmic loss is given by } P_o = I_o^2(4R_s + 2R_d + R_c)I_o = \frac{V_{in} - 2V_d - V_{cf1}}{4R_s + 2R_d + R_c} \quad (24)$$

where, I_o is the current referred-to output, V_{in} is the input voltage, V_d is the voltage drop of the diode, R_s—is the switch resistance, R_d—is the diode resistance, R_c—is the capacitor resistance.

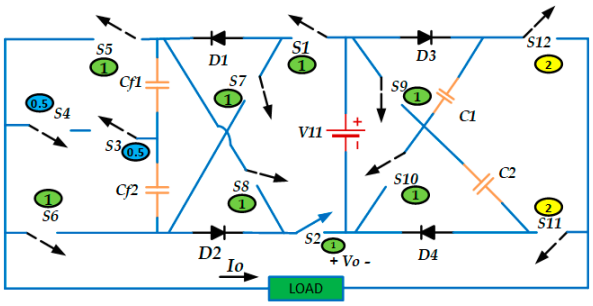

Figure 15. 13−Level MLI.

The output frequencies are 50 Hz and 400 Hz, which can be used for high switching operations.

2.2. MLI Design Based on the Application

The designed topologies are applied to various applications, some of which are mentioned below.

2.2.1. PV System Based/RES Applications

In [97], the FCML structure is intended to apply for lower voltage power switches. Accordingly, it has low ON resistance. To meet the utilization of 800 V, a three-stage AC/DC converter with GaN power semiconductors was developed with lesser losses. The scaling laws in the circuit show that it needs at least six levels to meet the load. These are primarily employed in aircraft motor drives. The effectiveness factor is additionally high when contrasted with different topologies. Ref. [98] uses the designed structure for charging station (CS) applications. The CS is planned where it coordinates the grid and the renewable energy source (RES). Power can sometimes be bidirectional, for this topology is intended to produce a three-level waveform among every leg and have a neutral point. When contrasted with a regular inverter, it lowers the filter circuits, voltage stresses, and unity power factors regardless of the functional model. It likewise balances the voltage across the capacitors. In [99], the 11-level is produced by SC-MLI, which delivers a voltage gain of 1.4 times more than the DC connect voltage appropriate for PV-based distribution systems. Ref. [100] refers to opto-isolation devices separating the voltage (either low/high) segments. The 1-φ, 13-level H-bridge inverter, which handles photovoltaic applications where it lessens the THD and has low frequencies (650 Hz), improves the efficiency. A chip ARM regulator is utilized to accomplish high efficiency at 180 MHz.

2.2.2. Electric Vehicles (EV)

In [101], the multi-input multi-output DC converter structure is designed, which has the most reliable and efficient operation. Single-input multiple-output (SIMO) has voltage gain where it is high, continuous input current, and soft switching. This can be applied to isolated and non-isolated forms [102]. Supercapacitors work for high-power density applications. The DC converter structure is designed with two bidirectional switches, and the voltage is boosted without a transformer. DC link voltage is kept constant, which is fed to the motor. The capacitor can be charged/discharged during the buck and boost operation, proposing the usage of a seven level MLI, where every one of the switches is associated in series. This is done to decrease the switching losses concerning switching frequency. The THD results are 11%. It likewise lessens the strain on the switches. For each two-level,

an IGBT/Diode switch is added. Blocking voltage is varied with the levels of clamping diodes. In [103], the NPC inverter builds effectiveness. The designed topology diminishes the weight on the switch, THD, and EMI. Overall, the quality of power is improved. In NPC-MLI is created with an independent DC source, which is utilized. It gives better power management while charging/discharging the battery [104]. To accomplish the objectives of the inverter, such as high-power density and low cost for traction drives, higher stable activity of the DC interface is required. By further developing the DC-link, EMI and voltage stress are the significant disadvantages. A [105], for lessening the size, weight, and filtering equipment of the multi-port converter, is created. This is particularly intended for electric vehicle applications with the utilization of hybrid energy storage systems. This builds the battery duration and the condition of charge level.

2.2.3. Motor Drive Applications

In [106], a cascaded T-Type multilevel inverter (CT2MLI) is proposed and applied to AC 415 V industrial application. In this, the converter shares a common emitter (CE) configuration. Along these lines, only one driver circuit is sufficient [107]. The designed topology is applied for PMSM drive applications. Where it works by double-level VSI for two and multilevel modes [108] by utilizing FCML structure in the inverter, the utilization of wideband gap (WBG) switches, and the exhibition of two-level 1200 V SiC switches, low voltage GaN HEMT switches accomplish 15.8 KW/dm^3 power density with an efficiency of 99.03%, and ML leg efficiency is noticed. It benefits 3-phase variable speed drives [109]. The designed converter uses eight switches, and is named the eight switches bridge converter (ESBC). This works to drive the brushless direct current motor (BLDCM), where the motor phases become detached through various switches. This likewise improves the system's reliability during fault conditions. In [105], a five-level diode clamped inverter is proposed to simplify the circuit, be robust-free, and have a great unique response. This is applied for direct torque control (DTC) and field-oriented control (FOC) in motor applications. In [110], different switching operations of the nine-level inverter are required to develop the dynamic load changing and the settling time of the applied induction motor further. The author in [16] presents that, although zero voltage vectors might also be employed, they appear to be useful for induction motor direct torque control in the OVT-ST inverter.

2.2.4. Industrial Applications

In [111], two identical DC–AC inverters are connected in parallel with the assistance of the standard capacitor. The designed circuit benefits high-power applications and accomplishes the greatest efficiency of 93.7%. In [112], the multi-port converters are (a) MISO-able to work as boost and Cuk converters (b) SIMO-switch losses are diminished, and (c) MIMO-different duty cycles can be worked for various modes and are proposed and utilized for high/low-level applications.

2.2.5. Multi-Purpose and Other Applications

The novel converter planned in [112] has simple and reliable inactivity, and can be applied for various AC–DC, DC–DC, DC–AC, and AC–AC applications. While utilizing traditional inverters because of many disadvantages, many adjusted forms of MLI are created. In [113], switched capacitor (SC) is developed, the voltage levels are greater in number, and the voltage level is boosted. Capacitors and inductors are eliminated within this topology to decrease the system's weight and cost. Along these lines, the effectiveness of the circuit can be improved to high and further develop the energy density. It is applied for AC–DC/DC–AC power conversions [113]. For different applications, such as EV and aerospace, the MLI is designed using silicon (Si) and gallium nitride (GaN). GaN e-FETs are preferred more than Si MOSFETs because the component is a three [114] plan 3φ five-level CHB, even though MLI employs 24 switches, produces more voltage, and utilizes only two separate DC sources. Results in [115] show that the THD is diminished, and power quality is further developed when the VFISPWM technique is applied to multi-purpose

applications. The authors of [116] proposed an inverter which is designed so that it has just a couple of parts counts, and it is used for naval ship propulsion rectifier applications.

3. Modulation Techniques for Derived Converters

Different modulation schemes are accessible to control the operations in the inverter. A portion of these is informed here. Changing the voltage or frequency waveform modulation technique finds use where it involves two signs: the carrier signal and the reference signal. By changing the pulse width in the sinewave, the resulting levels of the voltage/frequency are modified. For the most part, the pulse width modulation (PWM) methods are created to diminish the operations and switching losses, and to further develop the system's efficiency [117]. Overall, modulation methods are grouped into two classifications. Low frequency/high switching frequency, which is sub characterized by (a) selective harmonic elimination (SHE), (b) nearest vector, (c) nearest level, and (d) hybrid modulation. The second one is high switching frequency, and it is sub-delegated by (a) multi carrier PWM is further classified as phase shifted and level shifted, phase disposition (PD-PWM) which is in phase with each carrier, phase opposition disposition (POD-PWM) where carriers are in phase above the zero references and below 180° out of phase, alternate phase opposition disposition (APOD-PWM) which is 180° out of the phase, (b) space vector modulation (2D-Algorithm and 3D-Algorithm) and (c) hybrid modulation. According to the accessibility and the suitability, these techniques are utilized.

Figure 16 classifies the commonly used modulation techniques. In [2], the carrier-based PWM technique is easy to implement and control. Output can be modulated using CBPWM. SVPWM is used for controlling the neutral point; also, [115] was used to calculate the timings of the modulation with level information. Nearest vector PWM is a part of SVPWM, similar to CBPWM [11]. SVPWM gives the exact switching sequences; it can be derived from the dwell times with easy computational effects and can be implemented in FPGA. Ref. [116] proposes the two frequency operations. Firstly, the low-frequency modulation, where the works are with a f = 50 Hz grid, supply frequency. It generates a qualified output waveform. Cost and efficiency are added parameters. Secondly, high-frequency modulation works with a switching frequency of 200 KHz. Duty cycles are controlled to obtain the desired output voltage at a particular frequency (f) [5]. Spatial vector represents the recommended SVPWM. It is made of three hexagons, whose size fluctuates depending on the DC input voltages [6]. Conventional CII uses common carrier interleaving or a discontinuous form of PWM (DPWM). Line PWM frequency is always equal to $(2 \times n \times fc)$. Standard interleaving and carrier manipulation schemes are employed. In [117], for a seven-level symmetrical inverter, the modulation index is given as $m = \frac{\pi V1}{4*3Vdc}$ [30]. NPC topologies use (PD-SPWM) [53]. Modified PWM control strategy uses triangular signals as carrier signals and sinewaves as reference signals. PD strategy is used for carrier signals with a switching frequency of 1.1 KHz. Only two switching angles are required to calculate five-level output.

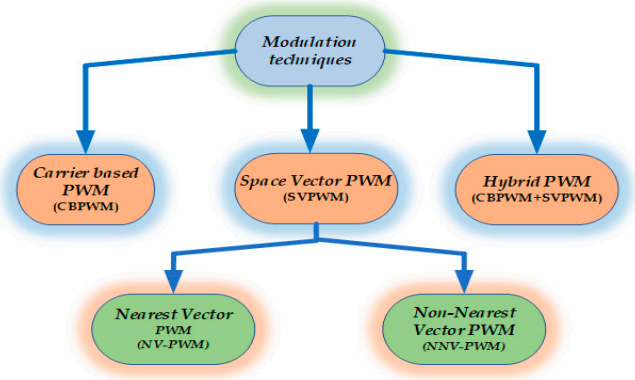

Figure 16. Classification of different modulation techniques.

Refs. [29,31] involves a P&O calculation-based MPPT procedure for the applications to extricate the maximum power from the PV array; the stable output is accomplished under all conditions (even partially shaded conditions).

3.1. Fundamental Frequency Switching (FFS) and High-Frequency Switching (HFS)

In [28], NLC control exchanges tasks and decreases THD. Reference [30] employs fundamental frequency switching (FFS), which is sub-classified as low switching frequency (LFS) and high switching frequency (HFS) [33]. It has an open loop and closed loop switching for specific applications [37]. It works so that only one switching operation is permitted in turn. Subsequently, it diminishes the losses in the system and accomplishes higher energy levels with minimal expense [38]. NLC is mostly used for higher levels because of its simple control [39]. It enjoys a significant benefit in that the computation angle switching can effectively store these qualities in the lookup table by the processor, and is perfectly carried out. Ref. [118] is used for a more severe level of adaptability in the exchanging activity with variable magnitude count.

3.2. Selective Harmonic Elimination (SHE)

In [32], to dispense with the odd-order harmonics (third, fifth, seventh, ninth, eleventh, thirteenth, fifteenth), PSO calculation is carried out in the selective harmonic elimination strategy [34,35]. PS1 structure utilizes carrier-based SPWM techniques [107], and the respective highlights of SHE are mentioned in Table 3. It likewise collaborates with the NR strategy for solving the angles of non-linear equations.

$$V(\omega t) = a_0/2 + \sum_{n=1}^{\infty}(a_n \cos(n\omega t) + b_n \sin(n\omega t) \quad (25)$$

Table 3. SHE-PWM technique advantages.

Type of Technique	Pros
SHE-PWM	✓ It has low switching frequency/low operation and conduction losses
	✓ In a single phase, triple harmonics are controlled.
	✓ Heavy computational calculations are reduced.
	✓ Balancing and unequal distribution of voltages can be controlled in the case of DC-link.
	✓ It can be dealt with in any switching pattern.
	✓ Dominant harmonics are monitored with intelligent algorithms in real-data implementation.

3.3. Pulse Width Modulation (PWM)

Refs. [37,115] utilize pulse width modulation, where level shifted and phase shifted schemes play a vital role in this strategy [40]. FPGA-based harmonic reduction (HR) calculations can likewise be carried out in the strategy [103]. Harmonics in this scheme are limited, and voltage adjusting can be accomplished [15]. Additionally, FFT investigation and current strategies can likewise be carried out in numerous applications, and advantages related to PS-PWM are mentioned in Table 4.

Table 4. PS-PWM technique advantages.

Type of Technique	Pros
PS-PWM	✓ MLI performance is balanced throughout the operation during the charging/discharging process.
	✓ It results in low leakage power and loss, therefore resulting in high efficiency.
	✓ It avoids leakage currents when applied to grid-connected systems.
	✓ It operates in a safer region with a high switching frequency.

3.4. Predictive Torque Control

In [107], the authors present the predictive torque control (PTC) and model predictive control (MPC) methods for calculating the errors present in the motor drives [105]. This additionally works on the decrease in system ripples and reduces the switching frequency.

3.5. Perturb and Observe (P&O) and MPPT-Based Approach

An MPPT controller is used to operate solar PV to extract the maximum power possible from the PV module. Solar PV's efficiency and life span have improved throughout all of the disruptions above. The solar source can be set to the load to obtain maximum power production under different climatic conditions. By adjusting the voltage from the array by a small amount, the controller measures the power and, if it rises, performs more adjustments in that direction until the power stops rising [29]. The most popular strategy is perturb and observe (P&O), which might lead to power output oscillations. It is often referred to as the "hill climbing" technique, since it depends on the power versus voltage curve rising below the maximum power point and falling above it [32]. The perturb and observe method is the most used since it is so simple.

4. Conclusions

The study covers recent developments in the recently established MLI, where different topologies are compared with the conventional inverters to continue research and advancement in multi-level generations. As a result, it is understood that each topology has a distinct feature that leads to significant inherent benefits, such as a decrease in switching losses, voltage ripples, voltage stress, active switches, diodes, capacitors, and driver circuits. In addition, there are reductions in DC sources, TSV, TBV, THD, EMI issues, standard mode voltages, fault operations, quality output voltage, cost, volume, and weight, which improve the efficiency that aids in reducing the complexity of inverters. These are mostly preferred for RECS, PV, EV, and industrial drive applications. Comparative analysis with different topologies also made for a clear understanding. Asymmetrical configurations with different topologies, their operations, benefits, and applications are explained in a broad way. In some topologies of the circulating inrush currents, voltage balancing is minimal. Various modulation techniques and control schemes are also highlighted to know which will suit a particular application. It can be observed that the maximum efficiency achieved is 99.06%, and the THD factor is 1.41%. The extensive review shows that MLI faced many problems, such as high switching rating, larger filtering devices for distortion-free output, heating problems, more sensing components, and a lack of DC sources. For switching/frequency operations for higher levels, GaN/SiC switches are preferred solutions due to their inherent benefits such as high thermal conductivity, which also lowers the device count.

Author Contributions: Conceptualization, K.N.D.V.S.E. and M.A.N.D.; methodology, M.B.; software, P.V.; validation, M.B. and H.K.; formal analysis, K.N.D.V.S.E. and M.A.N.D.; investigation K.N.D.V.S.E., M.A.N.D. and A.S.; resources, P.V. and S.K.; data curation, K.N.D.V.S.E.; writing—K.N.D.V.S.E.; writing—review and editing, M.B. and H.K.; visualization, A.S. and H.K.; supervision, M.A.N.D. and P.V.; project administration, M.A.N.D., P.V., A.S. and S.K.; funding acquisition, S.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by Science, Technology & Innovation Funding Authority (STDF) under grant (43180).

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

MLI	Multilevel Inverter
THD	Total Harmonic Distortion
PWM	Pulse Width Modulation
EV	Electric Vehicle
PV	Photovoltaic
RECS	Renewable Energy Conventional Sources
UPS	Uninterrupted Power Supply
RE	Renewable Energy
V2G	Vehicle-to-Grid
EMC/EMI	Electromagnetic Compatibility/Electromagnetic Interference
TBV	Total Blocking Voltage
TSV	Total Standing Voltage
SC	Super Capacitor
VSI	Voltage Source Inverters
CSI	Current Source Inverters
Q-ZSI	Quasi-impedance Source Inverters
SC	Super Capacitor
SOC	State of Charge
SOD	State of Discharge
SCSS	Switched Connected Switched Sources
SSPS	Switched Series Parallel Sources
IGBT	Insulated Gate Bi-polar Transistor
MOSFET	Metal Oxide Converter Field Effect Transistor
SC-MLI	Switched Capacitor—Multilevel Inverter
PIV	Peak Inverse Voltage
WBG	Wide Band Gap
LV	Low Voltage
HV	High Voltage
LDC	Level Doubling Circuits

References

1. Kumar, G.G.; Krishna, M.V.S.; Kumaravel, S.; Babaei, E. Multi-Stage DC-DC Converter Using Active LC2D Network with Minimum Component. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *68*, 943–947. [CrossRef]
2. Raju, K.N.; Rao, M.V.G.; Ramamoorthy, M. Hybrid modulation technique for neutral point clamped inverter to eliminate neutral point shift with minimum switching loss. In Proceedings of the TENCON 2015—2015 IEEE Region 10 Conference, Macao, China, 1–4 November 2015; Volume 2016, pp. 1–5. [CrossRef]
3. Rawa, M.; Ali, J.M.; Siddique, M.; Mekhilef, S.; Wahyudie, A.; Seyedmahmoudian, M.; Stojcevski, A. A new multilevel inverter topology with reduced dc sources. *Energies* **2021**, *14*, 4709. [CrossRef]
4. Mamede, H.R.; Santos, W.M.D.; Coelho, R.F.; Martins, D.C. A multicell Dual-Active Bridge converter for increasing the reliability of power supply in a DC microgrid. In Proceedings of the 2015 IEEE First International Conference on DC Microgrids (ICDCM), Atlanta, GA, USA, 7–10 June 2015; pp. 274–279. [CrossRef]
5. Dorn-Gomba, L.; Guo, J.; Emadi, A. Multi-source inverter for power-split hybrid electric powertrains. *IEEE Trans. Veh. Technol.* **2019**, *68*, 6481–6494. [CrossRef]
6. Tripathi, R.S.; Thukral, M.K. Switching Angles Computation of Multi-Level Inverter for Electrical Vehicle Application. In Proceedings of the 2019 Global Conference for Advancement in Technology (GCAT), Bangalore, India, 18–20 October 2019; pp. 5–9. [CrossRef]
7. Sathik, J.; Aleem, S.H.E.A.; Alishah, R.S.; Almakhles, D.; Bertilsson, K.; Bhaskar, M.S.; Savier, G.F.; Dhandapani, K. A multilevel inverter topology using diode half-bridge circuit with reduced power component. *Energies* **2021**, *14*, 7249. [CrossRef]
8. Bassi, H.M.; Salam, Z. A new hybrid multilevel inverter topology with reduced switch count and dc voltage sources. *Energies* **2019**, *12*, 977. [CrossRef]
9. Gopal, Y.; Birla, D.; Lalwani, M. Selected Harmonic Elimination for Cascaded Multilevel Inverter Based on Photovoltaic with Fuzzy Logic Control Maximum Power Point Tracking Technique. *Technologies* **2018**, *6*, 62. [CrossRef]
10. Iwaszkiewicz, J.; Bogusławski, P.; Krahel, A.; Łowiec, E. Three-phase voltage outages compensator with cascaded multilevel converter. *Arch. Electr. Eng.* **2012**, *61*, 325–336. [CrossRef]

11. Pallo, N.; Coday, S.; Schaadt, J.; Assem, P.; Pilawa-Podgurski, R.C.N. A 10-Level Flying Capacitor Multi-Level Dual-Interleaved Power Module for Scalable and Power-Dense Electric Drives. In Proceedings of the 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 15–19 March 2020; pp. 893–898. [CrossRef]
12. Nabae, A.; Takahashi, I.; Akagi, H. A New Neutral-Point-Clamped PWM Inverter. *IEEE Trans. Ind. Appl.* **1981**, *IA-17*, 518–523. [CrossRef]
13. Tsai, C.T.; Chen, W.M. Buck converter with soft-switching cells for PV panel applications. *Energies* **2016**, *9*, 148. [CrossRef]
14. Tobón, A.; Peláez-Restrepo, J.; Villegas-Ceballos, J.P.; Serna-Garcés, S.I.; Herrera, J.; Ibeas, A. Maximum power point tracking of photovoltaic panels by using improved pattern search methods. *Energies* **2017**, *10*, 1316. [CrossRef]
15. Siddique, M.D.; Mekhilef, S.; Shah, N.M.; Sarwar, A.; Iqbal, A.; Memon, M.A. A New Multilevel Inverter Topology with Reduce Switch Count. *IEEE Access* **2019**, *7*, 58584–58594. [CrossRef]
16. Hashad, M.; Iwaszkiewicz, J. A novel orthogonal-vectors-based topology of multilevel inverters. *IEEE Trans. Ind. Electron.* **2002**, *49*, 868–874. [CrossRef]
17. Lin, B.R.; Zhuang, Y.S.; Syu, H.S. Parallel soft switching converters: Analysis, design and implementation. In Proceedings of the 2018 13th IEEE Conference on Industrial Electronics and Applications (ICIEA), Wuhan, China, 31 May–2 June 2018; pp. 1016–1021. [CrossRef]
18. Pharne, I.D.; Bhosale, Y.N. A review on multilevel inverter topology. In Proceedings of the 2013 International Conference on Power, Energy and Control (ICPEC), Dindigul, India, 6–8 February 2013; pp. 700–703. [CrossRef]
19. Hasan, N.S.; Rosmin, N.; Osman, D.A.A.; Musta'Amal@jamal, A.H. Reviews on multilevel converter and modulation techniques. *Renew. Sustain. Energy Rev.* **2017**, *80*, 163–174. [CrossRef]
20. Rodriguez, J.; Bernet, S.; Steimer, P.K.; Lizama, I.E. A Survey on Neutral-Point-Clamped Inverters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2219–2230. [CrossRef]
21. Roy, A.D.; Umayal, C. A review of various multilevel inverter topologies with reduced component count. In Proceedings of the 2018 International Conference on Recent Trends in Electrical, Control and Communication (RTECC), Malaysia, 20–22 March 2018; pp. 234–239. [CrossRef]
22. Choudhury, S.; Bajaj, M.; Dash, T.; Kamel, S.; Jurado, F. Multilevel Inverter: A Survey on Classical and Advanced Topologies, Control Schemes, Applications to Power System and Future Prospects. *Energies* **2021**, *14*, 5773. [CrossRef]
23. Venkataramanaiah, J.; Suresh, Y.; Panda, A.K. A review on symmetric, asymmetric, hybrid and single DC sources based multilevel inverter topologies. *Renew. Sustain. Energy Rev.* **2017**, *76*, 788–812. [CrossRef]
24. McGrath, B.P.; Holmes, D.G. Analytical modelling of voltage balance dynamics for a flying capacitor multilevel converter. In Proceedings of the 2007 IEEE Power Electronics Specialists Conference, Orlando, FL, USA, 17–21 June 2007; Volume 23, pp. 1810–1816. [CrossRef]
25. Prabaharan, N.; Palanisamy, K. A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications. *Renew. Sustain. Energy Rev.* **2017**, *76*, 1248–1282. [CrossRef]
26. Malinowski, M.; Gopakumar, K.; Rodriguez, J.; Perez, M.A. A survey on cascaded multilevel inverters. *IEEE Trans. Ind. Electron.* **2009**, *57*, 2197–2206. [CrossRef]
27. Masoudina, F.; Babaei, E.; Sabahi, M.; Alipour, H. New cascaded multilevel inverter with reduced power electronic components. *Iran. J. Electr. Electron. Eng.* **2020**, *16*, 107–113. [CrossRef]
28. Dhanamjayulu, C.; Padmanaban, S.; Ramachandaramurthy, V.K.; Holm-Nielsen, J.B.; Blaabjerg, F. Design and Implementation of Multilevel Inverters for Electric Vehicles. *IEEE Access* **2020**, *9*, 317–338. [CrossRef]
29. Varesi, K.; Karimi, M.; Kargar, P. A New Cascaded 35-Level Inverter with Reduced Switch Count. In Proceedings of the 2019 Iranian Conference on Renewable Energy & Distributed Generation (ICREDG), Tehran, Iran, 11–12 June 2019; pp. 11–12. [CrossRef]
30. Hosseinzadeh, M.A.; Sarbanzadeh, M.; Sarbanzadeh, E.; Rivera, M.; Wheeler, P. New Asymmetric Cascaded Multi-level Converter with Reduced Components. In Proceedings of the 2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), Nottingham, UK, 7–9 November 2018; pp. 7–12. [CrossRef]
31. Khasim, S.R.; Dhanamjayulu, C.; Padmanaban, S.; Holm-Nielsen, J.B.; Mitolo, M. A Novel Asymmetrical 21-Level Inverter for Solar PV Energy System with Reduced Switch Count. *IEEE Access* **2021**, *9*, 11761–11775. [CrossRef]
32. Bana, P.R.; Panda, K.P.; Panda, G. Power Quality Performance Evaluation of Multilevel Inverter with Reduced Switching Devices and Minimum Standing Voltage. *IEEE Trans. Ind. Inform.* **2020**, *16*, 5009–5022. [CrossRef]
33. Varesi, K.; Hosseini, S.H.; Sabahi, M.; Babaei, E.; Saeidabadi, S.; Vosoughi, N. Design and Analysis of a Developed Multiport High Step-Up DC-DC Converter with Reduced Device Count and Normalized Peak Inverse Voltage on the Switches/Diodes. *IEEE Trans. Power Electron.* **2019**, *34*, 5464–5475. [CrossRef]
34. Panda, K.P.; Bana, P.R.; Panda, G. Design and Control of An Asymmetrical Cascaded Compact Module Multilevel Inverter for PV System. In Proceedings of the TENCON 2019-2019 IEEE Region 10 Conference (TENCON), Kochi, India, 17–20 October 2019; pp. 2616–2621. [CrossRef]
35. Ebadpour, M.; Bagher, M.; Sharifian, B.; Hosseini, S.H. A New Structure of Multilevel Inverter with Reduced Number of Switches for Electric Vehicle Applications. *Energy Power Eng.* **2011**, *3*, 198. [CrossRef]

36. Siddique, M.D.; Rawa, M.; Mekhilef, S.; Shah, N.M. A new cascaded asymmetrical multilevel inverter based on switched dc voltage sources. *Int. J. Electr. Power Energy Syst.* **2021**, *128*, 106730. [CrossRef]
37. Panda, K.P.; Bana, P.R.; Panda, G. A Reduced Device Count Single DC Hybrid Switched-Capacitor Self-Balanced Inverter. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 978–982. [CrossRef]
38. Panda, K.P.; Bana, P.R.; Panda, G. A Switched-Capacitor Self-Balanced High-Gain Multilevel Inverter Employing a Single DC Source. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 3192–3196. [CrossRef]
39. Kanimozhi, M.; Ramaprabha, R. Design of 500W standalone photovoltaic system with reduced switch count multilevel inverter. In Proceedings of the 2017 Trends in Industrial Measurement and Automation (TIMA), Chennai, India, 6–8 January 2017; pp. 4–10. [CrossRef]
40. Salem, A.; van Khang, H.; Robbersmyr, K.G.; Norambuena, M.; Rodriguez, J. Novel Three-Phase Multilevel Inverter with Reduced Components for Low- and High-Voltage Applications. *IEEE Trans. Ind. Electron.* **2021**, *68*, 5978–5989. [CrossRef]
41. Amadeh-Roodmajan, M.; Monfared, M.; Hashemizadeh-Ashan, S. A single-phase cascaded multilevel inverter composed of four-level sub-multilevel cells. In Proceedings of the 2017 8th Power Electronics, Drive Systems & Technologies Conference (PEDSTC), Mashhad, Iran, 14–16 February 2017; pp. 389–394. [CrossRef]
42. Gohari, A.; Mosallanejad, A.; Afjei, E. New symmetric cascaded multilevel inverter with reduced number of controlled devices and low blocked voltage by switches. In Proceedings of the 2017 8th Power Electronics, Drive Systems & Technologies Conference (PEDSTC), Mashhad, Iran, 14–16 February 2017; pp. 502–506.
43. Manjrekar, M.; Lipo, T. Hybrid multilevel inverter topology for drive applications. In Proceedings of the APEC'98 Thirteenth Annual Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 15–19 February 1998; Volume 2, pp. 523–529. [CrossRef]
44. Liu, J.; Cheng, K.W.E.; Ye, Y. A cascaded multilevel inverter based on switched-capacitor for high-frequency AC power distribution system. *IEEE Trans. Power Electron.* **2014**, *29*, 4219–4230. [CrossRef]
45. Samadaei, E.; Sheikholeslami, A.; Gholamian, S.A.; Adabi, J. A Square T-Type (ST-Type) Module for Asymmetrical Multilevel Inverters. *IEEE Trans. Power Electron.* **2018**, *33*, 987–996. [CrossRef]
46. Choi, J.S.; Kang, F.S. Seven-level PWM inverter employing series-connected capacitors paralleled to a single DC voltage source. *IEEE Trans. Ind. Electron.* **2015**, *62*, 3448–3459. [CrossRef]
47. Dhanamjayulu, C.; Meikandasivam, S. Implementation and Comparison of Symmetric and Asymmetric Multilevel Inverters for Dynamic Loads. *IEEE Access* **2017**, *6*, 738–746. [CrossRef]
48. Babaei, E.; Kangarlu, M.F.; Sabahi, M. Extended multilevel converters: An attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters. *IET Power Electron.* **2014**, *7*, 157–166. [CrossRef]
49. Babaei, E.; Gowgani, S.S. Hybrid multilevel inverter using switched capacitor units. *IEEE Trans. Ind. Electron.* **2014**, *61*, 4614–4621. [CrossRef]
50. Panda, K.P.; Panda, G. Application of swarm optimisation-based modified algorithm for selective harmonic elimination in reduced switch count multilevel inverter. *IET Power Electron.* **2018**, *11*, 1472–1482. [CrossRef]
51. Zhang, J.; Zou, Y.; Zhang, X.; Ding, K. Study on a modified multilevel cascade inverter with hybrid modulation. In Proceedings of the 4th IEEE International Conference on Power Electronics and Drive Systems. IEEE PEDS 2001—Indonesia. Proceedings (Cat. No.01TH8594), Denpasar, Indonesia, 25 October 2001; Volume 1, pp. 379–383. [CrossRef]
52. Liu, H.; Tolbert, L.M.; Khomfoi, S.; Ozpineci, B.; Du, Z. Hybrid cascaded multilevel inverter with PWM control method. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 162–166. [CrossRef]
53. Andela, M.; Shaik, A.; Beemagoni, S.; Kurimilla, V.; Veramalla, R.; Kodakkal, A.; Salkuti, S.R. Solar Photovoltaic System-Based Reduced Switch Multilevel Inverter for Improved Power Quality. *Clean Technol.* **2022**, *4*, 1–13. [CrossRef]
54. Babaei, E.; Laali, S.; Bayat, Z. A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches. *IEEE Trans. Ind. Electron.* **2015**, *62*, 922–929. [CrossRef]
55. Leon, J.I.; Kouro, S.; Vazquez, S.; Portillo, R.; Franquelo, L.G.; Carrasco, J.M.; Rodriguez, J. Multidimensional modulation technique for cascaded multilevel converters. *IEEE Trans. Ind. Electron.* **2011**, *58*, 412–420. [CrossRef]
56. Babaei, E.; Laali, S.; Alilu, S. Cascaded multilevel inverter with series connection of novel H-bridge basic units. *IEEE Trans. Ind. Electron.* **2014**, *61*, 6664–6671. [CrossRef]
57. Barzegarkhoo, R.; Zamiri, E.; Vosoughi, N.; Kojabadi, H.M.; Chang, L. Cascaded multilevel inverter using series connection of novel capacitor-based units with minimum switch count. *IET Power Electron.* **2016**, *9*, 2060–2075. [CrossRef]
58. Hasan, M.M.; Abu-Siada, A.; Islam, M.R. Design and implementation of a novel three-phase cascaded half-bridge inverter. *IET Power Electron.* **2016**, *9*, 1741–1752. [CrossRef]
59. Bana, P.R.; Panda, K.P.; Naayagi, R.T.; Siano, P.; Panda, G. Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application: Topologies, Comprehensive Analysis and Comparative Evaluation. *IEEE Access* **2019**, *7*, 54888–54909. [CrossRef]
60. Alishah, R.S.; Hosseini, S.H.; Babaei, E.; Sabahi, M. Optimal Design of New Cascaded Switch-Ladder Multilevel Inverter Structure. *IEEE Trans. Ind. Electron.* **2017**, *64*, 2072–2080. [CrossRef]
61. Zhou, L.W.; Zhu, B.X.; Luo, Q.M. High step-up converter with capacity of multiple input. *IET Power Electron.* **2012**, *5*, 524–531. [CrossRef]

62. Deihimi, A.; Mahmoodieh, M.E.S.; Iravani, R. A new multi-input step-up DC–DC converter for hybrid energy systems. *Electr. Power Syst. Res.* **2017**, *149*, 111–124. [CrossRef]
63. Samadaei, E.; Gholamian, S.A.; Sheikholeslami, A.; Adabi, J. An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters with Reduced Components. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7148–7156. [CrossRef]
64. Jayabalan, M.; Jeevarathinam, B.; Sandirasegarane, T. Reduced switch count pulse width modulated multilevel inverter. *IET Power Electron.* **2017**, *10*, 10–17. [CrossRef]
65. Alishah, R.S.; Hosseini, S.H.; Babaei, E.; Sabahi, M. A New General Multilevel Converter Topology Based on Cascaded Connection of Submultilevel Units with Reduced Switching Components, DC Sources, and Blocked Voltage by Switches. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7157–7164. [CrossRef]
66. Mokhberdoran, A.; Ajami, A. Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology. *IEEE Trans. Power Electron.* **2014**, *29*, 6712–6724. [CrossRef]
67. Taghvaie, A.; Adabi, J. A Self-Balanced Step-Up Multilevel Inverter Based on Switched-Capacitor Structure. *IEEE Trans. Power Electron.* **2018**, *33*, 199–209. [CrossRef]
68. Khenar, M.; Taghvaie, A.; Adabi, J.; Rezanejad, M. Multi-level inverter with combined T-type and cross-connected modules. *IET Power Electron.* **2018**, *11*, 1407–1415. [CrossRef]
69. Lin, W.; Zeng, J.; Liu, J.; Yan, Z.; Hu, R. Generalized Symmetrical Step-Up Multilevel Inverter Using Crisscross Capacitor Units. *IEEE Trans. Ind. Electron.* **2020**, *67*, 7439–7450. [CrossRef]
70. Varesi, K.; Hosseini, S.H.; Sabahi, M.; Babaei, E. A high-voltage gain nonisolated noncoupled inductor based multi-input DC-DC topology with reduced number of components for renewable energy systems. *Int. J. Circuit Theory Appl.* **2018**, *46*, 505–518. [CrossRef]
71. Banaei, M.R.; Ardi, H.; Alizadeh, R.; Farakhor, A. Non-isolated multi-input-single-output DC/DC converter for photovoltaic power generation systems. *IET Power Electron.* **2014**, *7*, 2806–2816. [CrossRef]
72. Chattopadhyay, S.K.; Chakraborty, C. A New Asymmetric Multilevel Inverter Topology Suitable for Solar PV Applications with Varying Irradiance. *IEEE Trans. Sustain. Energy* **2017**, *8*, 1496–1506. [CrossRef]
73. El-Hosainy, A.; Hamed, H.A.; Azazi, H.Z.; El-Kholy, E.E. A review of multilevel inverter topologies, control techniques, and applications. In Proceedings of the 2017 Nineteenth International Middle East Power Systems Conference (MEPCON), Cairo, Egypt, 19–21 December 2017; pp. 1265–1275. [CrossRef]
74. Lee, S.S.; Chu, B.; Idris, N.R.N.; Goh, H.H.; Heng, Y.E. Switched-Battery Boost-Multilevel Inverter with GA Optimized SHEPWM for Standalone Application. *IEEE Trans. Ind. Electron.* **2016**, *63*, 2133–2142. [CrossRef]
75. Prabaharan, N.; Palanisamy, K. Comparative analysis of symmetric and asymmetric reduced switch MLI topologies using unipolar pulse width modulation strategies. *IET Power Electron.* **2016**, *9*, 2808–2823. [CrossRef]
76. Sun, X.; Wang, B.; Zhou, Y.; Wang, W.; Du, H.; Lu, Z. A Single DC Source Cascaded Seven-Level Inverter Integrating Switched-Capacitor Techniques. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7184–7194. [CrossRef]
77. Saeidabadi, S.; Gandomi, A.A.; Hosseini, S.H.; Sabahi, M.; Gandomi, Y.A. New improved three-phase hybrid multilevel inverter with reduced number of components. *IET Power Electron.* **2017**, *10*, 1403–1412. [CrossRef]
78. Solanki, C.L.; Ayalani, M.H.; Gohil, S.N. Performance of Three Phase T-Type Multilevel Inverter with Reduced Switch Count. In Proceedings of the 2018 International Conference on Current Trends towards Converging Technologies (ICCTCT), Coimbatore, India, 1–3 March 2018; pp. 4–8. [CrossRef]
79. Guan, Q.-X.; Li, C.; Zhang, Y.; Wang, S.; Xu, D.D.; Li, W.; Ma, H. An Extremely High Efficient Three-Level Active Neutral-Point-Clamped Converter Comprising SiC and Si Hybrid Power Stages. *IEEE Trans. Power Electron.* **2018**, *33*, 8341–8352. [CrossRef]
80. Wang, Y.; Shi, W.W.; Xie, N.; Wang, C.M. Diode-free T-type three-level neutral-point-clamped inverter for low-voltage renewable energy system. *IEEE Trans. Ind. Electron.* **2014**, *61*, 6168–6174. [CrossRef]
81. Yang, F.; Ge, H.; Yang, J.; Dang, R.; Wu, H. A Family of Dual-Buck Inverters with an Extended Low-Voltage DC-Input Port for Efficiency Improvement Based on Dual-Input Pulsating Voltage-Source Cells. *IEEE Trans. Power Electron.* **2018**, *33*, 3115–3128. [CrossRef]
82. Wu, H.; Zhu, L.; Yang, F.; Mu, T.; Ge, H. Dual-DC-Port Asymmetrical Multilevel Inverters with Reduced Conversion Stages and Enhanced Conversion Efficiency. *IEEE Trans. Ind. Electron.* **2017**, *64*, 2081–2091. [CrossRef]
83. Inverter, T. A Seven-Level VSI with a Front-End Cascaded. *IEEE Trans. Ind. Appl.* **2019**, *55*, 6073–6088.
84. Salem, A.; Ahmed, E.M.; Orabi, M.; Ahmed, M. Study and Analysis of New Three-Phase Modular Multilevel Inverter. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7804–7813. [CrossRef]
85. Anderson, J.A.; Zulauf, G.; Papamanolis, P.; Hobi, S.; Miric, S.; Kolar, J.W. Three Levels Are Not Enough: Scaling Laws for Multilevel Converters in AC/DC Applications. *IEEE Trans. Power Electron.* **2021**, *36*, 3967–3986. [CrossRef]
86. Reis, F.E.U.; Torrico-Bascope, R.P.; Tofoli, F.L.; Bezerra, L.D.S. Bidirectional Three-Level Stacked Neutral-Point-Clamped Converter for Electric Vehicle Charging Stations. *IEEE Access* **2020**, *8*, 37565–37577. [CrossRef]
87. Sirohi, V.; Kumar, J.; Saggu, T.S.; Gill, B. An improved switched capacitor multi-level inverter topology with boosting capability and reduced component count. In Proceedings of the 2021 IEEE 12th Annual Information Technology, Electronics and Mobile Communication Conference (IEMCON), Vancouver, BC, Canada, 27–30 October 2021; pp. 853–857. [CrossRef]

88. Cesar, A.; Jappe, T.K.; Lazzarin, T.B.; Domingo, R.-D.; Reynaldo, A.; Luis, M.; Mussa, S.A. Performance of Three-Phase Asymmetric Multilevel Hybrid Inverter—Analysis and Experimentation. *Eletrônica De Potência* **2015**, *62*, 5983–5992.
89. Lee, S.S. Single-Stage Switched-Capacitor Module (S3CM) Topology for Cascaded Multilevel Inverter. *IEEE Trans. Power Electron.* **2018**, *33*, 8204–8207. [CrossRef]
90. Inverter, S.Q.N. Switched-Capacitor-Based Quadruple-Boost Nine-Level Inverter. *IEEE Trans. Power Electron.* **2019**, *34*, 7147–7150.
91. Pandiarajan, N.; Ramaprabha, R.; Muthu, R. Application of circuit model for photovoltaic energy conversion system. *Int. J. Photoenergy* **2012**, *2012*, 410401. [CrossRef]
92. Morshed, S.; Ankon, S.M.; Chowdhury, T.H.; Rahman, A. Designing of a 2kW stand-alone PV system in Bangladesh using PVsyst, Homer and SolarMAT. In Proceedings of the 2015 3rd International Conference on Green Energy and Technology (ICGET), Dhaka, Bangladesh, 11 September 2015; pp. 1–6.
93. Ali, J.S.M.; Krishnasamy, V. Compact Switched Capacitor Multilevel Inverter (CSCMLI) with Self-Voltage Balancing and Boosting Ability. *IEEE Trans. Power Electron.* **2019**, *34*, 4009–4013. [CrossRef]
94. Zeng, J.; Lin, W.; Cen, D.; Liu, J. Novel k-Type multilevel inverter with reduced components and self-balance. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 4343–4354. [CrossRef]
95. Rajalakshmi, D.; Mahalakshmi, R.; Praveenraj, K. A novel eleven-level inverter employing one voltage source and reduced components as high frequency ac power source. *Int. J. Eng. Adv. Technol.* **2018**, *8*, 1–6.
96. Alishah, R.S.; Hosseini, S.H.; Babaei, E.; Sabahi, M.; Gharehpetian, G.B. New High Step-Up Multilevel Converter Topology with Self-Voltage Balancing Ability and Its Optimization Analysis. *IEEE Trans. Ind. Electron.* **2017**, *64*, 7060–7070. [CrossRef]
97. Loukriz, A.; Dudley, S.; Brown, R.; Quinlan, T.; Walker, S. Experimental validation of a thirteen level H-bridge photovoltaic inverter configuration. In Proceedings of the 2017 IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe), Milan, Italy, 6–9 June 2017. [CrossRef]
98. Kannan, R.; Samad, N.I.A.; Romlie, M.F.; Nor, N.M.; Kumar, L.A. Design and execution of single input multiple output DC-DC converter. In Proceedings of the 2017 IEEE International Conference on Signal and Image Processing Applications (ICSIPA), Kuching, Malaysia, 12–14 September 2017; pp. 164–169. [CrossRef]
99. Herath, N.; Binduhewa, P.; Samaranayake, L.; Ekanayake, J.; Longo, S. Design of a dual energy storage power converter for a small electric vehicle. In Proceedings of the 2017 IEEE International Conference on Industrial and Information Systems (ICIIS), Peradeniya, Sri Lanka, 15–16 December 2017; pp. 1–6. [CrossRef]
100. Poorfakhraei, A.; Narimani, M.; Emadi, A. A Review of Multilevel Inverter Topologies in Electric Vehicles: Current Status and Future Trends. *IEEE Open J. Power Electron.* **2021**, *2*, 155–170. [CrossRef]
101. Sarker, R.; Datta, A.; Debnath, S. A Modified PWM Technique to Reduce Harmonic Content of Multi-level NPC Topology for Medium Voltage Electric Vehicle (EV) Applications. In Proceedings of the Michael Faraday IET International Summit 2020 (MFIIS 2020), Online, 3–4 October 2020; pp. 19–22. [CrossRef]
102. Sheir, A.; Youssef, M.Z. A novel power balancing technique in neutral point clamping multilevel inverters for the electric vehicle industry under distributed unbalance battery powering scheme. In Proceedings of the 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 17–21 March 2019; pp. 3304–3308. [CrossRef]
103. Badawy, M.O.; Sharma, M.; Hernandez, C.; Elrayyah, A.; Guerra, S.; Coe, J. Model Predictive Control for Multi-Port Modular Multilevel Converters in Electric Vehicles Enabling HESDs. *IEEE Trans. Energy Convers.* **2022**, *37*, 10–23. [CrossRef]
104. Kannan, S.A.; Jagadanand, G.; Sasidharan, N. A solo source based 27-level asymmetrical cascaded h-bridge converter fed open ended pmsm drive. In Proceedings of the 2021 7th International Conference on Electrical Energy Systems (ICEES), Chennai, India, 11–13 February 2021; pp. 352–357. [CrossRef]
105. Babaei, E.; Abbasi, O.; Sakhavati, S. An overview of different topologies of multi-port dc/dc converters for dc renewable energy source applications. In Proceedings of the 2016 13th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), Chiang Mai, Thailand, 28 June–1 July 2016; Volume 2, pp. 16–21. [CrossRef]
106. Hassanin, M.A.; Abdel-Kader, F.E.; Amer, S.I.; Abu-Moubarka, A.E. Increase the Reliability of the Operating System for Electric Vehicles Using Eight Switches Bridge Converter. In Proceedings of the 2018 Twentieth International Middle East Power Systems Conference (MEPCON), Cairo, Egypt, 18–20 December 2018; pp. 1014–1019. [CrossRef]
107. Lakshmi, G.S. Performance Analysis of Multi-Level Diode-Clamped Inverter fed IPMSM Drive for Electric Vehicles. In Proceedings of the 2018 IEEE Innovative Smart Grid Technologies-Asia (ISGT Asia), Singapore, 22–25 May 2018; pp. 54–61. [CrossRef]
108. Chakraborty, S.; Vu, H.N.; Hasan, M.M.; Tran, D.D.; Baghdadi, M.E.; Hegazy, O. Inverter for Electric vehicles. DC-DC Converter Topologies for Electric Vehicles: State of the Art and Future Trends. *Energies* **2019**, *2021*, 1474–1478.
109. Asa, E.; Colak, K.; Bojarski, M.; Czarkowski, D.M.; Bojarski, E. A 25 kW industrial prototype wireless electric vehicle charger. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 1756–1761. [CrossRef]
110. Guacci, M.; Anderson, J.A.; Pally, K.L.; Bortis, D.; Kolar, J.W.; Kasper, M.J.; Sanchez, J.; Deboy, G. Experimental Characterization of Silicon and Gallium Nitride 200 v Power Semiconductors for Modular/Multi-Level Converters Using Advanced Measurement Techniques. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *8*, 2238–2254. [CrossRef]

111. Pore, T.R.; Rathod, A.A.; Patil, S.K. Performance Analysis of Cascaded H-Bridge Multilevel Inverter with Variable Frequency ISPWM Technique. In Proceedings of the 2019 Innovations in Power and Advanced Computing Technologies (i-PACT), Vellore, India, 22–23 March 2019; pp. 1–5. [CrossRef]
112. Corzine, K.A.; Baker, J.R. Reduced-parts-count multilevel rectifiers. *IEEE Trans. Ind. Electron.* **2002**, *49*, 766–774. [CrossRef]
113. Periyanayagam, M.; Kumar, V.S.; Chokkalingam, B.; Padmanaban, S.; Mihet-Popa, L.; Adedayo, Y. A modified high voltage gain quasi-impedance source coupled inductor multilevel inverter for photovoltaic application. *Energies* **2020**, *13*, 874. [CrossRef]
114. Vishnuram, P.; Ramachandiran, G.; Sudhakar Babu, T.; Nastasi, B. Induction Heating in Domestic Cooking and Industrial Melting Applications: A Systematic Review on Modelling, Converter Topologies and Control Schemes. *Energies* **2021**, *14*, 6634. [CrossRef]
115. Yadav, A.K.; Gopakumar, K.; Raj, R.K.; Umanand, L.; Bhattacharya, S.; Jarzyna, W. A Hybrid 7-Level Inverter Using Low-Voltage Devices and Operation with Single DC-Link. *IEEE Trans. Power Electron.* **2019**, *34*, 9844–9853. [CrossRef]
116. Xu, Z.; Zheng, X.; Lin, T.; Yao, J.; Ioinovici, A. Switched-capacitor multi-level inverter with equal distribution of the capacitors discharging phases. *Chin. J. Electr. Eng.* **2020**, *6*, 42–52. [CrossRef]
117. Ooi, G.H.P.; Maswood, A.I.; Lim, Z. Five-Level Multiple-Pole PWM AC-AC Converters with Reduced Components Count. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4739–4748. [CrossRef]
118. Meraj, M.; Rahman, S.; Iqbal, A.; Tariq, M.; Lodi, K.A.; Ben-Brahim, L. A New Variable Frequency Control of 49-Level Cascaded Packed U-Cell Voltage Source Inverter. *IEEE Trans. Ind. Appl.* **2019**, *55*, 7537–7548. [CrossRef]