



# *Article* **A Fault-Tolerant Strategy for Three-Level Flying-Capacitor DC/DC Converter in Spacecraft Power System †**

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**Abstract:** With the development of space exploration, high-power and high-voltage power systems are essential for future spacecraft applications. Because of the effects of space radiation such as single event burnout (SEB), the rated voltage of power devices in converters for a spacecraft power system is limited to a level much lower than that for traditional ground applications. Thus, multi-level DC/DC converters are good choices for high-voltage applications in spacecraft. In this paper, a fault-tolerant strategy is proposed for a three-level flying capacitor DC/DC converter to increase the reliability with minimal cost. There is no extra hardware needed for the proposed strategy; the fault tolerance of the converter is only achieved by changing the software control strategy. A stage analysis of the proposed strategy is provided in detail for different fault locations and ratios between the input and output voltage. Finally, a simulation model and prototype are built to verify the effectiveness of the proposed strategy.

**Keywords:** fault-tolerant strategy; high voltage; three level; flying capacitor; DC/DC converter; spacecraft power system

## **1. Introduction**

The architecture of a high-power spacecraft distributed power system is shown in Figure [1.](#page-1-0) The spacecraft power system is a typical DC power system [\[1](#page-14-0)[,2\]](#page-14-1). It consists of solar arrays, batteries, a fuel cell, flying wheel, power converters, etc. The solar arrays provide the power for the load and charge the battery during the sunlight period of the orbit. Storages such as batteries provide the power for the load during the eclipse period of the orbit. The power converters are used to regulate the DC bus voltage and control the battery charging and discharging. With the development of space exploration, the power capacity of spacecraft has become larger and larger, and the voltage level of the spacecraft power system has become higher and higher. Currently, high voltage and high power are the trends and necessary factors for a spacecraft power system to meet the requirements of future spacecraft, such as high-power SAR satellites, electric propulsion spacecraft, deep space spacecraft, space stations, and space solar energy power stations, etc. [\[3\]](#page-14-2) The power ratings of these spacecraft will need to be larger than 100 kW, and the voltage level will need to be higher than 1000 V. However, the current power converters cannot meet the requirements of this high-voltage application. The characteristics of the power device in space are obviously different from that on the ground. Due to space radiation effects such as single event burnout, the high-voltage power device is the main limitation for spacecraft power converters. Currently, the available voltage of power devices such as power MOSFETs for spacecraft power converters is lower than 500 V. However, the requirement of the output voltage of converters is much higher than 500 V for future space



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applications. In order to solve the mismatch between future high-voltage applications and the available low-voltage power devices, the multi-level DC/DC converter is a better solution for these high-voltage applications with the voltage limitation of the power devices. Even though they are not used in traditional spacecraft power systems in which the highest DC bus voltage is 100 V, these converters are widely used in ground high-voltage applications. The voltage stress of the power devices in a multi-level DC/DC converter can clearly be reduced  $[4-10]$  $[4-10]$ . For multi-level DC/DC converters, the number of power devices is relatively larger than the traditional two-level converter. Each failure of the power device may cause the output interruption of the converter, so the reliability of the multi-level DC/DC converter is relatively low without a fault-tolerant strategy [\[11](#page-14-5)[–16\]](#page-14-6). In addition, the reliability of the converter is very important for the spacecraft. The failure of the converter will result in huge losses, especially for an unmanned spacecraft. Thus, the fault-tolerant strategy is very important for the multi-level converter in a spacecraft power system. Fault-tolerant schemes of multi-level DC/DC converters have been proposed by researchers [\[14](#page-14-7)[–20\]](#page-14-8). The redundant subsystem, units, circuits, or devices have been added to multi-level converters to improve their reliability [\[14](#page-14-7)[,15](#page-14-9)[,17](#page-14-10)[,18\]](#page-14-11). The fuse is a common component that is used to isolate the short-circuit fault parts of the converter. The main disadvantage of the fuses is that the blowing time of a fuse is difficult to control. Moreover, the use of a fuse will increase the parasitic inductance of the commutation loops of the converter, and larger parasitic inductance causes a higher voltage stress, which reduces the reliability of power devices [\[19](#page-14-12)[,20\]](#page-14-8). Additional hardware is needed for these former methods. However, the additional hardware increases the mass of the converter, which results in an obviously higher cost of the launch. For space application, the limitation of the mass of converters is extremely strict. A three-level flying capacitor DC/DC converter is the typical multi-level DC/DC converter. A fault-tolerant control strategy for three-level flying capacitor DC/DC converters is proposed in this paper. The reliability of the three-level DC/DC converter is improved with minimal cost. The fault tolerance of the converter is achieved by only changing the software strategy, and no extra hardware is needed. The concept of the fault-tolerant strategy can also be applied in other multi-level converters.

<span id="page-1-0"></span>

**Figure 1.** Typical high-power spacecraft distributed power system with DC/DC converters. **Figure 1.** Typical high-power spacecraft distributed power system with DC/DC converters.

In Section [2,](#page-2-0) the control scheme of the fault-tolerant strategy for a three-level flying capacitor DC/DC converter is introduced. In Section [3,](#page-3-0) the stage analysis of the converter under short-circuit fault conditions is given in detail. In Section [4,](#page-10-0) the proposed strategy under different conditions is verified by experiments and simulations. Finally, the conclusions are summarized.

### <span id="page-2-0"></span>**2. Control Scheme of Fault-Tolerant Strategy for Three-Level Flying Capacitor DC/DC Converter**

In order to achieve the fault-tolerant operation of the three-level flying capacitor DC/DC converter after a short-circuit fault of the power devices, a seamless transfer control from three-level mode to two-level mode is designed. Before the fault, the converter operates in three-level mode, and after the fault, the converter operates in two-level mode. The control scheme of the proposed fault-tolerant strategy for a three-level flying capacitor DC/DC converter is shown in Figure [2.](#page-2-1)

<span id="page-2-1"></span>

**Figure 2.** Control scheme of the fault-tolerant strategy for flying capacitor DC/DC converter. **Figure 2.** Control scheme of the fault-tolerant strategy for flying capacitor DC/DC converter.

The fault-tolerant strategy consists of three loops, including a three-level voltage ulation loop, a flying capacitor voltage loop, and a two-level voltage regulation loop. regulation loop, a flying capacitor voltage loop, and a two-level voltage regulation loop. When the power devices of the converter are normal, the output voltage and flying capacitor voltage are regulated by a three-level voltage regulation loop. Output voltage and flying capacitor voltage are two control targets for the three-level voltage regulation loop. The reference of flying capacitor voltage is half of the reference of the output voltage of the converter. When a short-circuit fault of the power device occurs, the converter is regulated by the flying capacitor voltage loop after the short-circuit fault of the power device is detected. If a short-circuit fault of inner switch  $S_2$  or  $S_3$  occurs, the voltage reference of the flying capacitor changes from half of the output voltage to zero. The normal inner the flying capacitor changes from half of the output voltage to zero. The normal inner power devices are opened immediately, and the driver signals of the normal inner switches are set as low. If a short-circuit fault of outer switch  $S_1$  or  $S_4$  occurs, the reference of the

flying capacitor voltage changes from half of the output voltage to the output voltage, and the driver signals of the normal outer switches are set as high. When the voltage of the flying capacitor reaches the reference value, the converter changes its mode to the two-level mode. If the inner switch is at fault, the driver of the other inner switch is set as high in the two-level mode. The driver signals of the two outer switches operate in the complementary state. If the outer switch is at fault, the driver of the other outer switch is set as high. The driver signals of the two inner switches operate in the complementary state.

#### **3. Analysis of Operation Modes for the Converter under Short-Circuit<br>Fault Conditions Fault Conditions**

<span id="page-3-0"></span>According to the analysis of the flying capacitor three-level DC/DC converter, the operation stages of the converter are different between the situation in which the ratio of the input and output voltage is smaller than 0.5 ( $V_L < 0.5 V_H$ ) and the situation in which the ratio is larger than 0.5 ( $V_L > 0.5 V_H$ ).

The diagram in Figure 3 shows the key quantity for the situation in which the short-The diagram in Figure [3 s](#page-3-1)hows the key quantity for the situation in which the shortcircuit fault occurs in switch  $S_3$  when the ratio of the input and output voltage is smaller than 0.5 ( $V_L < 0.5 V_H$ ). When the short-circuit fault of switch  $S_3$  is detected by the detection circuit, the converter is regulated from the three-level mode to the flying capacitor voltage circuit, the converter is regulated from the three-level mode to the flying capacitor voltage control mode. The reference of the flying capacitor voltage decreases from half of the output voltage  $V_H$  to zero. The voltage of the flying capacitor is changed by the flying capacitor voltage loop from half of the output voltage to zero during this stage. After the voltage of the flying capacitor is detected to have reached zero, the converter finishes the flying of the flying capacitor is detected to have reached zero, the converter finishes the flying capacitor voltage control mode and begins to operate in two-level mode. capacitor voltage control mode and begins to operate in two-level mode.

<span id="page-3-1"></span>

**Figure 3.** The diagram of the key quantity under the situation in which short-circuit fault occurs in **Figure 3.** The diagram of the key quantity under the situation in which short-circuit fault occurs in switch S<sub>3</sub>.

The analysis of operation stages under this fault situation is shown in Figure [4.](#page-4-0) The  $\rm g_{1},$  $g_2$ ,  $g_3$ , and  $g_4$  are gate drivers of switches  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$ , respectively. When  $V_L < 0.5$  $V_H$ , the duty cycle of inner switches  $g_3$  and  $g_4$  is larger than 0.5. The three-level mode is the pre-fault mode. The stages of the three-level mode are shown in Figure [5.](#page-4-1) There are

<span id="page-4-0"></span>

four stages in the three-level mode. In the three-level mode, the driver signal of  $g_1$  and  $g_4$ are complementary, and the driver signal of  $g_2$  and  $g_3$  are complementary.

Figure 4. Stages analysis when short-circuit fault occurs in S<sub>3</sub> (V<sub>L</sub> < 0.5 V<sub>H</sub>).

<span id="page-4-1"></span>

**Figure 5.** Stages of the three-level mode when V<sub>L</sub> < 0.5 V<sub>H</sub>.

The stages during the flying capacitor voltage control mode are shown in Figure 6. There are also three stages after the short-circuit fault occurs. In Stage V,  $S_3$  is short-circuited and  $S_2$  turns on, then the flying capacitor is short-circuited. There is a large current spike occurring in  $S_2$ , so the fault is detected. After the fault is detected, the converter operates in Stage VI and VIII; in these two stages,  $g_4$  is in the PWM state, and the values of  $g_1$ ,  $g_2$ , and  $g_3$  are 0 when the short-circuit fault occurs in  $S_3$ . Similarly,  $g_1$  is in the PWM state, and  $S_3$  are 0 when the short-circuit fault occurs in  $S_3$ . Similarly,  $S_1$  is in the PWM state, and the values of  $g_2$ ,  $g_3$ , and  $g_4$  are 0 when the short-circuit fault occurs in switch  $S_2$ . The and the values of  $g_2$ ,  $g_3$ , and  $g_4$  are 0 when the short-circuit fault occurs in switch  $S_2$ . The two-level mode is the post-fault mode. In the two-level mode, the driver signal of  $g_1$  and  $g_4$  are complementary, and  $g_2$  is set as 1 when the short-circuit fault occurs in switch  $S_3$ .  $S_4$  are complementary, and  $S_2$  is set as 1 when the short-circuit fault occurs.<br>Similarly,  $g_3$  is set as 1 when  $S_2$  is where the fault occurs. Similarly,  $g_3$  is set as 1 when  $S_2$  is where the fault occurs.

<span id="page-5-0"></span>

Figure 6. Stages of capacitor voltage control mode after short-circuit fault occurs in S3.

short-circuit fault occurs in the outer switch  $S_4$  when  $V_L$  is lower than 0.5  $V_H$ . Before the fault occurs, the converter operates in three-level mode. When the short-circuit fault of the switch  $S_4$  is detected, the converter begins to operate in flying capacitor voltage control mode. The flying capacitor voltage is regulated gradually from half of the output voltage to output voltage. When the flying capacitor voltage reaches the output voltage, the converter to output voltage. When the flying capacitor  $\frac{1}{2}$  of contract voltage reaches the output voltage reaches the con- $\mathbf{v}$ The diagram in Figure 7 shows the key quantities under the situation in which the The diagram in Figure [7 s](#page-5-1)hows the key quantities under the situation in which the turns to operate in two-level mode.

<span id="page-5-1"></span>

Figure 7. The diagram of the key quantity under the situation in which short-circuit fault occurs in switch S4. switch S4. switch S<sup>4</sup> .

The stage analysis in this situation is shown in Figure [8.](#page-6-0) The stages of the three-level mode are the same as those in which the short-circuit fault of  $S_3$  occurs. The stages of the flying capacitor voltage control mode after a short-circuit fault are shown in Figure 9. There are three stages after the short-circuit fault occurs in the outer switches. In Stage V of the flying capacitor voltage mode,  $g_4$  is short-circuited and  $g_1$  turns on; then the output capacitor is connected directly with the flying capacitor. Due to the existence of the voltage capacitor is connected directly with the flying capacitor. Due to the existence of the voltage difference between the output voltage and the flying capacitor voltage, there is a current difference between the output voltage and the flying capacitor voltage, there is a current spike occurring in  $S_1$ , and the fault can be detected. After Stage V, the converter operates in Stages VI and VII. In these two stages,  $g_3$  is in the PWM state, and  $g_1, g_2$ , and  $g_4$  are  $0$ when the short-circuit fault occurs in  $S_4$ . Similarly,  $g_2$  is in the PWM state, and  $g_1$ ,  $g_3$ , and  $g_4$  are 0 when the short-circuit fault occurs in  $S_1$ . In the two-level mode, the driver signal of  $g_2$  and  $g_3$  are complementary, and  $g_1$  is set as 1 when the fault occurs in  $S_4$ . Similarly,  $g_4$  is set as 1 when the fault occurs in  $S_1$ . the flying capacitor voltage mode,  $g_4$  is short-circuited and  $g_1$  turns on; then the output capacitor is connected directly with the flying capacitor. Due to the existence of the voltage difference between the output

<span id="page-6-0"></span>

**Figure 8.** Stage analysis (V<sub>L</sub> < 0.5 V<sub>H</sub>).

<span id="page-6-1"></span>

**Figure 9.** Stages of S4 short-circuited. **Figure 9.** Stages of S4 short-circuited. **Figure 9.** Stages of S<sup>4</sup> short-circuited.

Then the situation when  $V_L$  is higher than 0.5  $V_H$  is analyzed in detail. The stage analysis is shown in Figure 10 f[or w](#page-7-0)hen  $S_3$  is short-circuited in this situation. This situation is different from the situation when  $V_L$  is lower than 0.5  $V_H$ . The duty cycle of  $g_3$  and  $g_4$  is less than 0.5. less than 0.5.

<span id="page-7-0"></span>

Figure 10. Short-circuit fault analysis ( $V_L > 0.5 V_H$ ). (a) The stages when S<sub>3</sub> is short-circuited; (**b**) stage analysis.

When the short-circuit fault of  $S_3$  is detected, the converter is regulated by the flying capacitor voltage control loop. Then  $S_4$  is opened. Because  $V_L > 0.5 V_H$  and the initial value of  $v_{fly}$  is half of  $v_H$ , inequality (1) can be derived at the beginning of the fault. The voltage difference between the inductor is always positive. It should be noticed that if inequality (2) holds, the current of the inductor will continue to increase during Stage VI. When  $v_{fly}$  is lower than  $(v_H - v_L)$ , the converter operates in Stages VII and VIII. When the flying capacitor voltage reaches 0, the converter turns into the two-level mode, and the  $S_2$ is closed.

$$
v_L > v_H - v_{fly} \ (v_L > 0.5v_H, V_{fly} = 0.5v_H)
$$
 (1)

$$
v_{fly} > v_H - v_L \tag{2}
$$

The proper inductance value of the inductor L should be designed, and additional an over-current protection method should be considered. The flying capacitor voltage and inductor current can be calculated by  $(3)$ . The current spike analysis in this situation when  $S_3$  is short-circuited is shown in Figure [11.](#page-8-0)

$$
\begin{cases}\n v_{fly}(t) = \frac{I_L \sqrt{LC}}{C} \sin(\frac{1}{\sqrt{LC}}t) + (V_{fly} - V_H + V_L) \cos(\frac{1}{\sqrt{LC}}t) + (V_H - V_L) \\
 i_L(t) = I_L \cos(\frac{1}{\sqrt{LC}}t) - \frac{(V_{fly} - V_H + V_L)C}{\sqrt{LC}} \sin(\frac{1}{\sqrt{LC}}t)\n\end{cases}
$$
\n(3)

is the inductance of the input inductor, C is the capacitance of the flying capacitor, i<sub>L</sub> is the  $v_{fly}$  is the flying capacitor voltage,  $V_H$  is the output voltage,  $V_L$  is the input v The maximum current under different levels of inductance when  $S_3$  is short-circuited is voltage is 100 V, the input voltage is 80 V, the inductor is 1 mH, and the initial current of  $\tt current$  value of the inductor, and I $_{\rm L}$  is the initial value of the inductor current. If the output **−100** the inductor is 10 A, then it can be calculated that the maximum inductor current is 17.2 A. **−10** where *vfly* is the flying capacitor voltage, *V<sup>H</sup>* is the output voltage, *V<sup>L</sup>* is the input voltage, *L* (**a**) (**b**) shown in Figure [12.](#page-8-1)

<span id="page-8-0"></span>

Figure 11. The analysis of the stages under  $S_3$  fault. (a) Equivalent circuit; (b) the simulation curve (V<sub>L</sub> 80 V, V<sub>H</sub> 100 V, initial value of I<sub>L</sub>-10 A).

<span id="page-8-1"></span>

S3 is short-circuited is shown in Figure 11.

Figure 12. Maximum current under different levels of inductance when S<sub>3</sub> is short-circuited.

The current spike analysis when  $S_4$  is short-circuited is shown in Figure [13.](#page-9-0) When the short-circuit fault of S<sub>4</sub> is detected, S<sub>3</sub> is turned off. Because  $v_L$  is larger than 0.5  $V_H$  and the initial value of V<sub>fly</sub> is half of V<sub>H</sub>, inequality (4) can be derived at the beginning of the fault. The voltage difference between the inductor is always positive. It should be noticed that The voltage difference between the inductor is always positive. It should be noticed that if inequality (5) holds, the current of the inductor will continue to increase during Stage VI. When  $\rm{v_{fly}}$  is higher than 0.5  $\rm{V_H}$ , the converter operates in Stages VII and VIII.

$$
v_L > v_{fly} \ (v_L > 0.5v_H, V_{fly} = 0.5v_H)
$$
 (4)

$$
v_{fly} < 0.5v_H \tag{5}
$$

*g<sub>4</sub> g<sub>4</sub> g<sub>4</sub> g<sub>4</sub> g<sub>4</sub> g<sub>4</sub> g<sub>4</sub> g<sub>4</sub>* proper inductance should also be designed carefully. The flying capacitor voltage and *g3* current is 17.2 A. The maximum current under different levels of inductance when S<sub>4</sub> is ctor current can be calculat *VC*  $\frac{1}{2}$   $\frac{1}{2}$   $\frac{2}{3}$   $\frac{1}{2}$   $\frac{1}{2}$ *Vfly* **IDC 1**<br>
inductor current can be calculated by (4). The current spike analysis is given in Figure [14.](#page-9-1) *dicts as the situati* If we take the same parameters as the situation when S<sub>3</sub> is faulty, the maximum inductor When the voltage of the flying capacitor voltage reaches  $V_H$ ,  $S_1$  is turned off. The short-circuited is shown in Figure [15.](#page-9-2)

$$
\begin{cases}\nv_{fly}(t) = \frac{I_L \sqrt{LC}}{C} \sin(\frac{1}{\sqrt{LC}}t) + (V_{fly} - V_L) \cos(\frac{1}{\sqrt{LC}}t) + (V_L) \\
i_L(t) = I_L \cos(\frac{1}{\sqrt{LC}}t) - \frac{(V_{fly} - V_L)C}{\sqrt{LC}} \sin(\frac{1}{\sqrt{LC}}t)\n\end{cases}
$$
\n(6)

<span id="page-9-0"></span>

Figure 13. Short-circuit fault analysis ( $V_L > 0.5 V_H$ ). (a) The stages when  $S_4$  is short-circuited;  $$ **Figure 13.** Short-chealt and analysis  $(v_L > 0.5 v_H)$ . (a) The stages when  $54$  is short-che require is. Short-chean fault analysis  $(v_L > 0.5 v_H)$ . (a) the stages when  $S_4$  is short-chean

<span id="page-9-1"></span>

Figure 14. The analysis of the stages under  $S_4$  fault. (a) Equivalent circuit; (b) the simulation curve (V<sub>L</sub> 80 V, V<sub>H</sub> 100 V, initial value of I<sub>L</sub> 10 A).

<span id="page-9-2"></span>

**Figure 15.** Maximum current under different levels of inductance when  $S_4$  is short-circuited.

According to the stage analysis of the circuit, the inductance of the input inductor is derived<br>by (7) the appealing of the fixing appealing is derived by (8) and the appealing of the derived by  $(9)$ . tance of the flying capacitor is derived by  $(8)$ , and the capacitance  $\frac{1}{2}$  is derived by (9). by (7), the capacitance of the flying capacitor is derived by (8), and the capacitance of the output capacitor is derived by (9). The parameters of the flying capacitor DC/DC converter can be calculated as below.

$$
L_{IN} = \begin{cases} \frac{(\frac{U_0}{2} - U_{IN})(1 - D)}{\delta_I I_{in} \cdot f_s} & (D > 0.5) \\ \frac{(U_{IN} - \frac{U_0}{2}) \cdot D}{\delta_I I_{in} \cdot f_s} & (D < 0.5) \end{cases}
$$
(7)

$$
C_{fly} = \begin{cases} \frac{I_{IN}(1-D)}{2} & (D > 0.5) \\ \frac{I_{IN}D}{2} & (D < 0.5) \\ \frac{I_{IN}D}{2} & (D < 0.5) \end{cases}
$$
(8)

$$
C_o = \frac{I_o}{\delta_o U_o \cdot f_s} \tag{9}
$$

where the output voltage  $U_0$  is 100 V, the input voltage  $U_{IN}$  is 30~80 V, the switching frequency *f<sup>s</sup>* is 10,000 Hz, the duty cycle *D* is 0.2~0.7, the input current *IIN* is 33 A, the output current Io is 10 A, the ripple ratio of the input current  $\delta_I$  is 0.02, the ripple ratio of the flying capacitor voltage  $\delta_f$  is 0.1, and the ripple ratio of the output capacitor voltage  $\delta_c$ is 0.01. Then the inductor is 0.9 mH, the flying capacitor is 200  $\mu$ F, and the output capacitor is 1 mF. With the consideration of the current spike analysis after a short-circuit fault in the simulation, the inductance of the inductor is chosen as 1 mH, and the capacitances of the flying capacitor and the output capacitor are chosen as 200  $\mu$ F and 1 mF, respectively.

### <span id="page-10-0"></span>**4. Simulation and Experiment Verifications of the Fault-Tolerant Strategy**

In order to verify the proposed fault-tolerant strategy, the simulation model of the flying capacitor three-level DC/DC converter based on PSIM was built. In the model, the rated power of the flying capacitor three-level converter is 1 kW. The output voltage of the converter is 100 V. The two types of input voltage are considered, including 30 V ( $V_L$ <0.5  $V_H$ ) and 80 V ( $V_L > 0.5 V_H$ ). The inductance of the inductor is 1 mH. The capacitance of the flying capacitor is 200 uF, and the capacitance of the output capacitor is 1 mF. The parameters of the simulation are shown in Table [1.](#page-10-1)



<span id="page-10-1"></span>**Table 1.** The parameters of the different simulation cases.

<span id="page-10-2"></span>

Figure 16. The waveforms of  $S_4$  short-circuit fault ( $V_L < 0.5 V_H$ ). (a) Light load 100 W; (b) heavy load 1000 W. 1000 W.

The simulation waveforms when a short-circuit fault occurs in outer switch  $S_4$  under **20 0 110 110** converter is uninterruptible when a short-circuit fault of S<sup>4</sup> occurs. The mode transfer after the fault is seamless. wo load conditions are shown in Figure 16 two load conditions are shown in Figure [16.](#page-10-2) It can be seen that the output voltage of the

**95 90 95 90** The simulation results when the input voltage is lower than half of the output voltage **60 Flying 60 Flying**  are shown in Figure [17.](#page-11-0) The waveforms when a short-circuit fault occurs in inner switch

S<sup>3</sup> under different load conditions are shown in Figure [17a](#page-11-0),b. The two load conditions are **0.2 0.3 0.4 0.5 0.6 0.7 0.8** 100 W for a light load and 1000 W for a heavy load. It can be seen that the output voltage of the converter is uninterruptible after the  $S_3$  fault occurs. The spike of the current and voltage is in the normal range during the mode transition after the fault.  $\mu$  ander different load conditions are shown in Figure 17a,b. The two load cor **Figure 10. In the normal range during the mode transmonrance the name. S**<sub>3</sub> under different load conditions are shown

**90**

<span id="page-11-0"></span>

Figure 17. The waveforms of  $S_3$  short-circuit fault ( $V_L < 0.5 V_H$ ). (a) Light load 100 W; (b) heavy load 1000 W. 1000 W. 1000 W. **Figure 17.** The waveforms of S3 short-circuit fault (VL < 0.5 VH). (**a**) Light load 100 W; (**b**) heavy load

<span id="page-11-1"></span>

Figure 18. The waveforms of  $S_3$  short-circuit fault ( $V_L > 0.5 V_H$ ). (a) Light load 100 W; (b) heavy load 1000 W. 1000 W.

<span id="page-11-2"></span>

Figure 19. The waveforms of  $S_4$  short-circuit fault ( $V_L > 0.5 V_H$ ). (a) Light load 100 W; (b) heavy load 1000 W. 1000 W.

The simulation results when the input voltage is higher than half of the output voltage the simulation result when the only would be suggested that that the output are shown in Figures [18](#page-11-1) and [19.](#page-11-2) The waveforms when a short-circuit fault occurs in  $S_3$ under two different load conditions including a light load and a heavy load are shown in Figure  $18$ a,b, and the waveforms when a short-circuit fault occurs in  $\mathrm{S}_4$  under two different load conditions are shown in Figure [19a](#page-11-2),b. It can also be seen that the output voltage is uninterruptible when two types of faults occur. The spike and surge of the current and voltage are also in the normal range.

The prototype of the three-level flying capacitor DC/DC converter is built to verify the fault-tolerant strategy. The parameters of the prototype are shown in Table [2.](#page-12-0) The simulation results when the input voltage is higher than half of the output volt-



<span id="page-12-0"></span>**Table 2.** The parameters of the prototype of flying capacitor DC/DC converter.

The waveform when the short-circuit fault of S3 occurs is shown in Figure [20a](#page-12-1). CH1 is the output voltage of the converter. CH2 is the flying capacitor voltage. CH3 is the trigger signal. CH4 is the driver signal of the power switch S3. The waveform of the three-level mode before the fault occurs is shown in Figure [20b](#page-12-1). The waveform during the fault is shown in Figure [20c](#page-12-1). It can be seen that the output voltage is uninterruptible and the flying capacitor voltage is regulated from 16 V to 0. The waveform of the two-level mode after the fault occurs is shown in Figure [20d](#page-12-1). The waveform when the short-circuit fault of S4 occurs is shown in Figure [21a](#page-13-0). The waveform before an S4 fault is shown in Figure [21b](#page-13-0). The waveform during the fault is shown in Figure [21c](#page-13-0). It can be seen that the output voltage is uninterruptible and the flying capacitor voltage is regulated from 16 V to 32 V. After the S4 fault, the waveform is shown in Figure [21d](#page-13-0).

<span id="page-12-1"></span>

Figure 20. The experimental waveforms of  $S_3$  short-circuit fault. (a) Overall stages; (b) the waveform of three-level mode before  $S_3$  fault; (c) the waveform of  $S_3$  short-circuit fault during fault; (d) the waveform of two-level mode after  $S_3$  fault.



<span id="page-13-0"></span>

of three-level mode before S3 fault; (**c**) the waveform of S3 short-circuit fault during fault; (**d**) the

Figure 21. The experimental waveforms of  $S_4$  short-circuit fault. (a) Overall stages; (b) the waveform of three-level mode before  $S_4$  fault; (c) the waveform of  $S_4$  short-circuit fault during fault; (d) the waveform of two-level mode after  $S_4$  fault.

#### **5. Conclusions 5. Conclusions**

In order to improve the reliability of converters for the interface of the PV, battery, or In order to improve the reliability of converters for the interface of the PV, battery, or other sources in spacecraft power systems for future high-voltage application, the fault-other sources in spacecraft power systems for future high-voltage application, the faulttolerant strategy of a three-level flying capacitor DC/DC converter is proposed in this paper. If a short-circuit fault occurs in the power devices, the converter can provide uninterruptible power for the load. It can turn from the three-level mode to the two-level mode, and during force for the following the mode transition, the voltage of the flying capacitor is regulated to the different target ferent target value based on the different fault locations. There is no extra hardware value based on the different fault locations. There is no extra hardware needed for this needed for the fault tolerance of the converter is only achieved by chemical to the fault to  $\frac{1}{2}$ proposed strategy; the fault tolerance of the converter is only achieved by changing the with minimal converter is improved with minimal converter  $\frac{1}{2}$ . cost. The stage analysis of the three-level converter is provided in detail. Different ratios between the input and output voltage and different fault locations are considered. Finally, a<br>in the input and output voltage and different fault locations are considered. Finally, a simulation model and prototype of the converter with the fault-tolerant strategy are built to verify the proposed strategy. The results show the fault tolerance operation of the converter software control strategy, and the reliability of the converter is improved with minimal is achieved after a short-circuit fault occurs.

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