

Article

Decentralized Control for the Cell Power Balancing of a Cascaded Full-Bridge Multilevel Converter

Miguel Vivert ¹, Rafael Diez ², Marc Cousineau ^{3,*}, Diego Bernal Cobaleda ⁴ and Diego Patino ²

¹ Carrera de Ingeniería en Electricidad (CIELE), Facultad de Ingeniería en Ciencias Aplicada (FICA), Universidad Técnica del Norte, Ibarra 100105, Ecuador; mevivert@utn.edu.ec

² Department of Electronics Engineering, Pontificia Universidad Javeriana, Bogotá 110231, Colombia; rdiez@javeriana.edu.co (R.D.); patino-d@javeriana.edu.co (D.P.)

³ LAPLACE, Université de Toulouse, CNRS, INPT, UPS, 31062 Toulouse, France

⁴ Electrical Engineering Department (ESAT), EnergyVille Diepenbeek, KU Leuven, 3001 Genk, Belgium; diego.bernal@kuleuven.be

* Correspondence: marc.cousineau@laplace.univ-tlse.fr; Tel.: +33-764-495-465

Abstract: This article presents a decentralized control technique applied to a Cascaded Full-Bridge Multilevel Converter (CFBMC) to balance the amount of power provided by its independent cells connected in series. It is based on the use of elementary modular controllers, associated with each converter cell, communicating with their close neighbors to obtain the appropriate power balancing. A complete theoretical study of the system is provided in terms of modal responses, feedback loop bandwidth and stability criteria and the design method of the correctors is explained as well. Each modular controller can be dynamically removed or added to allow reconfiguration of the number of converter cells during operation for functional safety purposes. This method is illustrated with a five-cell CFBMC, studied both with simulations and experimental tests. The response of the system to load transients and cell voltage disturbances demonstrates the robustness of the proposed control method. Thanks to its modularity, the number of voltage levels of the converter can be easily increased by inserting new cells in series without adding complexity to the control part.

Keywords: multilevel converter; Cascaded Multilevel Converter; decentralized control; distributed control; balancing controller; converter reconfiguration; fault-tolerant controller



Citation: Vivert, M.; Diez, R.; Cousineau, M.; Bernal Cobaleda, D.; Patino, D. Decentralized Control for the Cell Power Balancing of a Cascaded Full-Bridge Multilevel Converter. *Energies* **2023**, *16*, 4352. <https://doi.org/10.3390/en16114352>

Academic Editor: Attilio Converti

Received: 10 March 2023

Revised: 16 May 2023

Accepted: 23 May 2023

Published: 26 May 2023



Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

The dependence of humanity on electricity-based technologies is continuously increasing, making efficiency in the consumption of this energy a matter of large importance. This subject is addressed with power converters which are based on passive elements and switching devices such as Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) or Insulated-Gate Bipolar Transistors (IGBTs) [1,2] which allow one to control their turning-on and turning-off at a relatively high speed, reducing the size of the passive elements. However, in high-power or high-voltage applications, these switching devices are limited by their voltage and current ratings or by their switching times.

In order to overcome this difficulty, Multi-Cellular Converters (MCCs) propose the distribution of the total power among several power modules or cells, each one supporting less power. Depending on the connection of these cells (series or parallel), the current or voltage is divided. Within the family of multicellular converters, one can mention the following, among others: the Flying Capacitor Multilevel Converter (FCMC) [3–7], CFBMC [8–13] and the Multiphase Buck Converter [14–16]. They distribute, respectively, the input voltage, the output voltage and the output current. This makes it possible to use low voltage/current switches and brings the advantage of power converters, regarding their efficiency and flexibility, to high-power uses.

Another feature of the multi-cellular converters is that with suitable frequency modulation techniques [17–20] it is possible to obtain a much higher output frequency than the MOSFET or IGBT switching frequency, giving the option of either increasing the efficiency by the reduction of the switching losses, or shrinking even more the size of the passive elements.

In contrast, MCCs bring some complex subjects that need to be analyzed, such as the control of the cells that guarantees an equilibrium of the power delivered by each cell or the secure operation of the switches, avoiding overvoltage or overcurrent. For instance, in FCMC the capacitor voltages are the variables to balance [3,4,21], also improving the output voltage ripple. In the Multiphase Buck Converter, the sharing must be ensured in the output current of each leg [16]. For the CFBMC, the output voltage is the one to equalize [22–25]. This last converter has been widely explored in recent times for energy storage systems, where the State-Of-Charge (SOC) of batteries is the variable to equalize [26,27]. In this case, since the output current is the same for all the cells, the modulation index for the output voltage of one cell can be increased/decreased if more/less power is to be transferred from or to the battery supplying this module.

The modularity of MCCs also offers the opportunity to propose fault-tolerant solutions. Here, one challenge is to insert or remove cells during operation [3,15,21,23], which additionally provides the possibility to increase the power of the system without interruption. There exist many controllers that satisfy all these specifications. In [3,21], a control structure is proposed for an FCMC, which balances the capacitor voltages, regulates the output current and allows a cell insertion/removal ability, obtaining interesting results.

The present article applies to the CFBMC, proposing a decentralized controller based on [3,21] that differs from most of the works found in the literature, where the balancing is achieved by means of a controller that finds the error comparing the control variable of one cell with the average of all the other cell variables. This task needs to be assumed by a supervisor in a centralized way, either for the SOC [26,27], the DC link voltage [28] or the output power [29]. With this control approach, the average computation of the state variables is strongly dependent on the reliability of all the connections with respect to obtaining the measurements, meaning that if one measurement is lost or mistaken, all the control signals will be erratic.

In the proposed work, each cell is responsible for its control depending only on the two measurements of the adjacent cells to calculate the error, ensuring a decentralized management for the balancing and avoiding problems with a single point of failure.

This article develops a mathematical approach for the design of the controllers and provides a modal response study, and also experimentally validates the principles with the CFBMC. The article describes, in Section 2, the topology of the CFBMC and models it. Section 3 presents a description of the decentralized controller. Then, in Section 4, an in-depth analysis of the controller applied to the CFBMC is shown, presenting the closed-loop and open-loop transfer functions, analyzing the bandwidth of the system. In Section 5, the design of the controller is presented, based on the open-loop transfer functions of the system, obtaining, theoretically, the eigenvalues of the system. This design is validated in Section 6 by simulations and experimental results using three tests: load step, input voltage step and cell insertion tests. Finally, the conclusion and future works are presented in the last section.

2. Description of the System

This article proposes an adaptation of a decentralized control applied previously to FCMC in [3,21], now implemented in a CFBMC of N Full-Bridges (FBs) with inductive filter and resistive load. Figure 1 shows the topology of the converter, using MOSFET as the switching device, where the control is implemented. S_{ky} represents the position of the High-Side switches. It is equal to 1 if the switch of the k th FB cell is in the ON state and 0 if it is in the OFF state, with $k = 1, 2, \dots, N$. $y = a$ for the left-side branch of the k th FB cell and $y = b$ for the right side. \overline{S}_{ky} is the complementary signal of S_{yk} . v_{ek} , v_{Hk}^{sw} , v_{Ck}^{sw} and i_k^{sw} are the input voltage, the switching output voltage, the switching FB cell input capacitor voltage and the switching FB cell input inductance current of the k th FB cell, respectively,

while i_o^{sw} and v_o^{sw} correspond to the output current and voltage of the inverter, respectively. Depending on the position of the switches, the value of S_{ky} varies and affects the internal cell signal waveforms. In order to simplify the equations, a slow variation assumption is made by considering the signal frequency is kept low relative to the switching frequency. An average model can be proposed where the variable x represents the moving average of the x^{sw} , where x can be replaced either by v_{Hk} , v_{Ck} , i_k , v_o or i_o . In this work, the objective is to balance the values of the output voltages of the FB cells, v_{Hk} , called the Cell Variable (CV), and to regulate the output current, i_o , which is the Global Variable (GV). A distributed approach for the control implementation is proposed to provide a way to easily insert or remove an FB cell without adding complexity to the balance control system.

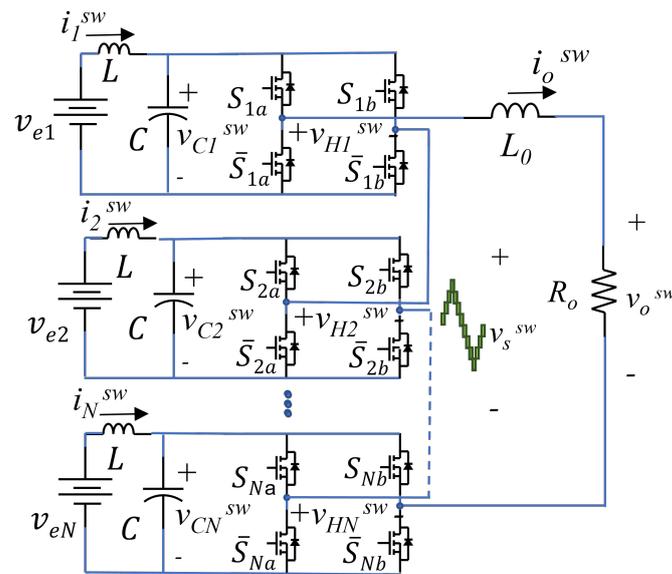


Figure 1. Cascaded Full-Bridge Multilevel Converter of N FB cells.

Considering that the outputs of the FB cells are connected in series, the same average current i_o flows through the output nodes of each FB cell. Therefore, balancing their output voltages is equivalent to balancing the power delivered by each cell. In accordance with Figure 1, the dynamic equations of the signals of the FB cell are:

$$i_k = \frac{1}{L} v_{ek} - R_L \frac{1}{L} i_k - \frac{1}{L} v_{c_k} \tag{1}$$

$$\dot{v}_{c_k} = \frac{1}{C} i_k - \frac{1}{C} u_k i_o \tag{2}$$

$$i_o = \frac{1}{L_o} \sum_{k=1}^N v_{c_k} u_k - \frac{1}{L_o} (R_x + R_o) i_o \tag{3}$$

where R_L is the series resistance of the inductance L and R_x corresponds to $2NR_{ds} + R_{L_o}$, R_{DS} is the drain-source-ON resistance of the MOSFET and R_{L_o} is the series resistance of L_o . $u_k = d_{ka} - d_{kb}$, d_{ky} is the duty cycle of S_{ky} . The modulation strategy used for this converter corresponds to an interleaved unipolar PWM. Therefore, $d_{bk} = 1 - d_{ak}$, producing $u_k = 2d_{ak} - 1$. It should be mentioned that because the maximum and minimum values of the duty-cycles are 1 and 0, respectively, u_k is bounded in $-1 < u_k < 1$.

The dynamical model of the FB cell output voltage v_{Hk} is:

$$v_{H_k} = v_{C_k} u_k \tag{4}$$

In accordance with (1), (2), (3) and (4), the equivalent circuit of the converter is obtained and is shown in Figure 2:

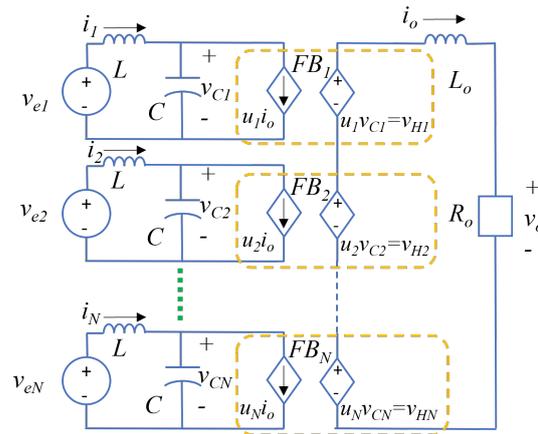


Figure 2. Equivalent circuit of the average model of the Cascaded Multilevel Converter of N FB-cells.

Considering that, in the CFBMC, all the input voltages v_{ek} present an identical average value, they can be computed as the sum of a DC component \bar{v}_e and a local deviation \hat{v}_{ek} . Hence, according to [12,30], it is possible to simplify the model, considering that the deviations of the input voltage and the resulting oscillations produced by the input filter operate as a disturbance. Therefore:

$$v_{Ck} = \delta_{v_{Ck}} + \bar{v}_e + \hat{v}_{ek} \tag{5}$$

where $\delta_{v_{Ck}}$ is the contribution of the filter oscillations on the cell capacitor voltage.

Based on (3) and (5), the converter behaves like the presented model:

$$i_o = \frac{1}{L_o} \sum_{k=1}^N (\bar{v}_e u_k + \delta_{v_{Hk}}) - \frac{1}{L_o} (R_x + R_o) i_o \tag{6}$$

$$v_{Hk} = \bar{v}_e u_k + \delta_{v_{Hk}} \tag{7}$$

where $\delta_{v_{Hk}} = (\delta_{v_{Ck}} + \hat{v}_{ek}) u_k$ represents the total contribution of the disturbances.

Based on (6) and (7), Figure 3 presents the equivalent linear circuit:

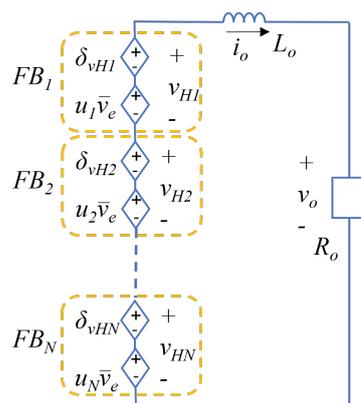


Figure 3. Equivalent circuit of the linear model of the Cascaded Multilevel Converter of $N + 1$ voltage levels.

This linear equivalent circuit is simpler than the previous one and takes into account the variations that the input voltages of each cell may present. Because (6) represents the linear model of the inverter, it becomes possible to express its linear behavior in the Laplace domain:

$$I_o(s) = \frac{1}{L_o s + (R_x + R_o)} \sum_{k=1}^N (\bar{v}_e U_k(s) + \Delta_{V_{Hk}}(s)) \tag{8}$$

$$V_{Hk}(s) = \bar{v}_e U_k(s) + \Delta_{V_{Hk}}(s) \tag{9}$$

where $\Delta_{V_{Hk}}(s)$ is the Laplace transform of $\delta_{v_{Hk}}$.
Then, expressing it as a matrix form:

$$I_o(s) = G(s) \mathbf{V}_1^T (\bar{v}_e \mathbf{U}(s) + \Delta_{\mathbf{V}_H}(s)) \tag{10}$$

$$\mathbf{V}_H(s) = \bar{v}_e \mathbf{U}(s) + \Delta_{\mathbf{V}_H}(s) \tag{11}$$

where $G(s) = \frac{1}{L_o s + (R_x + R_o)}$, $\Delta_{\mathbf{V}_H}(s) = [\Delta_{V_{H1}}(s) \ \Delta_{V_{H2}}(s) \ \dots \ \Delta_{V_{HN}}(s)]^T$, $\mathbf{U}(s) = [U_1(s) \ U_2(s) \ \dots \ U_N(s)]^T$, $\mathbf{V}_1 = [1 \ 1 \ \dots \ 1]^T$.

Finally, Figure 4 shows the block diagram of (10) and (11). It clearly shows that the resulting output current $I_o(s)$ flowing through the converter inductor is a contribution of the average value of the cell battery voltages \bar{v}_e , the disturbances they can produce $\Delta_{\mathbf{V}_H}(s)$ and the duty-cycles of the PWM control signals $\mathbf{U}(s)$ applied to the cells.

Thanks to this model, a decentralized controller which is used to balance the output voltage of the cells v_{Hk} can be proposed. It is presented in the next chapter.

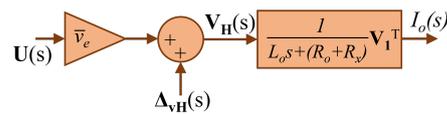


Figure 4. Block diagram of the linear model of the cascaded FB multilevel converter.

3. Description of the Decentralized Controller

The control proposed here is based on a local controller described in [3,21] for the voltage-cell balancing of an FCMC. Its first application to a grid-tied cascaded multilevel inverter was presented in [23] where simulations presented interesting results. Here, more investigations are carried out for the implementation of this controller in a CFBMC connected to a resistive load with an inductive filter using isolated input voltage sources per cell, such as batteries. Figure 5 shows the proposed local control structure.

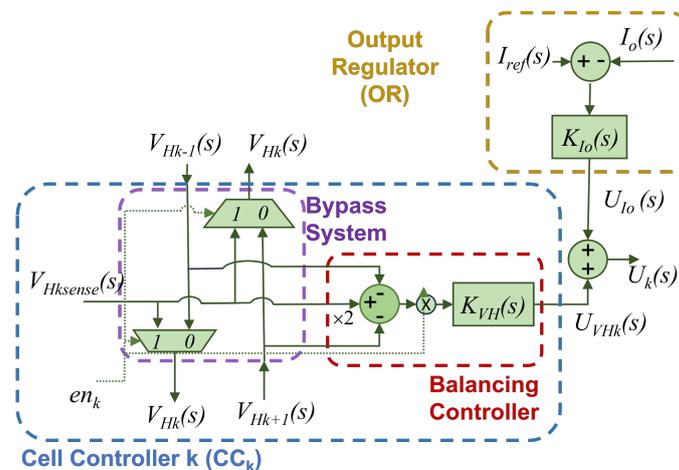


Figure 5. Block diagram of the cell controller (CC) computing a local correction for the duty-cycle $U_{V_{Hk}}(s)$ to balance the cell output voltages.

It comprises two stages, i.e., a Bypass Stage and a Balancing Controller, and receives a global signal computed via the output current regulator.

3.1. The Cell Power Balancing Controller

This stage of the control structure is the cell balancing controller. First, a comparison is made between the value of the FB cell output voltage $V_{Hk}(s)$ with the average value of the output voltages of the neighboring active FB cells, $V_{Hk-1}(s)$ and $V_{Hk+1}(s)$. An error is obtained and then canceled by a linear controller, $K_{VH}(s)$. This controller can be either a simple proportional (P) corrector providing constant static balancing errors or a proportional-integrator (PI) canceling the static errors or also a more sophisticated one to address high frequency concerns. A local duty-cycle correction $U_{V_{Hk}}(s)$ is obtained as described in (12). This correction is then applied to the local cell duty-cycle as shown in Figure 5.

$$U_{V_{Hk}}(s) = K_{VH}(s)(2V_{Hk}(s) - V_{Hk+1}(s) - V_{Hk-1}(s)) \quad (12)$$

Assuming all the cell controllers carry out the same operation and are connected with their close neighbors in a closed chain of communications, we may expect the system to converge toward the correct balancing of all the cell output voltages, leading to cell power balancing.

This method differs from what is commonly found in the literature, where the average of the output voltage for all the cells is calculated in a centralized way. Here, there is no need for high-speed communication between the cells and a centralized controller.

3.2. The Bypass Stage

The main goal of this block is to manage the communication between the cell controllers depending on their states (active or inactive, enabled or disabled). In accordance with Figure 5, the cell controller receives an enable signal used to turn OFF or ON the FB cell. When the k th FB cell is enabled, the bypass system sends the value of the cell output voltage provided by a local voltage sensor $V_{Hksense}(s)$ to the neighboring $(k + 1)$ th and $(k - 1)$ th cells, respectively. The values of the neighboring cell output voltages $V_{Hk+1}(s)$ and $V_{Hk-1}(s)$ are received to compute the local balancing error. When the k th FB cell is disabled, it is bypassed and the value of $V_{Hksense}(s)$ is no longer sent to the neighbors. Instead, the $(k + 1)$ th and $(k - 1)$ th cells directly receive the values of $V_{Hk-1}(s)$ and $V_{Hk+1}(s)$, respectively. This bypass stage guarantees the chain of communications is always closed. It allows the insertion or the removal of FB cells easily without adding complexity to the overall control system. This can be done during the converter operation. It should be noted also, if an FB cell is disabled, both High-Side switches S_{ka} and S_{kb} are turned on while the others are turned off. This allows the current I_o to continue flowing through the bypassed cell.

3.3. The Output Current Regulator

This part of the controller regulates the output current supplied to the load. It is a typical linear controller, $K_{I_o}(s)$, that can be either a classical PI compensator or any type of regulator depending on the specifications of the application in terms of bandwidth, transient step response and stability criteria. Its design is based on the knowledge of the open-loop transfer function of the system considered. In accordance with Figure 5, the signal $U_{I_o}(s)$ provided by the output current regulator, which represents the main duty-cycle of the system, is defined as:

$$U_{I_o}(s) = K_{I_o}(s)(I_{ref}(s) - I_o(s)) \quad (13)$$

In accordance with (12) and (13) and Figure 5, the local corrected duty-cycle signal of the FB cell is defined as:

$$U_k(s) = U_{I_o}(s) + U_{V_{Hk}}(s) \quad (14)$$

$$U_k(s) = K_{I_o}(s)(I_{ref}(s) - I_o(s)) + K_{VH}(s)(2V_{Hk}(s) - V_{Hk+1}(s) - V_{Hk-1}(s)) \quad (15)$$

It is important to note that only one output current regulator is present in the system. Its output signal $U_{I_o}(s)$ is shared among the converter FB cells to obtain the local corrected duty-cycle signals $U_k(s)$.

The control method illustrated in Figure 5 is applied to each FB cell. Then the cells are connected together in a closed-loop chain of communications to exchange with their close neighbors the values of their output voltage. The resulting control scheme is shown in Figure 6.

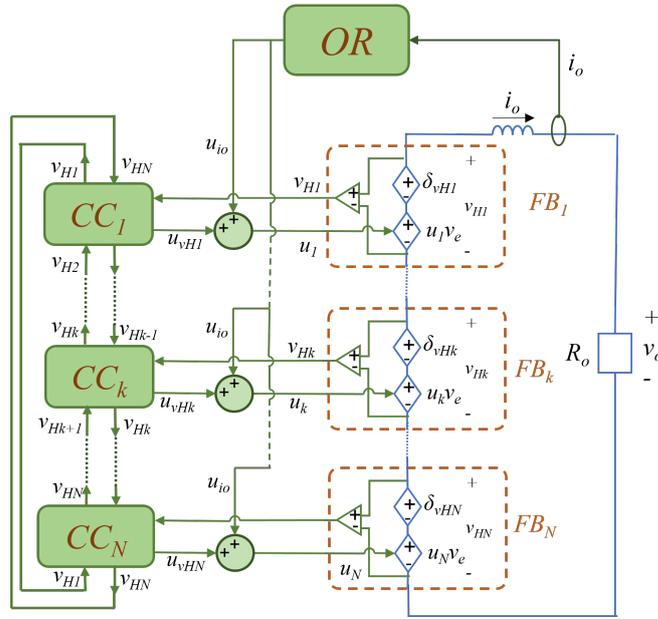


Figure 6. Architecture of the decentralized control of the CFBMC.

A global output current loop is present to regulate the current delivered to the load. It computes the value of the duty-cycle applied to the FB cells connected in series. Thanks to the interleaving of the PWM signals obtained, an apparent frequency equal to N times the switching frequency is observed at the output and reduces the inductor current ripple. This helps to decrease the value of the converter inductor for a given current ripple constraint. The cell controllers compute local corrections $U_{V_{Hk}}(s)$, add this correction to the main duty-cycle value $U_{I_o}(s)$ and produce a local corrected duty-cycle $U_k(s)$ to balance their own cell output voltage with those of their neighbors. They are all involved in a closed-loop chain of communications.

Notice that the N th cell communicates with the first and the $(N - 1)$ th cells and the first cell communicates with the second and the N th ones, closing the chain of the communications.

Expressing (15), for all the values of k , $\{1, 2, \dots, N\}$ as a matrix form, it follows that:

$$\mathbf{U}(s) = K_{I_o}(s) \left(I_{ref}(s) - I_o(s) \right) \mathbf{V}_1 + K_{V_H}(s) \mathbf{D}_{\text{diff}} \mathbf{V}_H(s) \tag{16}$$

where

$$\mathbf{D}_{\text{diff}} = \begin{bmatrix} 2 & -1 & 0 & \dots & 0 & -1 \\ -1 & 2 & -1 & \ddots & \vdots & 0 \\ 0 & -1 & 2 & \ddots & 0 & \vdots \\ \vdots & 0 & \ddots & \ddots & -1 & 0 \\ 0 & \vdots & \ddots & -1 & 2 & -1 \\ -1 & 0 & \dots & 0 & -1 & 2 \end{bmatrix}$$

The local duty-cycles $K_k(s)$ are then a contribution of the computation result $U_{I_o}(s)$ of the global current loop, dependent on the difference of the converter output current $I_o(s)$

and the current reference $I_{ref}(s)$ imposed by the user and the local correction $U_{V_{Hk}}(s)$ balancing the FB cell output voltages dependant on the isolated input cell voltage $V_{Hksense}(s)$ mismatches. It should be noted that the matrix \mathbf{D}_{iff} represents the topology of the interconnections put in place to help the cell controller to compute its duty-cycle correction, i.e., communicating only with their close neighbors. This matrix is circular and has the advantage of being easily diagonalizable. It will help to determine the different responses of the modes presented by this balancing method.

4. Closed-Loop System Analysis

This section is dedicated to the mathematical study of the closed-loop system using the proposed controller. An analysis of the closed-loop transfer functions which comprise the output current regulator and the local balancing controller makes it possible to determine the nature and the appropriate parameters of the controllers used. Their design is discussed in the next chapter. The block diagram of the system including the linear model of the converter with the controllers is shown in Figure 7.

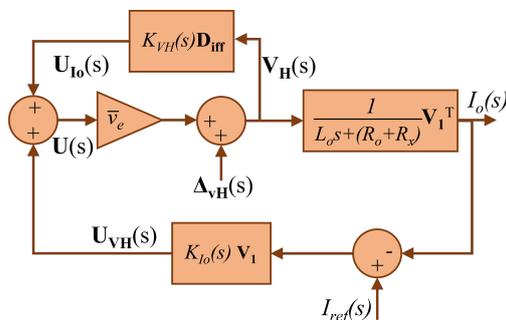


Figure 7. Block diagram of the Closed-Loop system with the proposed controller.

Compared to the one of Figure 4, it can be seen that two control loops have been added, i.e., the output current regulation loop using $K_{I_o}(s)$ and the FB cell output voltage balancing loop using the corrector $K_{V_H}(s)$. Because the converter implements several cells, the system is a matrix. The vector $\Delta_{V_H}(s)$ represents the voltage deviations from the value \bar{v}_e which may exist on the input voltages of the cells. It acts as a disturbance input vector and the resulting vector $\mathbf{U}(s)$ represents the corrected duty-cycles of the cells.

Thanks to Figure 7, both the open-loop and the closed-loop transfer functions of the output current regulation loop and the ones of the cell output voltage balancing loops can be determined. They are necessary to determine the appropriate parameters of the correctors for a desired bandwidth and to ensure the system stability.

4.1. Output Current Regulation Loop Analysis

To design the output regulator, it is necessary to determine the output current regulation loop transfer function. Inserting the decentralized controller expression proposed in (16) into the model of the output current control loop of the inverter and taking into account that $\mathbf{V}_1^T \mathbf{V}_1 = N$ and $\mathbf{V}_1^T \mathbf{D}_{iff} = 0$ in (10), one obtains:

$$I_o(s) = \underbrace{\frac{N\bar{v}_e K_{I_o}(s)}{L_o s + R_{x0}}}_{F_{ol_{I_o}}(s)} (I_{ref}(s) - I_o(s)) + \frac{1}{L_o s + R_{x0}} \mathbf{V}_1^T \Delta_{V_H}(s) \tag{17}$$

where $R_{x0} = R_x + R_o$ and $F_{ol_{I_o}}(s)$ is the open-loop transfer function of the output current regulator.

Notice that the term related to the balancing control stage is removed in the transfer function $F_{ol_{I_o}}(s)$ because \mathbf{D}_{iff} represents the Laplacian of a graph. Indeed, according to [3,21,23], the sum of its elements of the rows and the sum of its elements of the columns

is zero. Because this matrix is post multiplied by \mathbf{V}_1 , the results are zero. Based on $F_{olI_o}(s)$, the design of $K_{I_o}(s)$ is provided in the Section 5.

In order to obtain a better understanding of the influence of the balancing control loop on the output current $I_o(s)$, it is necessary to analyze the closed-loop transfer function of the output current regulation loop, $F_{clI_o}(s)$, which is defined below.

$$I_o(s) = \underbrace{\frac{N\bar{v}_e K_{I_o}(s)}{L_o s + R_{x0} + N\bar{v}_e K_{I_o}(s)}}_{F_{clI_o}(s)} I_{ref}(s) + \underbrace{\frac{1}{L_o s + R_{x0} + N\bar{v}_e K_{I_o}(s)}}_{F_{dist}(s)} \mathbf{V}_1^T \Delta \mathbf{V}_H(s) \quad (18)$$

This shows that the resulting regulated output current is provided by the separate contribution of the current loop $F_{clI_o}(s)$ and that of the cell input voltage disturbances via the transfer function $F_{dist}(s)$. Indeed, disturbances on the cell input voltages imply cell voltage mismatches and generate also slightly damped oscillations on the cell capacitors due to the second-order filter LC. Temporary variations appear on the cell local duty-cycles, generating output current transients.

For the following analysis of the control loops, it should be considered, if the output regulator is well designed, when $I_{ref}(s)$ is a step, $I_{ref}(s) = \frac{I_a}{s}$ at $t \rightarrow \infty$ means that with $s \rightarrow 0$, $i_o(t) = I_a$, producing $F_{clI_o}(s) = 1$ when $s \rightarrow 0$.

4.2. Cell Voltage Balancing Control Loop Analysis

Now, the balancing control loop has to be analyzed inserting (16) in (11); it follows that:

$$\mathbf{V}_H(s) = \bar{v}_e K_{V_H}(s) \mathbf{D}_{\text{iff}} \mathbf{V}_H(s) + \bar{v}_e K_{I_o}(s) (I_{ref}(s) - I_o(s)) \mathbf{V}_1 + \Delta \mathbf{V}_H(s) \quad (19)$$

Inserting (18) into (19), one obtains:

$$\begin{aligned} \mathbf{V}_H(s) = & \bar{v}_e K_{V_H}(s) \mathbf{D}_{\text{iff}} \mathbf{V}_H(s) + \frac{\bar{v}_e K_{I_o}(s) (L_o s + R_{x0})}{L_o s + R_{x0} + N\bar{v}_e K_{I_o}(s)} I_{ref}(s) \mathbf{V}_1 \\ & + \left(\mathbb{I} - \frac{\bar{v}_e K_{I_o}(s)}{L_o s + R_{x0} + N\bar{v}_e K_{I_o}(s)} \mathbf{V}_1 \mathbf{V}_1^T \right) \Delta \mathbf{V}_H(s) \end{aligned} \quad (20)$$

Then, the expression is simplified and an open-loop transfer function is considered by inserting an excitation signal on the cell output voltages:

$$\begin{aligned} \mathbf{V}_H(s) = & \underbrace{\bar{v}_e K_{V_H}(s) \mathbf{D}_{\text{iff}}}_{\mathbf{F}_{olV_H}(s)} \mathbf{V}_H'(s) + \frac{1}{N} F_{clI_o}(s) (L_o s + R_{x0}) I_{ref}(s) \mathbf{V}_1 \\ & + \left(\mathbb{I} - \frac{1}{N} F_{clI_o}(s) \mathbf{V}_1 \mathbf{V}_1^T \right) \Delta \mathbf{V}_H(s) \end{aligned} \quad (21)$$

where $\mathbf{V}_H'(s)$ is the excitation signal.

One can see that the FB cell output voltages are dependent on the current reference value $I_{ref}(s)$ and the input voltage disturbances $\Delta \mathbf{V}_H(s)$. The voltage balancing open-loop transfer function $\mathbf{F}_{olV_H}(s)$ is then identified.

The controller $K_{V_H}(s)$ will be defined in the Section 5 based on the desired bandwidth of $F_{olV_H}(s)$, which is directly linked to the eigenvalues of the matrix \mathbf{D}_{iff} .

4.3. Global Closed-Loop Analysis

In accordance with (17) and (19), Figure 8 shows the simplified closed-loop block diagram.

This block diagram of the closed-loop system is similar to the one presented in Figure 7, but the two loops, i.e., the output current regulation loop and the cell output voltage balancing loop, are presented separately. This is possible because the vector $\mathbf{V}_H(s)$ is made

of the sum of a constant term \bar{v}_e and a disturbance. This helps in considering the separate contributions of the disturbances on the two closed-loop systems involved.

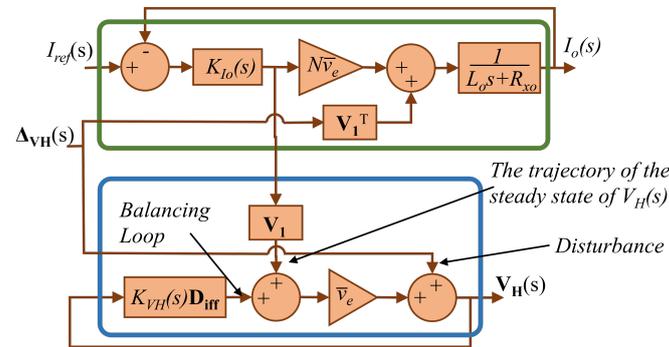


Figure 8. Simplified closed-loop transfer function of the system.

Notice that the FB cell voltage vector $\mathbf{V}_H(s)$ depends on three inputs; one corresponds to the balancing controller, another depends on the disturbance, $\Delta \mathbf{V}_H(s)$, and the last one depends on the output current loop, which affects all the cell voltages at the same time. Analyzing in steady state, in accordance with (21), when $s \rightarrow 0$, if the controller is well designed, $F_{clIo}(s) = 1$, entailing that the trajectory in steady states for $\mathbf{V}_H(s)$ is $\frac{R}{N} I_{ref}(s)$.

5. Design of the Controllers

Now, both controllers have to be designed, taking into account some criteria, such as the bandwidth of the loops and the stability of the overall system.

5.1. Design of the Output Current Regulator

Based on $F_{olIo}(s)$, for a stable and low bandwidth system, a simple integral corrector can be proposed for $K_{Io}(s)$. Then, the static error between I_{ref} and I_o is canceled and the stability is ensured by considering the open-loop transfer function phase margin.

Because the chosen controller type for the output current regulator is an Integral (I) controller:

$$K_{Io}(s) = k_i \frac{1}{s} \tag{22}$$

The Bode analyses of $F_{olIo}(s)$, $K_{Io}(s)$ and $G(s)$ are shown in Figure 9, where $G(s)$ correspond to the natural response of the converter.

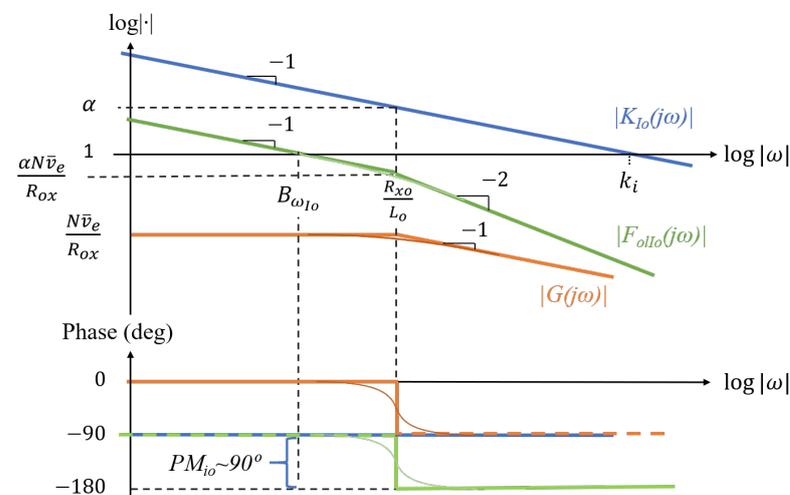


Figure 9. Bode diagram of $G(s)$, $K_{Io}(s)$ and $F_{olIo}(s)$.

At low frequency, with $\omega \ll R_{xo}/L_o$, the module of the open-loop transfer function presents a slope of -20 dB/decade. That is to say, its phase is equal to -90° . At high frequency, with $\omega \gg R_{xo}/L_o$, due to the pole provided by $G(s)$, a slope of -40 dB/decade is obtained, which corresponds to a phase close to -180° . In order to guarantee a sufficient phase margin, i.e., more than 60° , for stability purposes, the bandwidth $B_{\omega_{I_o}}$ has to be less than half of R_{xo}/L_o .

Considering Figure 9, it becomes possible to determine the value of the corrector parameter k_i for a given bandwidth $B_{\omega_{I_o}}$. It follows that:

$$\alpha = \frac{k_i L_o}{R_{xo}} \tag{23}$$

$$\frac{\alpha N \bar{v}_e}{R_{xo}} = \frac{B_{\omega_{I_o}} L_o}{R_{xo}} \tag{24}$$

$$k_i = \frac{B_{\omega_{I_o}} R_{xo}}{N \bar{v}_e} \tag{25}$$

where $B_{\omega_{I_o}}$ is the bandwidth of the output regulator.

In practice, $B_{\omega_{I_o}}$ is fixed ten times less than the switching frequency of the MOSFETs, f_{sw} .

5.2. Design of the Cell Voltage Balancing Controllers

The cell voltage balancing controller is designed based on the $F_{ol_{VH}}(s)$ expression. In accordance with (21), $F_{ol_{VH}}(s)$ is proportional to the matrix D_{iff} . Then, the study of the eigenvectors of this matrix makes it possible to replace it by a diagonal matrix whose terms reveal its eigenvalues. Decomposing D_{iff} in a diagonal matrix leads to:

$$D_{\text{iff}} = V_{\text{eig}} \Lambda V_{\text{eig}}^{-1} \tag{26}$$

$$F_{ol_{VH}}(s) = V_{\text{eig}} \underbrace{\bar{v}_e K_{VH}(s)}_{\Pi(s)} V_{\text{eig}}^{-1} \tag{27}$$

$$V_{\text{eig}}^{-1} V_H(s) = \Pi(s) V_{\text{eig}}^{-1} V'_H(s) \tag{28}$$

where Λ is a diagonal matrix and V_{eig} is the eigenvector of D_{iff} .

Consequently, the open-loop transfer function of the cell output voltage balancing system can be expressed on a new basis where the vector $V_{\text{eig}}^{-1} V_H(s)$ is deduced from the excitation vector $V_{\text{eig}}^{-1} V'_H(s)$ using the diagonal matrix $\Pi(s)$. It should be noted that one eigenvalue of D_{iff} is equal to 0, because it is a Laplacian of a graph.

$$\Lambda = \begin{bmatrix} \lambda_1 & 0 & \dots & 0 \\ 0 & \lambda_2 & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \dots & 0 & \lambda_N \end{bmatrix}; \lambda_1 = 0 \tag{29}$$

$\Pi(s)$ represents the transfer function of the modal responses of the balancing system, defined as:

$$\Pi(s) = K_{VH}(s) \begin{bmatrix} p_1(s) & 0 & \dots & 0 \\ 0 & p_2(s) & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \dots & 0 & p_N(s) \end{bmatrix} \tag{30}$$

where $p_k(s) = \bar{v}_e \lambda_k$.

Finally, on this new basis, N modes exist and have to be studied. The open-loop transfer function $F_{olm_k}(s)$ of the k th mode is:

$$F_{olm_k}(s) = \bar{v}_e \lambda_k K_{VH}(s) \tag{31}$$

It should be mentioned that \mathbf{D}_{iff} corresponds to a circulant matrix \mathbf{M}_C , which is described as:

$$\mathbf{M}_C = \begin{bmatrix} c_1 & c_2 & \cdots & c_N \\ c_N & c_1 & \ddots & \vdots \\ \vdots & \ddots & \ddots & c_2 \\ c_2 & \cdots & c_N & c_1 \end{bmatrix} \tag{32}$$

Since \mathbf{D}_{iff} is a circulant matrix, it is possible to obtain an expression of its eigenvalues. According to [31], the eigenvalues of a circulant matrix are:

$$\lambda_k = \sum_{n=1}^N c_n e^{j \frac{2\pi(n-1)(k-1)}{N}} \tag{33}$$

where $\hat{j} = \sqrt{-1}$.

It can be observed that for the case of the matrix \mathbf{D}_{iff} , the coefficients, c_k s, are:

$$c_n = \begin{cases} 2 & ; n = 1 \\ -1 & ; n = \{2, N\} \\ 0 & ; n = \{3, 4, \dots, N-1\} \end{cases} \tag{34}$$

Therefore, in accordance with (33) and (34), the eigenvalues of \mathbf{D}_{iff} are defined as:

$$\begin{aligned} \lambda_k &= c_1 + c_2 e^{\frac{2\pi(k-1)}{N} \hat{j}} + c_N e^{\frac{2\pi(k-1)(N-1)}{N} \hat{j}} \\ \lambda_k &= 2 \left(1 - \cos \left(\frac{2\pi(k-1)}{N} \right) \right) \end{aligned} \tag{35}$$

Notice that the first eigenvalue, λ_1 , is equal to 0, validating that it also represents the Laplacian of a graph. λ_1 corresponds to the common mode of the balancing system. This mode is only influenced by the output current regulation loop which imposes the average value of the cell output voltages. Furthermore, because of the symmetric property of the cosine, the k th eigenvalue is equal to the $(N + 1 - k)$ th eigenvalue. Finally, the highest eigenvalue is obtained for $k = \frac{N}{2} + 1$ when N is even and $k = \frac{N \pm 1}{2} + 1$ when N is odd. The maximum case is produced when N is even, generating $\lambda_{max} = 4$. For odd values of N the highest eigenvalue tends to be 4 when N increases. The design of the balancing controller is based on the possible maximum eigenvalue, λ_{max} , and the minimum eigenvalue, $\lambda_{min} = \lambda_1$, whose values are 4 and 0, respectively.

$\lambda_{min} = 0$ means the system presents a pure integrator that theoretically is stable. However, due to numerical approximations in the implementation, the system may diverge after a long period of time. For that reason, the selected controller corresponds to a low-pass filter that ensures the stability of the system, with a pole located at low frequency. Hence, the proposed controller is:

$$K_{VH}(s) = k_{pV} \left(\frac{k_{iV}}{s + k_{iV}} \right) \tag{36}$$

In order to determine the parameters of the controller, Figure 10 shows the Bode diagram of $K_{VH}(s)$, $p_k(s)$ and $f_{olm_k}(s)$, respectively. The higher the value of λ_k , the higher the bandwidth of the mode. Consequently, the maximum value of λ_k is considered, i.e., $\lambda_{max} = 4$. The proportional term of the low-pass filter k_{pV} is determined by the

maximum tolerated accuracy for the balancing of the cell output voltages. Then, as shown in the Bode diagram of Figure 10, the bandwidth $B_{\omega V}$ is set using the k_{iV} parameter:

$$v_e \lambda_{max} k_{pV} = \frac{B_{\omega V}}{k_{iV}} \tag{37}$$

$$k_{iV} = \frac{B_{\omega V}}{v_e \lambda_{max} k_{pV}}$$

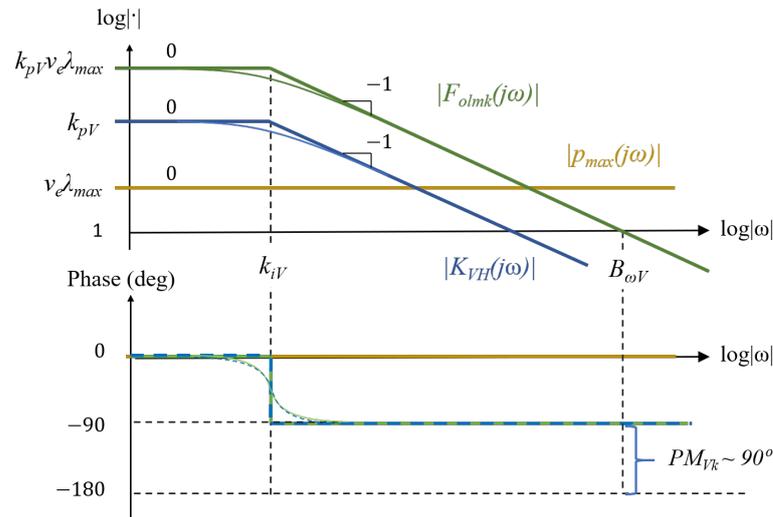


Figure 10. Bode diagram of $p_{max}(s)$, $K_{VH}(s)$ and $F_{olmk}(s)$ of the CFBC.

In order to avoid any interference between the loops, the bandwidth, $B_{\omega V}$, must be ten times less than the bandwidth of the output current regulation loop, $B_{\omega I_o}$. Stability is guaranteed because the phase of the open loop function is always greater than or equal to -90° leading to a phase margin greater than 90° .

5.3. Modal Response Simulation

The simulations are performed with a 5-FB cell CFBMC, using 48V batteries. The parameters of the application and the ones of the controllers are shown in Table 1.

Table 1. Parameters of the CFBMC.

Parameter	Value	Unit
Number of FB Cells N	5	
Input Voltage (v_e)	48	V
Input Inductance (L)	1.8	mH
ESR of L (R)	200	mΩ
Input Capacitance (C)	4	mF
Drain-Source ON Resistance (R_{DS})	58	mΩ
Frequency of the Inverter (f)	60	Hz
I_{ref} as an Inverter	$1.7 \sin(2\pi ft)$	A
I_{ref} as a DC/DC Converter	1.7	A
Switching Frequency (f_{sw})	12.5	kHz
Load Resistance (R_o)	60–100	Ω
k_i	1884	$A^{-1}s^{-1}$
k_{pV}	39	$V^{-1}s^{-1}$
k_{iV}	37.7	rads/s

The objective here is to observe the modal response of the voltage balancing loop. For $N = 5$, Λ corresponds to:

$$\Lambda = \frac{\sqrt{5}}{2} \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & \sqrt{5}-1 & 0 & 0 & 0 \\ 0 & 0 & \sqrt{5}+1 & 0 & 0 \\ 0 & 0 & 0 & \sqrt{5}+1 & 0 \\ 0 & 0 & 0 & 0 & \sqrt{5}-1 \end{bmatrix} \quad (38)$$

Appendix A shows the demonstration of these values; their numeric values are:

$$[\lambda_1 \ \lambda_2 \ \lambda_3 \ \lambda_4 \ \lambda_5]^T = [0 \ 1.38 \ 3.62 \ 3.62 \ 1.38]^T$$

while the modal matrix, V_{eig} , is:

$$V_{\text{eig}} = \begin{bmatrix} 1.00 & 1.00 & 1.00 & 1.00 & 1.00 \\ 1.00 & -0.57 & -0.52 & -2.00 & 1.33 \\ 1.00 & -1.35 & -0.16 & 2.23 & -0.18 \\ 1.00 & -0.26 & 0.78 & -1.61 & -1.44 \\ 1.00 & 1.19 & -1.1 & 0.38 & -0.72 \end{bmatrix} \quad (39)$$

$\underbrace{\hspace{1.5cm}}_{V_{\text{eig}}(\lambda_1)} \ \underbrace{\hspace{1.5cm}}_{V_{\text{eig}}(\lambda_2)} \ \underbrace{\hspace{1.5cm}}_{V_{\text{eig}}(\lambda_3)} \ \underbrace{\hspace{1.5cm}}_{V_{\text{eig}}(\lambda_4)} \ \underbrace{\hspace{1.5cm}}_{V_{\text{eig}}(\lambda_5)}$

Using the eigenvectors as the initial conditions, Figure 11 shows the modal response of the system.

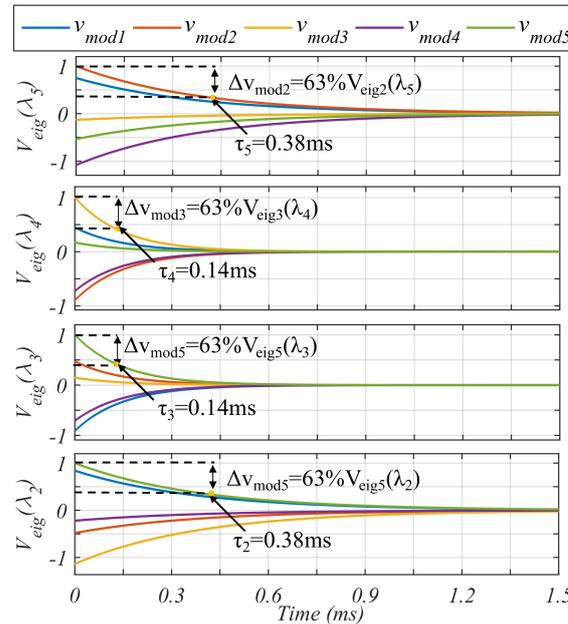


Figure 11. Modal response of the CFBMC with the decentralized controller.

It is clearly observed that the system is stable and the time responses of the modes are very different. Depending on the parameter k_{pV} of the decentralized controller, this time response can be adjusted. Table 2 shows a comparison between the theoretical time constants and the ones obtained via simulation.

Table 2. Time constants related to the modes of the CFBMC.

Mode Time Constant τ_k	Theoretical (ms)	Simulated (ms)
τ_2	0.384	0.38
τ_3	0.146	0.14
τ_4	0.146	0.14
τ_5	0.384	0.38

It should be noted that, since there are two pairs of similar eigenvalues, there are also two pairs of time constants, which means that there are two double poles for each time constant. Furthermore, it can be observed that simulated and theoretical values are very similar, validating the performance of the controller.

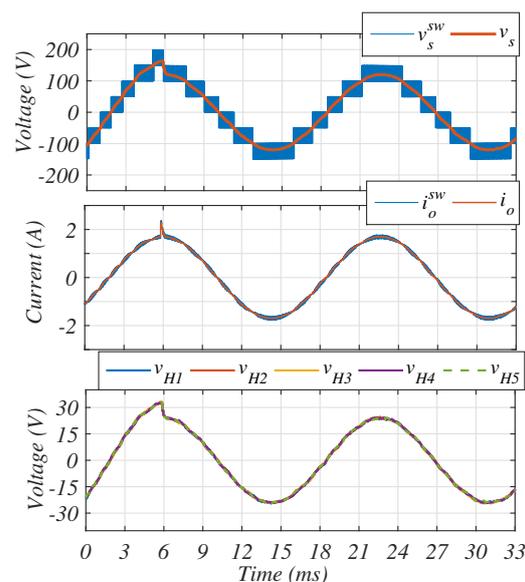
6. Simulations and Experimental Results

Both simulations and experimental results, developed hereafter, are obtained with the converter working as a DC/AC converter, with three different tests: an input voltage step, a load step and a cell insertion during operation.

6.1. Full System Simulation Results

The simulations are developed in Simulink with SimPowerSystem tool, with sampling frequency of $1000f_{sw}$. The solver algorithm used ODE23tb(stiff/TR-BDF2), which is a differential equation solver method for Stiff equations that use the trapezoidal rules with a backward differential formula of second degree. The first simulation test corresponds to a load transient from 95Ω to 70Ω . Figure 12 shows v_s and i_o when the converter works as a DC/AC converter.

It is observed that before the disturbance occurs, the multilevel converter uses nine voltage levels. After the disturbance, only seven levels are required to regulate the output current. Notice also that the CVs are balanced throughout the simulation, before and after the disturbance, validating for DC/AC conversion that when a disturbance in the output current occurs, the CVs are not unbalanced; only their common average value are affected. Furthermore, the current is stabilized during a small transient, less than 1 ms.

**Figure 12.** Load transient test as a DC/AC converter.

The next simulation result, shown in Figure 13, corresponds to an input cell voltage disturbance, i.e., a step voltage from 40 to 50 V for the inverter with a resistive load of 77Ω .

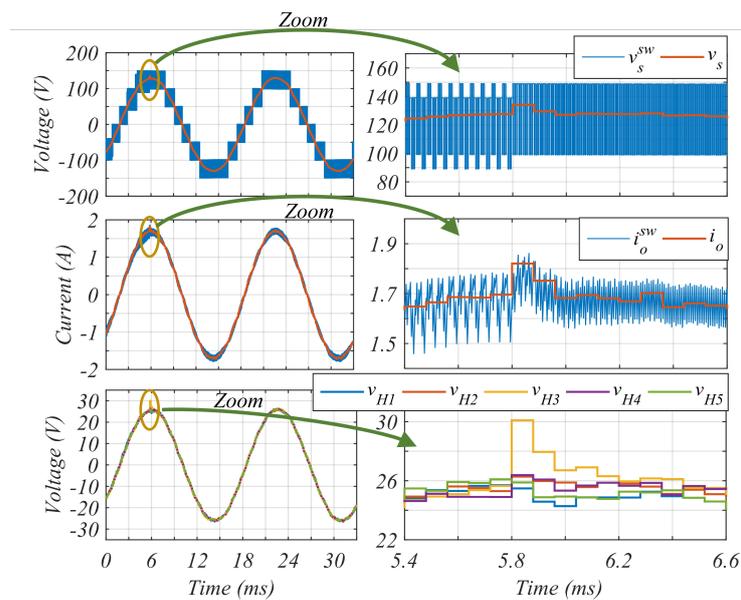


Figure 13. Input cell voltage step response simulation for the inverter case.

It should be noted that the voltage disturbance almost affects neither the output current i_o nor the output voltage v_s , while the CVs are automatically balanced thanks to the decentralized controllers in only 0.5 ms. Figure 13 also shows that, by the nature of the inverter, when one of the input voltages is 40 V, there exists an asymmetric ripple in i_o^{sw} and v_s^{sw} and when the input voltage is 50 V, the ripples are equalized. However, in both cases the average output current i_o and the v_{Hk} s are well regulated and balanced, respectively.

The next simulation corresponds to a cell insertion during operation, going from 4 FB cells to 5 FB cells, when the converter operates as an inverter. Figure 14 shows the results obtained for the v_{Hk} s, i_o and v_s signals.

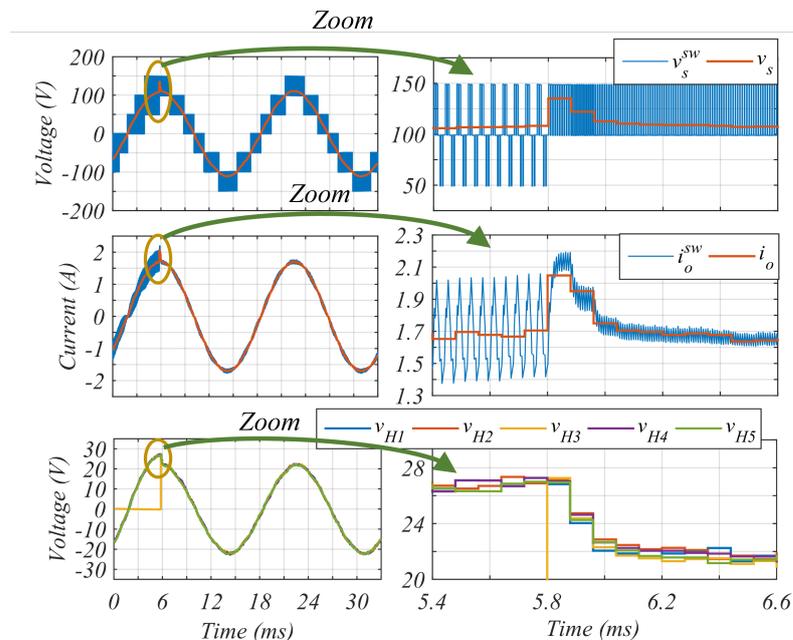


Figure 14. FB insertion simulation for blue, the inverter case.

It should be noticed that before the cell insertion, both i_o and v_s present a high ripple, due to a constant control signal interleaving set for five cells, i.e., signal phase. Even if the ripple is high, the average value of the output current is regulated when only four cells

are activated. When the fifth FB cell is inserted, i_o presents an overshoot and then it is stabilized in less than 0.25 ms. v_{Hk} voltages are balanced when there are four FB cells and then, when the fifth cell is inserted, they are auto balanced, reaching a new operation point in 0.25 ms approximately.

This test validates via simulation the three functions of the controller, the balancing of the CV, the regulation of the GV and the bypass system activation. It can be inferred that all the simulation results are in concordance with the previous theoretical study, producing the expected behavior in terms of reconfigurability, bandwidth and stability for this multilevel converter topology.

6.2. Experimental Results

The five-cell CFBMC is implemented in a laboratory prototype, as shown in Figure 15, with the parameters described in Table 1. It is fed by five 48 V Li-ion batteries. The switching device used in the FB cells is the IRFI4212H MOSFET. Voltage is read with the AMC1200 differential amplifier and current with the ACS714 Hall effect sensor. The control algorithm runs in a LAUNCHXL-F28379D development board. The measurements are carried out with an MSO-X 4034A oscilloscope, using N2783B and N2790 probes for current and voltage, respectively. More details related to the construction of this inverter are presented in [32].

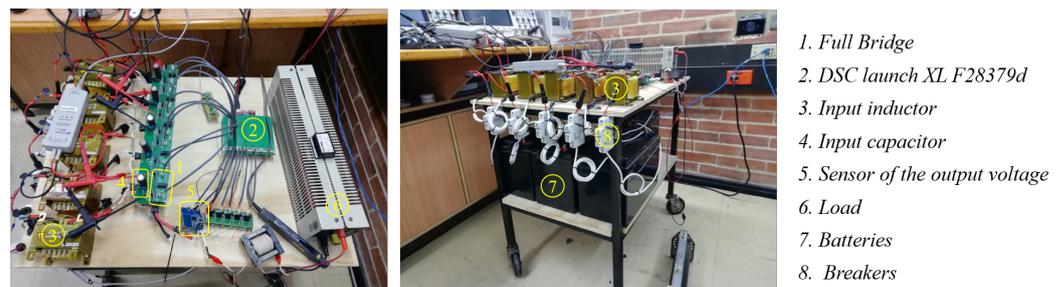


Figure 15. Setup of the Cascaded Full-Bridge Multilevel Inverter.

In order to compare the simulation and experimental results, the tests developed here are the same as the ones illustrated in the previous simulations.

Figure 16 shows the experimental results of the first test, corresponding to a load step (or load transient). It can be seen that there exists a concordance with the simulation results of this test, presenting similar overshoot in the current and similar settling time. Moreover, the switching levels of v_s are the same. Furthermore, as happened in the simulation, the operating points of v_{Hk} s change in 0.5 ms without any unbalance between them.

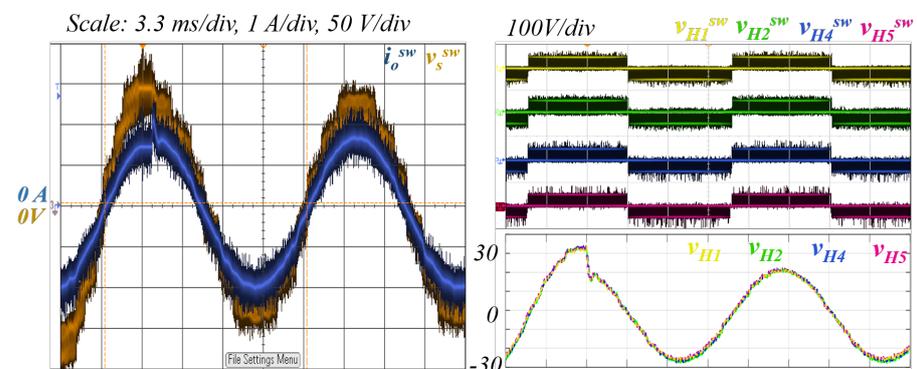


Figure 16. Load transient experimental test in DC/AC mode.

The next result corresponds to the disturbance in one input voltage FB cell. Figure 17 shows the behavior of the output current i_o^{sw} , the output voltage v_s^{sw} , the switching output voltage of each FB 1, 4 and 5, $v_{Hk}^{sw}, \forall k = \{1, 4, 5\}$, and their respective moving average, v_{Hk} .

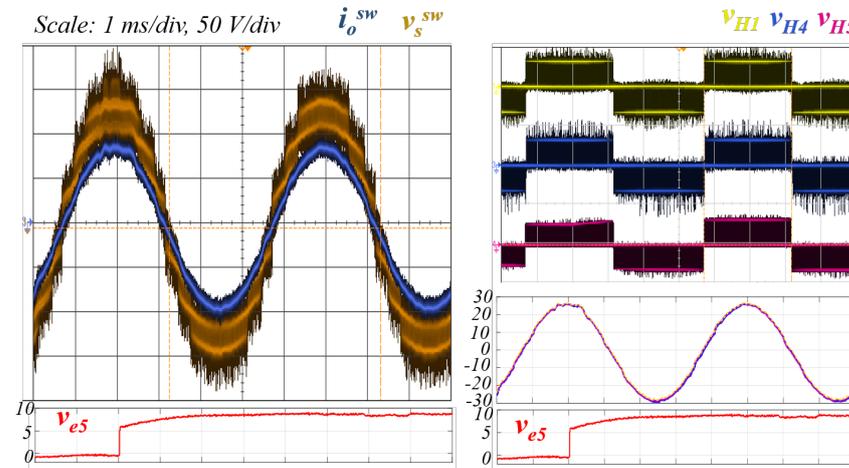


Figure 17. Input cell voltage disturbance experimental test.

It should be noted that the step voltage is almost not detected in v_{H5} . This is because the input filters presented in the converter smooth the effect of the voltage disturbance. Furthermore, it can be observed that during all the experiments v_{Hk} voltages are well balanced. This observation also validates the balancing controller, maintaining the same output voltage of each FB cell even when the input voltages change. Additionally, the output current is well regulated.

The next result, presented in Figure 18, corresponds to an FB cell insertion during operation, starting with four FB cells and inserting the fifth FB cell. It is important to note that the current follows the reference during all the experiments, presenting a small transient when the FB cell is inserted. Furthermore, it can be observed that the CVs are well balanced after the insertion, reaching a new operating point with a settling time of 0.6 ms, approximately. These values are in concordance with the predicted time constants of the system and show a strong similarity with the simulation results. This test validates the three stages of the controller, the balancing controller, the GV regulator and the bypass system.

It can be inferred that all the experimental tests are in concordance with the simulation tests and the theoretical studies developed in this paper, demonstrating the good performance of the controller for this topology.

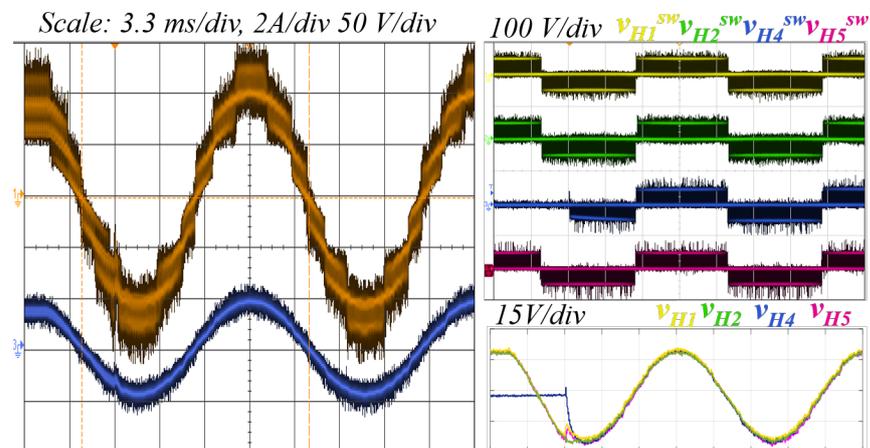


Figure 18. FB cell insertion experimental test in DC/AC mode.

7. Conclusions

A decentralized control method for balancing the power delivered by the cells of a cascaded full-bridge multilevel converter has been presented. It associates a controller for each full-bridge cell that communicates with its neighbors to balance the output cell voltages, making unnecessary the calculation of the average voltage value with a centralized controller.

The presented work gives to the cascaded full-bridge multilevel converter the ability to reconfigure by inserting or removing cells during operation without complicating the control architecture, which is valuable for systems integrating functional safety in the event of hardware faults. This characteristic also offers the option to easily set the number of cells to be used to track the converter maximum power efficiency, as a function of the load power.

Simulations and experimental results, with a five-cell converter, demonstrate robust and stable operation, guaranteeing the balance of the powers delivered by the cells, against load step transients, battery voltage disturbances and cell insertion.

Due to its modularity, this control method can manage any number of cells, making it viable for applications where several sources need to contribute with the same amount of power to the load, as might be the case with solar panels in a farm or batteries in energy storage systems or even any other power converter with multi-sources that must deliver the same amount of power, and, moreover, in high power applications where efficiency could be improved by using low voltage devices.

Future work is planned for balancing the state-of-charge of battery cells using a similar distributed control method. Moreover, a sensitivity analysis will be carried out to test the robustness of the system against the variability of the parameters.

Author Contributions: Investigation, M.V., R.D., M.C. and D.B.C.; Writing—original draft, M.V.; Writing—review & editing, M.V., R.D. and M.C.; Supervision, D.P. All authors have read and agreed to the published version of the manuscript.

Funding: This research was a collaboration project funded by the Institut National Polytechnique de Toulouse (INPT), and by Pontificia Universidad Javeriana (Project ID 9606). The APC was funded by the INPT.

Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this article:

v_{ek}	Input voltage of the k th FB cell
N	Number of FB cells
L	Inductance of the input filter of the FB cells
C	Capacitance of the input filter of the FB cells
L_o	Output Inductance of the MCC
R_o	Output Resistive Load
S_{ky}	Position of the switch of the High-Side of the k th FB cell and the branch y , which can be a for left side and b for right side
\bar{S}_{ky}	Position of the switch of the Low-Side of the k th FB cell and the branch y , which can be a for left side and b for right side
x^{sw}	Switching variable of the moving average variable x
i_k	Moving average current through the input voltage v_{ek}
v_{Ck}	Moving average voltage at the output of the input filter of the k th FB cell
v_s	Moving average of the converter output voltage before the output inductance

d_{ky}	Duty-cycle of the switch S_{ky}
\bar{i}_o	Moving average of the output current
v_{Hk}	Output voltage of the k th FB cell
\bar{v}_e	DC value of the input voltages of the FB cells
\hat{v}_{ek}	Variation of the input voltage of the k th FB cell
$\delta_{v_{Ck}}$	Ripple in the v_{Ck} produced by the effect of the input filter
\hat{v}_{ek}	Variation of the input voltage of the k th FB cell
\hat{v}_{ek}	Variation of the input voltage of the k th FB cell
CC	Cell controller
CFBMC	Cascaded Full-Bridge Multilevel Converter
CV	Cell Voltage
FB	Full-Bridge
FCMC	Flying Capacitor Multilevel Converter
GV	Global Variable
IGBT	Insulated-Gate Bipolar Transistor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MCC	Multi-Cellular Converter
OR	Output Regulator
SOC	State Of Charge

Appendix A. Demonstration of the Eigenvalues

For $N = 5$, the eigenvalues are:

$$\begin{aligned}\lambda_1 &= 2(1 - \cos(0)) \\ \lambda_2 &= 2(1 - \cos(\frac{2\pi}{5})) \\ \lambda_3 &= 2(1 - \cos(\frac{4\pi}{5})) \\ \lambda_4 &= 2(1 - \cos(\frac{6\pi}{5})) \\ \lambda_5 &= 2(1 - \cos(\frac{8\pi}{5}))\end{aligned}$$

Using trigonometric identities, follows to:

$$\begin{aligned}\lambda_1 &= 0 \\ \lambda_2 &= 2(1 - \cos(\frac{2\pi}{5})) \\ \lambda_3 &= 2(1 + \cos(\frac{\pi}{5})) \\ \lambda_4 &= 2(1 + \cos(\frac{\pi}{5})) \\ \lambda_5 &= 2(1 - \cos(\frac{2\pi}{5}))\end{aligned}$$

assigning $\alpha = \cos(\pi/5)$ and using trigonometric identities follows:

$$\begin{aligned}\lambda_1 &= 0 \\ \lambda_2 &= 4(1 - \alpha^2) \\ \lambda_3 &= 2(1 + \alpha) \\ \lambda_4 &= 2(1 + \alpha) \\ \lambda_5 &= 4(1 - \alpha^2)\end{aligned}$$

Hence, obtaining α all the eigenvalues are found. Taking into account that $\cos(\frac{\pi}{2}) = 0$, $\cos(2\frac{\pi}{5} + (\frac{1}{2})\frac{\pi}{5}) = 0$, hence:

$$\cos(2\frac{\pi}{5}) \cos\left(\left(\frac{1}{2}\right)\frac{\pi}{5}\right) - \sin(2\frac{\pi}{5}) \sin\left(\left(\frac{1}{2}\right)\frac{\pi}{5}\right) = 0$$

Using the double and half angle formulas and taking into account that $\alpha = \cos\left(\frac{\pi}{5}\right)$ follows:

$$(2\alpha^2 - 1) \frac{\sqrt{1+\alpha}}{\sqrt{2}} - 2\alpha \sqrt{1-\alpha^2} \frac{\sqrt{1-\alpha}}{\sqrt{2}} = 0$$

$$(\sqrt{1+\alpha})(2\alpha^2 - 1 - 2\alpha(1-\alpha)) = 0$$

$$(\sqrt{1+\alpha})(4\alpha^2 - 2\alpha - 1) = 0$$

$\alpha = -1$ ✗ because it produces an angle of $\pi/2$

$\alpha = \frac{1-\sqrt{5}}{4}$ ✗ because α should be positive

$$\alpha = \frac{1+\sqrt{5}}{4} \checkmark$$

Hence:

$$\lambda_1 = 0$$

$$\lambda_2 = \frac{\sqrt{5}}{2} (\sqrt{5} - 1)$$

$$\lambda_3 = \frac{\sqrt{5}}{2} (\sqrt{5} + 1)$$

$$\lambda_4 = \frac{\sqrt{5}}{2} (\sqrt{5} + 1)$$

$$\lambda_5 = \frac{\sqrt{5}}{2} (\sqrt{5} - 1)$$

References

1. Mohan, N.; Undeland, T.; Robbins, W.P. *Power Electronics: Converters, Applications and Design*; Wiley: Hoboken, NJ, USA, 1989.
2. Rashid, M.H. *Power Electronics: Devices, Circuits and Applications*; Pearson: London, UK, 2014.
3. Vivert, M.; Cousineau, M.; Ladoux, P.; Fabre, J. Decentralized Controller for the Cell-Voltage Balancing of a Multilevel Flying Cap Converter. In Proceedings of the PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 7–9 May 2019; pp. 1–8.
4. Fabre, J.; Ladoux, P.; Solano, E.; Gateau, G.; Blaquièrre, J. Full SiC multilevel chopper for three-wire supply systems in DC electric railways. In Proceedings of the 2016 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles International Transportation Electrification Conference (ESARS-ITEC), Toulouse, France, 2–4 November 2016; pp. 1–7. [[CrossRef](#)]
5. Fabre, J.; Ladoux, P.; Solano, E.; Gateau, G.; Blaquièrre, J. MVDC Three-Wire Supply Systems for Electric Railways: Design and Test of a Full SiC Multilevel Chopper. *IEEE Trans. Ind. Appl.* **2017**, *53*, 5820–5830. [[CrossRef](#)]
6. Meynard, T.A.; Foch, H. Multi-level conversion: High voltage choppers and voltage-source inverters. In Proceedings of the PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference, Nottingham, UK, 7–9 June 1992; Volume 1, pp. 397–403. [[CrossRef](#)]
7. Meynard, T.A.; Fadel, M.; Aouda, N. Modeling of multilevel converters. *IEEE Trans. Ind. Electron.* **1997**, *44*, 356–364. [[CrossRef](#)]
8. Negash, M.F.; Manthathi, U.B. Development of 7-level cascaded H-bridge inverter topology for PV applications. In Proceedings of the International Conference on Electrical, Electronics and Optimization Techniques, ICEEOT 2016, Chennai, Tamil Nadu, India, 3–5 March 2016; pp. 1847–1852. [[CrossRef](#)]
9. Vivert, M.; Diez, R.; Cousineau, M.; Bernal Cobaleda, D.; Patino, D.; Ladoux, P. Real-Time Adaptive Selective Harmonic Elimination for Cascaded Full-Bridge Multilevel Inverter. *Energies* **2022**, *15*, 2995. [[CrossRef](#)]
10. Luo, F.L.; Ye, H. Multilevel DC/AC Inverters. In *Advanced DC/AC Inverters: Applications in Renewable Energy*; CRC Press: Boca Raton, FL, USA, 2013; Chapter 8; pp. 137–154.
11. Luo, F.L.; Ye, H. Trinary Hybrid Multilevel Inverters. In *Advanced DC/AC Inverters: Applications in Renewable Energy*; CRC Press: Boca Raton, FL, USA, 2013; Chapter 9; pp. 155–205.
12. Vivert, M.; Patino, D.; Diez, R. Modulation Strategy and Controller for Grid-Tied Trinary Hybrid Multilevel Inverter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *99*, 539–548. [[CrossRef](#)]
13. Liu Yu, F.L. Trinary hybrid 81-level multilevel inverter for motor drive with zero common-mode voltage. *IEEE Trans. Ind. Electron.* **2008**, *55*, 1014–1021. [[CrossRef](#)]

14. Cousineau, M.; Cougo, B. Interleaved converter with massive parallelization of high frequency GaN switching-cells using decentralized modular analog controller. In Proceedings of the 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, Canada, 20–24 September 2015; pp. 4343–4350. [\[CrossRef\]](#)
15. Le Bolloch, M.; Cousineai, M.; Meynard, T. New Masterless Modular Current-Sharing technique for DC/DC Parallel converters. In Proceedings of the 14th International Power Electronics and Motion Control Conference EPE-PEMC 2010, Ohrid, Macedonia, 6–8 September 2010; pp. T3-73–T3-80. [\[CrossRef\]](#)
16. Fabre, J.; Ladoux, P. Parallel Connection of 1200-V/100-A SiC-MOSFET Half-Bridge Modules. *IEEE Trans. Ind. Appl.* **2016**, *52*, 1669–1676. [\[CrossRef\]](#)
17. Sahoo, S.K.; Bhattacharya, T. Phase-Shifted Carrier-Based Synchronized Sinusoidal PWM Techniques for a Cascaded H-Bridge Multilevel Inverter. *IEEE Trans. Power Electron.* **2018**, *33*, 513–524. [\[CrossRef\]](#)
18. Huang, Q.; Huang, A.Q. Feedforward Proportional Carrier-Based PWM for Cascaded H-Bridge PV Inverter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 2192–2205. [\[CrossRef\]](#)
19. Wang, T.; Zhu, Y. Analysis and comparison of multicarrier PWM schemes applied in H-bridge cascaded multi-level inverters. In Proceedings of the 2010 5th IEEE Conference on Industrial Electronics and Applications, Taichung, Taiwan, 15–17 June 2010; pp. 1379–1383. [\[CrossRef\]](#)
20. Arazm, S.; Vahedi, H.; Al-Haddad, K. Phase-shift modulation technique for 5-level packed U-cell (PUC5) inverter. In Proceedings of the 2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), Doha, Qatar, 10–12 April 2018; pp. 1–6. [\[CrossRef\]](#)
21. Vivert, M.; Cousineau, M.; Ladoux, P.; Fabre, J.; Mannes-Hillesheim, M.; Diez, R.; Patino, D. Decentralized Control for Balancing the Cell Voltages of a High Conversion Ratio Flying Capacitor Multilevel Converter. *IEEE J. Emerg. Sel. Top. Ind. Electron.* **2022**, *3*, 635–646. [\[CrossRef\]](#)
22. Xu, B.; Tu, H.; Du, Y.; Yu, H.; Liang, H.; Lukic, S. A Distributed Control Architecture for Cascaded H-Bridge Converter. In Proceedings of the 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 17–21 March 2019; pp. 3032–3038. [\[CrossRef\]](#)
23. Vivert, M.; Patino, D.; Diez, R.; Cobaleda, D.B.; Cousineau, M. Decentralized Controller for a Grid Tied Cascade Multilevel Invert. In Proceedings of the IEEE 3rd Colombian Conference on Automatic Control (CCAC), Medellin, Colombia, 15–18 October 2019.
24. Achanta, P.K.; Maksimovic, D.; Ilic, M. Decentralized control of series stacked bidirectional DC-AC modules. In Proceedings of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018; pp. 1008–1013. [\[CrossRef\]](#)
25. He, J.; Li, Y.; Liang, B.; Wang, C. Inverse Power Factor Droop Control for Decentralized Power Sharing in Series-Connected-Microconverters-Based Islanding Microgrids. *IEEE Trans. Ind. Electron.* **2017**, *64*, 7444–7454. [\[CrossRef\]](#)
26. Eroğlu, F.; Kurtoğlu, M.; Eren, A.; Vural, A.M. A novel adaptive state-of-charge balancing control scheme for cascaded H-bridge multilevel converter based battery storage systems. *ISA Trans.* **2023**, *135*, 339–354. [\[CrossRef\]](#) [\[PubMed\]](#)
27. Eroğlu, F.; Kurtoğlu, M.; Eren, A.; Mete Vural, A. State-of-Charge Balancing Control in Grid-Connected Single-Phase Cascaded H-Bridge Multilevel Converter Based Battery Storage Systems. In Proceedings of the 2022 4th Global Power, Energy and Communication Conference (GPECOM), Cappadocia, Turke, 14–17 June 2022; pp. 20–25. [\[CrossRef\]](#)
28. Park, D.H.; Tahir, H.; Lee, J.D.; Kim, R.Y. Hierarchical Single-Objective Model Predictive Control With Reduced Computational Burden in Cascaded H-Bridge Converter Based on 3-Level Flying Capacitor Unit Cell. *IEEE Access* **2022**, *10*, 54730–54741. [\[CrossRef\]](#)
29. Zapata, H.M.; Perez, M.A.; Marquez Alcaide, A. Control of Cascaded Multilevel Converter for Wave Energy Applications. *Energies* **2023**, *16*, 71. [\[CrossRef\]](#)
30. Vivert, M.; Patino, D.; Diez, R. Variation of a sliding mode control applied to a trinary hybrid multilevel inverter. In Proceedings of the 2017 IEEE 3rd Colombian Conference on Automatic Control (CCAC), Cartagena, Colombia, 18–20 October 2017; pp. 1–6. [\[CrossRef\]](#)
31. Gray, R.M. *Toeplitz and Circulant Matrices: A Review*; Now Publishers: Delft, The Netherlands, 2006.
32. Cobaleda, D.B.; Miguel Vivert, R.D.G.P. Low-Voltage Cascade Multilevel Inverter with GaN Devices for Energy Storage System. In Proceedings of the 13th IEEE International Conference on Power Electronics and Drive Systems (PEDS 2019), Toulouse, France, 9–12 July 2019.

Disclaimer/Publisher’s Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.