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A Regulated 400-mV CMOS DC-DC Converter with On-the-Fly Equivalent Output Resistance Tuning

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Abstract: Energy harvesting is a technology that can be applied to IoT systems to eliminate the need for batteries. Many types of energy sources are available for energy harvesting, such as light, thermal, vibration, and electromagnetic energy. Indoors, where most IoT devices are located, artificial light, such as from LED lamps, can be used for energy harvesting in circuits with very ultra-low power consumption. Integrated switch-capacitor DC-DC converters are required for this type of system to convert the harvested energy into a constant output voltage suitable for powering an electronic circuit. The idea of this work is to use a hysteretic feedback control consisting of comparators and a logic system to adjust the switching frequency and the voltage conversion ratio (VCR) of the converter. With this, the equivalent output resistance is tuned to a value that results in a constant output voltage. A new method for modeling the equivalent output resistance based on charge flow analysis is proposed, which also considers the effects of source resistance. An integrated energy-harvesting system consisting of a switched-capacitor DC-DC converter is implemented to obtain an output voltage of 400 mV using a small photovoltaic cell for energy harvesting from indoor light. The proposed system can power an ultra-low-power device between 20 µW and 40 µW with a minimum input voltage of 230 mV. Electrical simulation results show that the implemented converter can achieve a peak efficiency of 81.24% at an input voltage of 260 mV for a 20 µW load.

Keywords: energy harvesting; equivalent resistance; photovoltaic cell; DC-DC converter; integrated circuit

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1. Introduction

Energy harvesting is an alternative way of achieving large autonomy in devices with low power consumption, with the advantage of being maintenance-free. Energy can be defined as a "force" transmitted in the form of matter or waves through a medium such as water, air, or metals [1]. Energy harvesting is about collecting ambient energy that would otherwise be lost in the form of heat and converting it into electrical energy using a transducer. For example, a photovoltaic (PV) cell converts the energy supplied by a light source into electricity. Harvested energy can be stored or immediately used by small wireless autonomous IoT devices such as those used in wearable electronics, condition monitoring, and wireless sensor networks. The size of the transducer must be compatible with the size of the IoT device, which is generally only a few centimeters. This characteristic limits the amount of energy generated and restricts the application to ultra-low-power devices, typically in the range of nanowatts to microwatts [2].

Besides light, other types of transducers are used for harvesting energy in the form of vibration, thermal gradient, or RF. The power density of an RF source is highly dependent on the distance from the transmitting device [3]. RF energy harvesting can be a reliable

option for powering a device located in a place with a high concentration of RF signals, such as a city center or commercial building. However, in remote locations where RF signals have low intensity, this may be a poor option. The same occurs with thermal and vibration energy sources. They offer good power density, but are not always available and their application is limited to certain environments [4].

Light is a commonly used ambient energy source for energy harvesting. Besides being renewable energy, light is abundant in nature and has a very high power density (in the order of 10 $\mu W/cm^2$ indoors and 100 $\mu W/cm^2$ outdoors [4]). Photovoltaic cells are common transducers that can be used to harvest energy from indoor and outdoor light. Organic solar cells, including dye-sensitized solar cells (DSSCs), have been recognized as one of the key permanent power source elements for indoor IoT devices [5].

Harvesters consisting of optical nanoantennae have been proposed as an alternative to the low efficiency of solar cells [6]. The main obstacles to the use of this type of transducer are the relatively low conversion efficiency and the low-power transfer to the load, both caused mainly by the mismatch between the impedance of the rectifier (several kilohms) and that of the antenna (hundreds of ohms). Some methods have been proposed to overcome this problem [7].

Conventional amorphous Si solar cells have also been shown to be suitable for energy harvesting, although the low efficiency of about 22% is limited by the material bandgaps of the p–n junction. In [8], a 42 × 42 mm polycrystalline photovoltaic cell was characterized in an indoor lighting environment with average office illuminance levels provided by LED lamps. At 470 lux and 700 lux, output powers of 23 μW and 42 μW, respectively, were measured, which are sufficient to feed an ultra-low-power IoT circuit [9].

Many IoT applications require devices to be self-sufficient and sustainably powered. Most devices are battery-powered due to cost, convenience, size, and the fact that they are deployed in hard-to-reach areas. Battery life must be maximized to avoid battery replacement. In some cases, the battery is completely removed from the system, and the circuit is fully powered by energy harvested from environmental sources. In this case, the circuit must operate with a power consumption compatible with the instantaneous energy harvesting, which is of the order of a few μW [10].

In batteryless systems, capacitors or supercapacitors can be used to replace batteries as the energy-storing component during the time required to operate the circuit [11]. In some applications, such as RF transceivers, a very low active-to-sleep duty cycle ratio is expected. In other words, a power-hungry active mode operates for only a small portion of a full cycle, while the remainder of the cycle is spent in a sleep mode to recover the energy consumed [12]. This type of application can benefit from energy harvesting because the long sleep period is used to recover the energy consumed during the active period.

Newly developed wireless communication protocols such as Bluetooth Low Energy (BLE) [13,14], Zigbee [13,14], Thread [15], EnOcean [16], and Trench [9] feature extremely low-power scenarios. They can achieve low energy requirements on the order of tens of microwatts for communication in a local area network. This enables the application of indoor-light energy harvesting for batteryless IoT devices, since the power consumption of these circuits is in the same magnitude as the power generated by a small PV cell.

This work focuses on the use of small PV cells to harvest light energy indoors. A typical light-based energy-harvesting system using a PV cell is shown in Figure 1. It consists of three main components: a transducer, a voltage converter, and an energy storage element. The energy-storing element can be a battery, a capacitor, or a supercapacitor. DC-DC voltage converters are important modules in the energy-harvesting system because they are responsible for producing a functional output voltage from unregulated or non-constant voltage sources, such as the voltage generated by PV cells. A voltage converter is the interface between an unregulated or poorly regulated source and specific voltage rails in an electronic system. Linear converters can be employed for this task, but they are very inefficient because of excessive power loss due to heat. In addition, they function only as buck (step-down) converters, limiting their operation only to higher input voltage levels.

In contrast, switched-mode DC-DC converters are very versatile and efficient. Switched-mode converters can be either inductive or capacitive. The inductor-based converter consists of an inductor, a capacitor, and switches, while the capacitor-based converter contains no magnetic component and consists only of capacitors and switches [17]. In integrated circuits, small areas are often desired for cost reasons, and capacitor-based converters demand less silicon area than inductor-based converters [18,19]. For this reason, this work focuses on the development of a switched-capacitor DC-DC converter.

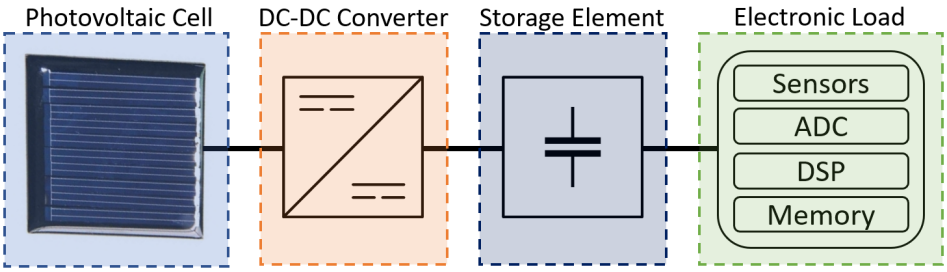


Figure 1. Diagram of a typical light-powered energy harvesting system.

Topologies of switched-capacitor converters have a static ideal voltage conversion ratio (iVCR), a specification that limits the input-output range of the conversion and the efficiency. Multiple topologies can be combined into a single converter with selectable modes to provide greater flexibility in iVCRs and a wider input-output range of upconversion and downconversion [17]. Another advantage is that the topologies can share flying capacitors to reduce silicon area.

The efficiency of a converter topology decreases when the input or output voltage values cause the VCR (voltage conversion ratio) to deviate from the iVCR. Multitopology converters can improve this by combining multiple conversion ratios.

1.1. Related Works

Various integrated DC-DC converters for different applications are described in the literature. Some DC-DC converter topologies are used in a power management unit (PMU) that converts a fluctuating voltage supplied by a battery into a desired fixed and steady output voltage. They can also be used to provide multiple voltage domains for microprocessor and SoC designs and reduce system power dissipation. For these applications, Naidu and Kittur [20] and Ghiasi et al. [21] present different topologies with switched capacitors, but they only perform downconversion. The work of Manohar and Balsara [22] follows the same buck conversion approach and presents a partially integrated buck DC-DC converter. A different approach is presented by Souvignet et al. [23] using a more versatile and fully integrated switched-capacitor converter for down and up conversions.

In the field of energy harvesting, a study conducted by Goeppert and Manoli [24] addressed the development of an inductive DC-DC boost converter that uses temperature differences to harness energy through thermoelectric generators. Chowdary et al. [25] investigated the implementation of a modular power management system that includes a DC-DC buck-boost inductor-type converter capable of simultaneously harvesting energy from three different sources: solar, vibration, and RF. In their research, Mondal and Paily [26] introduced an efficient on-chip switching power supply converter for solar energy harvesting that eliminates the need for an on-chip inductor. They proposed a tree-like charge-pump circuit to amplify the voltage obtained from the PV cell and transfer the energy to an energy buffer, such as a supercapacitor or rechargeable battery. Dini et al. [27] employed a DC-DC buck-boost converter with an off-chip inductor as a fully autonomous integrated circuit (IC) to harvest energy from various sources, including piezoelectric, photovoltaic, thermoelectric, and RF transducers. Chen et al. [28] integrated a step-up switched capacitor into a compact single-chip IC for solar energy harvesting. This IC used parallel-connected photodiodes as on-chip solar cells and was specifically designed for biomedical implant applications. Megahed and Anand [29] proposed a switched-capacitor-

based solar energy harvester with integrated maximum power point tracking (MPPT) for ultra-low-power applications. Their design achieves the same charge redistribution loss (CRL) as a cross-coupled DC-DC converter, but with only half as many capacitors as needed. Kukunuru et al. [30] suggested a method in which the PV cells of a series of solar strings are periodically connected in parallel to balance their voltages and extract the maximum available power, even under the presence of mismatch conditions.

Chen et al. [31] introduces a solution that eliminates the need for batteries, employing a DC-DC boost converter architecture with an off-chip inductor specifically created for applications involving thermoelectric energy harvesting. Devaraj et al. [32] presents a multitopology converter with 11 iVCRs, from 1/3 to 11/3. This converter is designed for multiple inputs, in this case a piezoelectric generator and a photovoltaic panel. Each source has its own converter block, which contains two multitopology converters, one for integer values of 1, 2, and 3 and one for fractional values of 1/3 and 2/3. It also has an adder topology to sum the fractional and integer converters to obtain a new iVCR.

Cheng et al. [12] presents a redistributable SC converter for batteryless IoT devices. It consists of 16 charge-pump submodules with iVCRs of 1.5 and 2 and a low-dropout regulator (LDO) to reduce excess voltage. The submodules redistribute in two stages depending on the operating mode (sleep and active).

1.2. Contribution

Although most of the related works propose a feedback loop to control the output voltage by selecting the proper VCR, none of them consider the adjustment of the equivalent output resistance as a control parameter. This technique is explored in this work, in which the equivalent impedance of the DC-DC converter is modeled considering the internal resistance of the energy source (in this case a PV cell).

Recent advances in the development of ultra-low voltage circuits with supply voltages from 400 mV down to 150 mV enabled the development of many electronic circuits such as amplifiers [33,34], voltage references [35], analog filters [11,36], data converters [37–39], integrated sensors [40], and microprocessors [41]. However, harvesting energy from the environment and providing such a controlled supply voltage remains a challenging task.

Considering autonomous applications, the goal of this work is to describe the design of a DC-DC integrated converter used for energy harvesting from indoor light to power a batteryless IoT system. The output voltage is regulated to 400 mV, independent of the input voltage generated by the PV cell. To regulate the output voltage to a fixed value, an on-the-fly tuning of the equivalent output resistance is performed. This tuning is achieved by varying the switching frequency in the switched-capacitor converter. The main contribution is the application of this technique to an ultra-low-power and ultra-low voltage system with an artificial-light-driven PV cell as the power source, where the power levels are in the range of tens of μW. The output level of 400 mV was set aiming at ULV applications such as those previously stated. Since this voltage is in the range of the threshold voltage of CMOS transistors, extra design complexity is imposed, which will be described later in the paper.

The main contributions of this work are outlined as follows:

- The modeling of the equivalent output resistance including the internal resistance of the PV cell is presented;
- The complete electrical design of an integrated circuit in a 180 nm technology containing a regulated DC-DC converter for ultra-low-power and ultra-low voltage applications is described;
- The output voltage regulation by tuning the equivalent output resistance through an on-the-fly changing of switching frequency is demonstrated for ultra-low voltage applications;
- The design of a cold-start system with a low input voltage of 231.5 mV in a start-up time of only 30.7 μs is presented;
- The application of indoor-light energy harvesting using small PV cells for batteryless ultra-low voltage circuits is demonstrated.

The remaining of this paper is organized as follows: Section 2 presents the modeling of the equivalent output resistance of a switched-capacitor converter, including the source resistance; Section 3 describes the electrical implementation of the proposed integrated DC-DC converter; Section 4 discusses the obtained results; and finally, Section 5 summarizes the main conclusions.

2. Modeling the Equivalent Output Resistance

There are some state-of-the-art techniques for modeling SC converters in the literature. Charge flow analysis is a method that provides very accurate results using the asymptotes of the Slow Switching Limit (SSL) and Fast Switching Limit (FSL) to model the equivalent output resistance ($R_{out,eq}$) [17,42]. However, this method does not take into account the effects of the source resistance R_s. In addition, the inclusion of R_s for modeling $R_{out,eq}$ in SC converters may have lower accuracy when higher values of R_s are considered.

The purpose here is to present an accurate method for modeling the equivalent output resistance of SC converters when a significant source resistance is present at the converter input. The proposed method is based on the inclusion of R_s in the FSL equation.

Figure 2 shows a generic DC-DC voltage converter with a PV cell connected at the input. The simplified equivalent circuit of the PV cell is called the 1D1R model and consists of a current source, a diode, and a series resistor (R_s) [43]. The electrical properties of the PV cell change dynamically as a function of illuminance [44]. For example, R_s can vary from 2 kΩ to 2.8 kΩ when the illuminance in a commercial PV cell of 20.2 cm^2 changes from 700 lux to 400 lux [8].

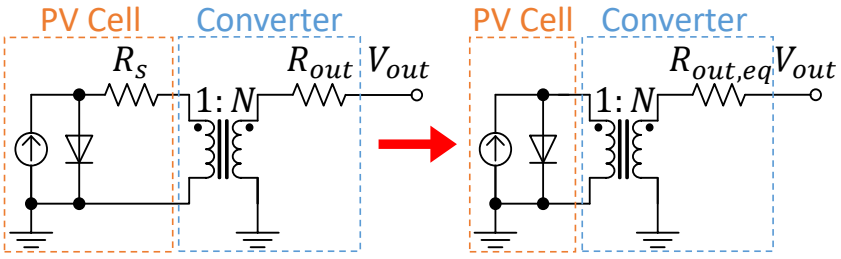


Figure 2. Transformer-based model of a DC-DC voltage converter with a PV Cell connected at its input.

The generic voltage converter can be modeled analogously as an ideal transformer with an output resistance R_{out} [42]. The transformer voltage ratio (1:N) corresponds to the ideal Voltage Conversion Rate (iVCR) of the converter [17]. The resistance $R_{out,eq}$ corresponds to an impedance of N^2R_s in series with R_{out} on the secondary side due to the impedance conversion effect of the transformer. The transformer-based (TR-based) equivalent output resistance ($R_{out,eq}$) is given by:

$$R_{out,eq} = R_{out} + N^2 R_s \tag{1}$$

The series resistance at the converter input significantly affects $R_{out,eq}$, especially at higher values of iVCR. This effect is even worse in cascaded converter stages [45].

2.1. Charge Flow Analysis

Charge flow analysis is used to determine the individual amounts of charge flowing in each switch and capacitor of the SC converter [42]. The analysis is performed for each topological state using Kirchhoff's current law (KCL) to obtain the normalized charge multipliers $a_i^{(j)}$, as shown in Equation (2), where $q_i^{(j)}$ is the charge flow in component i during state j and q_{out} is the charge delivered to the output.

$$a_i^{(j)} = \frac{q_i^{(j)}}{q_{out}} \tag{2}$$

Due to the principle of electric charge conservation, the sum of all individual charges in each component should be zero [17]. The charge flow analysis is divided into two modes: slow and fast switching limits. The SSL occurs when the switching frequency is slow enough that the charge in each flying capacitor fully equalizes at each state. For this reason, finite resistances of switches and capacitors are ignored because they are not large enough to prevent capacitors from being fully charged [42]. In FSL, the on-state resistances of switches are large enough that flying capacitors cannot reach equilibrium during a switching period [17,42].

As an example, consider the circuit of a voltage doubler shown in Figure 3. In the topological state ϕ_1, the charge q_{in} flows from the voltage source to the flying capacitor C_1. In the topological state ϕ_2, C_1 is connected in series with the input voltage, and the charge $q_{c,1}$ flows from C_1 to the buffer capacitor C_{out}.

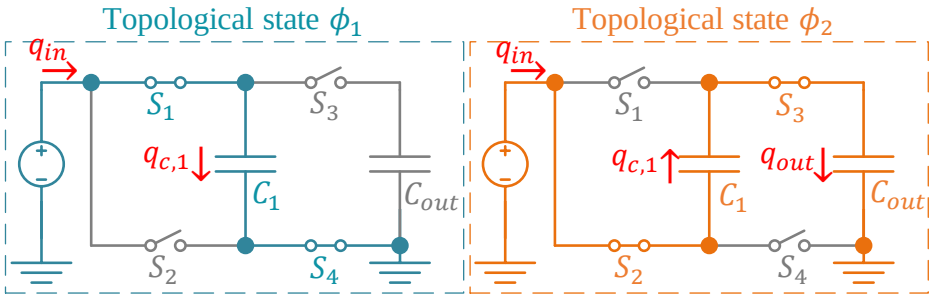


Figure 3. Charge flow analysis in the doubler topology.

In SSL mode, the resistances of all components are ignored when extracting the vectors of the capacitor charge multipliers. The vectors are given by Equation (3), where $a_{out}^{(j)}$, $a_{c,1}^{(j)}$ and $a_{in}^{(j)}$ are the charge multipliers in state j for the output, C_1 and the input, respectively, resulting in Equation (4). The SSL resistance is given by Equation (5), where n is the number of flying capacitors, f_{sw} is the switching frequency, C_i is the capacitor i, and $a_{c,i}$ is the charge flow in capacitor i [17].

$$a_c^{(j)} = \left[a_{out}^{(j)},\ a_{c,1}^{(j)},\ a_{in}^{(j)}\right] \tag{3}$$

$$a_c^{(1)} = [0,\ 1,\ 1], \qquad a_c^{(2)} = [1,\ -1,\ 1] \tag{4}$$

$$R_{SSL} = \sum_{i=1}^{n} \frac{(a_{c,i})^2}{C_i \cdot f_{sw}} = \frac{1}{C_1 f_{sw}} \tag{5}$$

In FSL mode, the vectors of the switch charge multipliers are determined by the charge flowing through the switches. The vectors are given by Equation (6), where $a_{r,i}^{(j)}$ is the charge flow during state j for switch i, resulting in Equation (7). The FSL resistance is given by Equation (8), where n is the number of switches, D_i is the duty cycle in switch i, $a_{r,i}$ is the charge flow multiplier in switch i, and R_i is the on-state resistance in switch i. We assumed that the switches in Equation (8) have equal resistances and duty cycles, therefore R_{on} is the on-state resistance for a single switch.

$$a_r^{(j)} = \left[a_{r,1}^{(j)},\ a_{r,2}^{(j)},\ a_{r,3}^{(j)},\ a_{r,4}^{(j)}\right] \tag{6}$$

$$a_r^{(1)} = [1,\ 0,\ 0,\ 1], \qquad a_r^{(2)} = [0,\ 1,\ 1,\ 0] \tag{7}$$

$$R_{FSL} = \sum_{i=1}^{n} \frac{(a_{r,i})^2 \cdot R_i}{D_i} = \frac{4R_{on}}{D} \tag{8}$$

An exact value for $R_{out,eq}$, which applies to a wide range of switching frequencies, may be difficult to obtain for certain topologies [42,46]. An approximate value for the output equivalent resistance of an SC converter is given by Equation (9) [42].

$$R_{out} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} = \sqrt{\frac{1}{C_1^2 f_{sw}^2} + \frac{16R_{on}^2}{D^2}} \tag{9}$$

2.2. Output Equivalent Resistance considering Source Resistance—R_s

The effects of the input series resistance (R_s) can be calculated using Equation (1) with the values of R_{out} and N obtained with Equation (9) and the iVCR of the topology, respectively. In this section, we present a more accurate method where R_s is considered during FSL evaluation.

2.2.1. Generic Method

The proposed generic method is based on considering the source resistance R_s as an always-on switch. It is illustrated in Figure 4, where a PV cell is connected as input of a doubler SC converter.

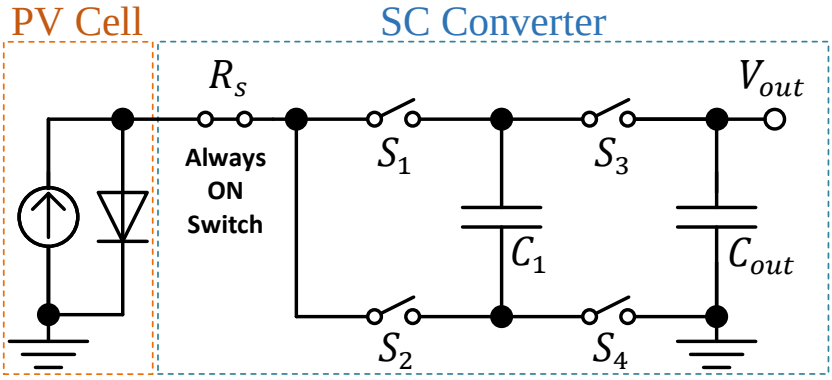


Figure 4. Voltage doubler with a photovoltaic cell as source.

The SSL is not affected by resistances, so R_{SSL} remains equal to Equation (5). The FSL is analyzed again since q_{in} now flows through R_s in both topological states. Thus, Equation (6) becomes Equation (10), where $a_{r,R_s}^{(j)}$ is the charge multiplier of R_s.

$$a_{r,eq}^{(j)} = \left[a_{r,R_s}^{(j)}, a_{r,1}^{(j)}, a_{r,2}^{(j)}, a_{r,3}^{(j)}, a_{r,4}^{(j)}\right] \tag{10}$$

FSL resistance is calculated using Equation (10) in Equation (8), which gives the expression from Equation (11). Applying this to Equation (9), one obtains the output equivalent resistance of the SC converter, as in Equation (12).

$$R_{FSL} = \left(\frac{2R_s + 4R_{on}}{D}\right) \tag{11}$$

$$R_{out,eq} \approx \sqrt{\left(\frac{1}{C_1 f_{sw}}\right)^2 + \left(\frac{2R_s + 4R_{on}}{D}\right)^2} \tag{12}$$

2.2.2. Complementary Method for Symmetric SC Converters

Symmetric SC converters have the advantage of lower output resistance [46–48]. They consist of n converters connected in parallel, each one identical in topology and component values, but operating in opposite topological states.

The proposed generic method can be applied to symmetric SC converters, but the analysis is complex due to the large number of elements. Therefore, a complementary method for symmetric topologies is presented.

An example of a symmetrical converter is the cross-coupled doubler in Figure 5. It has two doubler topologies connected in parallel, i.e., $n = 2$. The source resistor R_s is shared by n single blocks and is considered to be a parallel resistor. The series resistance $R_{s,single}$ of each individual block is given as:

$$R_{s,single} = n \cdot R_s \tag{13}$$

The generic method is applied to the single block to obtain $R_{out,single}$. To obtain the output resistance of the entire topology, $R_{out,single}$ must be divided by n single blocks, as shown below:

$$R_{out,eq} = \frac{R_{out,single}}{n} \tag{14}$$

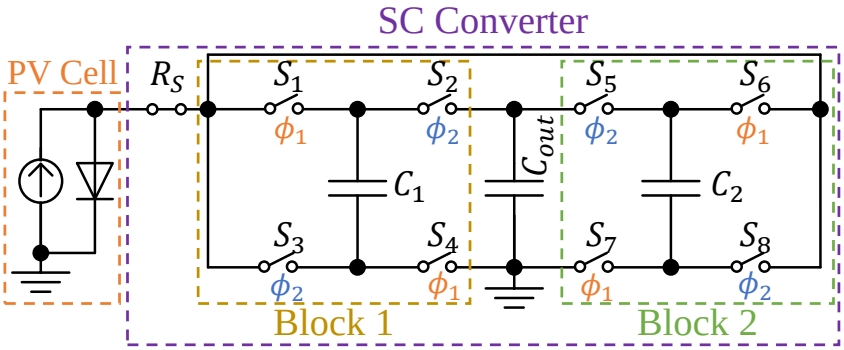


Figure 5. Cross-coupled voltage doubler.

2.3. Results

The methods proposed in Section 2.2 are compared with the transformer-based (TR-based) model in Equation (1). We use SPICE electrical simulation as a golden model to evaluate the quality of the analytical methods.

The topology used in the simulations is a doubler SC converter with a 200-pF flying capacitor. The analysis is performed for ideal switches with on-resistance of 100 Ω, and R_s equal to 200 Ω, 2 kΩ, and 20 kΩ. Figure 6 shows the evaluation results of $R_{out,eq}$, considering a variation of the switching frequency from 1 kHz to 100 MHz.

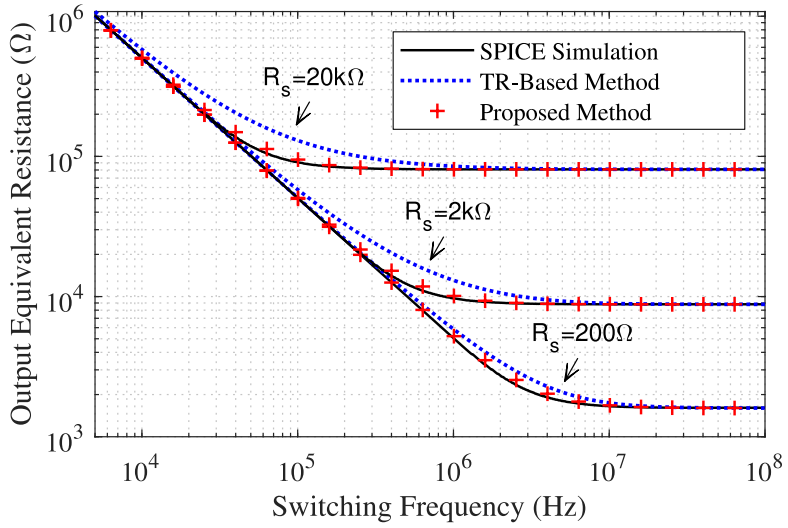


Figure 6. Output equivalent resistance as a function of switching frequency f_{sw} for various values of R_s, using ideal switches with R_{on} equal to 100 Ω. The TR-based method is calculated using Equation (1) and the proposed method by Equation (12).

It is important to have good accuracy in the corners, because the maximum efficiency of an SC converter is in the range where SSL and FSL resistances tend to be the same [44]. The optimal frequency for the doubler topology for a duty cycle of 50% is given as follows:

$$f_{sw,optimal} = \frac{1}{C_1 \cdot R_{FSL}} = \frac{1}{C_1 \cdot (4R_s + 8R_{on})} \tag{15}$$

The proposed method presented results over the entire frequency range for the three values of series resistance R_s that were very close to the simulations. The TR-based method presented good accuracy for low and high frequencies, but has significant errors at intermediate frequencies in the corners.

To validate the method with real nonlinear components, CMOS transmission-gate switches are used in the doubler SC converter. The MOSFETs are from a 180-nm CMOS technology and have a channel length of 0.18 µm and eight fingers with a width of 2 µm and 5.4 µm for the NMOS and PMOS, respectively. The simulated on-resistance of the CMOS switch is shown in Figure 7.

The evaluation of the results of $R_{out,eq}$ as a function of switching frequency is shown in Figure 8 for CMOS switches.

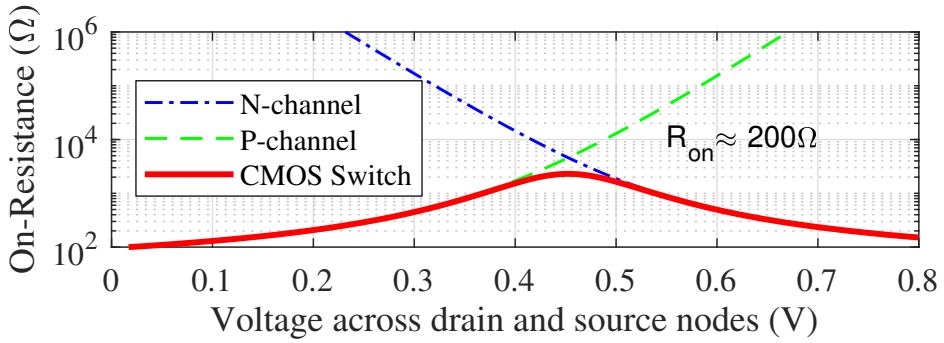


Figure 7. On-state resistance vs. voltage across a transmission-gate CMOS switch.

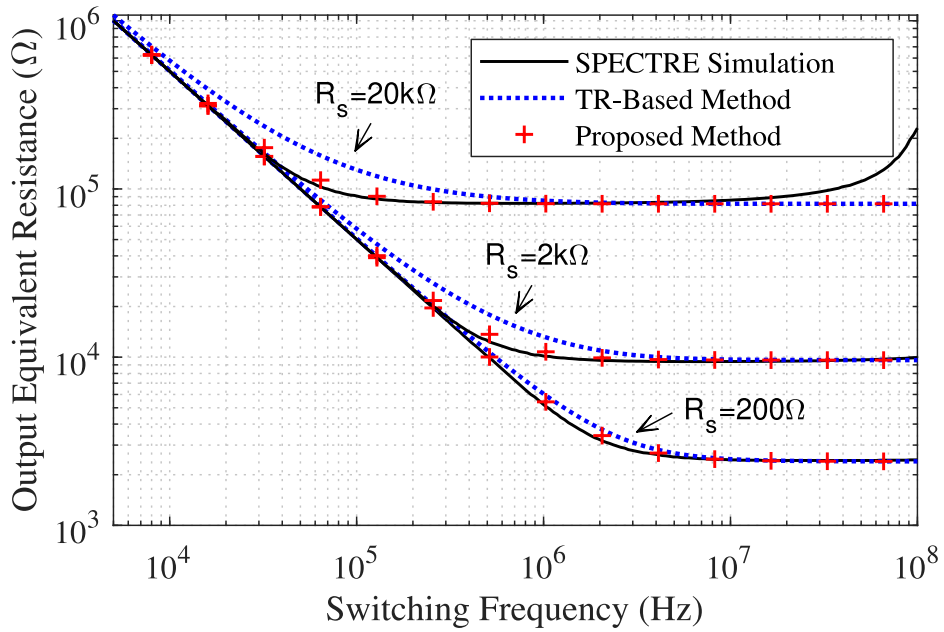


Figure 8. Output Equivalent Resistance as function of switching frequency f_{sw} for different values of R_s, using CMOS switches. The TR-based method is calculated through Equation (1) and the proposed method through Equation (12).

Similar to the previous evaluation, the proposed method for the three values of series resistance R_s for CMOS switches over the entire frequency range showed results that were very close to the simulations. The TR-based method also provided good accuracy for low and high frequencies, but has significant errors at intermediate frequencies in the corners.

Table 1 summarizes the results for the doubler converter from Figure 4 and the cross-coupled (CC) doubler converter from Figure 5. In addition, a 1/2 divider topology presented in [17] is used to validate the method at iVCR < 1. The three topologies are compared at the optimal frequency where the FSL and SSL frequencies are equal. This is the range that has the highest errors.

Table 1. Equivalent output resistance $R_{out,eq}$ at the optimal frequency point estimated using the proposed method, transformer-based method (TR-based), and SPICE simulation. The errors are calculated using the SPICE simulation.

Topology	R_s (kΩ)	$R_{out,eq}$ (kΩ)			Error	
		Our Method	TR-Based	SPICE	Our Method	TR-Based
Cross Coup. Doubler	0.2	2.30	2.62	2.13	7.21%	18.67%
	2	12.48	16.86	11.56	7.37%	31.46%
	20	114.30	160.80	106.80	6.56%	33.60%
Doubler	0.2	3.47	3.73	3.20	7.80%	14.36%
	2	13.66	24.91	12.36	9.52%	50.38%
	20	115.50	240.80	104.90	9.18%	56.44%
Divider	0.2	0.72	0.59	0.95	23.87%	37.66%
	2	2.00	4.22	2.27	11.89%	46.21%
	20	15.73	41.33	16.67	11.64%	59.67%

Our method presents maximum errors of 7.37%, 9.52%, and 23.87% for the cross-coupled doubler, doubler, and divider, respectively. In contrast, the TR-based method presents maximum errors of 33.6%, 56.44%, and 59.67% for the same topologies, respectively.

Further comparisons show that the error increases for both methods as the percentage of SSL resistance increases, although our proposed method has a relatively smaller error increase. Moreover, the TR-based method does not model topologies where the source resistance is isolated from the converter in any of the topological states—for example, the divider topology where the error becomes apparent at higher source resistances.

3. Design of the DC-DC Converter

This section describes the design of an integrated DC-DC converter that uses the technique of on-the-fly equivalent output impedance matching to regulate the output voltage. The energy transducer is a 20 × 40 mm PV cell, which is operated indoors and thus generates power of the order of μW [43]. The goal is to power a batteryless IoT device with ultra-low-power consumption (ULP) and ultra-low voltage (ULV) [49]. A regulated voltage of 400 mV is provided for a load of 30 μW, as these are typical values for ULP energy harvesters. Therefore, the goal of this DC-DC voltage converter is to sustain a steady load indefinitely while supplying a minimum voltage of 400 mV.

Generally, the load for these systems consists of a large capacitor. Although it makes it easier to estimate the resistance, under these circumstances it is difficult to estimate the efficiency of the system because the capacitor has a low impedance when discharged and a high impedance when charged. The load in a batteryless system is not constant, as it alternates between a power-hungry active mode for a short period of time and a sleep mode to charge the capacitor for a longer period of time.

The proposed DC-DC switched-capacitor converter is based on the assumption that the equivalent output impedance can be modified by controlling the converter switching frequency. The circuit receives the energy generated by a PV cell as an input and converts it to a fixed voltage at the output. The output impedance of the converter is adjusted during

operation by a feedback control module to provide a fixed voltage of 400 mV at the output. This is possible by sensing the generated output voltage and feeding it back via a digital controller that adjusts the switching frequency f_{sw} in a closed-loop fashion.

The advantage of this technique is a simplified control logic since a simple digital counter can select the appropriate switching frequency. The number of available VCRs is reduced, reducing the number of switches and flying capacitors (resulting in savings in the silicon area). In addition, the regulation of the output voltage by an SC converter avoids the use of an LDO regulator at the output. Using an LDO would require the converter to produce a larger output voltage, which would require more VCRs.

Since the goal is to operate a batteryless system, the PV cell bias does not have to search for the maximum power point. When the charge storage capacity is full, the excess power delivered to the load is not used. Therefore, the regulation of the equivalent output impedance of the converter is more important than the adjustment of the PV cell output load. High efficiency is an important parameter for a DC-DC converter, but not a requirement in energy-harvesting systems where high power output is the ultimate goal.

The complete schematic diagram of the proposed DC-DC converter is shown in Figure 9. It is a dual-mode converter with feedback control composed of a primary and a secondary converter, a cold-start oscillator, a 4-bit Digitally Controlled Oscillator (DCO), and a control system consisting of a 5-bit synchronous up/down counter and two comparators. The output of the PV cell is the input terminal of the DC-DC converter V_{IN}. This signal enters the primary DC-DC converter and is regulated to 400 mV at the output node V_{OUT}. The primary converter control signal (V_{MODE}) and the SC switching frequency f_{sw} determine the voltage conversion ratio and the equivalent output impedance. These signals are generated by the feedback loop, which senses the instantaneous value of V_{OUT} and determines if it is between V_{LOW} and V_{HIGH} using two comparators (CMP1 and CMP2). The V_{UP} and V_{DOWN} signals control a 5-bit counter, whose binary output controls the DCO oscillation frequency and the primary converter VCR. For the control module and the DCO to start operating, the supply voltage V_{DD} is generated using a secondary converter, which also acts as a cold-start system. It has its own auxiliary oscillator (CS OSC) that can oscillate at low voltages. The input of the secondary oscillator is also the voltage generated by the PV cell, and its output is regulated to 630 mV to supply the active feedback modules. The following sections describe in detail the implementation of each block of the proposed DC-DC converter.

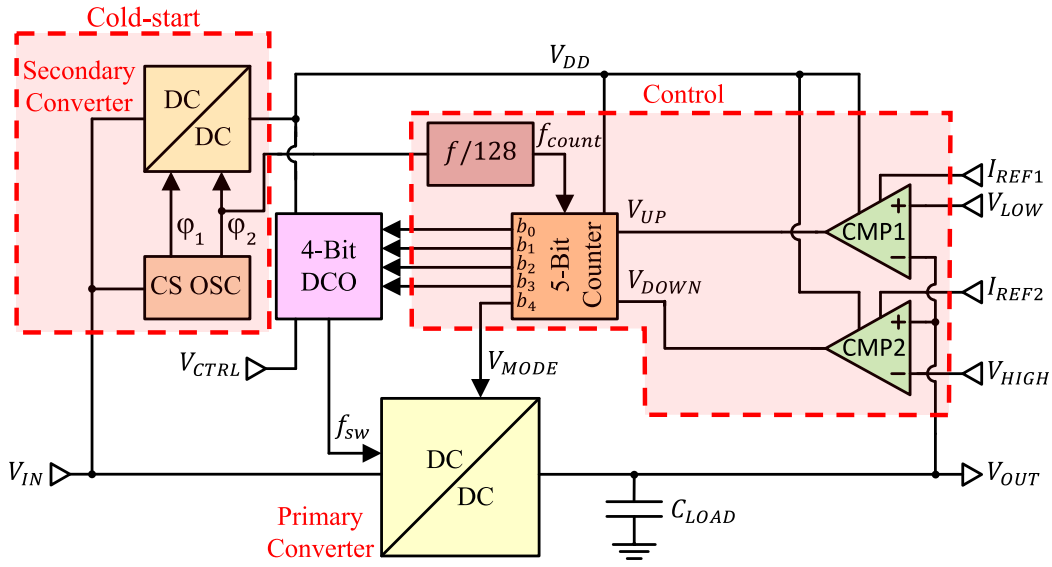


Figure 9. Complete schematic diagram of the Energy Harvester, consisting of a primary and secondary converter, a cold-start oscillator, a 4-bit Digitally Controlled Oscillator, and a control system that consists of a 5-bit synchronous up/down counter and two comparators.

3.1. Primary Converter

The primary converter is the core of the entire system. It receives as input the voltage generated by the PV cell (V_{IN}) and provides as output the regulated 400 mV output voltage (V_{OUT}). For this purpose, a control signal V_{MODE} selects the proper VCR, and the signal f_{sw} controls the operating frequency of the switches.

A multitopology converter is used to obtain different voltage conversion ratios (VCRs) [44]. The use of multiple VCRs can affect the output impedance of the converter because the output equivalent resistance of the converter increases exponentially with the number of stages [17]. To avoid large output impedance, we limited the VCRs of the primary converter to 2 and 3. To achieve these VCRs, a series-parallel doubler and tripler is used. The schematic of the implemented dual-mode (2× and 3×) SC converter is shown in Figure 10. It consists of eight CMOS switches and two flying capacitors (C_1 and C_2).

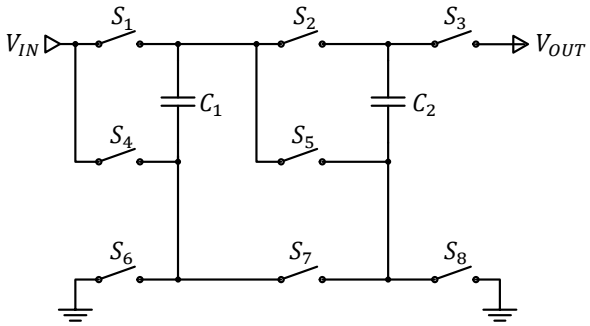


Figure 10. Schematic diagram of a doubler/tripler SC converter.

The switches are controlled by the ϕ_1 and ϕ_2 signals, which determine the topological state of the converter and its mode of operation. These signals are generated from f_{sw} by a non-overlapping clock generator to avoid simultaneous conduction at the clock transitions and, at the same time, to reduce the dead time of the switch transistors. In doubler mode, in the ϕ_1 topological state, switches S_1, S_2, S_6, and S_8 are closed, and the remaining switches are open. Therefore, the flying capacitors C_1 and C_2 are connected in parallel with the voltage source V_{IN}. In the topological state ϕ_2, the switches S_2, S_3, S_4, and S_7 are closed, and the other switches remain open. Therefore, the flying capacitors C_1 and C_2 are connected in parallel and then connected in series with the voltage source V_{IN}. The output voltage V_{OUT} is the sum of the input voltage V_{IN} and the previously charged capacitors. The charge flow in both topological states for the doubler mode is shown in Figure 11.

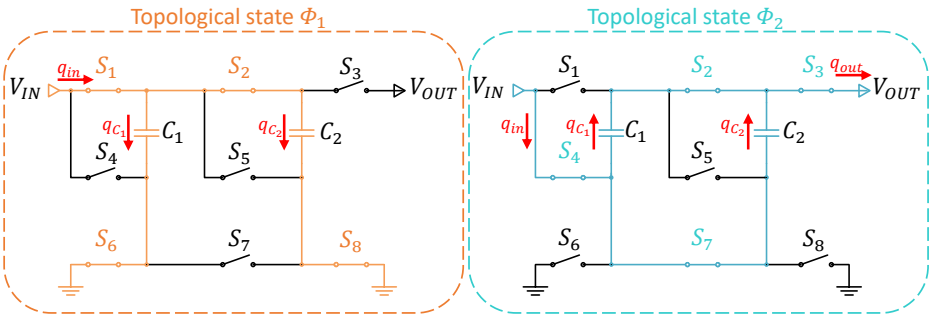


Figure 11. Charge flow of topological states ϕ_1 and ϕ_2 for the SC converter in doubler mode.

The charge multipliers for the doubler mode can be extracted by applying the charge flow analysis to the SC converter and then applied to the SSL and FSL equations to obtain the output equivalent resistance, as shown below:

$$R_{out,2x} = \sqrt{\left(\frac{0.5}{f_{sw} \cdot C_{fly}}\right)^2 + (4R_s + 8.5R_{on})^2} \quad (16)$$

The same analysis can be performed for the converter operating in tripler mode. In the topological state ϕ_1 the switches S_1, S_2, S_6 and S_8 are closed. Therefore, the flying capacitors C_1 and C_2 are connected in parallel with the voltage source V_{IN}. In the topological state ϕ_2, the switches S_3, S_4 and S_5 are closed, and the flying capacitors C_1 and C_2 are connected in series with the voltage source V_{IN}. Thus, the output voltage is the sum of the voltages between the input V_{IN} and the capacitors. The charge flow in both topological states for the tripler mode is shown in Figure 12.

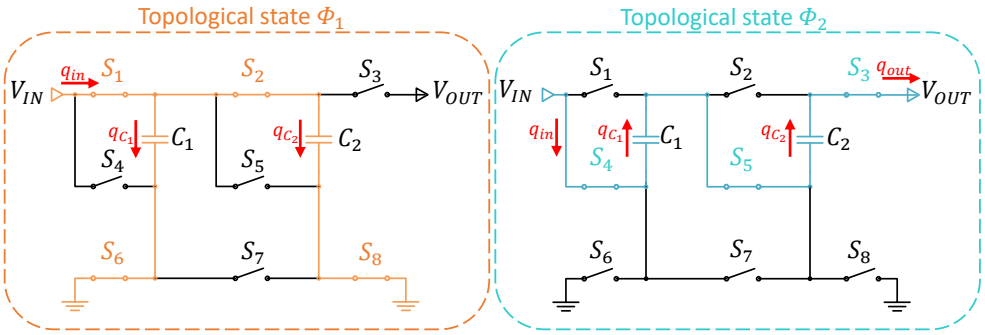


Figure 12. Charge flow of topological states ϕ_1 and ϕ_2 for the SC converter in tripler mode.

Similarly, the charge multipliers for the tripler mode can be extracted by charge flow analysis and applied to Equations (5) and (8) to obtain the Output Equivalent Resistance:

$$R_{out,3x} = \sqrt{\left(\frac{2}{f_{sw} \cdot C_{fly}}\right)^2 + (8R_s + 14R_{on})^2} \tag{17}$$

The switches were implemented as CMOS transmission gates using low-VT transistors with W/L ratios of 5/0.25 and 17.5/0.3 for NMOS and PMOS transistors, respectively, also using 10 fingers each. Figure 13 shows the on-state resistance (R_{on}) according to the voltage of the CMOS switches used in the primary converter implementation. To evaluate the effect of process variability, the average R_{on} of the CMOS switches was evaluated using 5000-run Monte Carlo analysis, considering process and mismatch parameters. Figure 14 shows the frequency histogram of R_{on} in which the obtained average resistance is 76.8 Ω with a standard deviation of 8.2 Ω.

Considering flying capacitors of 1 nF and CMOS switches with an average resistance of 76.8 Ω and applying this value into Equations (16) and (17), the optimal frequencies can be calculated as 561 kHz and 1.3 MHz for the doubler and tripler topologies, respectively. The graph of the output equivalent resistance as a function of the switching frequency for both modes of the converter is shown in Figure 15.

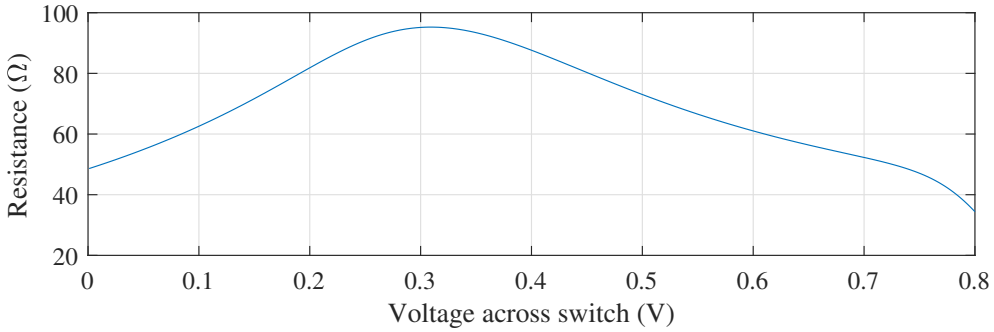


Figure 13. On-state resistance of the CMOS switch for the SC converter.

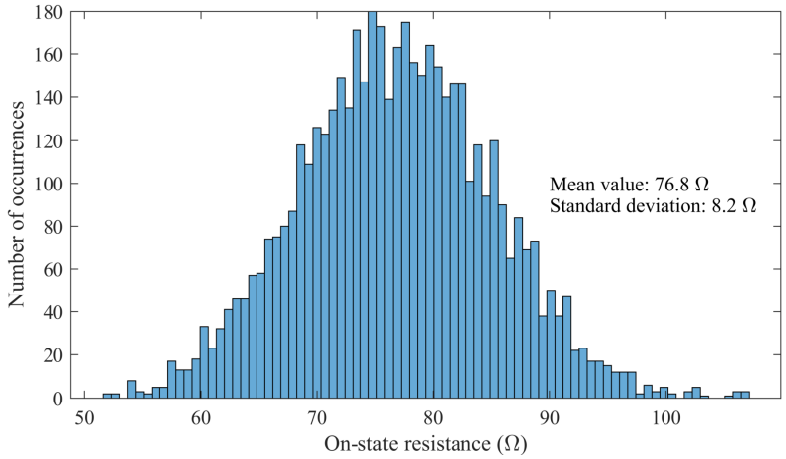


Figure 14. 5000-run Monte Carlo analysis of the on-state resistance of the CMOS switch considering mismatch and process effects.

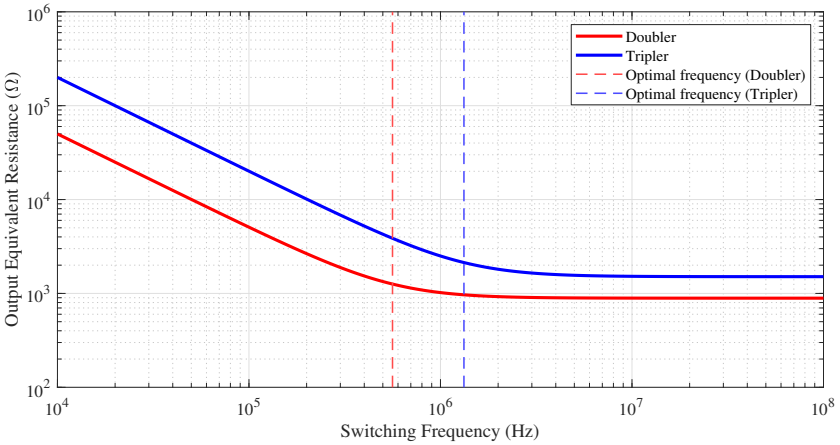


Figure 15. Output equivalent resistance and optimal frequencies for doubler and tripler operating modes as a function of switching frequency.

Table 2 shows the combinations of topological states used to select between the doubler and tripler topologies. Three 2-to-1 multiplexers are used to select the control signals for switches S_2, S_5, and S_7. A single-bit signal V_{MODE} controls the multiplexers and provides the selection of VCR 2 (V_{MODE} = 0) or VCR 3 (V_{MODE} = 1). Figure 16 shows this implementation in detail. The control signals for switches S_2, S_5, and S_7 are different depending on the selected VCR. The remaining switches behave the same regardless of whether the converter is operating in doubler or tripler mode, so they are not affected by V_{MODE}. The implementation of the multiplexers using transmission gates is detailed in the same figure.

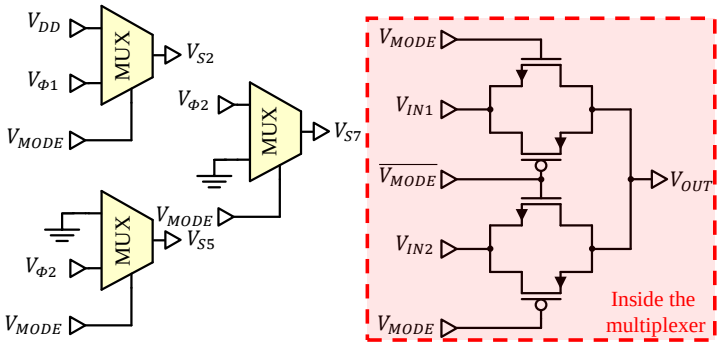


Figure 16. Doubler/tripler mode selector with three 2-to-1 multiplexers.

The sizes and types of the components belonging to the primary converter are summarized in Table 3.

Table 2. Combination of topological states for the SC converter.

Switch	Doubler	Tripler
S_1	ϕ_1	ϕ_1
S_2	ON	ϕ_1
S_3	ϕ_2	ϕ_2
S_4	ϕ_2	ϕ_2
S_5	OFF	ϕ_2
S_6	ϕ_1	ϕ_1
S_7	ϕ_2	OFF
S_8	ϕ_1	ϕ_1

Table 3. Sizing of components in the primary converter (Figures 10 and 16).

Specification	Sizing	Type	Fingers
S_1 to S_8 (W_N/L_N)	5 µm/0.3 µm	Low-VT	10
S_1 to S_8 (W_P/L_P)	17.5 µm/0.25 µm	Low-VT	10
Mux (W_N/L_N)	1 µm/0.18 µm	Nominal-VT	1
Mux (W_P/L_P)	2 µm/0.18 µm	Nominal-VT	1
C_{fly}(C_1 and C_2)	1 nF	External	-
C_{LOAD}	50 nF	External	-

3.2. Digitally Controlled Oscillator

The strategy used in this work is to control the switching frequency of the primary converter using a Digitally Controlled Oscillator (DCO). The implementation of this block considers the maximum and minimum switching frequency signal that must be generated. The strategy used in this work is to control the generated frequency by adjusting the capacitive load of a ring oscillator through a configurable capacitor bank. Shunt capacitors are switched on and off to change the capacitive load in each oscillator stage, resulting in a change in propagation delay and consequently oscillation frequency [50].

According to the output equivalent resistance of a typical PV cell shown in Figure 8, we arbitrarily set the oscillation frequency range from 300 kHz to 5 MHz, which covers the optimal switching frequency for source resistances from 200 Ω to 2 kΩ.

The proposed digitally controlled ring oscillator is shown in Figure 17 and the complete design is described in [51]. A minimum supply voltage V_{DD} of 630 mV is required for the DCO to achieve an oscillation frequency around 5 MHz [51].

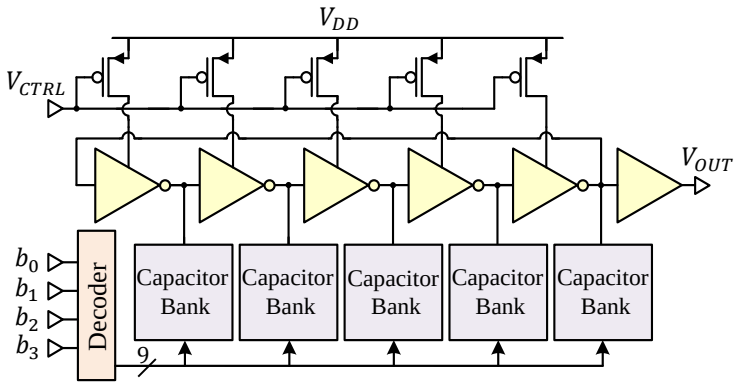


Figure 17. Schematics of the ring-oscillator DCO, showing the CMOS inverter stages, capacitor banks, current-starving transistors and the signal decoder. Reproduced with permission from [51], IEEE, 2022.

To reduce the power consumption of the circuit, a current-starving PMOS transistor is used. This transistor also allows coarse adjustment of the oscillation frequency, which is useful to avoid larger capacitances, although a reference voltage of about 90 mV is required to bias the transistor and lower the frequency to 5 MHz. A transistor with a channel width of 1.5 µm and a channel length of 0.18 µm is used, which allows low-power consumption while providing coarse adjustment of the maximum and minimum oscillation frequencies.

A monotonic 0.3–5 MHz digitally controlled ring oscillator controlled by a four-bit digital word was implemented. Monte Carlo analysis for the highest frequency shows that 18.2% of the frequencies are below 4 MHz, so calibration by an external signal V_{CTRL} is required to compensate for operating temperature, process variations, and mismatch effects. The maximum output power is 4.9 µW, considering V_{CTRL} of 20 mV to achieve 5 MHz. Figure 18 shows the DCO oscillation frequency with respect to digital control for the implemented block at a schematic level and post-layout with $V_{CTRL} = 90$ mV and $V_{CTRL} = 20$ mV. A good linearity of the generated frequency between the minimum and maximum limits can be observed.

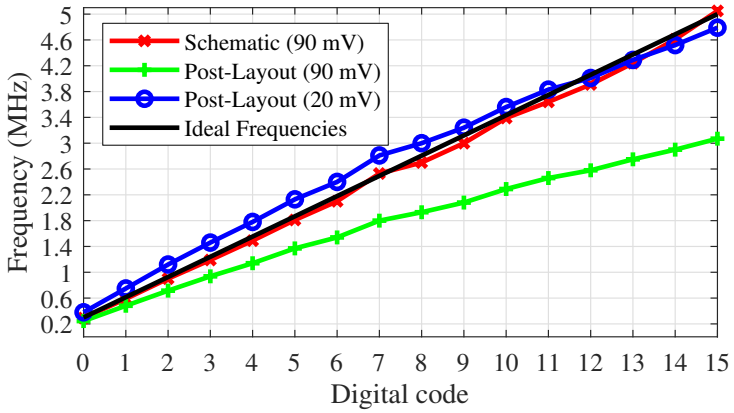


Figure 18. Comparison of frequency in function of digital code for schematic and post-layout simulations of the designed DCO. Reproduced with permission from [51], IEEE, 2022.

3.3. Cold-Start System

A cold-start system is needed to self-start the DC-DC SC converter using indoor light energy and small PV cells. It is responsible for providing power to the control module (comparators and 5-bit counter) and to the DCO even in low light conditions. Since the primary converter depends on the control signals and switching frequency for its operation, the cold-start system must be independent of it. It receives as input the voltage generated by the PV cell and boosts it to 650 mV.

The cold-start system was specified to provide a power of 10 µW, with 4.9 µW for the DCO (which operates at 5 MHz) and 2.0 µW for the control module. The remaining power is used as a safety margin that accounts for switching and parasitic losses during the operation of the main converter.

To ensure the continuous provision of the appropriate supply voltage to the entire control system, the cold-start circuit needs to remain operational even after the converter system has achieved steady-state operation.

Figure 19 illustrates the complete schematic-level implementation of the proposed cold-start system. The key component is the Dickson charge pump, responsible for amplifying the voltage supplied by the PV cell ($V_{IN,PV}$) four-fold and generating the cold-start output voltage, denoted as $V_{DD,OUT}$. This output voltage serves as the power source for the other blocks within the DC-DC converter. It is crucial for $V_{DD,OUT}$ to have a minimum value of 650 mV, as this voltage threshold is necessary to activate the DCO (Digitally Controlled Oscillator) responsible for generating the clock signal for the primary converter. Additionally, this voltage level is employed to control the switches in the primary converter. The Dickson charge pump, depicted in Figure 19c, consists of three capacitors and ten

switches, controlled by the signals ϕ_1 and ϕ_2. The generation of these control signals involves a sequence of components, including a ring oscillator (Figure 19a), a clock-booster (Figure 19d), a voltage booster (Figure 19e), a non-overlapping clock circuit (Figure 19f), and two bootstrapped CMOS inverters (Figure 19b).

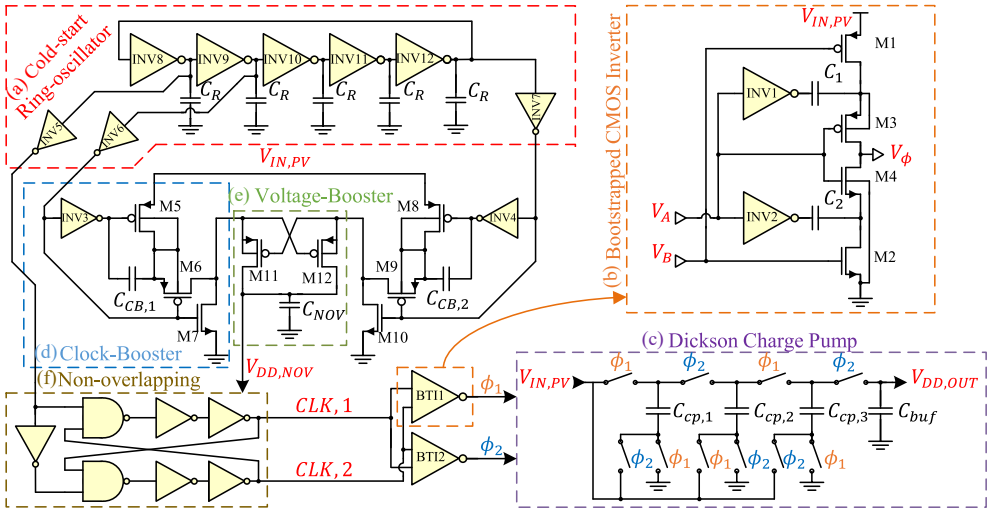


Figure 19. Comprehensive overview of the proposed cold-start circuit, encompassing various components: (**a**) cold-start ring oscillator with all inverters operating at a supply voltage of $V_{IN,PV}$; (**b**) bootstrapped CMOS inverter; (**c**) Dickson charge-pump; (**d**) clock boosters; (**e**) voltage booster; and (**f**) non-overlapping clock. Reproduced with permission from [52], IEEE, 2023.

To accommodate low supply voltages, the inverters INV8 to INV12 in the ring oscillator employ transistors with a low threshold voltage (V_T). NMOS and PMOS transistors are sized with a W/L ratio of 30 µm/0.30 µm and 20 µm/0.25 µm, respectively. The NMOS transistor is wider to compensate for a longer fall time due to the lower gate voltage compared to the threshold voltage of the low-V_T transistor.

In the circuit depicted in Figure 19a, the INV6 and INV7 inverters are used for signals with a 180° phase difference. Both inverters have identical dimensions, with a W/L ratio of 14 µm/0.3 µm for NMOS and 17.5 µm/0.25 µm for PMOS.

For the three-stage Dickson rectifier, although it generates a high output voltage, its impedance is relatively high and not suitable for handling heavy loads. The desired output voltage is approximately 650 mV. To minimize the impedance of the CMOS switches and decrease the voltage drop without increasing the size of the transistors, it is necessary to enhance the voltage swing of the clock signal.

The bootstrapped inverter (BTI) depicted in Figure 19b allows for a higher voltage swing. Originally designed for a differential ring oscillator [53], it requires signals with slightly higher amplitudes. To address this issue, two clock-boost circuits (Figure 19d) are incorporated to inject charge into C_{NOV} using a pair of cross-coupled transistors (Figure 19e), resulting in an elevated voltage at $V_{DD,NOV}$. This voltage is employed to power the non-overlapping clock circuit (Figure 19f). The PMOS transistors M11 and M12 in the Voltage Booster have a W/L ratio of 10 µm/0.25 µm.

Within the Clock-Booster circuit, the transistors in inverters INV3 and INV4 are sized with a W/L ratio of 5 µm/0.30 µm for NMOS and 20 µm/0.25 µm for PMOS. Transistors M5, M6, M8, and M9 have dimensions of 20 µm/0.25 µm, while M7 and M10 are sized at 5 µm/0.25 µm.

Inverters INV1 and INV2 are employed to charge capacitors C_1 and C_2 to the voltage $V_{IN,PV}$. When the signal V_A is high and V_B is low, INV1 and INV2 generate a low-level output signal. However, only transistor M1 is conducting, allowing V_{C1} to charge up to $V_{IN,PV}$. As a result, the source terminal of M3 is connected to $V_{IN,PV}$ and V_{C1}, causing the output signal to be $2 \cdot V_{IN,PV}$. Conversely, when the signals invert and V_A is low while V_B

is high, INV1 and INV2 produce a high-level logic signal. Transistor M2 conducts, enabling V_{C2} to charge up to $V_{IN,PV}$. Consequently, the source terminal of M4 is at $0 - V_{C2}$, resulting in the output signal being $-V_{IN,PV}$.

Simulation results show that the designed cold-start system can provide an output voltage of 625.7 mV from a minimum input voltage of 195.79 mV generated by the PV cell. The start-up time is only 30.7 µs.

The complete description of the cold-start circuit implementation can be found in [52].

3.4. Digital Control

The control module of the SC converter must be as simple as possible to consume low power and use a reduced silicon area. The implemented digital control module is responsible for sensing the output voltage and acting on the DCO to increase or decrease the switching frequency to match the impedance of the primary converter. It is also able to set the iVCR of the primary converter to 2 or 3. The closed-loop control system is based on the hysteretic effect generated by two comparators (CMP1 and CMP2) that compare the output voltage with respect to V_{LOW} and V_{HIGH} and adjust V_{UP} and V_{DOWN}, respectively.

The effective VCR of the primary converter depends on the switching frequency, which is determined by the DCO in the function of the 4-bit control signal. Figure 20 shows the VCR of the SC converter for input voltages generated by the PV cell from 230 mV to 260 mV. It can be seen that the VCR for the SSL region depends on the switching frequency in both doubler and tripler topologies. After reaching the optimum frequency where the SSL and FSL equivalent resistances are equal, the FSL region begins, and the VCR does not increase regardless of the switching frequency.

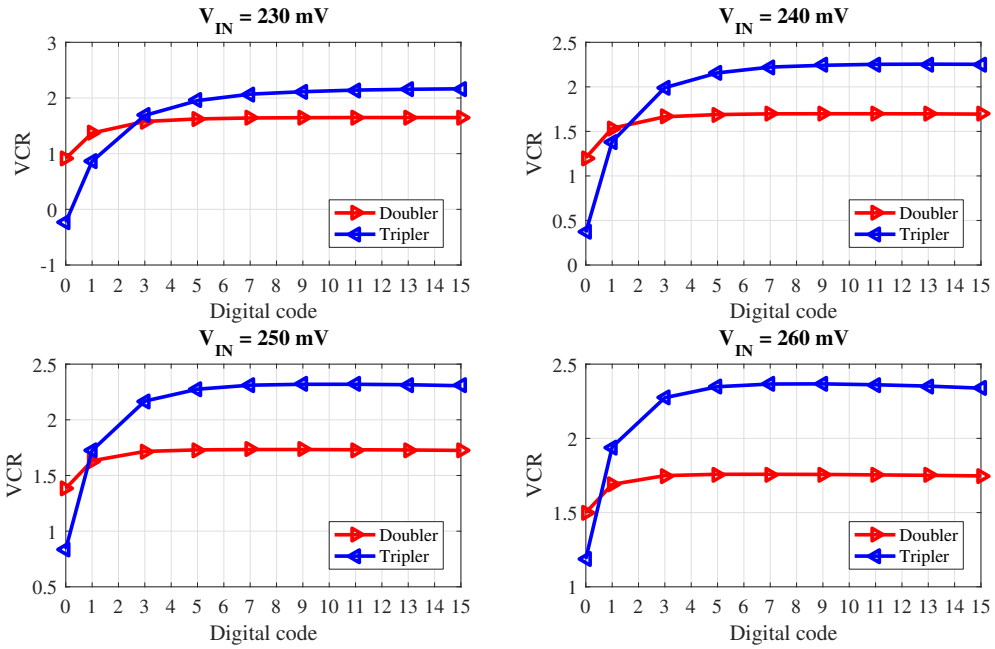


Figure 20. Steady-state Voltage Conversion Ratio (VCR) in the function of a digital code for DCO frequency.

The 4-bit control signal and the VCR mode are generated by a digital counter whose topology is shown in Figure 21. In practice, it is a 5-bit counter composed of an adder/subtractor and a register implemented with D-type flip-flops.

Using a synchronous counter, the counter increments or decrements on each positive edge of the clock signal. This is done by dividing the clock of the counter module by 128 with respect to the clock generated by the cold-start module. This makes the closed-loop control more effective, since the effect on the output voltage of the converter occurs only after a certain time.

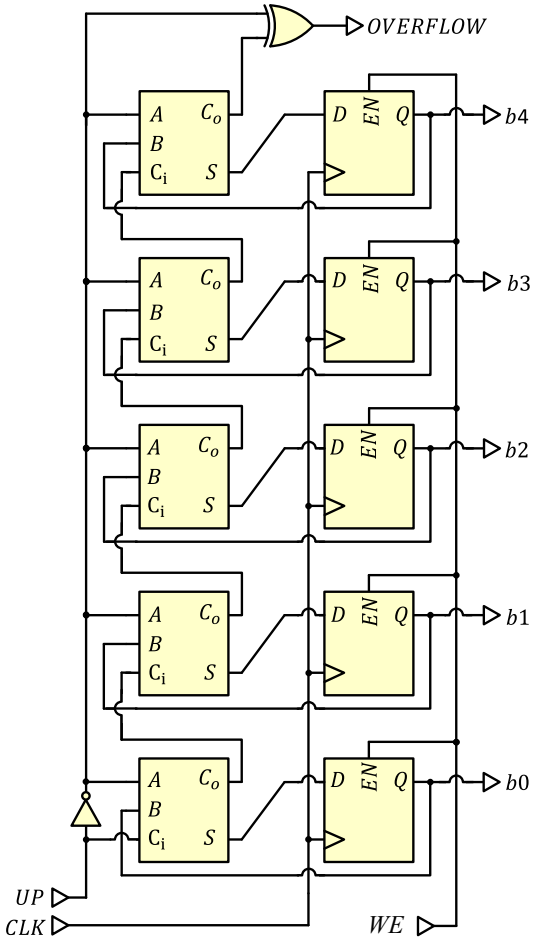


Figure 21. Synchronous 5-bit up/down counter using full-adder and registers.

The counter module should be disabled when the output voltage is stable between threshold voltages V_{LOW} and V_{HIGH} to reduce oscillations and ripple. Figure 22 shows the logic control that disables the counter when it has an overflow or when the output has stabilized.

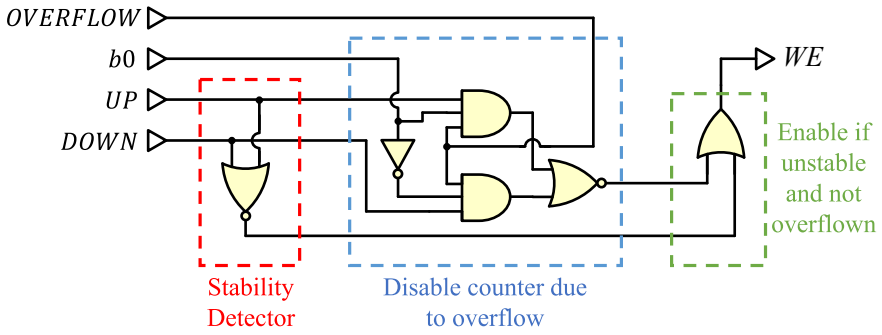


Figure 22. Write enable logic to avoid overflow and changes in the 5-bit counter when the converter output is stable.

When both signals V_{UP} and V_{HIGH} are low, the output voltage is stable, so the stability detector returns '1' for signal WE (write enable). In addition, the counter does not change when an overflow is detected. For example, the write enable of the counter is zero when the signal V_{UP} is high and has already reached the highest value ('11111'). The same is true in case the signal V_{DOWN} is '1' and the register is storing the lowest code ('00000').

4. Results

In this section, we present and discuss the results of the electrical simulations for the complete proposed energy-harvesting system shown in Figure 9.

Figure 23 shows a transient simulation of the energy-harvesting system considering a current load of 75 µA and a constant output power of roughly 30 µW. The initial state is $V_{OUT} = 0$ V and the converter is in sleep mode. In $t = 0$ s, the input voltage reaches 240 mV, which is sufficient to wake up the system. The input and output voltages are shown in Figure 23a. From the beginning of the transient simulation until 400 µs, the system is in the cold-start phase, where the supply voltage V_{DD} is generated for all subsystems—including the control module and the DCO. After this phase, the circuit starts the operation phase, and the output voltage quickly reaches a steady state of 400 mV. The DCO code generated by the control module, shown in Figure 23b, reaches a stable value of '0001' just before 1.5 ms. The iVCR selection value, also generated by the control module, is shown in Figure 23c. It can be seen that it also stabilizes in VCR = 3 at this moment. At 2.5 ms, the input voltage is increased to 250 mV, and the iVCR code begins to oscillate between doubler and tripler modes, causing the output voltage to rise and fall sharply. The control module attempts to regulate the output voltage by adjusting the DCO code, but in this case there is no combination of switching frequency and iVCR that results in an output voltage within the expected range. At 5 ms, the input is increased to 260 mV. The DCO code oscillates between zero and two for a while until it finally stabilizes at '0001'. At 7.5 ms, the input voltage is increased to 270 mV, changing the mode to doubler, but starting from the highest code, resulting in a sharp increase in the output voltage above the higher reference value of 420 mV. It finally stabilizes at '0000' in doubler mode. This means that an input voltage of 270 mV is the maximum input voltage for a current load of 75 µA.

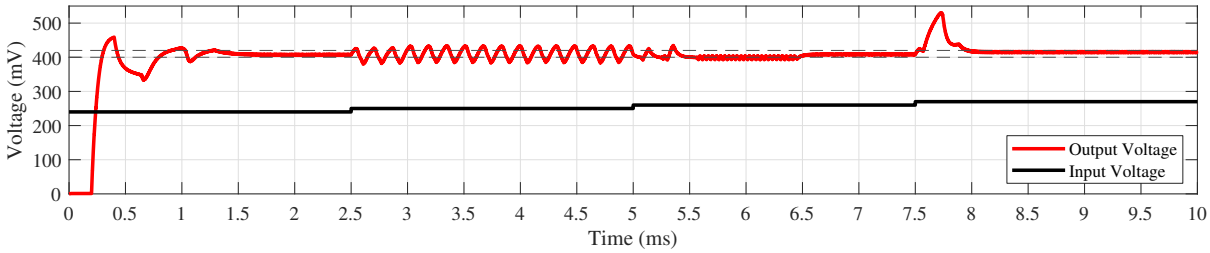
Please note that the DCO code increases sharply a few times, especially between 2.5 ms and 5 ms, due to the change in iVCR. This is due to the combination of the 5-bit control signal, where the most significant bit (MSB) b_4 controls the doubler/tripler mode selection and b_3 to b_0 are the inputs to the DCO. Therefore, when MSB b_4 changes from low to high, the subsequent bits start again from zero ('01111' to '10000').

Figure 24 shows a similar transient simulation but considering the values of current loads equal to 50 µA, 75 µA, and 100 µA, which represents output power levels of 20 µW, 30 µW and 40 µW, respectively. It is possible to see in these graphs that the system can start and regulate the output voltage for this level of load. At the input level of 230 mV it was not possible to reach the 400 mV output level with the 100 µA load, but from 240 mV of input load the target level is obtained. At the minimum load of 50 µA the system operates well at the reduced input levels, but surpassing the target level for an input voltage of 260 mV or higher.

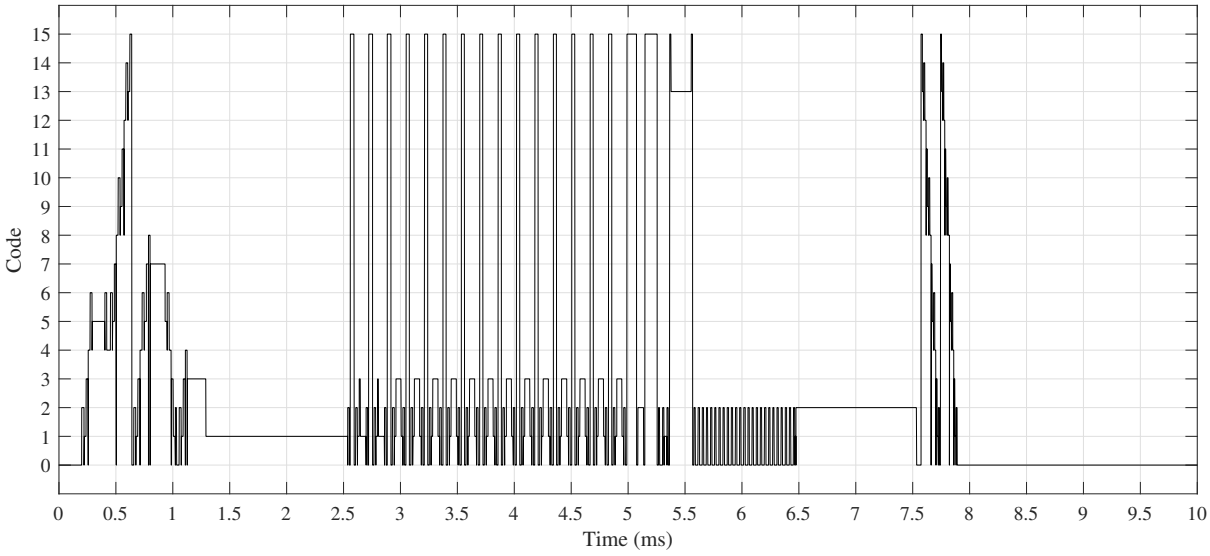
The output voltage is highly dependent on the input voltage, as shown by the VCR analysis in Figure 20, as it starts at a voltage of 230 mV and reaches a voltage of 400 mV at the output, except for the simulation for a 100 µA current load, which cannot reach the required voltage. The high voltage ripple in the output voltage V_{OUT} can affect circuits that require a stable supply voltage, such as ADCs and DACs. However, the converter can also be used in cases where a very stable voltage is not needed. Ripple can be reduced using a large external buffer capacitor in the microfarad range, although this is not practical for simulation due to simulation time, so tests are performed using a 50 nF buffer capacitor.

The average module of the instantaneous power at a steady state is used to measure the efficiency of the SC converter. Figure 25 shows a surface of steady-state efficiency of the SC converter in the function of input voltage and current load. The peak efficiency of the converter is 81.6% at an input voltage of 260 mV and a current load of 50 µA. The efficiency drops to 40% as the input voltage decreases and the current load increases.

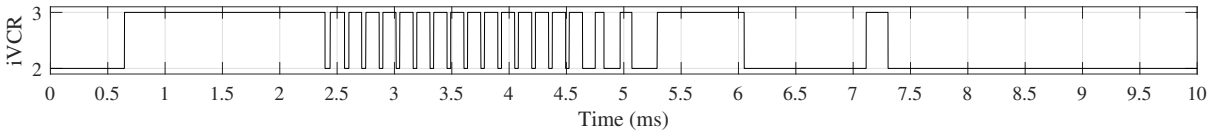
A transient simulation at a schematic level of an abrupt variation in current load is illustrated in Figure 26. The output voltage remains stable through the abrupt load changes. Similar to the tests above, the DCO digital code is at its lower limit for a low load of 50 µA, and for high loads it begins to rise and fall until stability is achieved.



(**a**) Input and output voltages



(**b**) DCO code generated by the control module



(**c**) iVCR generated by the control module

Figure 23. Transient simulation of the energy-harvesting system, considering a current load of 75 µA.

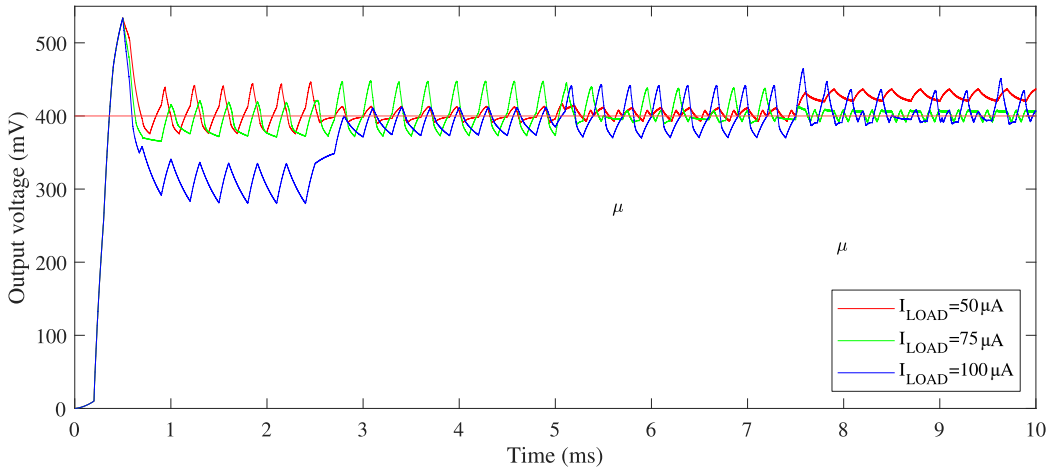


Figure 24. Output voltage of the converter for current loads of 50 µA, 75 µA, and 100 µA with input voltages of 230 mV up to 260 mV.

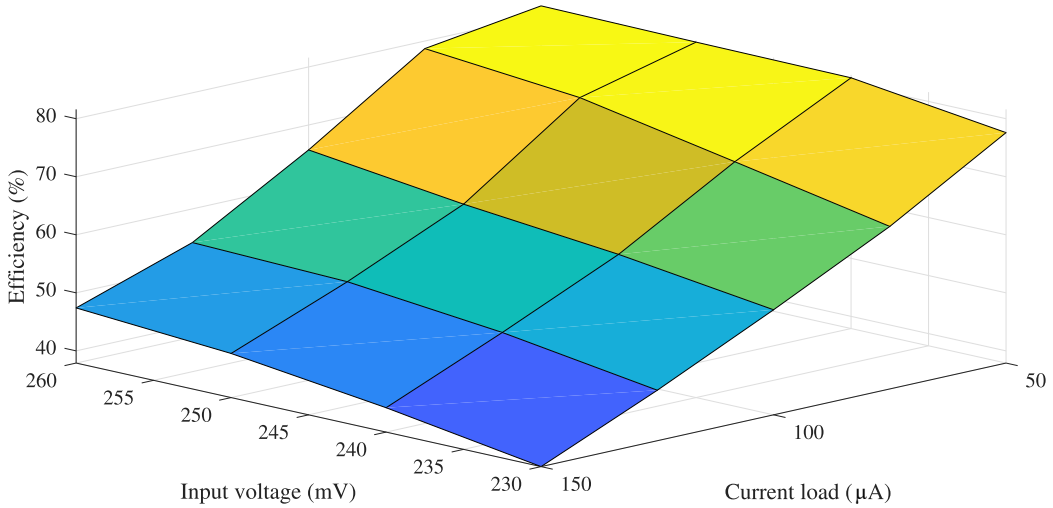


Figure 25. Efficiency of the designed DC-DC converter in the function of the input voltage and current load. Colors indicate the efficiency level, from blue (low) to yellow (high).

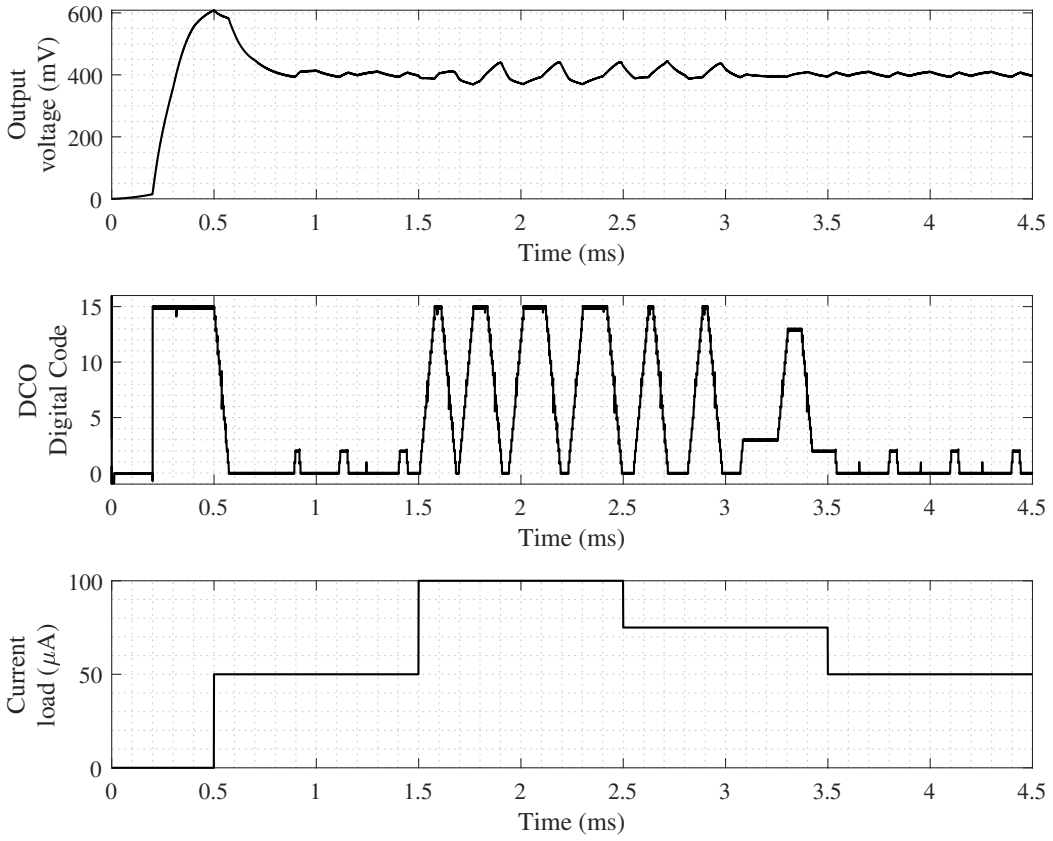


Figure 26. Transient simulation of an abrupt change in current load.

The settling time of the proposed DC-DC converter was measured according to the start-up time, since no significant delay was observed during the transient simulation with the variation of input voltage and output load. Based on Figure 24, the measured settling time is 0.69 ms, 0.63 ms, and 0.60 ms for the current load of 50 µA, 75 µA, and 100 µA, respectively. Since the proposed circuit aims to generate a stable voltage V_{DD} of 400 mV, we also estimated the line and load regulation, which are the main characteristics of a linear voltage regulator. A line regulation of 13% and load regulation of 0.48% were estimated. These values are higher compared to commercial linear regulators, but this was expected due to the lower output voltage level and input voltage range in the target application.

In addition, ultra-low voltage and ultra-low-power circuits targeting autonomous battery-less devices are expected to have lower performance compared to circuits designed to operate at standard supply voltages (1.8 V for this 180 nm CMOS process).

Figure 27 shows the distribution of power consumption on the energy-harvesting system considering an input voltage of 250 mV and a load of 30 µW. In this scenario, 73% of the energy is delivered to the load. The remaining 27% of the energy consumed by the DC-DC converter is distributed among the digital counter (less than 1%), the comparators (2%), the multiplexers (4%), the DCO (9%) and the losses in switches and in the cold start-up circuit (11%).

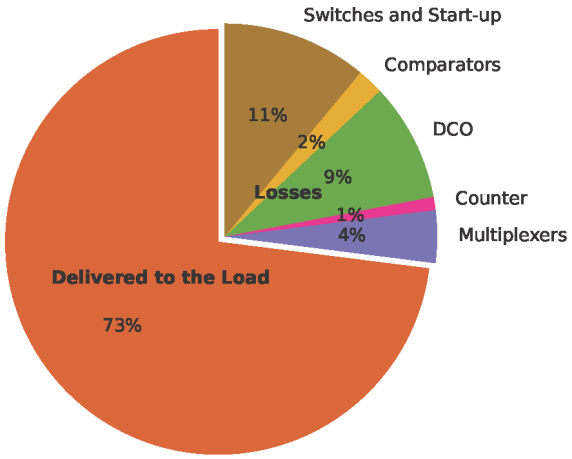


Figure 27. Pie-chart of the input power distribution in the DC-DC converter, considering a V_{IN} of 250 mV and a load of 30 µW.

Table 4 shows a comparison of the proposed energy harvester with three state-of-the-art switched-capacitor DC-DC converters. The proposed converter presents a peak efficiency of 81.6% at an input voltage of 260 mV and a 20 µW load. This is an acceptable efficiency compared to other works, but, as mentioned earlier, the fact that the output is regulated to 400 mV makes the efficiency a non-critical parameter. Additionally, three external capacitors are required—two flying capacitors and a buffer capacitor for the primary SC converter. The secondary SC converter, which generates the supply voltage for subsystems, is fully integrated with MIM capacitors. Our circuit provides an output voltage of 400 mV and a minimum output power of 20 µW with an input voltage of 231.5 mV, which is an advantage compared to other works. The maximum output power is of the same order of magnitude as [32,54], and higher than [55]. It is particularly suitable for use in solar energy harvesting with small PV cells that provide low voltage levels indoors.

Table 4. Comparison with state-of-the-art energy low-power harvesters.

Specification	This Work	Ref. [32]	Ref. [55]	Ref. [54]
Technology	180 nm	65 nm	130 nm	28 nm
Topology	SC	SC	SC	SC
Minimum input voltage	231.5 mV	550 mV	2.5 V	1.15 V
Output voltage	0.4 V	1.8–2.5 V	0.44 V	0.35–0.45 V
Output power	20–40 µW	35–70 µW	2–250 nW	0.02–100 µW
Peak efficiency	81.6%	74.6%	56%	92%
Energy source	Indoor Light	Piezo and Solar	Battery	Battery
Has cold-start?	Yes	No	No	No
External components	Capacitors	No	No	Capacitors

5. Conclusions

The proposed energy-harvesting system can power a ULP device between 20 µW and 40 µW for input voltages of 231.5 mV and 270 mV, respectively, and supplying it with a voltage of 400 mV. The idea of this work is to use a control system with comparators and a digital counter to tune the switching frequency and output voltage of a switched-capacitor converter powered by indoor-light energy harvesting. The output voltage is regulated by tuning the equivalent output resistance through the switching frequency of the converter. The advantages are the small number of VCRs in the primary converter, which minimizes the number of switches and capacitors, and the simplification of the control circuit. This results in a smaller silicon footprint. In addition, the proposed technique does not require an LDO at the output, so there is no need to boost the output voltage to a higher value. The integrated DC-DC converter has a peak efficiency of 81.24% at 260 mV and requires only three external capacitors. The disadvantage is the reduction of efficiency at low input voltages and high current loads, which drops to 40% in the case of 230 mV input voltage and 150 µA load. The obtained results show that the proposed converter is suitable for harvesting artificial light energy available in typical indoor environments.

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Abbreviations

The following abbreviations are used in this manuscript:

DC	Direct Current
DCO	Digitally Controlled Oscillator
FSL	Fast Switching Limit
IoT	Internet of Things
iVCR	Ideal Voltage Conversion Ratio
LDO	Low Dropout
LSB	Least-significant bit
MIM	Metal-Insulator-Metal
MSB	Most significant bit
Mux	Multiplexer
PV	Photovoltaic
SC	Switched-Capacitor
SSL	Slow Switching Limit
ULP	Ultra-Low-Power
ULV	Ultra-Low Voltage
VCR	Voltage Conversion Ratio

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