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Review

A Comprehensive Review of Reduced Device Count Multilevel Inverters for PV Systems

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Abstract: This article presents a comprehensive review of reduced device count multilevel inverter (RDC MLI) topologies for PV systems. Multilevel inverters are widely used in medium-voltage and high-power applications such as wireless power transform applications, flexible AC transmission (FACT), active filters, AC motor drives, high-voltage DC transmission (HVDC), and renewable energy sources due to their high modularity and high-power quality output. Multilevel inverters have the ability to diminish the harmonics content in the output voltage by applying various modulation techniques. The literature in this field showed that the high-power quality and high modularity of the output demand an undeniable need for multilevel inverter topology. Research in this field has identified various multilevel inverter topologies, each possessing their own merits and demerits. The ubiquitous availability of multilevel inverter topologies illustrates the complexity of their accurate selection. To avoid such complexity, this review shows the state of the art of various reduced device count (RDC) multilevel inverter (MLI) topologies. Details of the various RDC MLIs, along with their comparisons, are provided in this paper. This review will be an important reference tool for future work on RDC MLI for photovoltaic (PV) systems.

Keywords: multilevel inverters; reduced device count; maximum power point tracking (MPPT); photovoltaic (pv) system

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1. Introduction

Due to the latest development in fast switching solid state devices, power electronics technology is expanding in the areas of residential, commercial, industrial, aerospace, electric vehicles, motor drives, and power system utilities [1–3]. The switch mode action of semiconductor devices increases the efficiency of power electronic systems by up to 99% [1]. Day-by-day demand for modern power system networks is increasing, thus various steps, including integration of renewable energy sources, upgradation of existing generation systems, and building of new lines to enhance transmission line capacities are required to meet demand [4]. Expanding power generation and transmission systems increases problems for power system planners. Various renewable energy resources are integrated with power system networks through inverters. Square wave and quasi-square wave inverters were used for power conversion and had poor quality output due to high harmonic content. These drawbacks were overcome by the conventional multilevel inverters introduced in 1975.

A multilevel inverter is superior to a two-level inverter in terms of efficiency, performance, and better harmonic spectrum. However, the increased number of levels tends to increase the number of devices and gate drivers for switches, making the overall design complex, bulky, and uneconomical for medium-voltage applications. Therefore, reducing the number of devices without reducing the output voltage level is a key area of research

in the field of multilevel inverters. This has given rise to the concept of RDC MLIs. Several topologies have recently been proposed to reduce the number of devices in multilevel inverters. The popularity of RDC MLIs is increasing due to lower harmonics and less radio frequency interference in the output. Moreover, these converters have low power dissipation and lower voltage stress on solid-state devices [5–10]. The reduced device count multilevel inverters reduce the harmonics in the output voltage waveform by varying the number of levels, resulting in fewer switching devices and trigger circuits, diodes, capacitors, and other devices [6,11–19]. These topologies make it possible to use the device effectively and simplify the overall system design compared with available conventional designs. Several topologies have recently been proposed to reduce the number of devices in multilevel inverters. The following sections discuss recent studies that have been conducted on current trends in the era of multilevel inverters.

Siddique, Marif Daula et al. [20] suggested a new single-phase topology with a reduced number of switches and DC voltage sources with higher numbers of voltage levels. Three different algorithms were also proposed for a cascaded connection. The 71 levels were obtained at the output by implementing the selective harmonic elimination pulse width modulation (PWM) technique.

Bana, Prabhat Ranjan et al. [21] reviewed RDC MLI and recently developed topologies in renewable energy and drive applications. The study also presented comparisons between various topologies.

Kanaujia, Anoop Kumar, and Sanjiv Kumar [22] proposed an RDC MLI for open-end winding induction motor (OEWIM) drive applications. A hybrid flying capacitor (FC) configuration supported one OEWIM terminal, whereas another terminal was provided for a three-level-cascaded H-bridge inverter. A three-level FC cascaded to obtain a capacitor-fed H-bridge. A practical solution for a nine-level active-neutral-point-clamped switched capacitor MLI with an alleviated capacitor charging current is presented in [23]. Elias et al. [24] proposed a hybrid MLI based on series connection of half-bridge and full-bridge for its level generation together with a T-type inverter. The proposed MLI generated an 11-level line output voltage. However, the research consisted of more components, which made the system uneconomical.

Several review articles on multilevel inverters have been published. Gupta, K.K. et al. [6] presented quantitative and qualitative features of some reduced device count multilevel inverters in 2016. Multilevel inverters are single DC as well as multi-DC sources. Single DC source multilevel inverters reduce the cost and complexity of the circuit and are available in a compact size. A review of transformer-based single DC source multilevel inverters was conducted by J. Singh et al. [12]. A number of studies focused on the use of MLIs for applications, including wind energy, induction motors, fuel cells, and traction [25–48]. Latran, M. B., and A. Teke [44] reviewed 100 papers on grid-connected inverters. P. Kala and Arora [48] also conducted a review of hybrid multilevel inverters for grid-connected applications.

This review offers a single reference containing a considerable number of studies on multilevel inverter topologies: over 120 papers reporting on different RDC MLI topologies published up to the year 2022 have been compiled. This article reviews several MLI topologies, providing a brief discussion and comparison. This article concludes with comparisons of reduced count device MLIs based on MLI type, modulation scheme, calculated parameter, software used, and controller implementation. Tables containing summaries of the conclusions are also provided.

The research paper has been organized as follows: Section 2 gives an overview of conventional MLIs. Section 3 presents a comprehensive review of recently developed reduced device count MLIs. Section 4 gives a comparative analysis of reduced device count multilevel inverters. Section 5 presents applications of RDC MLI to the PV system, and Section 6 contains conclusions with insights on some future topics.

2. Conventional Multilevel Inverters

Multilevel inverters synthesize the AC output voltage waveform in multiple steps but with less distortion compared with conventional inverters [6,11]. This lower distortion makes MLI popular in medium-voltage and high-power applications. A conventional two-level inverter is used for low-voltage applications due to limitations of switching losses that occur due to high switching frequency and device ratings. High power is achieved by switching several solid-state devices in MLI together with several lower voltage DC levels and thus reducing the voltage stress on a solid-state switch. Moreover, these topologies require less space for installation, are low cost, and have high efficiency, a modular structure, less complexity, and fewer devices [12–17].

The MLIs generate the required high voltage without the use of transformers with low harmonics. Due to these remarkable features, MLIs are widely used in photovoltaic systems [10,18,19], wind energy conversion systems [8,25], fuel cells [26], traction [27–29], induction motors [30,31], active filters [32,33], wireless power transforms [34], HVDC [35,36], electric vehicles [37], and flexible AC transmission systems [38–40]. The MLI input is DC, which is obtained from wind conversion systems, fuel cells, photovoltaic panels, or energy storage devices. The classical multilevel inverters are illustrated in Figure 1, and their salient aspects are further reviewed in the next subsections.

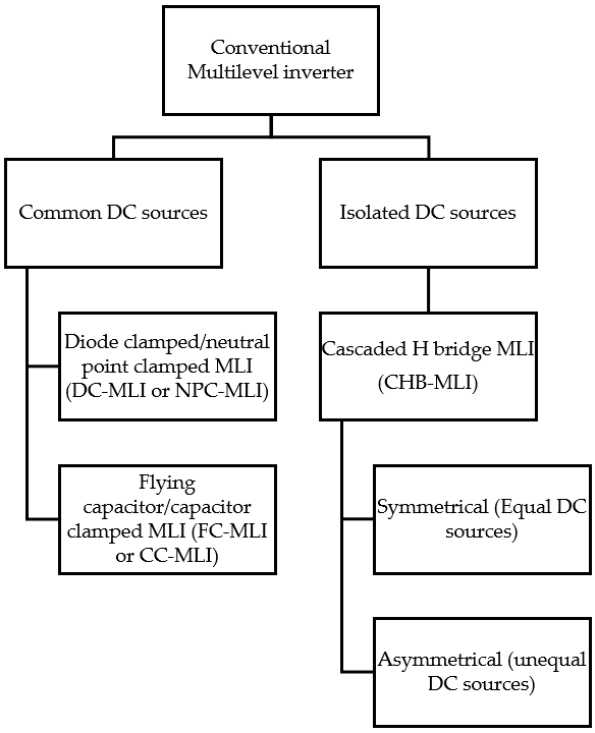

Figure 1. Conventional MLI classification.

2.1. Diode-Clamped/Neutral-Point-Clamped Multilevel Inverter (DC-MLI)

A diode-clamped multilevel inverter was proposed in 1981 by Nabae, Takashi, and Agae [41]. DC-MLI has small leakage current, high efficiency [42,43], and simple construction. It is composed of switching devices, diodes, and capacitors. A five-level DC-MLI is shown in Figure 2. In a k-level MLI, the switching devices S_d, DC link capacitors C_{DC}, and clamping diodes C_d can be expressed as in Equations (1), (2) and (3), respectively [41,44]. The voltage across each capacitor is the same and is given by Equation (4) [45]. DC-MLI requires more clamping diodes as the levels increase [46]. The line voltages have $2(k-1)$ levels.

$$S_d = 2 \times (k-1) \quad (1)$$

$$C_d = (k-1) \times (k-2) \tag{2}$$

$$C_{DC} = (k-1) \tag{3}$$

$$Voltage\ accross\ each\ capacitor = \frac{V_{dc}}{k-1} \tag{4}$$

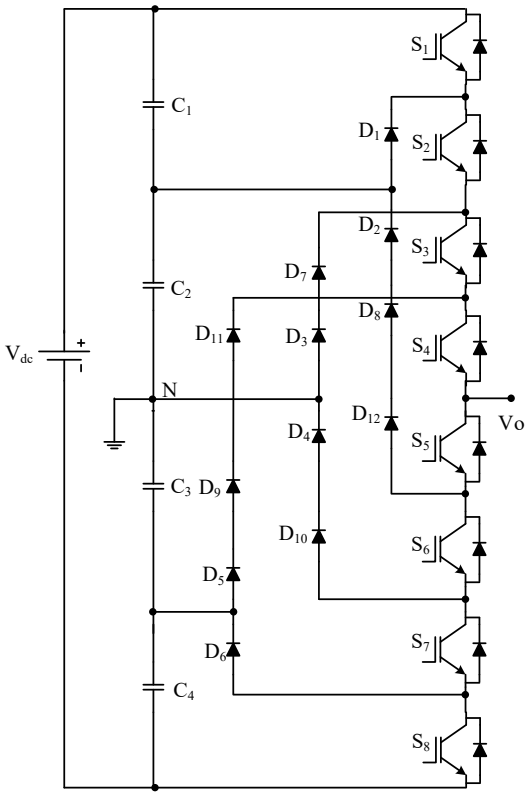

Figure 2. Five level DC MLI.

2.2. Capacitor Clamped/Flying Capacitor Multilevel Inverter

In 1992, Meynard proposed the first multilevel flying capacitor inverter (FC MLI). For a *k*-level single-phase FC MLI, the number of required switching devices, balancing capacitors C_b and DC link capacitors are computed using Equations (5)–(7). A single-phase FC MLI circuit diagram is shown in Figure 3. The line voltage has 2 $(k-1)$ levels.

$$S_d = 2 \times (k-1) \tag{5}$$

$$C_b = \frac{(k-1)(k-2)}{2} \tag{6}$$

$$C_{DC} = (k-1) \tag{7}$$

The FC MLI reduces the harmonics in the output voltage waveform, thereby avoiding the demand of filters. In addition, these converters can control active and reactive power. The FC MLI increases the cost based on an increase in the number of levels due to more capacitor requirements.

2.3. Cascaded H-Bridge Multilevel Inverter (CHB-MLI)

The CHB-MLI topology requires several isolated DC sources, whereas DC MLI and FC MLI only need a single DC source [47]. The CHB-MLI do not require balancing capacitors and clamping diodes. CHB-MLI is a hybrid combination of a series of connected single-phase two-level voltage source converters. The two-level converter, also called a H-bridge converter, includes four switching semiconductor devices and a single DC source [48].

In CHB, output levels can be increased by adding DC sources. These DC sources can be acquired from photovoltaic cells [41], biomass, fuel cells, and batteries. CHB can be referred as symmetrical when the magnitude of the DC sources is the same. Similarly, the CHB is known as asymmetric when the DC sources possess different magnitudes. Unlike DC MLI and FC MLI, CHB-MLI requires fewer devices for the same output voltage level. Moreover, these inverters possess important characteristics, such as reliability, modularity, low cost, and high efficiency [49–55]. CHB suffers from the drawback in a way that it requires separate DC sources for power conversion. The circuit diagram of single phase CHB-MLI is shown in Figure 4a. If n represents the number of cells in a single phase symmetric CHB, then output levels (k) and maximum output voltage V_o can be found using Equations (8) and (9), respectively. Similarly, output voltage levels in a single phase asymmetric CHB can be selected by a geometric progression (GP) with a binary and a trinary factor. The output voltage levels are given by Equation (10) and peak output voltage by Equation (11) for the binary operation. Similarly, the output voltage levels for the trinary operation are expressed in Equations (12) and (13), respectively. The GP with a binary factor of 2 for number of voltage levels at the output of CHB multilevel is given in Equation (10), where k is the number of levels, and n is the number of sources. For example, if two sources are connected with a CHB multilevel inverter, the number of levels that will be generated at the output becomes 7 according to Equation (10). Similarly, the GP with trinary factor of 3 for the number of levels will be 9 (when $n = 2$) according to Equation (12). The switching devices for symmetric and asymmetric CHB can be found by Equation (14). Figure 4b describes variations in the number of levels versus the number of sources in symmetrical and asymmetrical (binary, trinary) CHB-MLIs. Moreover, the number of levels are expressed in logarithm scale on y-axis in Figure 4b to clearly express the relative variation versus number of sources and type of CHB: symmetrical/asymmetrical (binary, trinary). It can be observed that the progression is arithmetic (linear) in the case of symmetrical CHB, whereas it is approximately a GP for binary asymmetric CHB and purely a GP for the case of trinary asymmetric CHB.

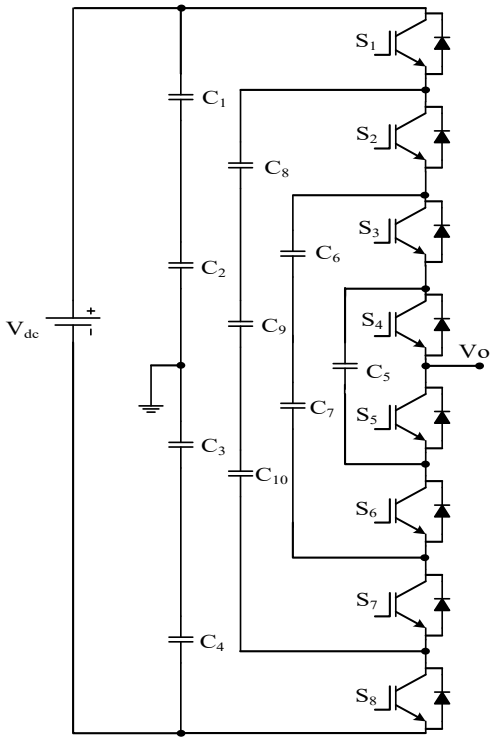

Figure 3. Five level FC MLI.

$$k = (2 \times n) + 1 \tag{8}$$

$$V_o = n \times V_{dc} \tag{9}$$

$$k = 2^{n+1} - 1 \tag{10}$$

$$V_o = (2^n - 1) \times V_{dc} \tag{11}$$

$$k = 3^n \tag{12}$$

$$V_0 = \frac{(3^n - 1)V_{dc}}{2} \tag{13}$$

$$S_d = 2 \times (k - 1) \tag{14}$$

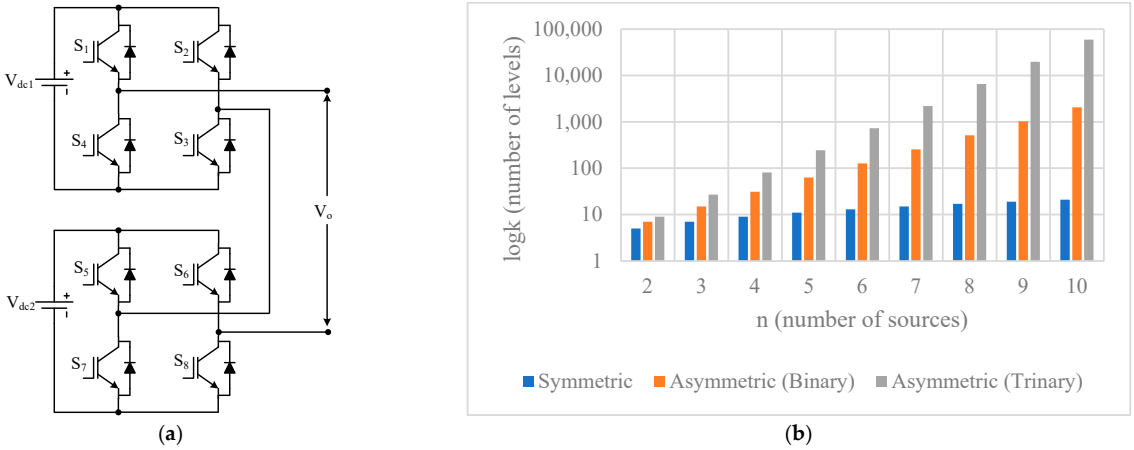

Figure 4. Five-level CHB MLI. (**a**). Symmetric. (**b**). Sources vs. levels in symmetric and asymmetric (binary, trinary) CHB MLI.

The CHB-MLIs with a single DC source are classified as listed below [12]:

- Cascaded transformer;
- PWM inverter cascaded transformer;
- Forward converter cascaded transformer;
- Stacked inverter with cascaded transformer;
- Z-source cascaded transformer.

The comparison of conventional topologies [5,30,48,56,57] are given in Table 1, where m is the number of inverter levels. The number of components that are required in five level topologies are compared in Figure 5.

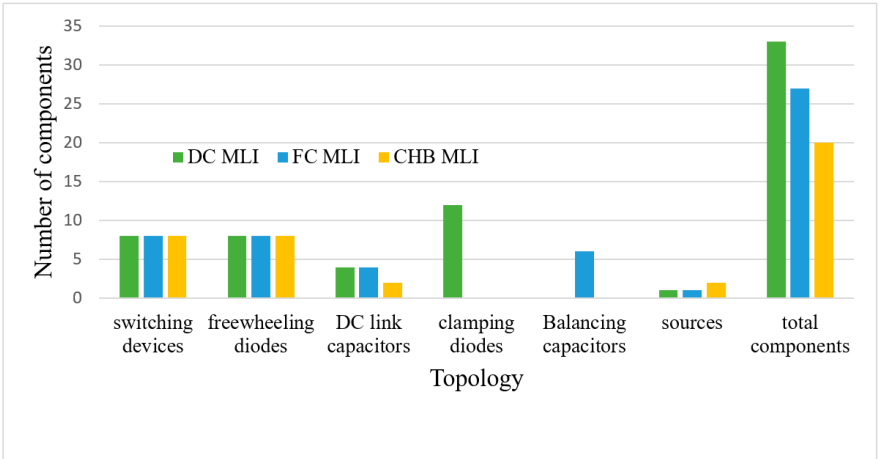

Figure 5. Comparison of five level topologies based on components.

Table 1. Comparison of classical multilevel inverters.

Sr No.	Implementation Factors	NPC	FC	CHB
1	Switching devices	$2(k-1)$	$2(k-1)$	$2(k-1)$
2	DC sources	1	1	$(k-1)/2$
3	Voltage levels	$2(k-1)$	$2(k-1)$	$k = 2n+1$ $(for\ symmetrical)$ $k = 2^{n+1}-1$ $(for\ binary)$ $k = 3^n$ $(for\ trinary)$
4	Clamping diodes	$(k-1)(k-2)$	0	0
5	DC side capacitors	$(k-1)$	$(k-1)$	$(k-1)/2$
6	Freewheeling diodes	$2(k-1)$	$2(k-1)$	$2(k-1)$
7	Balancing capacitor	0	$(k-1)(k-2)/2$	0
8	Carrier waves	$(k-1)$	$(k-1)$	$(k-1)$
9	Modularity	Low	High	High
10	Design complexity	Low	Medium	High
11	Structure	Symmetric, bulky	Symmetric, bulky	Symmetric, light
12	Switch/source utilization	Poor	Good	Good
13	Implementation complexity	Low	Medium	High
14	Control concern	Voltage balancing	Voltage setup	Power sharing
15	Redundancy	Line	Phase and line	Phase
16	Fault tolerance	Difficult	Easy	Easy
17	Cost	Low	High	Medium
18	Introduced by	Nabae, Takashi, and Akagi	Meynard	Baker and Bannister
19	Introduced year	1981	1992	1975

When it comes to the modulation scheme as an implementation factor, the space vector modulation control scheme leads to proper matching between the converter and the control scheme in NPC and CHB cases, whereas the matching is undesirable in the case of FC. On the other hand, the selective harmonic elimination pulse width modulation control scheme leads to most appropriate, proper, and undesirable matching between the converter and control scheme in the cases of NPC, FC, and CHB, respectively. For the cases of NPC and FC, proper matching, while most appropriated for the CHB, can be achieved between the converter and the sinusoidal pulse width modulation control scheme.

3. Reduced Device Count Multilevel Inverter Topologies

The reduced device count multilevel inverters have minimized the harmonics in the output voltage waveforms by varying the number of levels with a fewer switching devices, their triggering circuits, diodes, capacitors, and other devices. These topologies require a single DC source or several isolated DC sources to produce a multilevel output voltage. Multiple source topology includes symmetric and asymmetric. In symmetric topology, all the DC sources have the same magnitude, whereas, in asymmetric topology, all the DC sources possess different magnitudes. DC sources in symmetric topologies may differ in practice due to the shading effects of PV panels or different charging states of batteries. These problems are overcome by battery balancing systems [58,59]. Several reduced device count topologies have been recently developed, which are categorized in Figure 6. A comprehensive review of most recently developed topologies is presented in this section further.

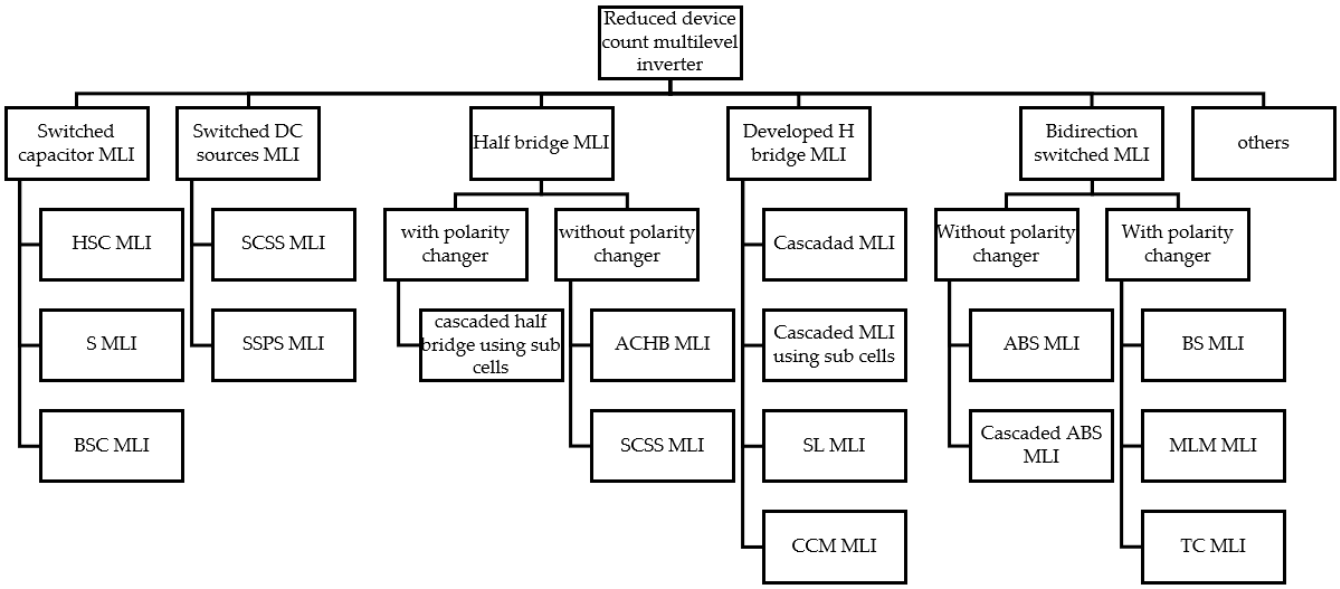

Figure 6. Reduced device count MLI.

3.1. Cascaded Half-Bridge Multilevel Inverters (CHB-MLI)

Cascaded half-bridge multilevel inverters are categorized as with or without a H-bridge. A CHB-MLI with full H-bridge topologies is composed of level generated and polarity generated parts [15,16,60–65]. The level generated part is the main part that produces positive and zero levels. The other polarity generated part is also called an auxiliary part, which generates a negative level. Another category of cascaded half-bridge MLI topologies is without a polarity changer that does not require a H-bridge inverter [66–70]. A cascaded half-bridge multilevel CHB-MLI converter is depicted in Figure 7 and is documented in [16,66,71], which solely consists of unidirectional switching devices and can operate in symmetrical or asymmetric mode. The basic unit, called a sub-cell, consists of a DC source and two unidirectional switching devices. It generates a positive and a zero level. The switching devices are never operated simultaneously due to short circuit across a DC source. The negative level is generated by the H-bridge inverter.

Mahrous et al. [66] presented an asymmetric cascaded half-bridge (ACHB) topology with a reverse polarity DC source half-bridge cell that generated the negative level for the topology. The magnitude of a DC source of a reverse polarity is the summation of all DC sources connected in the topology. This topology does not require polarity changer. Therefore, this MLI reduces the number of switching devices, switching losses, costs, and sizes. The seven-level asymmetric multilevel inverter is shown in Figure 8.

3.2. Bidirectional Switch Multilevel Inverter

These topologies can be configured without a polarity changer [17] or with a polarity changer [72–80]. The topology with a polarity changer is employed with bidirectional and unidirectional switching devices. But, the topology without a polarity changer is only designed with bidirectional devices.

The asymmetric bidirectional switch multilevel inverter (ABS MLI) was presented by Ebrahim Babaei et al. [17]. The basic unit of this topology consisted of four common emitter bidirectional switching devices and a DC source that generated a three-step quasi-square waveform. By increasing the number of DC sources (n), the output level could be extended to a higher level. An extended thirteen-level ABS MLI is shown in Figure 9. The MLI topology of the asymmetric bidirectional switch can be cascaded using sub-cells [17,81].

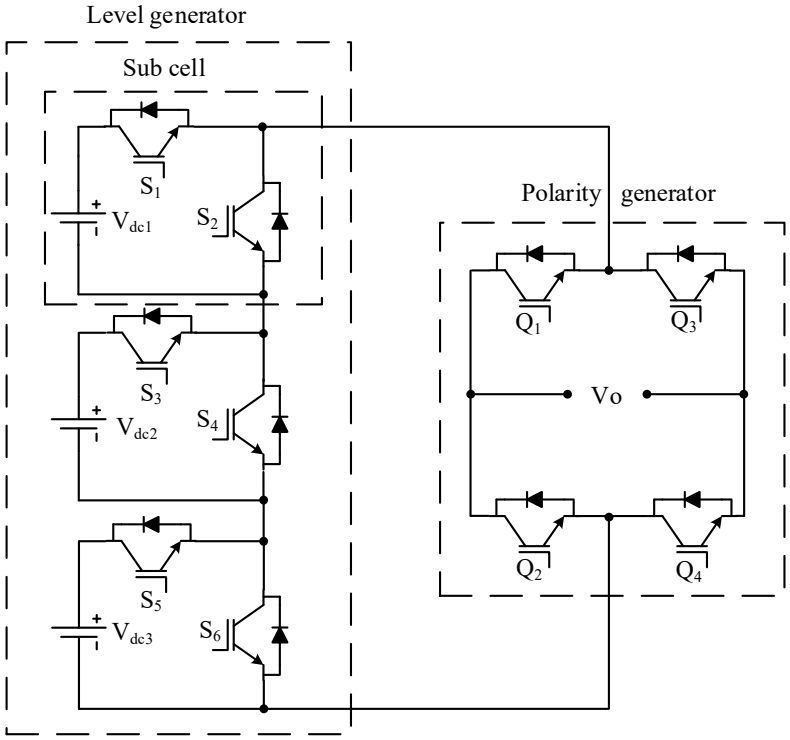

Figure 7. Cascaded half-bridge MLI using sub cells.

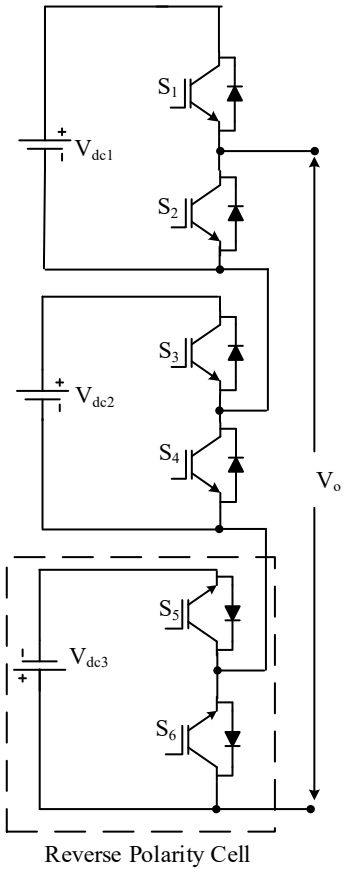

Figure 8. Cascaded half-bridge MLI with reverse polarity cell.

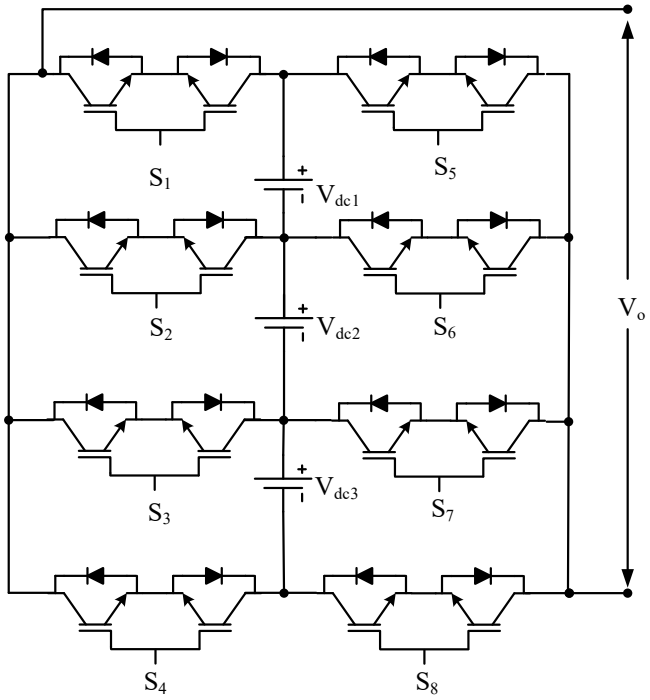

Figure 9. A 13-level asymmetric bidirectional switch MLI.

Ebrahimi et al. [80] presented the topology based on a multilevel module (MLM), as shown in Figure 10. In this topology, the multilevel module produces a positive polarity voltage with the help of bidirectional switching devices and DC sources. The different configurations of bidirectional switches are available in [82]. At the end of MLM, an H-bridge polarity generator is connected, which alternates the polarity and produces an output voltage waveform that has positive and negative levels. The polarity changer is composed of unidirectional devices. The asymmetrical source arrangement is not possible in this topology.

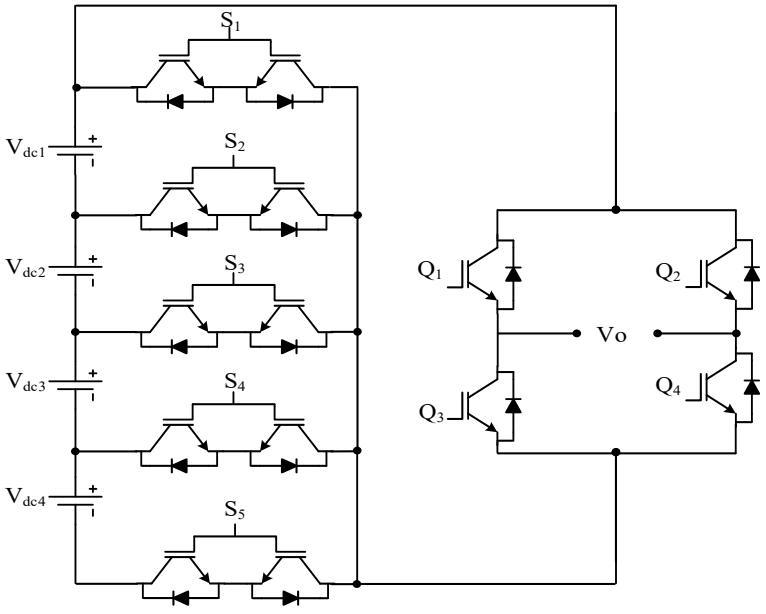

Figure 10. Multilevel module multilevel inverter.

A transistor-clamped multilevel inverter (TC MLI) topology reported in [72–79] is a combination of bidirectional and unidirectional switching devices. Bidirectional switching

devices (S1, S2 and S3) are used to generate the levels of topology, whereas unidirectional devices (Q1, Q2, Q3, and Q4) are used for a polarity generation. This topology needs fewer devices compared to conventional topologies. Figure 11 shows a transistor-clamped MLI. In Figure 11, since the insulated gate bipolar transistors are connected, the converter is said to be a transistor clamped multilevel inverter. The transistors (Q1, Q2, Q3, and Q4) are unidirectional transistors, and this part is connected as a polarity changer in Figure 11.

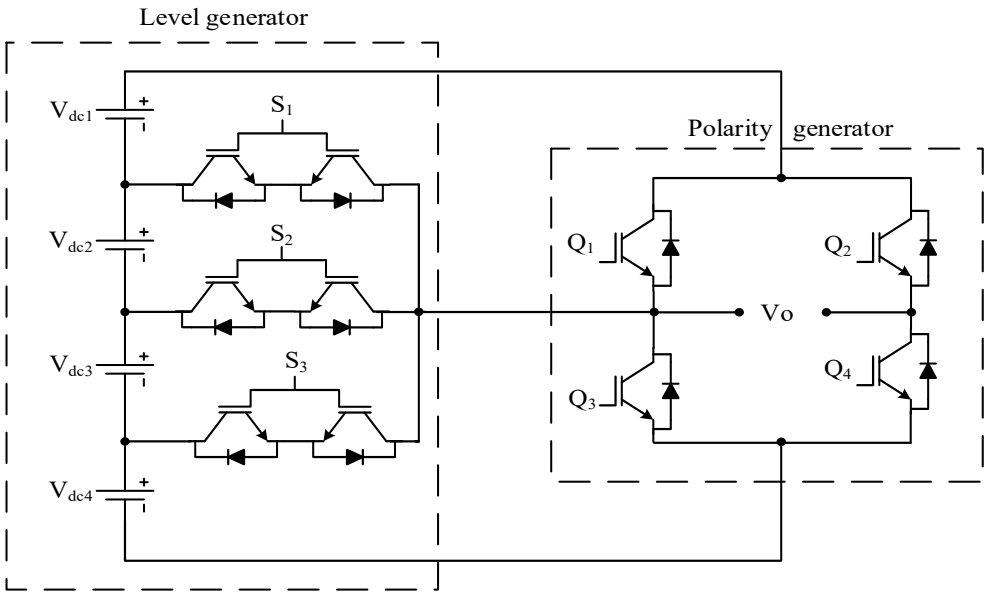

Figure 11. Five-level transistor-clamped MLI.

3.3. DC Switched Sources MLI

The series-connected switched sources (SCSS) topology developed by Gupta and Jain [71] comprises multiple DC sources connected in opposite polarities with switching devices. It does not require a two-level full bridge voltage source inverter to change the polarity. The basic unit includes a single DC source and two unidirectional switching devices. Figure 12 shows the circuit diagram of this topology. The five-level SCSS topology needs six switching devices, whereas the conventional five-level CHB requires eight switching devices. Therefore, the SCSS topology synthesizes the output voltage waveform with a lesser number of devices, unlike the CHB. The switching losses, conduction losses, and triggering circuit complexities are also minimized.

Hinago and Koizumi [83] introduced a novel switched-series-parallel-sources (SSPS) topology consisting of an H-bridge, as shown in Figure 13. With the use of an LC filter, the harmonic distortion is further reduced in this topology [83].

3.4. Switched Capacitor Multilevel Inverter

The switched capacitor topologies produce more output voltage levels with several capacitors and switching devices, but fewer symmetrical and asymmetric DC sources are required [84–96].

The hybrid-switched capacitor multilevel inverter (HSCMLI) that includes switched capacitors is presented by Fong et al. [84] and is shown in Figure 14. HSCMLI is a combination of a switched capacitor unit, a bidirectional switched MLI, and an H-bridge. The topology provides the bidirectional power flow, which is most suitable for motor drives, particularly for regenerative braking. The SCMLI topology is further simplified by replacing some active switches into diodes, such as when used as a grid, tie inverter for renewable energy farms, or drive high displacing power factor loads.

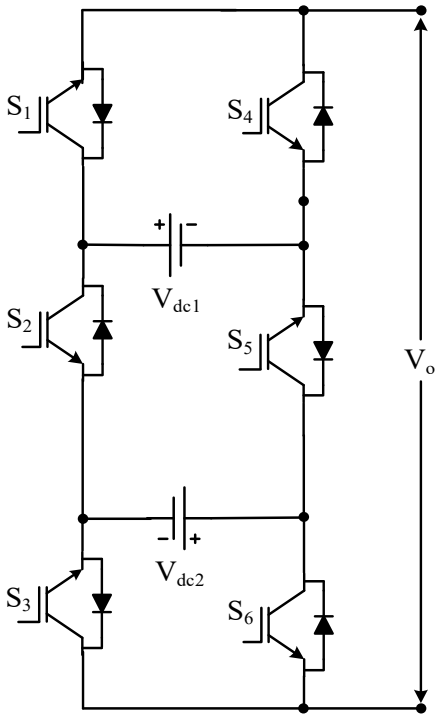

Figure 12. Five-level SCSS MLI.

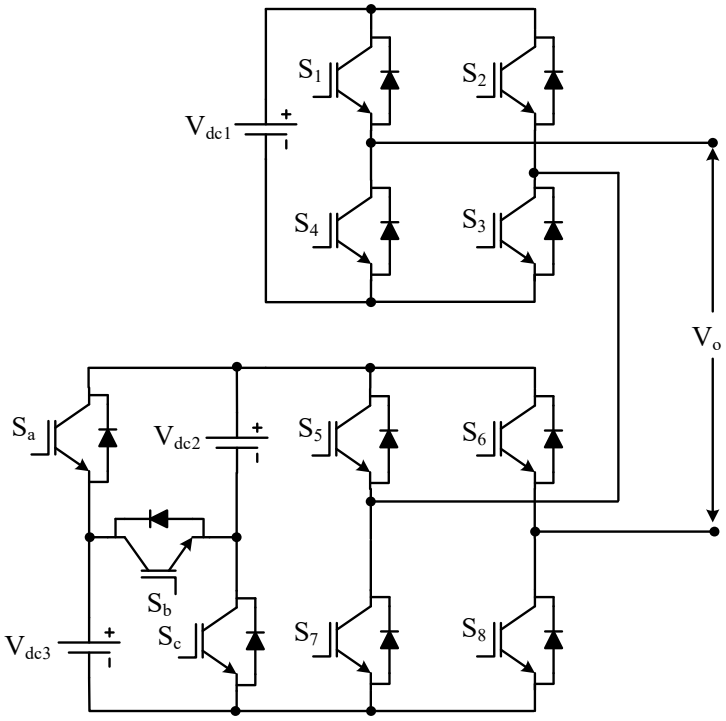

Figure 13. Switched series parallel DC sources multilevel inverter.

Another topology of a switched capacitor is known as the sub-multilevel inverter (SMLI) [85], which is capable of boosting and possesses self-charge balancing property. It generates polarity for a high number of output voltage levels (*k*) without using the H-bridge. The basic unit of SMLI consists of a pair stage of switched capacitor converter (SSC), two half bridges, and two unidirectional switches. This topology is operated in symmetric as well as asymmetric mode. An asymmetrical 17 level SMLI is shown in Figure 15.

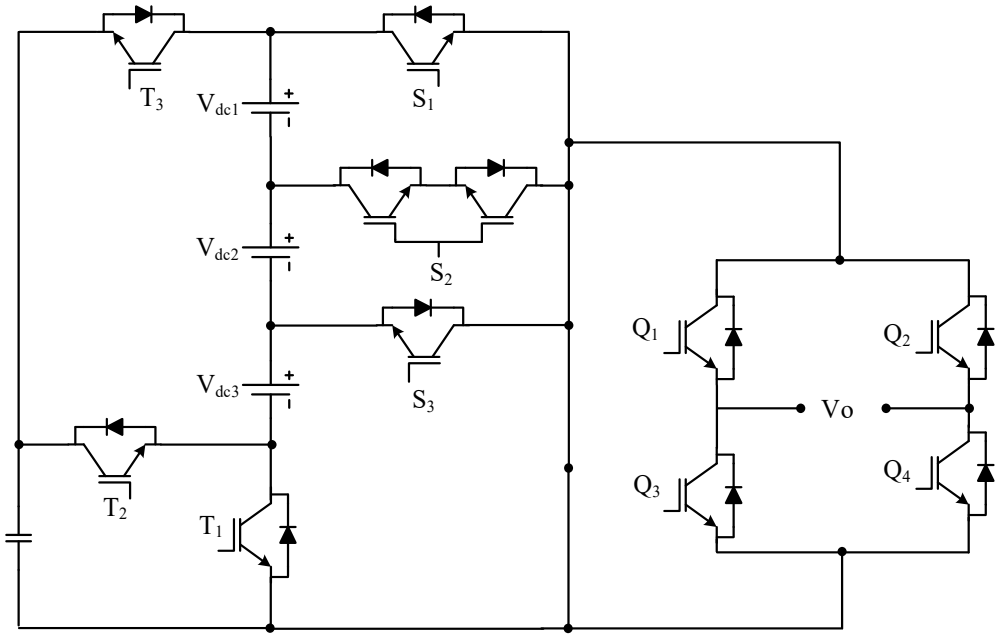

Figure 14. A 13-level hybrid SCMLI.

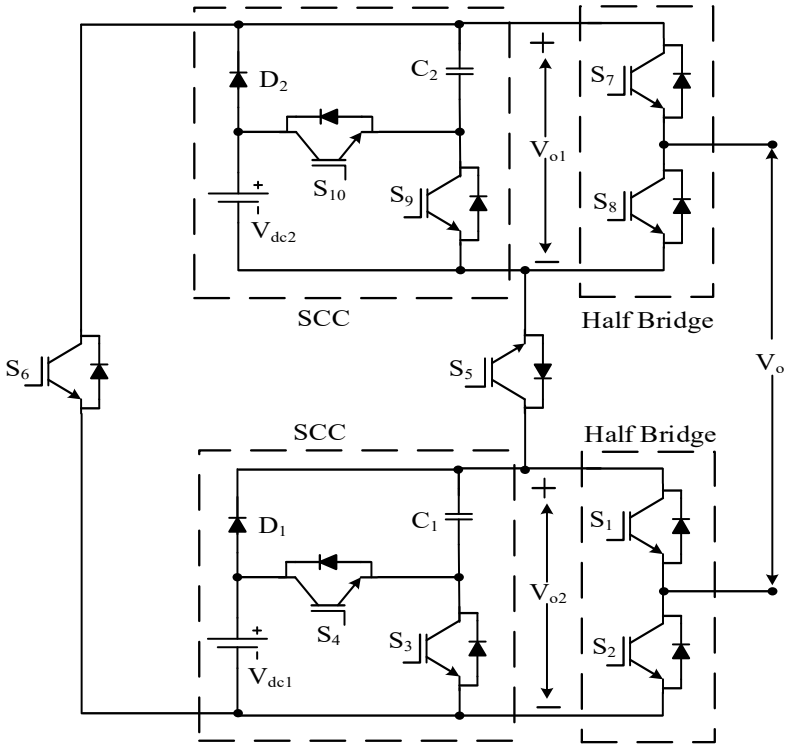

Figure 15. A 17-level hybrid SMLI.

Barzegarkhoo et al. [86] presented a new boost capacitor MLI BSCMLI topology with boosting property. The basic unit generates nine levels in the output voltage, which is composed of a switched capacitor (SC) cell and one bidirectional and four unidirectional switching devices. Figure 16 shows the boost SCMLI. The proposed topology is capable of boosting and possesses self-charge balancing properties. It also generates more voltage levels with reduced switching devices compared to conventional CHB.

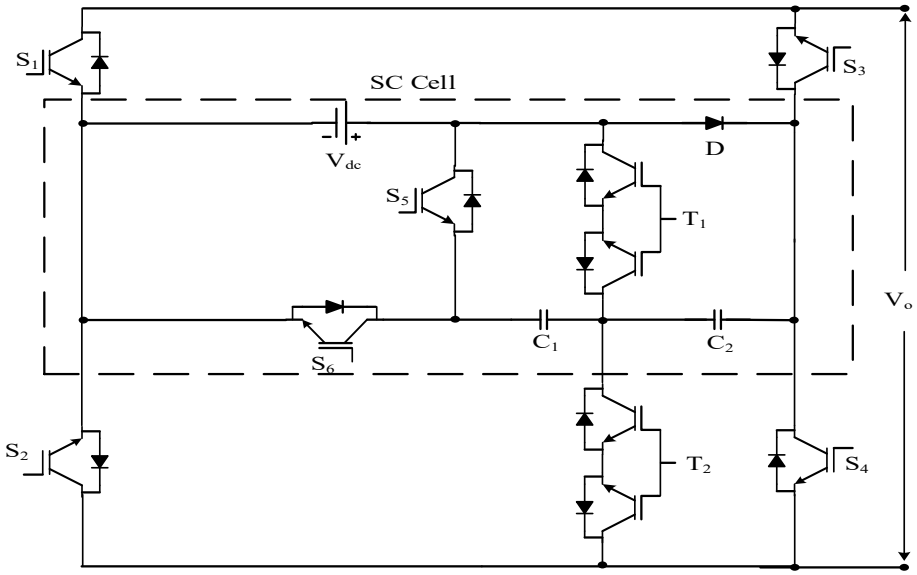

Figure 16. A 9-level boost SCMLI.

3.5. Developed H-Bridge Multilevel Inverters

Babaei et al. [97] introduced a new H-bridge topology, which was also referred to as the developed H-bridge topology in that study. The developed H-bridge topology in [97] needs a lower number of switching devices to synthesize the output voltage. The basic unit includes two DC sources and six unidirectional switching devices that generate the output voltages of seven levels. The basic unit of topologies in [97] can be easily configured by adding an additional DC source and two unidirectional switching devices in a conventional two-level H-bridge converter. The proposed unit should operate with asymmetric voltage sources, otherwise the unit of topology operates at voltage levels lower than seven. The basic circuit arrangement unit of the topology is given in Figure 17 [97,98].

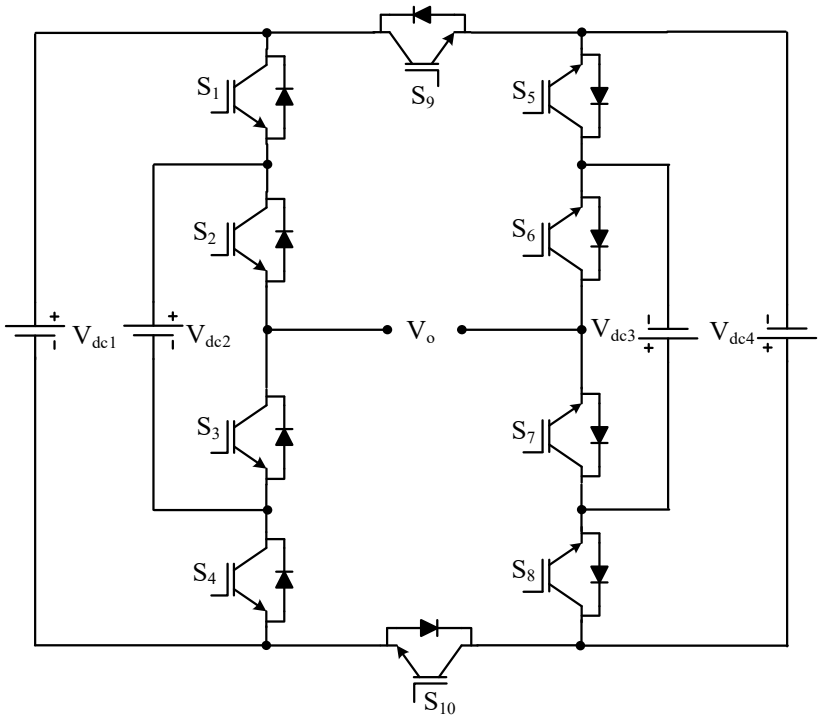

Figure 17. Developed H-bridge MLI.

Sarbanzadeh et al. [99] presented a submodule structure for MLI. The basic sub module unit of topology in a cascaded connection is shown in Figure 18. Each sub module includes four isolated DC sources, two bidirectional devices, and six unidirectional devices. In the structure of the sub module, two V_{dc1} and two V_{dc2} are used with different magnitudes (for example, $V_{dc1} = V_{dc}$ and $V_{dc2} = 3V_{dc}$). The basic unit generates an output voltage waveform of seventeen levels with positive and negative polarities, and it does not require an H-bridge polarity generator. The cascaded structure of sub modules is used either symmetrically or asymmetrically.

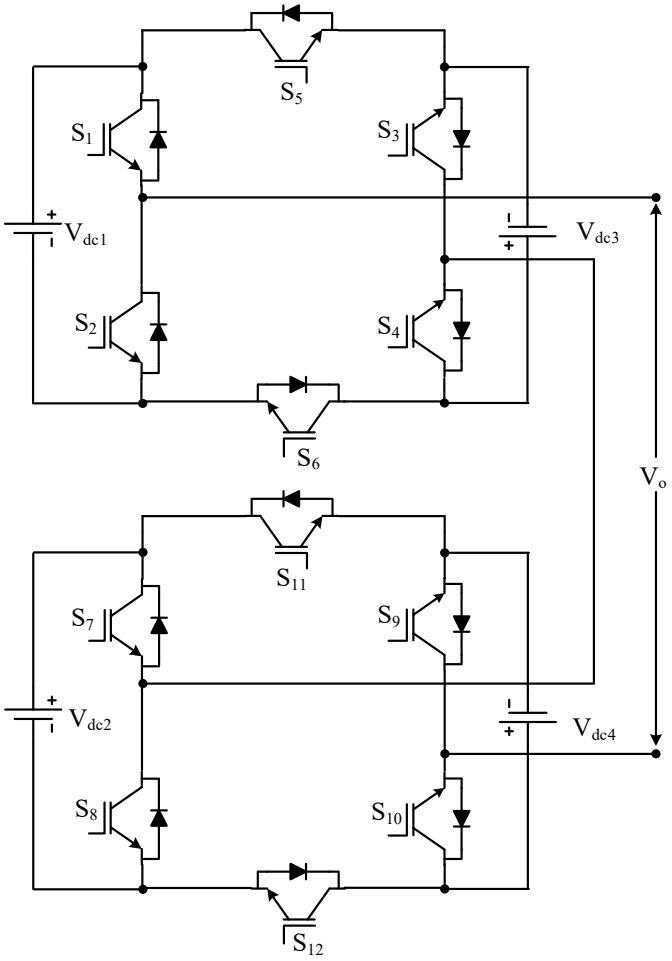

Figure 18. Cascaded MLI with sub module.

A switch ladder multilevel inverter (SLMLI) was proposed by Alishah et al. [100]. The basic unit of the SLMLI topology is a combination of four DC sources, six unidirectional devices, and two bidirectional devices. An extended form of the basic unit is given in Figure 19, which generates 31 levels in the output voltage waveform. This extended topology has a high modularity and a connected SLMLI number in a cascaded connection to assure more voltage levels [100].

Lee et al. [101] presented a cascaded topology that includes a compact module. The topology has a lower number of switching devices and provides mitigation against voltage spikes generated during the dead time. In inductive loads, the topology has well facilitated the smooth flow of inductive current by providing a freewheeling path. A 7-level cascaded compact module multilevel inverter (CCMMLI) is shown in Figure 20.

3.6. Packed U-Cell Multilevel Inverter (PUCMLI)

A packed U-cell (PUC) MLI topology can produce a higher number of levels of the output voltage with a reduction in devices unlike the conventional multilevel inverters. Therefore, less power losses are generated, a lesser number of triggering circuits are needed, and the complexity of the topology is reduced [102–105]. The basic unit of this topology comprises of a DC source or a capacitor and two unidirectional switching devices. Figure 21 shows a 7-level single phase PUC topology introduced by Al-Haddad et al. [102]. The same author controls even more the dynamics of the PUC topology by using a hysteresis controller in [104].

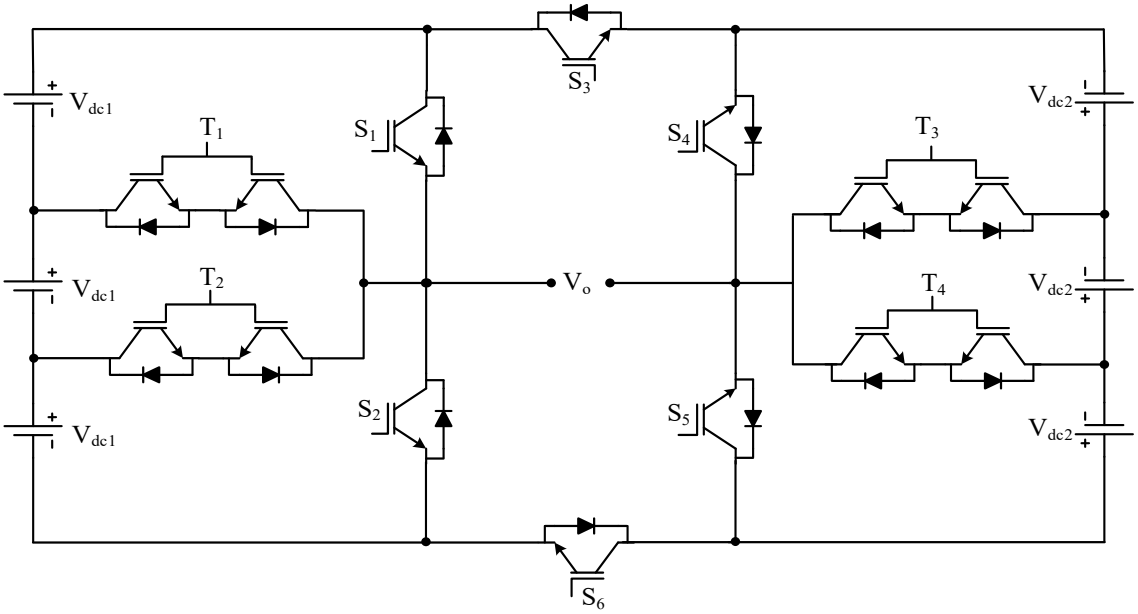

Figure 19. A 31-level switch-ladder MLI.

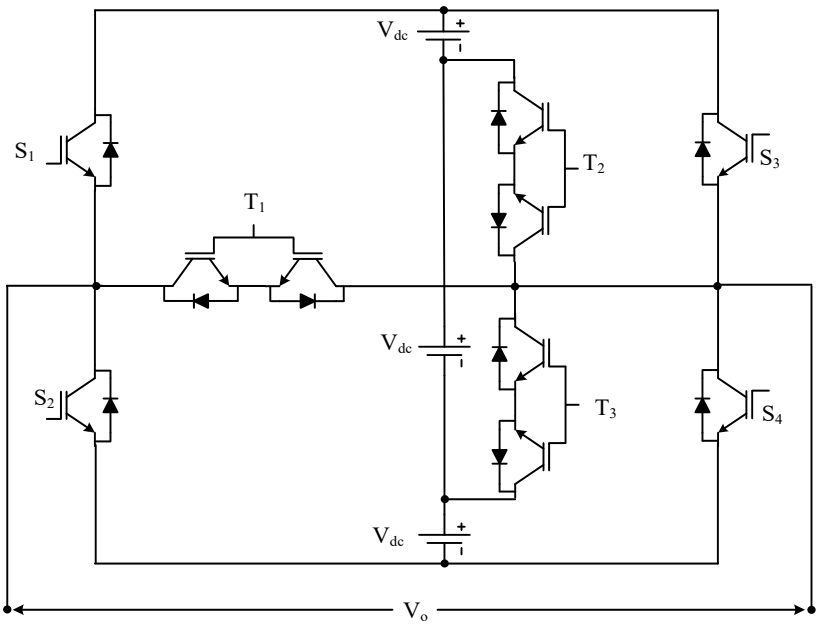

Figure 20. A 7-level cascaded compact module MLI.

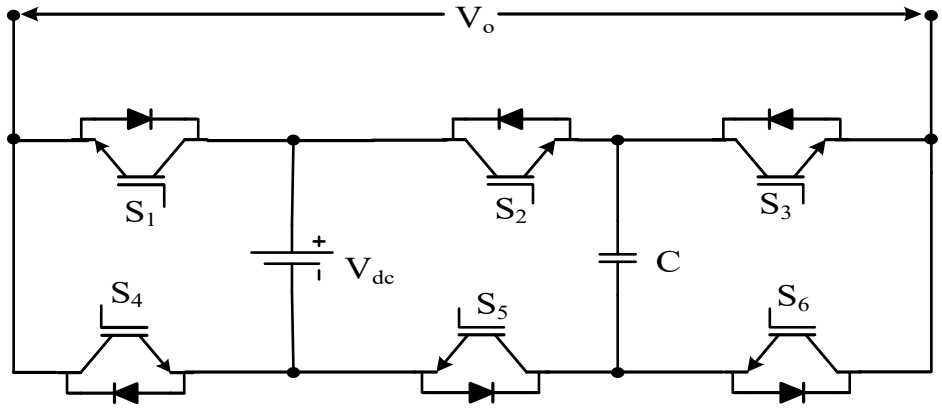

Figure 21. A 7-level packed U-cell MLI.

3.7. Other Reduced Device Count Multilevel Inverter

Oskuee et al. [106] proposed a multilevel voltage source inverter (MVSI), which had a reduced number of components that included switching devices and their triggering circuits in comparison to the conventional CHB-MLI. Subsequently, conduction losses, switching losses, costs, and complexities of the MVSI topology are minimized significantly. This topology is a symmetric topology. If there is an inequality in the DC sources, then the output voltage has undesirable harmonics. The circuit diagram of a nine-level MVSI topology is given in Figure 22.

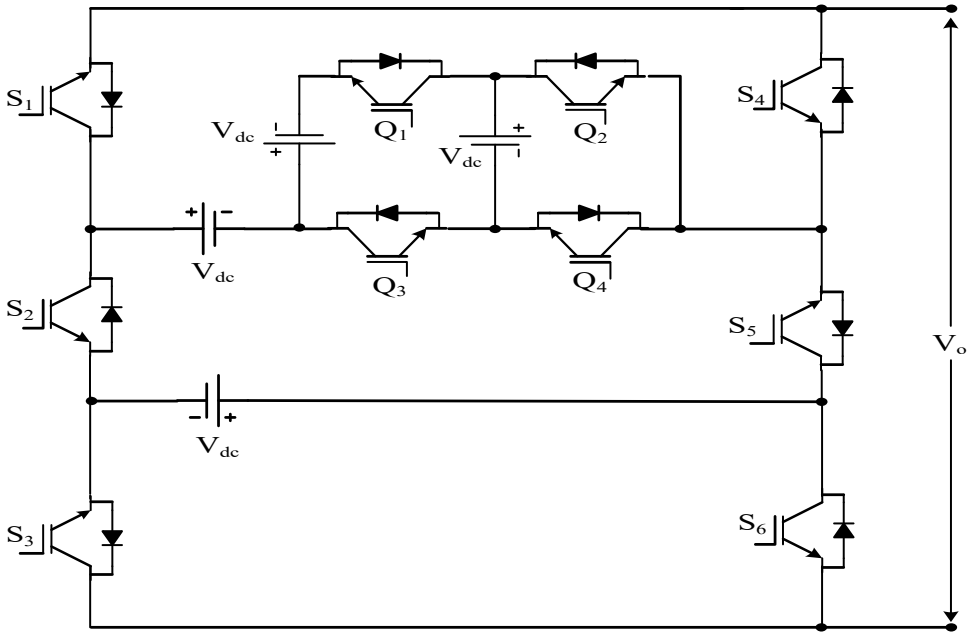

Figure 22. A nine-level asymmetric multilevel voltage source inverter.

Samadaei et al. [107] introduced an asymmetrical square T (ST) module based multilevel inverter. The basic unit of this topology, as shown in Figure 23, generates 17 levels in the output voltage without using a H-bridge. The basic unit extends in a cascaded connection to generate more levels of the output voltage.

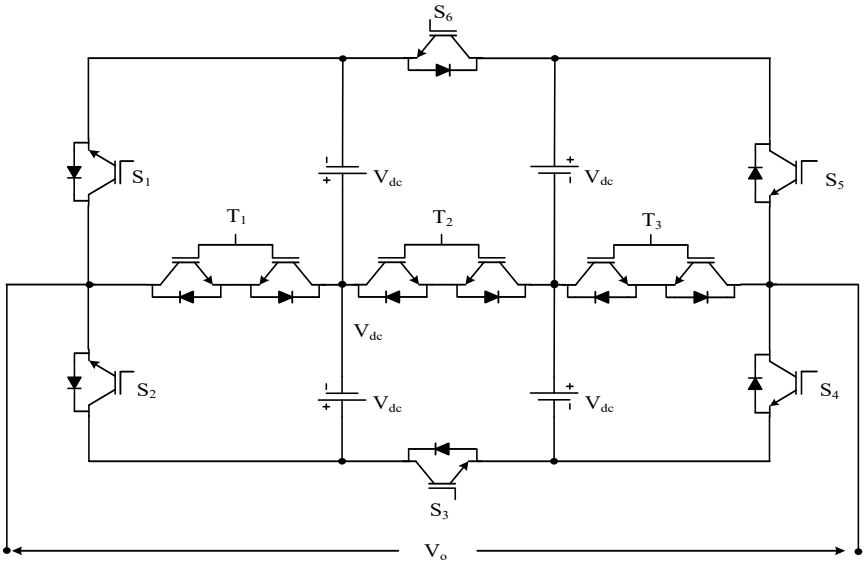

Figure 23. A 17-level asymmetric ST module type MLI.

Siddique et al. [108] presented a double H-bridge MLI, which produced more levels compared to the conventional CHB-MLI. This topology is shown in Figure 24.

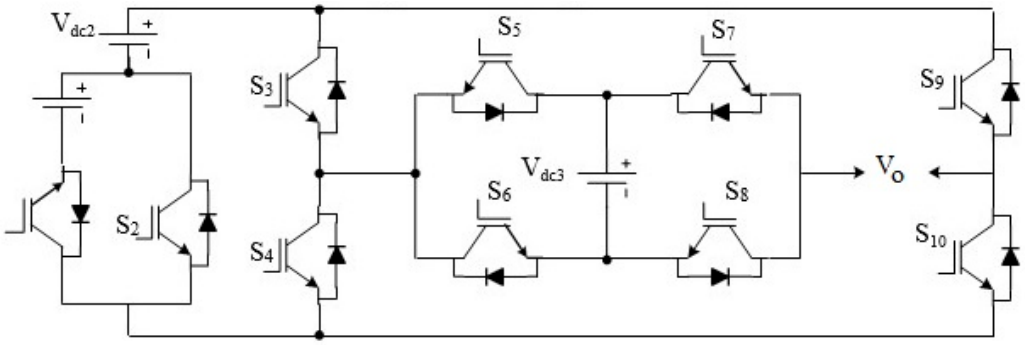

Figure 24. Asymmetric double H-bridge MLI.

4. Comparative Study of Reduced Device Count MLIs

The focus of reduced device count multilevel inverters is to generate more levels in output voltage waveform with use of a minimum number of devices. For this regard, comparisons are made in this section. The details of the component and the output voltages of several reduced device count multilevel inverters are tabulated in Table 2. The comparison of switching devices versus the number of levels is made and is shown in Figure 25, which clearly shows that the RDC multilevel inverters have fewer switching devices compared to classical CHBs. An asymmetric cascaded half-bridge MLI (Figure 8) uses less switching devices to generate a specific level compared to all RDC multilevel inverters reviewed in this paper. The topologies given in (Figures 9, 15, 17 and 21) also have less numbers of switching devices. The RDC topology illustrated in Figure 20 needs the highest switching devices as the levels increase. The topologies as shown in Figures 9–11 have bi-directional switches and have bidirectional power flow capabilities that are suitable for applications, such as renewable energy systems, motor drives, and FACTS controllers. Figure 26 shows the number of DC sources with respect to the number of levels of RDC multilevel inverters. The ACHB and PUC topologies have more reduced number of DC sources at specific levels in comparison to the RDC multilevel inverters. The RDC topologies given in Figures 7, 10, 18 and 20 demand the highest DC sources as the levels increase. The research works of various authors related to RDC multilevel inverters are summarized in Table 3.

Table 2. Component and output voltage details of reduced device count multilevel inverters.

Number of Required Switching Devices (S_d)	Output Voltage Levels (k)	Type of RDC-MLI	Figure	Reference
$k+3$ (symmetrical) $\frac{2\ln[2(k+1)]}{ln2}$ $k+9$ (asymmetrical) 2	$2n+1$ (symmetrical) $2^{n+1}-14n-1$ (asymmetrical)	Cascaded half-bridge MLI using sub cells	Figure 7	[16]
$2n$ Where n is number of cells	2^n-1	Cascaded half- bridge MLI with reverse polarity cell	Figure 8	[66]
$2(n+1)$	$n\,(n+1)+1$	BS-MLI	Figure 9	[17]
$2(n+1)$	$2n+1$	MLM MLI	Figure 10	[71]
$6n+4$	$1+2^{n+2}+2^{2n+1}$	SMLI	Figure 15	[85]
$6n+2$	$8n+1$	BSCMLI	Figure 16	[86]
$4n+2$	$2^{n+1}-1$	Developed H-bridge MLI	Figure 17	[97]
8 ns Where ns is number of sub modules	$8ns+1$	Cascaded MLI with sub module	Figure 18	[99]
10 ncm Where ncm is number of cascaded modules	$6ncm+1$	CCMMLI	Figure 20	[101]
2 $nc+2$ Where nc is total number of capacitors and DC sources	$2^{nc+1}-1$	PUCMLI	Figure 21	[102]
12 nst Where nst is number of ST modules	$16nst+1$	ST module type MLI	Figure 23	[107]
$2nh+8$ Where nh is number of half-bridge configured sources	$6nh+9$	Double H-bridge MLI	Figure 24	[108]

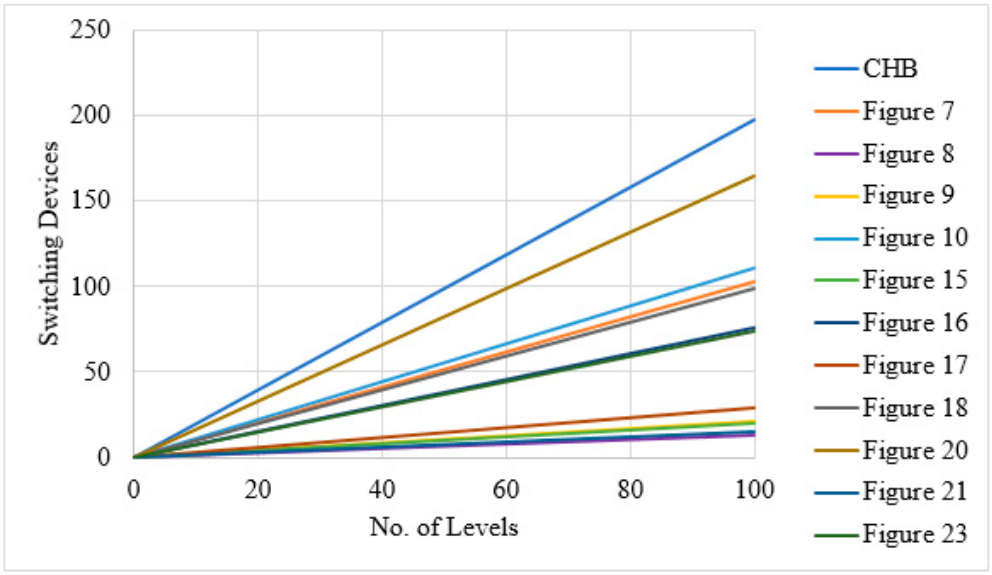

Figure 25. Comparison of switching devices vs. no. of levels of reduced switched count MLIs.

Table 3. Comparison details of reduced device count multilevel inverter.

Reference	Author (Year)	MLI Type	Modulation Scheme	Calculated Parameters	Software	Controller	Summary
[16]	Babaei, E et al. (2009)	Cascaded half-bridge MLI	Fundamental switching frequency technique	THD, output voltage	PSCAD	89C52 ATMEL micro-controller	Reduced device count topology sub cells were presented, which were extended to form a cascaded connection. Three algorithms were also presented to find out the components and voltage levels. The method was validated with simulation and experimental results.
[17]	Babaei, E et al. (2007)	common emitter bi-directional switch based MLI	Switching angle	THD, Standing voltage	PSCAD/EMTDC	89C52 ATMEL micro-controller	RSB-MLI was proposed for the series connection of sub multilevel inverters. Theoretical issues were verified with simulated and experimental results with new 49-level inverter.
[60]	Kotb, K.M et al. (2016)	cascaded half-bridge inverter	IPD (In phase deposition), POD (Phase opposite deposition), APOD (Alternative POD)	THD	MATLAB/ Simulink	NI PCI-6013	Multicarrier PWM techniques were employed in a 15-level cascaded half-bridge inverter.
[66]	Ahmed, M et al. (2017)	asymmetric cascaded half-bridge inverter	selective harmonic elimination	THD	MATLAB/ Simulink	DSP TMS320F28335 controller	Authors introduced the topology with reverse polarity cell; therefore, it did not require polarity changer, thus reducing the switching devices, costs, and complexities of the circuit.
[71]	Gupta, K.K. and Jain, S (2014)	SCSS-MLI	PD-SPWM	THD, conduction losses, switching losses	MATLAB/ Simulink	DS1103 dSpace	A novel topology and its principle of operation was presented. The simulation results of this topology were also compared with conventional topologies.
[80]	Ebrahimi, J et al. (2012)	MLM-based MLI	-	THD, conduction losses, switching losses	PSCAD/EMTDC	ATMEL 89C52 micro-controller	The multilevel module based MLI was proposed in this study. Various optimal structures related with reduced device count were also presented. The proposed topology was evaluated with its prototype hardware and simulation.
[81]	Babaei, E (2010)	CHB-MLI using sub cells	switching angle	--	PSCAD/EMTDC	89C52 ATMEL micro-controller	The authors developed bi-directional based topologies in this study. Authors presented how the basic units can be extended, and also these extended units were configured in a cascaded connection. The performances of these topologies were validated with simulated and prototype results.

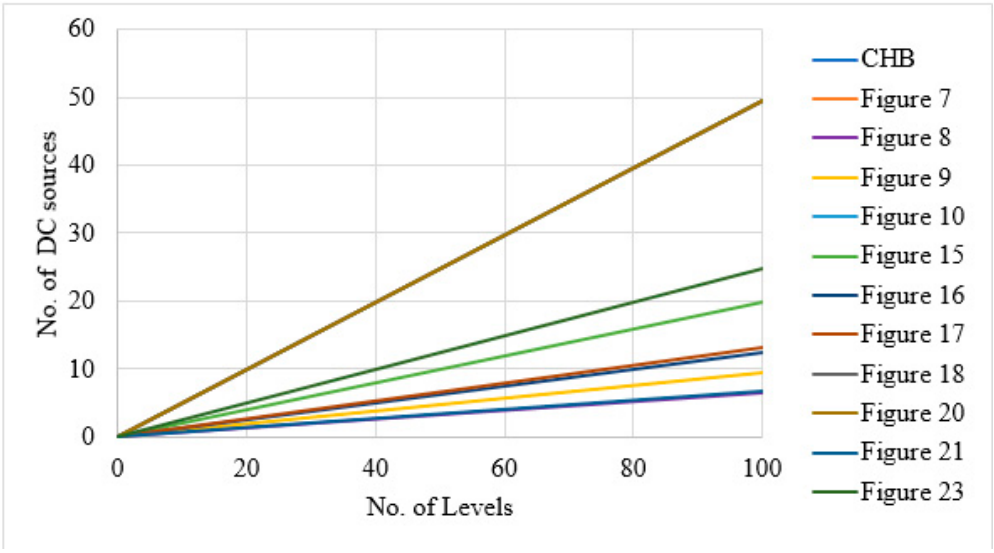

Figure 26. Comparison of DC sources vs. no. of levels of reduced switched count MLIs.

5. Reduced Device Count Multilevel Inverters in Photovoltaic Systems

Nowadays, the focus of researchers in this field is also devoted mainly to improve the design of multilevel inverters (a review on previous trends appears in [109]) in such a way that not only their power consumption is reduced but their harmonic contents are also minimized with less number of switching devices and their control circuitries. For this purpose, many topologies of multilevel inverters have been recently developed with a lower number of switching devices that give a multi-level output that is closer to a harmonic-free sinusoidal waveform. Some recently developed multilevel inverters for PV applications are discussed as under:

Regarding single-phase MLIs, as in [110], Sambasivam Rajalakshmi et al. [111] proposed a single-phase-modified multilevel inverter for PV applications. This topology requires nine switching devices, three diodes, and three DC sources for thirteen levels at the output voltage. Prabhat Ranjan Bana [112] proposed a reduced device count multilevel inverter, which was configured with a H-bridge-based MLI and a level-doubling circuit. The polarity changer was also used to generate negative voltage levels. The output voltage of the MLI was controlled with the selective harmonic elimination pulse width modulation (SHE-PWM) technique.

Prem Ponnusamy et al. [113] developed the dual-source multilevel inverter for PV system. The MLI consisted of level generator and polarity changer. The MLI was tested with symmetric and asymmetric modes of operation using nearest-level modulation (NLM). Alireza Pourfaraj [114] proposed a single-phase dual-mode interleaved multilevel inverter. A step-up chopper was integrated with this inverter, which enabled it to operate in step-up and step-down modes. This topology also consisted of polarity changer. Nirmal Mukundan et al. [115] integrated a support vector machine (SVM) converter with a newly developed multilevel inverter. The positive levels were generated with a level generator, whereas negative levels were changed with polarity changer.

The comparison of recent reduced device count multilevel inverter topologies for PV system is summarized in Table 4.

Several modulation techniques are available for reduced device count multilevel inverters. A modulation technique is an essential part of multilevel inverters. The number of levels and contents of harmonics in the output voltage is controlled by these techniques. The various types of modulation techniques are shown in Figure 27. Multicarrier PWM techniques consist of modulators, reference signals, and carrier waves. The carrier wave is either a triangular wave or an inverted cosine wave.

Table 4. Comparison of recent reduced device count MLIs for PV system.

Reference	Year	MLI				Modulation Scheme	Calculated Parameters	Software	Controller	MPPT Algorithm	PV Configuration
		Configuration	k *	S_d *	n *						
[111]	2019	Modified CHB	9	8	4	PD, POD, APOD	THD, output voltage	MATLAB/ Simulink	PIC 16F877A Micro-controller	-	Standalone
[112]	2019	Reduced switch H- bridge-based (RSHB) MLI with LDC	9	17	7	SHE-PWM PD-PWM	THD, output voltage	MATLAB/ Simulink	Arduino Mega 2560	Incremental conductance (IC)	Standalone
[113]	2020	Dual source multilevel inverter	9	11	2	NLM	THD, output voltage, voltage stress, switching and conduction losses, efficiency	MATLAB/ Simulink	FPGA Spartan 6 processor	-	Standalone
[114]	2019	Dual-mode interleaved multilevel inverter		10	1	PWM	THD, Power loss		STMicroelectronics STM32F407 DSP	-	Grid connected
[115]	2021	Improved H-bridge multilevel inverter	6	5	2	PWM	THD, Power loss, total standing voltage	MATLAB/ Simulink (R2009a)	dSPACE Micro Lab Box	IC	Grid connected
[116]	2019	Modified H-bridge MLI	31	8	4	PWM	THD	MATLAB/ Simulink	FPGA Spartan	Artificial neural network	Standalone
[117]	2022	Cascaded H-bridge sub-MLI	15	7	3	PD-CPWM	THD	MATLAB/ Simulink	Xilinx Spartan 3E-500 FPGA	Fuzzy logic	Standalone
[118]	2016	CHB with double level circuit	13	14	4	PD-CPWM	THD, Power loss	MATLAB/ Simulink	dSpace 1104 controller	Perturb and observe (P & O)	Standalone
[119]	2020	Voltage level boost (VLB) MLI	15	10	5	PD-CPWM	THD, Power loss	MATLAB/ Simulink	DSP controller	IC	Grid connected
[120]	2020	Micro multilevel inverter	5	5	2	PD-CPWM	THD, Power loss	MATLAB/ Simulink	d-SPACE 1104	P & O	Standalone
[121]	2020	Switched capacitor MLI	29	9	3	SHE-PWM	THD, Power loss	MATLAB/ Simulink	DSPIC30F2010 controller	Grey Wolf optimization technique and fuzzy logic control	Standalone
[122]	2023	Switched capacitor MLI	7	8	1	Anti predatory particle swarm optimization	THD	MATLAB/ Simulink	-	Fuzzy controller	Standalone
[123]	2023	S-packed U-cells	5	5	1	PWM	THD	MATLAB/ Simulink	-	IC with hysteresis control	Grid connected

* k (number of levels), S_d (number of switches) and n (number of PV sources).

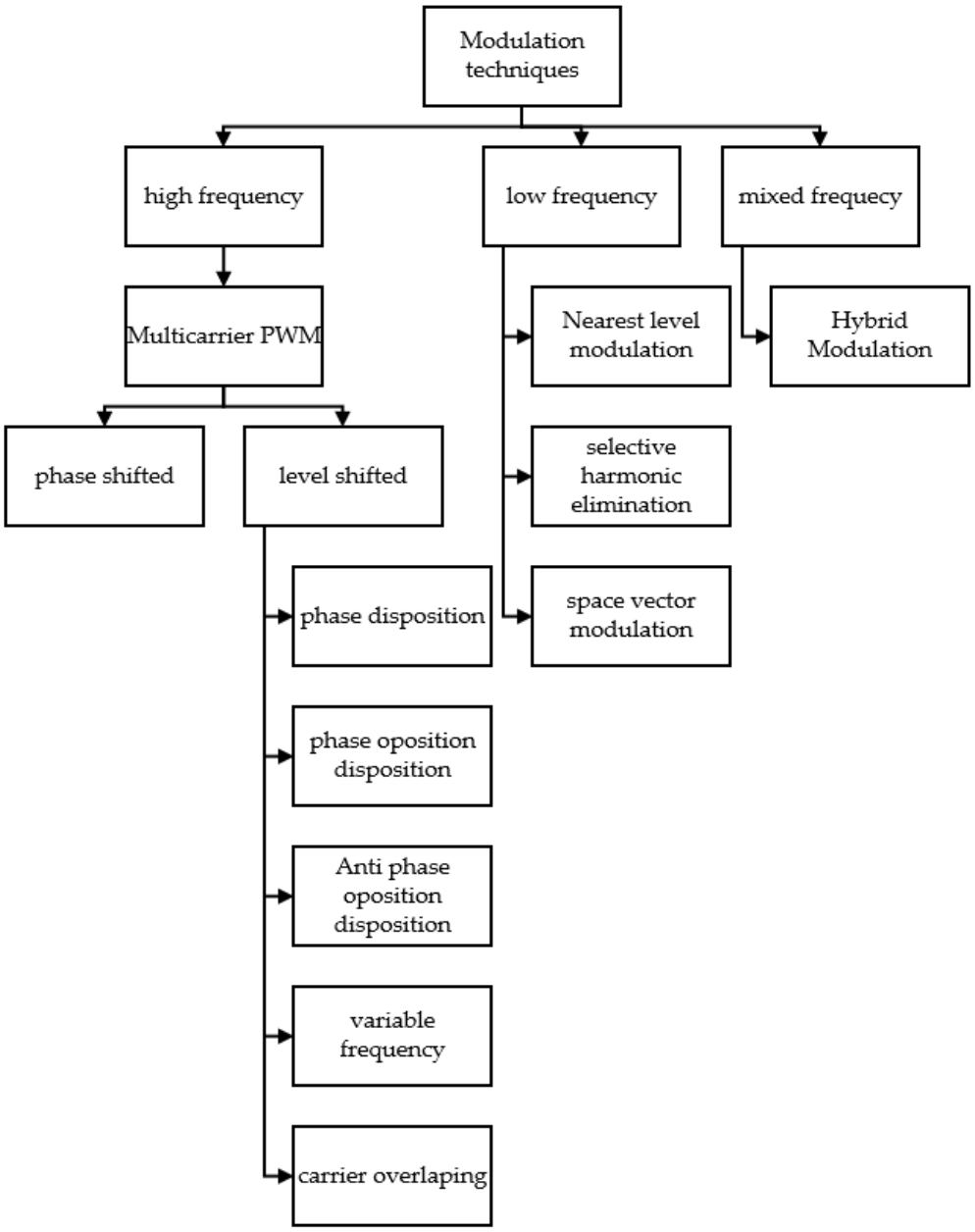

Figure 27. Modulation techniques for RDC MLI.

6. Conclusions

This paper contains a detailed discussion of classical multilevel inverters. Their features and limitations are also given in detail. The main focus of this paper is on reduced device count multilevel inverters. More than 120 studies on different RDC MLI topologies published up to 2022 have been reviewed and summarized. This paper provides a paradigm for RDC MLIs based on the switching configuration. A comparison between the number of levels, the number of switching devices, and the number of DC sources required for several RDC multilevel inverters is also presented. The information on these inverters is useful for researchers developing new RDC MLI topologies. Recently, several newly proposed topologies were introduced by researchers who synthesized a higher number of levels of the output voltage with a reduced number of power electronic devices. Therefore, this paper has reviewed the recently developed reduced device count topologies. This paper also provides a paradigm of RDC multilevel inverter topologies for a PV system that will be a constructive tool for readers to select an appropriate topology for this application. From the review, it is concluded that RDC topologies have gained popularity in various power

utility and industrial applications over the last few years because the topologies reached a certain level of maturity. There is still a lot of space to conduct research on RDC multilevel inverters for further optimization. A few future directions on RDC MLIs are the following:

- Fault-tolerant operations;
- Integration with PV systems, wind-energy-conversion systems, fuel cells, etc.;
- Speed control of drives;
- Asymmetric operation such as natural, binary, and trinary progression;
- Cascaded and hybrid configurations;
- Implementation of modulation and control schemes.

Author Contributions: Conceptualization, A.J.M. and M.A.M.; methodology, A.S.L. and M.M.S.; software, A.J.M., M.A.M. and M.M.S.; validation, A.J.M., M.A.M., A.S.L. and M.M.S.; formal analysis, A.J.M.; investigation, A.J.M., M.A.M., A.S.L. and M.M.S.; resources, M.A.M.; data curation, A.J.M. and M.M.S.; writing—original draft preparation, A.J.M.; writing—review and editing, M.A.M., A.S.L. and M.M.S.; visualization, M.A.M. and M.M.S.; supervision, M.A.M., A.S.L. and M.M.S.; project administration, M.A.M., A.S.L. and M.M.S.; funding acquisition, A.J.M. All authors have read and agreed to the published version of the manuscript.

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