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Optimal Asymmetric Duty Modulation for Dual Active Bridge Converters with DC Blocking Capacitors

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Abstract: Aiming at the optimization of current stress with low voltage ratio and full ZVS, a control method combining variable duty cycle and phase shift was proposed based on dual active bridge (DAB) converters with DC blocking capacitors. By adding DC bias to the DC blocking capacitors, asymmetric duty modulation (ADM) can adjust the bias as needed. Based on the theoretical analysis of steady-state operation, the operating modes can be divided into eight modes. According to the features of each mode, equivalent circuits are established. The transmission power and the boundary of zero-voltage-switching (ZVS) are deduced through a detailed analysis of each mode. Based on the theoretical deduction, ADM is more suitable for a low voltage ratio. Verified by experiment, optimized asymmetric duty modulation (OADM) can increase efficiency by 3.58%, 6.57%, 8.81%, and 10.33% compared with DPS when P is equal to 0.36 and m is equal to 0.4, 0.3, 0.2, and 0.1, respectively. Using this method, the current stress of the converter is lighter than that under regular modulation when the voltage ratio $m \leq 0.5$ with full ZVS.

Keywords: DC blocking capacitor; DAB; asymmetric duty modulation; ZVS; current stress

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1. Introduction

In recent years, the proportion of renewable energy in the power grid has rapidly increased. However, as a significant source of renewable energy, solar power could not be connected to the AC grid directly. As a result, the DC microgrid was proposed and has developed greatly [1]. The DC microgrid could not only realize local consumption but also relatively reduce the times of electric energy conversion, which significantly improved efficiency [2]. In a DC microgrid, solar power could not work stably. It would lead to damage to the converter, and even DC-link voltage fluctuation, causing grid fault [3]. Bidirectional isolated DC-DC converters can not only transmit power bidirectionally between DC buses of different voltage levels, but also have the advantages of higher power density, simple structure, and isolation, which have vital research value.

R.W. De Doncker proposed DAB converters for the first time in the late 20th century [4]. Their excellent properties soon led to a series of studies by different researchers. They are now widely used in renewable energy, energy storage, electric vehicle charging, energy routers, and other fields [5–7].

The most common modulation of DAB converters is phase shift modulation (PSM), mainly including single phase shift (SPS) modulation [4], extended phase shift (EPS) modulation [8,9], dual phase shift (DPS) modulation [10,11], and triple phase shift (TPS) modulation [12]. To avoid magnetic bias, PSM can only operate at a fixed 50% duty cycle. For the same reason, pulse width modulation (PWM) also cannot be used directly. In [13], a three-level DAB is proposed. Its modulation is a combination of PSM and PWM. Although the complexity of control is reduced, the cost and the complexity of hardware increase. Furthermore, [14] proposed a modulation that applies PWM on both sides of the DAB converter.

For the optimization of current stress, the most direct method is derivation [15]. However, it is challenging to derive or obtain the analytical conditional extreme points when the equation of current stress is complex. On this basis, the Lagrange multiplier method is applied [16]. However, this method could only solve the current stress optimization problem with equality conditions, namely transmission power. When it needs to meet both the ZVS conditions and mode boundary, inequality conditions should be added. To solve this, the Karush–Kuhn–Tucker method (KKT) is applied [17]. However, with the increase in constraint conditions, the difficulty of the analytical solution increases exponentially. So, in [18], a graphic method was proposed. The characteristics of the optimal operating point can be determined by analyzing the variation in current stress and constraint conditions. This simplifies the analytical process and helps achieve optimization. However, when the ZVS conditions, boundary conditions, and current stress equations are complex and their trends are difficult to analyze, the above methods may not be effective. To address this issue, this paper presents an optimization method that involves discretizing and numerical solutions.

The research on the topology, modulation, and optimization of DAB converters has been relatively detailed, while the research based on DC blocking capacitors is still insufficient. The research on DC blocking capacitors is currently still focused on SPS under the hybrid bridge modulation [19,20].

Due to the insufficient analysis of PWM and current stress optimization, a novel ADM based on DC blocking capacitors is proposed. By using PWM to generate a DC component that is then converted into DC bias, the proposed modulation enables DAB to adapt to a wide range of voltage ratios. By adjusting the duty cycle of the full bridge output voltage on the input side and the phase between the full bridge output voltages on both sides, the power and transmission direction can be controlled without changing its fundamental topology. The different operating modes of the converter are classified based on the output voltage waveforms of the full bridge on both sides of the power transmission process. The transmission power and ZVS boundary of all modes are mathematically deduced. Furthermore, the OADM is proposed, which can be used to optimize the current stress. By this method, minimum current stress and full ZVS for voltage ratios of $m \leq 0.5$ is achieved. Finally, the proposed OADM is validated through comparative experiments. It also makes it possible to achieve a smoother transition of mode switching in the method proposed in [20].

The structure of this article is as follows: In Section 2, the basic definition of the proposed ADM is introduced. In Section 3, the working principles of the proposed ADM are analyzed in detail. In Section 4, the optimization of the ADM with ZVS and inductor current, namely OADM, is given. In Section 5, the experimental results are given to verify the analysis and compare with those of the conventional modulation. Finally, the conclusions are presented in Section 6.

2. ADM with the Aid of DC Blocking Capacitors

The topology of a DAB converter with DC blocking capacitors is shown in Figure 1. V_1 and V_2 are input and output DC-link voltage, respectively. The turn ratio of the transformer is n. V_{AB} is the primary side bridge output voltage, and V_{CD} is the secondary side bridge output voltage. V_p is the primary side voltage of the transformer, and V_s is the secondary side voltage of the transformer. C_{bp} is the DC blocking capacitor of the primary side, and C_{bs} is the DC blocking capacitor of the secondary side. L is the sum of external series inductance and transformer leakage inductance. i_L is the inductor current. i_o is the output current. C_1 and C_2 are the DC bus capacitors for input and output. With the aid of DC blocking capacitors, ADM can adjust the DC bias of DC blocking capacitors to control the output voltage.

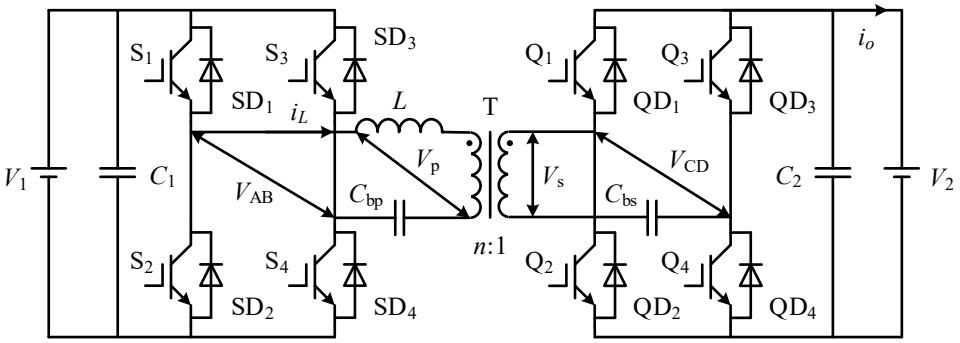

Figure 1. Topology of a DAB converter with DC blocking capacitors.

The typical ADM waveforms based on DC blocking capacitors are shown in Figure 2. T_{hs} represents half of a switching cycle. V_{cbp} and V_{cbs} represent DC bias voltage on the primary and secondary side DC blocking capacitors, respectively. D is the duty cycle of primary bridge output in one switching cycle. The phase shift angle φ, which is calculated in radians as the difference between the rising edges of the primary and secondary side voltages of the transformer, varies between $-\pi$ and π. A positive phase shift ($\varphi > 0$) is shown in Figure 2, corresponding to the phase shift ratio D_φ in half a switching period. D_φ is the ratio of the difference between the rising edges of the primary and secondary side voltages of the transformer to half a switching period.

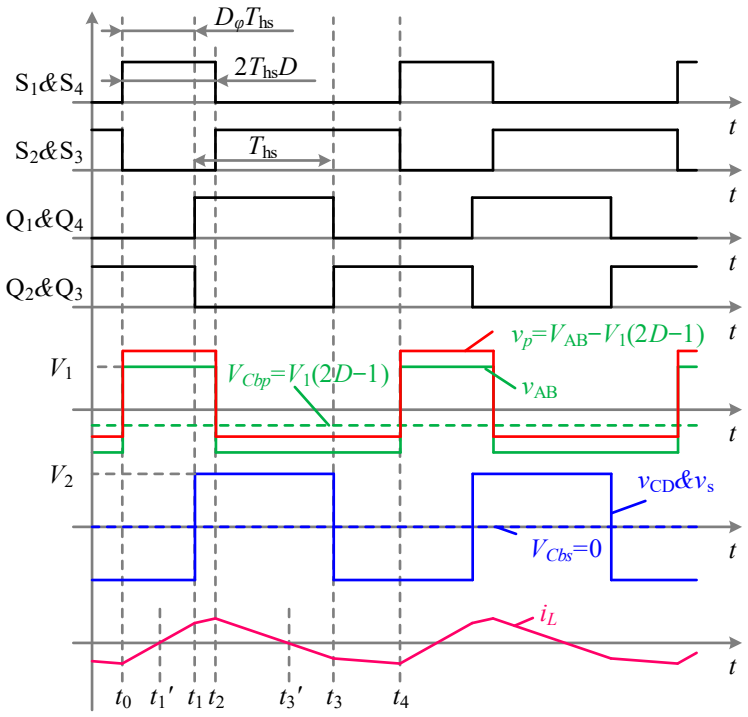

Figure 2. Typical waveforms of ADM.

According to the definitions of D and D_φ, the ranges are as follows:

$$\begin{cases} |D_\varphi| \le 1 \\ 0 \le D \le 1 \end{cases} \tag{1}$$

3. Principles of the Proposed ADM

The principle of ADM control is relatively easy to understand. Its main idea is to apply different DC biases to the DC blocking capacitors by changing the duty cycle to match the

voltage of the primary side and the secondary side of the transformer, thus reducing the current stress and increasing the soft switching range. There are eight operating modes. This section analyzes each operating mode in detail. The transmission power and the conditions of ZVS for each mode are discussed with a specific analysis of mode A as an example.

3.1. Analysis of Operation Mode

D and D_φ are controlled variables in the ADM based on DC blocking capacitors. Distinctions between different control combinations are mainly reflected in the waveforms and voltages across the DC blocking capacitors on the changed duty cycle side. Whether $D \geq 1/2$ determines the polarity of the voltage on the DC blocking capacitors. So, the relationship between the waveforms of V_p and V_s and the voltage across DC blocking capacitors can be used to classify the operation modes of the converter.

Firstly, when $D_\varphi \geq 0$ and $D \leq 1/2$, the rising edge of V_p is ahead of $\mathrm{V_s}$. In this case, when $D > D_\varphi/2$, the operation state is mode A, and when $D \leq D_\varphi/2$, the operation state is mode B. Secondly, when $D_\varphi \geq 0$ and $D \geq 1/2$, the rising edge of V_p is ahead of $\mathrm{V_s}$. Therefore, when $D > D_\varphi/2 + 1/2$, the operation state is mode C, and when $D \leq D_\varphi/2 + 1/2$, the operation state is mode D. Thirdly, when $D_\varphi \leq 0$ and $D \leq 1/2$, the rising edge of V_s is ahead of V_p. In this situation, when $D > D_\varphi/2 + 1/2$, the operation state is mode E, and when $D \leq D_\varphi/2 + 1/2$, the operation state is mode F. Lastly, when $D_\varphi \leq 0$ and $D \geq 1/2$, the rising edge of V_s is ahead of V_p. Thus, when $D > D_\varphi/2 + 1$, the operation state is mode G, and when $D \leq D_\varphi/2 + 1$, the operation state is mode H. The waveforms of V_p and V_s in different modes are shown in Figure 3, and the ranges of corresponding variables are presented in Table 1.

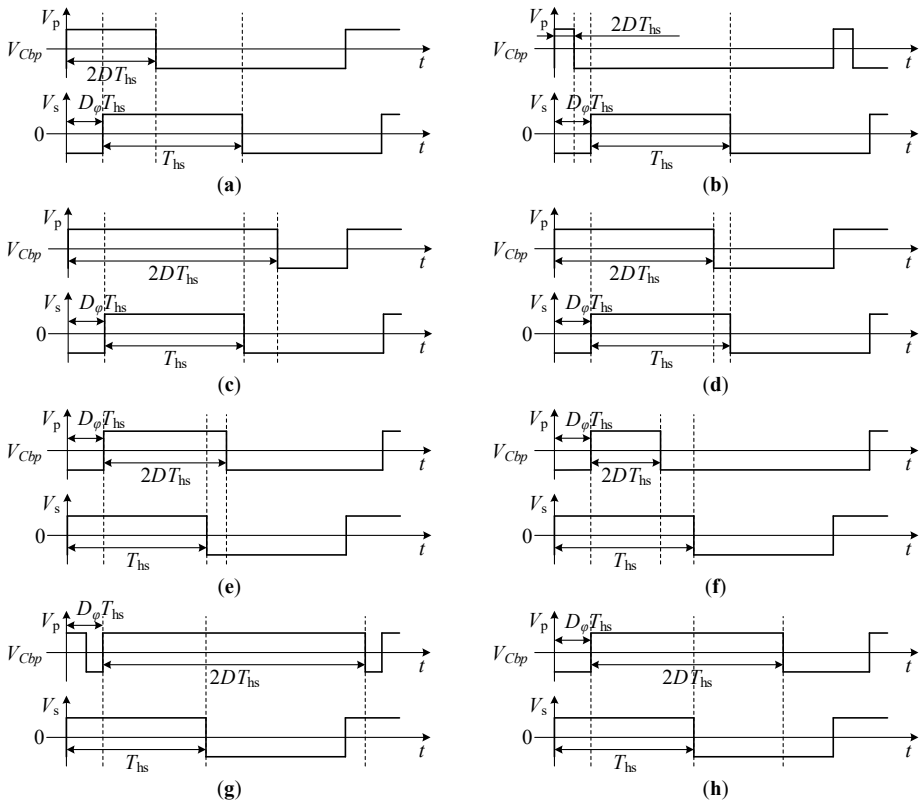

Figure 3. ADM operation mode classification: (**a**) mode A; (**b**) mode B; (**c**) mode C; (**d**) mode D; (**e**) mode E; (**f**) mode F; (**g**) mode G; (**h**) mode H.

Table 1. Range of D, D_φ under each mode.

The Boundary Conditions	Mode
$0 \le D \le 1/2, 0 \le D\varphi \le 1, D > D\varphi/2$	Mode A
$0 \le D \le 1/2, 0 \le D\varphi \le 1, D \le D\varphi/2$	Mode B
$1/2 \le D \le 1, 0 \le D\varphi \le 1, D > D\varphi/2 + 1/2$	Mode C
$1/2 \le D \le 1, 0 \le D\varphi \le 1, D \le D\varphi/2 + 1/2$	Mode D
$0 \le D \le 1/2, -1 \le D\varphi \le 0, D > D\varphi/2 + 1/2$	Mode E
$0 \le D \le 1/2, -1 \le D\varphi \le 0, D \le D\varphi/2 + 1/2$	Mode F
$1/2 \le D \le 1, -1 \le D\varphi \le 0, D > D\varphi/2 + 1$	Mode G
$1/2 \le D \le 1, -1 \le D\varphi \le 0, D \le D\varphi/2 + 1$	Mode H

The range of modes is shown in Figure 4.

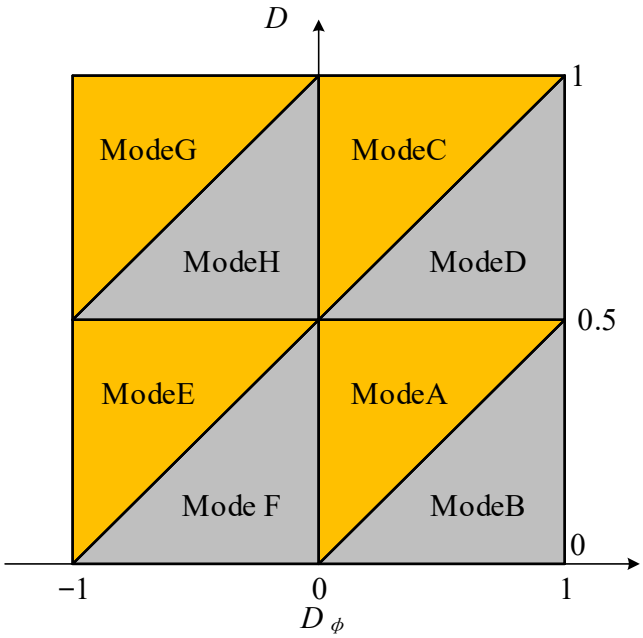

Figure 4. Range of modes.

There is no overlap between the modes. The range of modes exactly covers (1), ensuring the wholeness and uniqueness of classification.

3.2. Transmission Power Analysis

Transmission power varies across different modes. The operation mode shown in Figure 2 is used as an example to illustrate the deduction.

The equivalent circuit of each stage in mode A from t_0 to t_4 can be drawn according to Figure 2, and the results are shown in Figure 5. The red lines in Figure 5 indicate the current flow of each stage in mode A.

Stage 1 ($t_0 - t_1'$): At t_0, S_1 and S_4 turn on, while S_2 and S_3 turn off. As the current on L is negative, diodes SD_1 and SD_4 conduct, allowing the power devices to realize ZVS. The current through diodes QD_2 and QD_3 on the secondary side of the transformer remains continuous. The voltage across L can be derived as $[V_1 - V_1(2D - 1)] + nV_2$. So, i_L at this stage can be derived as:

$$i_L(t) = i_L(t_0) + \frac{[V_1 - V_1(2D-1)] + nV_2}{L}(t - t_0) \quad (2)$$

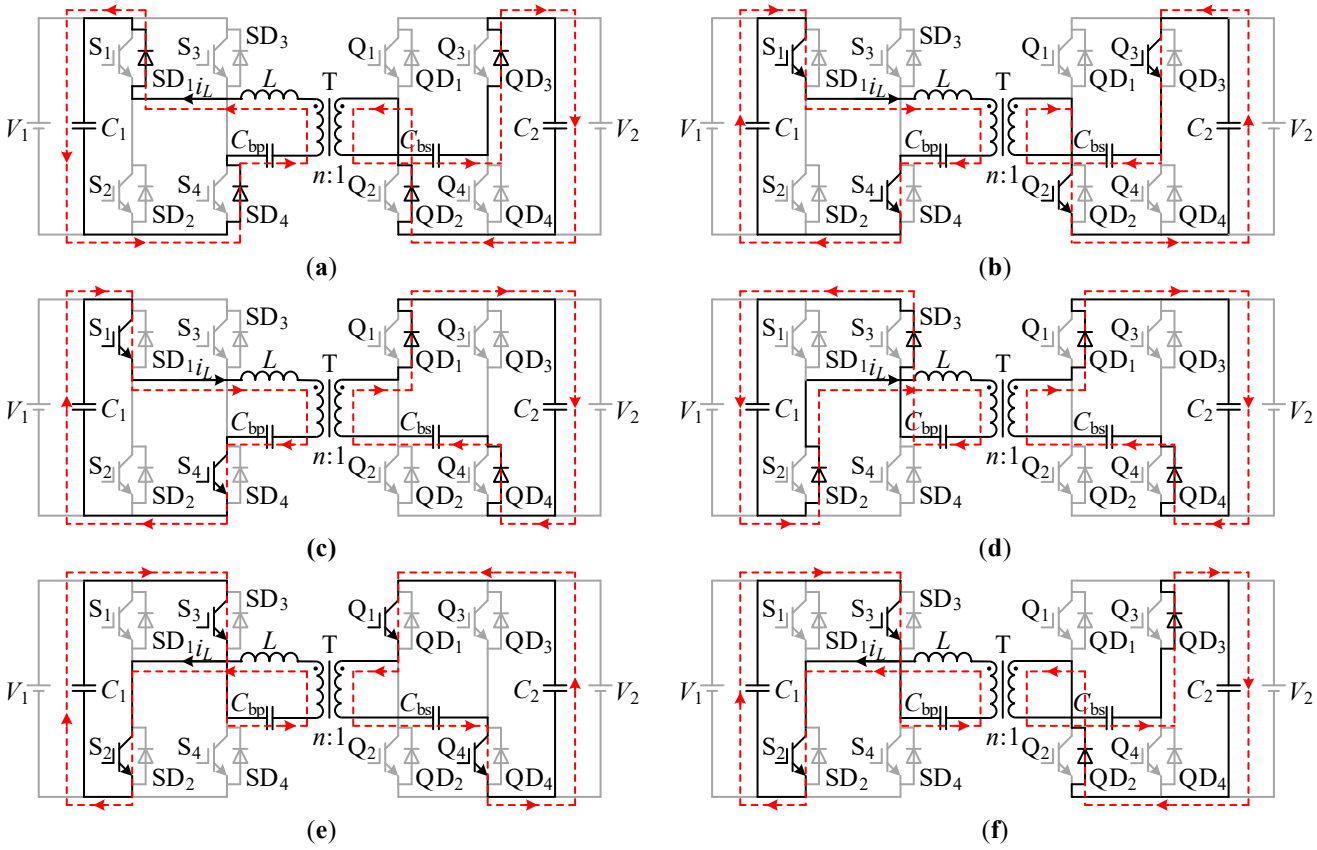

Figure 5. Equivalent circuits of stages in mode A: (**a**) stage 1; (**b**) stage 2; (**c**) stage 3; (**d**) stage 4; (**e**) stage 5; (**f**) stage 6.

Stage 2 ($t_1{}' - t_1$): At $t_1{}'$, the current through L begins to increase from zero. The current flows through S_1 and S_4 on the primary side of the transformer and through Q_2 and Q_3 on the secondary side. The voltage on L can be deduced as $[V_1 - V_1(2D-1)] + nV_2$. So, i_L at this stage can be derived as:

$$i_L(t) = i_L(t_1{}') + \frac{[V_1 - V_1(2D-1)] + nV_2}{L}(t - t_1{}') \tag{3}$$

Stage 3 ($t_1 - t_2$): At t_1, Q_1 and Q_4 turn on, while Q_2 and Q_3 turn off. The current on L increases; the current on the primary side of the transformer flows through S_1 and S_4, and the current on the secondary flows through QD_1 and QD_4. The voltage across the inductor is $[V_1 - V_1(2D-1)] - nV_2$, so the power devices achieve ZVS. The current through L reaches its maximum absolute value at this stage and can be expressed as:

$$i_L(t) = i_L(t_1) + \frac{[V_1 - V_1(2D-1)] - nV_2}{L}(t - t_1) \tag{4}$$

Stage 4 ($t_2 - t_3{}'$): At t_2, S_2 and S_3 realize ZVS while S_1 and S_4 turn off. The current flows through QD_1 and QD_4 on the secondary side of the transformer. The voltage on L is $[-V_1 - V_1(2D-1)] - nV_2$. At this stage, i_L falls to zero, and the expression is:

$$i_L(t) = i_L(t_2) + \frac{[-V_1 - V_1(2D-1)] - nV_2}{L}(t - t_2) \tag{5}$$

Stage 5 ($t_3{}' - t_3$): At $t_3{}'$, the current on L begins to increase negatively from zero. The current on the primary side flows through S_2 and S_3, and the current on the secondary side

flows through Q_2 and Q_3. The voltage across L at this stage is $[-V_1 - V_1(2D-1)] - nV_2$, and i_L increases in the reverse direction, expressed as:

$$i_L(t) = i_L(t_3') + \frac{[-V_1 - V_1(2D-1)] - nV_2}{L}(t - t_3') \tag{6}$$

Stage 6 ($t_3 - t_4$): At t_3, Q_2 and Q_3 realize ZVS, while Q_1 and Q_4 turn off. The current on L increases in the reverse direction. The primary side current of the transformer flows through S_2 and S_3, while the secondary side current flows through QD_2 and QD_3. The voltage across L is $[-V_1 - V_1(2D-1)] + nV_2$, and the expression of i_L is:

$$i_L(t) = i_L(t_3) + \frac{[-V_1 - V_1(2D-1)] + nV_2}{L}(t - t_3) \tag{7}$$

According to the condition of zero integral of current on the DC blocking capacitors in a steady state:

$$\int_0^{2T_{\mathrm{hs}}} i_L(t)dt = 0 \tag{8}$$

Solving Formulas (2) to (8), the inductor current at different times is shown below:

$$\begin{cases} i_L(t_0) = \frac{4D^2-4D-2mD_\varphi+m}{2L}V_1T_{\mathrm{hs}} \\ i_L(t_1) = \frac{4D^2-4D-4DD_\varphi+4D_\varphi+m}{2L}V_1T_{\mathrm{hs}} \\ i_L(t_2) = \frac{-4D^2+4D+m-4mD+2mD_\varphi}{2L}V_1T_{\mathrm{hs}} \\ i_L(t_3) = \frac{4D^2-4DD_\varphi-m}{2L}V_1T_{\mathrm{hs}} \end{cases} \tag{9}$$

m represents the voltage ratio and $m = nV_2/V_1$.

The transmission power of mode A is derived as follows:

$$\begin{aligned} P_{\mathrm{out\_A}} &= \frac{1}{2T_{\mathrm{hs}}}\int_0^{2T_{\mathrm{hs}}} v_{\mathrm{p}}(t)i_L(t)dt \\ &= \frac{V_1^2 m[-2D^2-{D_\varphi}^2+D(1+2D_\varphi)]}{L}T_{\mathrm{hs}} \end{aligned} \tag{10}$$

The maximum power that a DAB converter with DC blocking capacitors can transmit under SPS control is as follows:

$$P_{\mathrm{N}} = \frac{mV_1^2}{4L}T_{\mathrm{hs}} \tag{11}$$

For the simplification of the analysis, the transmission power expression of Formula (10) is normalized by P_{N} expressed as a function of D and D_φ as follows:

$$P_{\mathrm{A}} = -8D^2 - 4{D_\varphi}^2 + 4D(1+2D_\varphi) \tag{12}$$

Similar to the derivation process of transmission power for mode A, the expression for each mode is as follows:

$$P = \begin{cases} -8D^2 - 4{D_\varphi}^2 + 4D(1+2D_\varphi) & \text{Mode A} \\ 4D(2D - 2D_\varphi + 1) & \text{Mode B} \\ 4(D-1)(2D - 2D_\varphi - 1) & \text{Mode C} \\ -8D^2 - 4{D_\varphi}^2 + 4D(1+2D_\varphi) & \text{Mode D} \\ 4[2D^2 + (1+D_\varphi)^2 - D(3+2D_\varphi)] & \text{Mode E} \\ 4D(1 - 2D + 2D_\varphi) & \text{Mode F} \\ 4(D-1)(2D_\varphi - 2D + 3) & \text{Mode G} \\ 4[2D^2 + (1+D_\varphi)^2 - D(3+2D_\varphi)] & \text{Mode H} \end{cases} \tag{13}$$

Normalized transmission power is shown in Figure 6 based on Formula (13).

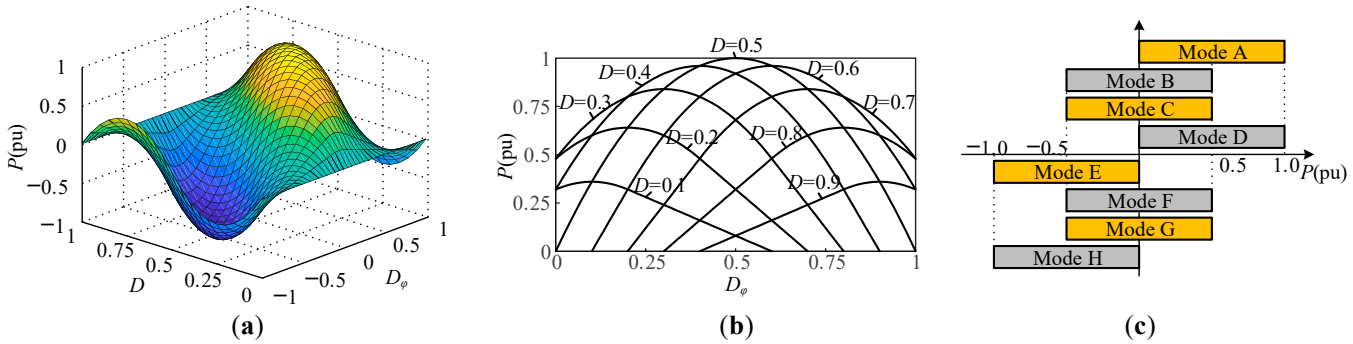

Figure 6. Transmission power: (**a**) 3D figure of D, D_φ, and P; (**b**) $D_\varphi \geq 0$, $P \geq 0$, 2D figure of D, D_φ, and P; (**c**) transmission power range of each mode.

Under the ADM based on DC blocking capacitors, the transmission power characteristics are as follows: (1) the forward and reverse transmission powers are symmetrical and have a maximum value that is equal to 1; (2) there exist equal power points, which provide a basis for optimizing current stress; (3) the transmission power in modes B, C, F, and G can range from −0.5 to 0.5.

3.3. ZVS Analysis

ZVS has different boundary conditions in different modes. The software Mathematica is used to simplify boundary conditions and the figure of the ZVS range is verified and plotted using MATLAB. To make a switch achieve ZVS, the current has to flow reversely when an on signal is set. Take mode A in Figure 2 as an example. At t_0, S_1 and S_4 are turned on, and S_2 and S_3 are turned off. At this time, the current on the inductor is less than zero to achieve ZVS. At t_1, Q_1 and Q_4 are turned on, and Q_2 and Q_3 are turned off. At this moment, the current on the inductor is more than zero to realize ZVS. At t_2, S_2 and S_3 are turned on, and S_1 and S_4 are turned off. At this moment, the current on the inductor is greater than or equal to zero to realize ZVS. At t_3, Q_2 and Q_3 are turned on, and Q_1 and Q_4 are turned off. At this moment, the current on the inductor is less than or equal to zero to realize ZVS. The same methods can be used to analyze the boundary conditions of every mode. The boundary conditions are shown in Table 2.

Table 2. Boundary conditions of ZVS in each mode.

Mode	t_0	t_1	t_2	t_3
A	$i_L(t_0) \leq 0$	$i_L(t_1) \geq 0$	$i_L(t_2) \geq 0$	$i_L(t_3) \leq 0$
B	$i_L(t_0) \leq 0$	$i_L(t_1) \geq 0$	$i_L(t_2) \geq 0$	$i_L(t_3) \leq 0$
C	$i_L(t_0) \leq 0$	$i_L(t_1) \geq 0$	$i_L(t_2) \leq 0$	$i_L(t_3) \geq 0$
D	$i_L(t_0) \leq 0$	$i_L(t_1) \geq 0$	$i_L(t_2) \geq 0$	$i_L(t_3) \leq 0$
E	$i_L(t_0) \leq 0$	$i_L(t_1) \leq 0$	$i_L(t_2) \geq 0$	$i_L(t_3) \geq 0$
F	$i_L(t_0) \leq 0$	$i_L(t_1) \geq 0$	$i_L(t_2) \leq 0$	$i_L(t_3) \geq 0$
G	$i_L(t_0) \leq 0$	$i_L(t_1) \leq 0$	$i_L(t_2) \geq 0$	$i_L(t_3) \geq 0$
H	$i_L(t_0) \leq 0$	$i_L(t_1) \leq 0$	$i_L(t_2) \geq 0$	$i_L(t_3) \geq 0$

Take the boundary conditions of ZVS under mode A as an example:

$$\begin{cases} 0 \leq D_\varphi \leq 1; 0 \leq D \leq \frac{1}{2}; D \geq \frac{1}{2} D_\varphi \\ i_L(t_0) \leq 0; i_L(t_1) \geq 0; i_L(t_2) \geq 0; i_L(t_3) \leq 0 \end{cases} \tag{14}$$

To simplify the calculation, the maximum transmission power current is taken as the reference current, and the current is normalized.

$$i_N = \frac{P_N}{V_1} = \frac{mV_1T_{hs}}{4L} \tag{15}$$

The normalized current at each moment under mode A is:

$$\begin{cases} i_L(t_0) = 2 - 4D_\varphi + \frac{8(-1+D)D}{m} \\ i_L(t_1) = 2 + \frac{8(-1+D)(D-D_\varphi)}{m} \\ i_L(t_2) = 2 - 8D + 4D_\varphi + \frac{8D(1-D)}{m} \\ i_L(t_3) = -2 + \frac{8D(D-D_\varphi)}{m} \end{cases} \tag{16}$$

By combining Formulas (16) and (14), Formula (17) can be derived, which represents the ZVS region under mode A. The boundary of this region varies with m.

$$\begin{cases} 0 < D_\varphi < \frac{1}{2} \\ \frac{1}{2}D_\varphi < D \le D_\varphi \\ m < \frac{-4D + 4D^2}{-1 + 2D_\varphi} \end{cases} \text{or} \begin{cases} 0 < D_\varphi < \frac{1}{2} \\ D_\varphi < D < \frac{1}{2} \\ 4(D - D_\varphi)(1 - D) < m \\ m < \frac{-4D + 4D^2}{-1 + 2D_\varphi} \end{cases} \tag{17}$$

$$\text{or} \begin{cases} \frac{1}{2} \le D_\varphi < 1 \\ \frac{1}{2}D_\varphi < D < \frac{1}{2} \end{cases}$$

The same method can be used to solve the other seven modes. Thus, the range of ZVS in the full operating area is shown in Figure 7. Figure 7 shows the range of ZVS in the full operating area when m = 0.1, m = 0.1, m = 0.3, and m = 0.4, respectively.

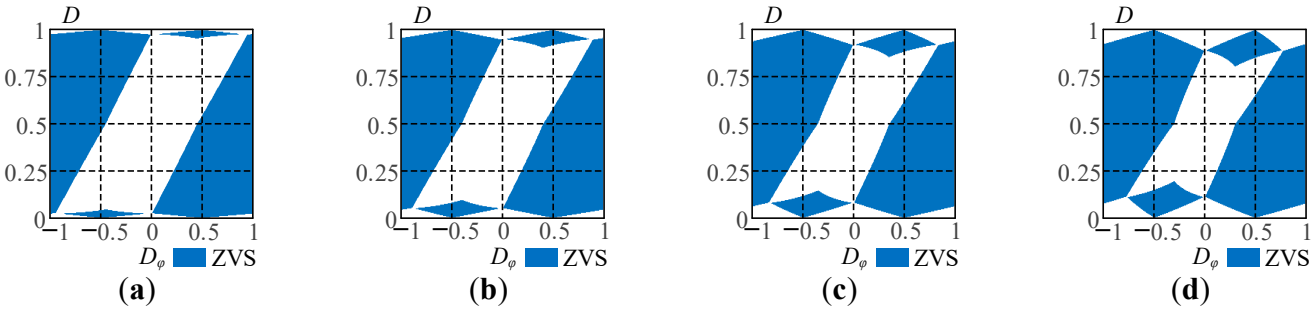

Figure 7. Range of ZVS under the full operational area: (**a**) m = 0.1; (**b**) m = 0.2; (**c**) m = 0.3; (**d**) m = 0.4.

4. Optimal Asymmetric Duty Modulation

4.1. Current Stress Optimization under ZVS

The optimization of current stress using an optimal numerical solution in a discretized domain is based on normalization. Assuming that i^* represents current stress, the equation for current stress under mode A can be derived as:

$$i^* = 2 - 8D + 4D_\varphi + \frac{8D(1-D)}{m} \tag{18}$$

Likewise, current stress under other modes can be determined. So, the current stress is shown in Figure 8 under m = 0.1, m = 0.2, m = 0.3, and m = 0.4, respectively.

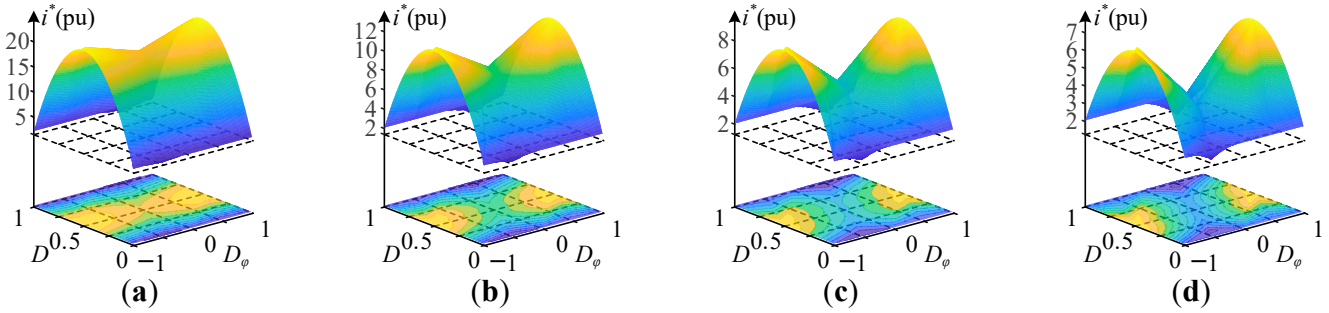

Figure 8. Current stress under the full operational area: (**a**) m = 0.1; (**b**) m = 0.2; (**c**) m = 0.3; (**d**) m = 0.4.

According to Table 2, the current stress under ZVS conditions can be optimized by combining Formulas (18) and (13), given that m has been determined.

However, because of the complexity of the optimization conditions and the numerous requirements, it is hard to solve the optimization problem with analytical methods. The optimal numerical solution of the discretization region can effectively address this problem. The crux of this method is to establish the optimal control table offline, as depicted in Figure 9.

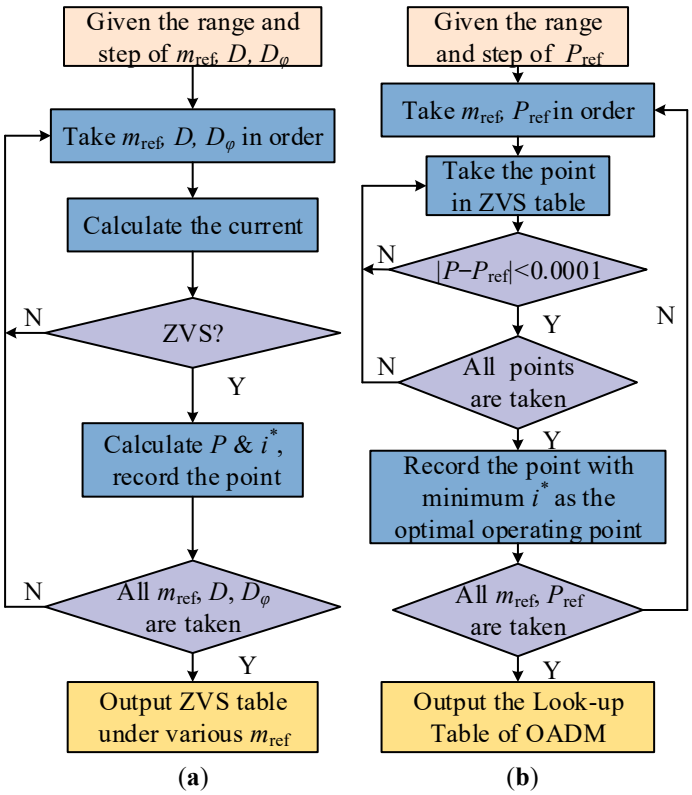

Figure 9. Flow chart of the off-line table-building procedure: (**a**) flow chart of the ZVS table; (**b**) flow chart of the optimal table.

m_{ref} represents the reference voltage ratio, and P_{ref} represents the reference transmission power. They form the basis for establishing and looking up the tables. According to the control accuracy requirements, the table can be established by offline theoretical calculation based on exponential step value. During online table lookups, the algorithm utilizes real-time values of m and P to locate the optimal points within the region centered on m_{ref} and P_{ref}. The output value for the operation is then determined based on this optimal solution. When the values of m_{ref} and P_{ref} are precise enough, the control can be considered approximately equivalent to that of a continuous system.

The basic idea is to find the discrete regional optimal numerical solution in the operating region by traversal. By setting the step size of the control variables, the whole operation area is divided into grids, so that the problem of non-convex optimization is transformed into a problem of numerical comparison. The operating area is discretized into a limited number of points to solve for the transmission power and current stress at each point. The optimal operating point is then determined by comparison. Figure 10 shows a schematic diagram of optimization when m = 0.3, P = 0.4.

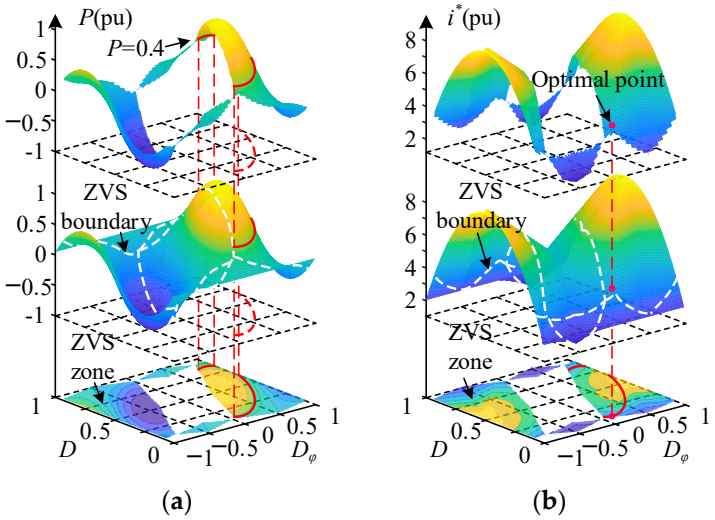

Figure 10. Optimization process of current stress with full ZVS: (**a**) equal power line with full ZVS; (**b**) optimal point.

According to the tabulation method in Figure 9, the online control table of OADM can be obtained using the offline optimization program.

4.2. Control Scheme of OADM

The control scheme of OADM is shown in Figure 11. Based on the theoretical analysis in the previous section, it was found that different voltage ratios and transmission powers result in different optimal operation points with varying values of D and D_φ.

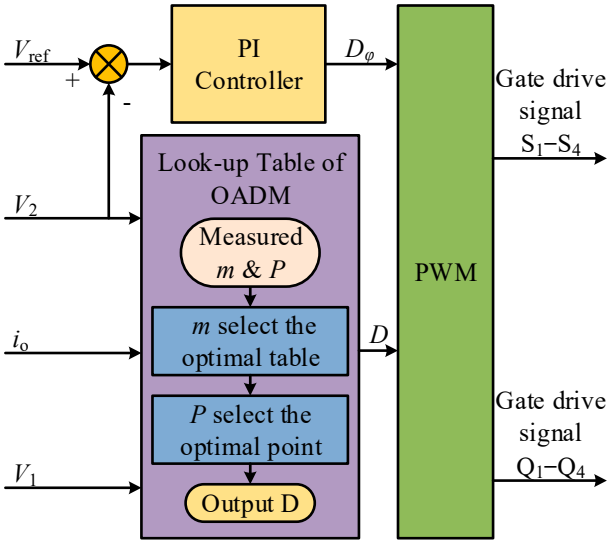

Figure 11. Overall control scheme of OADM.

The overall control scheme contains an outer control loop for output voltage and an inner control loop for efficiency optimization. The outer loop is mainly composed of a PI

controller. Firstly, the measured output voltage V_2 is compared to the set point value V_{ref} and fed into a PI controller to determine the required D_φ. The inner loop is mainly made up of a lookup table for OADM. The lookup table is of utmost importance for efficiency improvement. It directly decides the output value of D and requires actual values of P and m to be calculated through sampling. By combining the actual sampling values with Formula (11), the actual P can be obtained as Formula (19). The measured DC bus voltages V_1 and V_2, and the output current i_o are fed into the lookup table controller to calculate the actual value of P, m. The value of D is determined by comparing the actual value of P, m with the value in the lookup table. The actual value of m will select an optimal table with various values of P. The actual value of P will select the optimal point and output the value of D. The output value of D from the table can limit the current stress of the converter. For robustness, D_φ cannot be directly assigned to the value of the optimal point in the inner control loop from the lookup table but needs to be adjusted by a PI controller. This ensures the reliability of the system during dynamic transitions to a certain extent. With D and D_φ the PWM signal can be generated.

$$P = \frac{V_2 i_o}{P_{\text{N}}} = \frac{4Li_o}{\text{n}V_1 T_{\text{hs}}} \tag{19}$$

D is obtained using the lookup table of the OADM directly, calculating m and P, finding the lookup table of m_{ref} that is closest to the current operation point, and similarly taking the value of P_{ref}. Based on this, the value of D is obtained. To increase the robustness, D_φ cannot be directly assigned to the value of the optimal point in the lookup table but needs to be adjusted by a PI controller. This ensures the reliability of the system during dynamic transitions to a certain extent.

5. Experimental Verification

5.1. Experimental Verification of ADM

The prototype of a DAB converter with DC blocking capacitors was built using TMS320F28335 as the controller, and the practical platform is shown in Figure 12. The switches use 1KW40N120T2. The main parameters of the prototype are shown in Table 3.

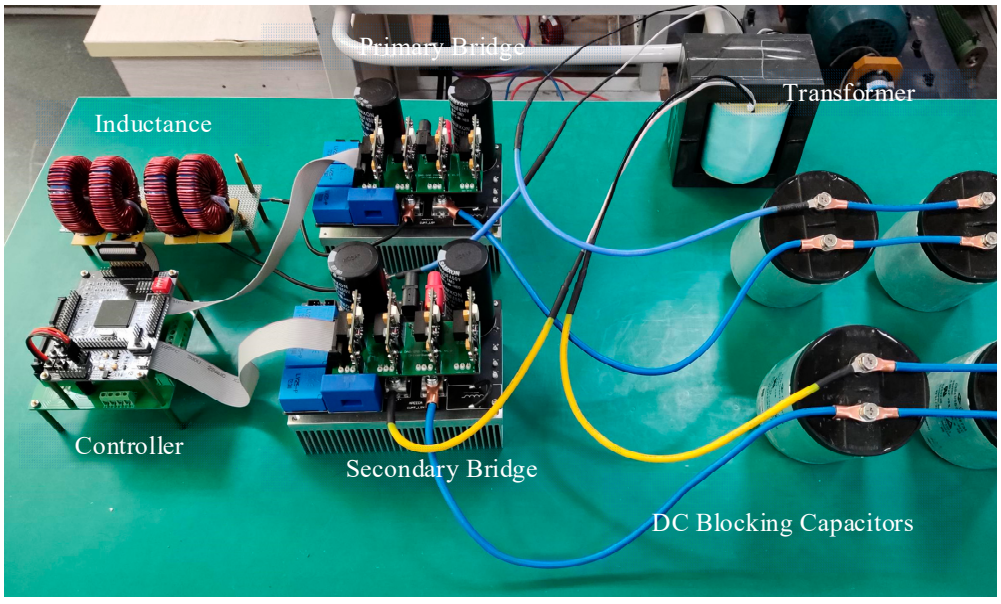

Figure 12. The prototype of a DAB converter with DC blocking capacitors.

Table 3. Parameters of the prototype.

Parameter	Value
Input Voltage V_1/V	200
Turns ratio of transformer n	1:2
Transfer inductor L/μH	269
Blocking capacitors C_{bp}, C_{bs}/μF	1300
Input capacitor C_1/μF	500
Output capacitor C_2/μF	500
Switching frequency f/kHz	10
Switches	1KW40N120T2
Nominal power/W	915.36

The DC blocking capacitors are the key to the modulation. This is different from *LC* resonance, and the capacitors will cause voltage ripple when it is charged and discharged. If they are too small, the voltage ripple will be large. So, the capacitors should satisfy:

$$f > \frac{1}{2\pi\sqrt{LC_{bp}}} \tag{20}$$

Therefore, two 650 μF capacitors in parallel are selected in this paper, that is, C_{bs} = 1300 μF and C_{bp} = 1300 μF.

Figure 13 is the experimental waveform of mode A under the ADM when D_φ = 0.4 and V_2 = 120 V. As indicated in Figure 13, when D_φ is the same under mode A, transmission power changes accordingly as the duty cycle increases. Its trend is consistent with theoretical power transmission characteristics in Figure 6b.

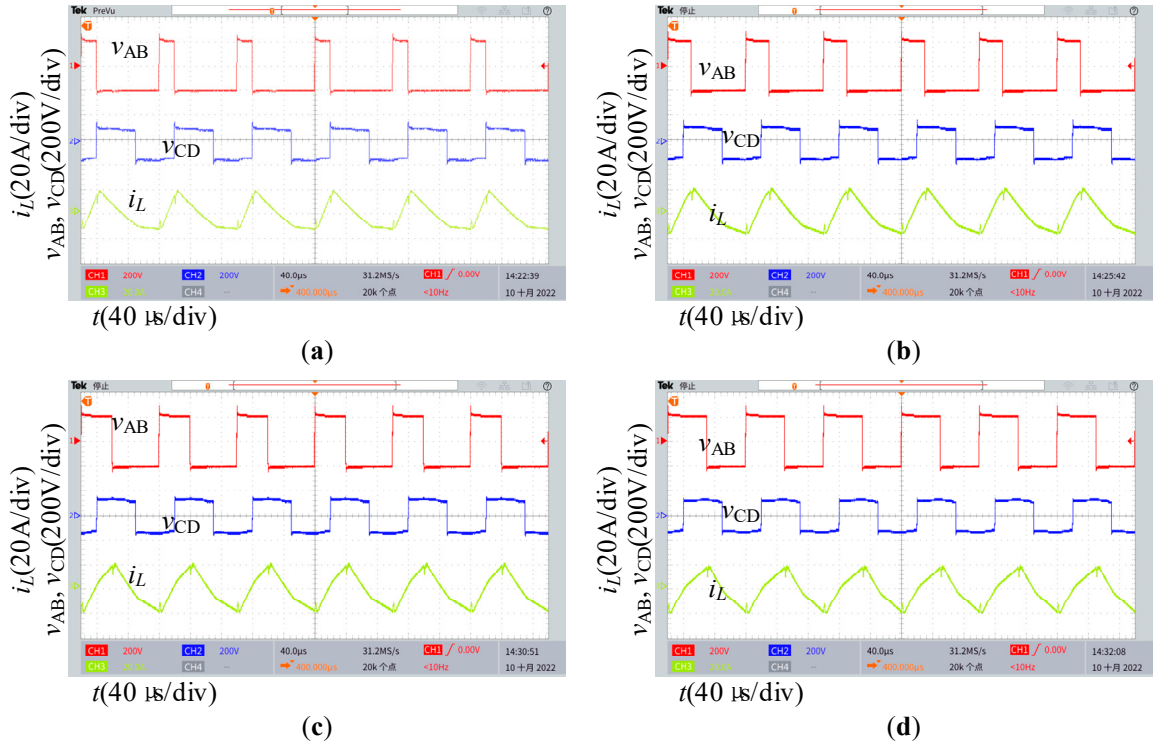

Figure 13. Waveforms of mode A with the same phase shift: (**a**) D = 0.2 (P = 0.465); (**b**) D = 0.3 (P = 0.782); (**c**) D = 0.4 (P = 0.952); (**d**) D = 0.5 (P = 0.948).

Figure 14 is the experimental waveform under mode A when D = 0.4 and V_2 = 120 V. As indicated, when D is the same, changes in transmission power are also consistent with the theoretical transmission power characteristics in Figure 6b.

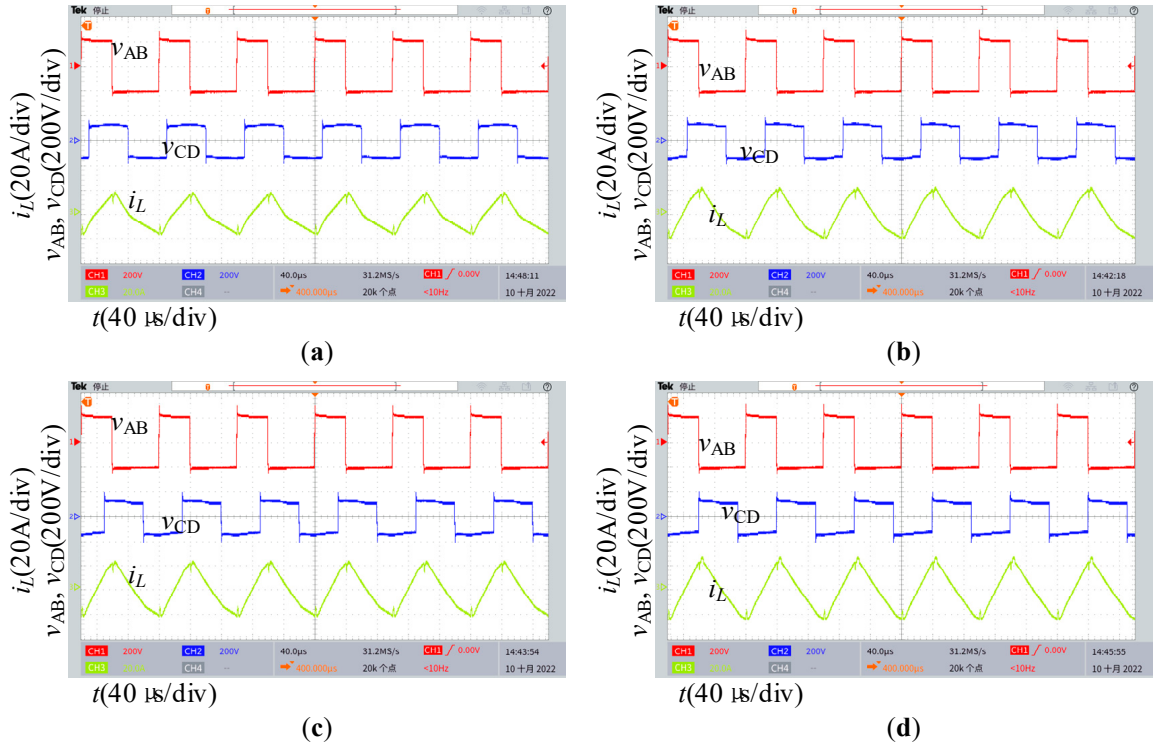

Figure 14. Waveforms of mode A with the same duty cycle: (**a**) D_φ = 0.2 (P = 0.776); (**b**) D_φ = 0.5 (P = 0.914); (**c**) D_φ = 0.6 (P = 0.784); (**d**) D_φ = 0.8 (P = 0.287).

Figure 15 shows the experimental waveform under the ADM when P = 0.76, V_2 = 120 V, and m = 0.3. As shown in Figure 15, different combinations of D and D_φ can transmit the same power, thereby confirming the feasibility of optimization.

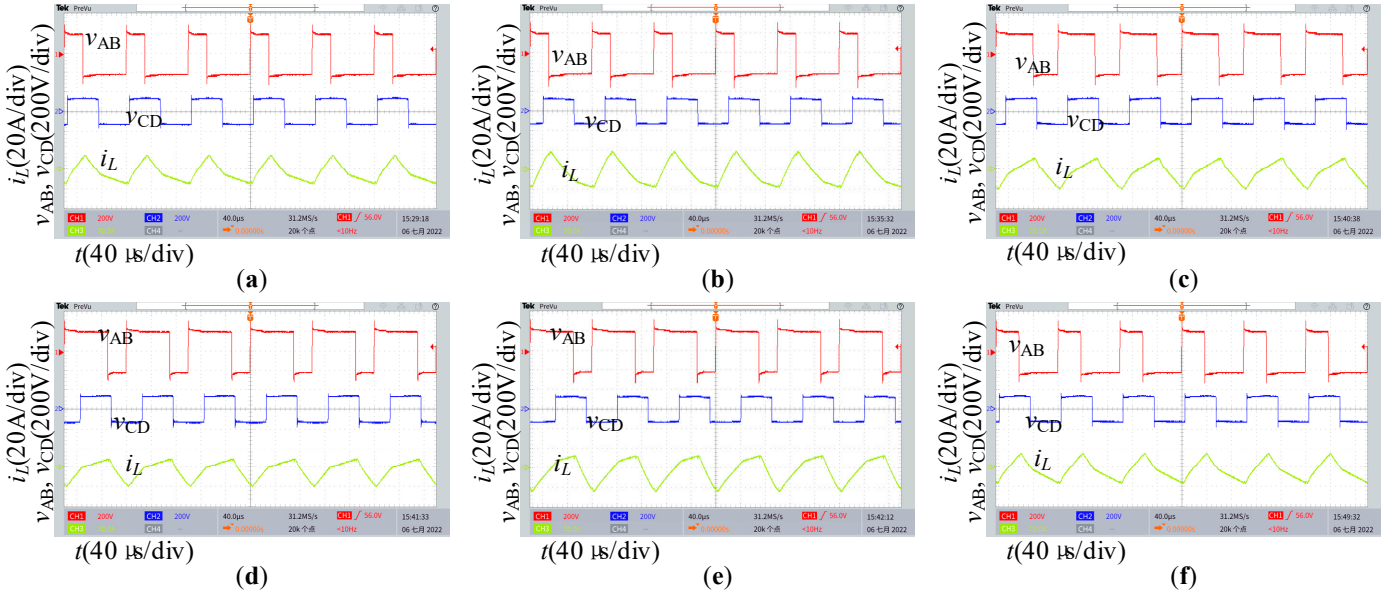

Figure 15. Waveforms of P = 0.76: (**a**) D = 0.31, D_φ = 0.09; (**b**) D = 0.31, D_φ = 0.42; (**c**) D = 0.61, D_φ = 0.31; (**d**) D = 0.69, D_φ = 0.51; (**e**) D = 0.71, D_φ = 0.82; (**f**) D = 0.37, D_φ = 0.11.

By adding D in the experiment, it was possible to obtain equal transmission power lines for different transmission powers in the entire operating region, which is consistent with the theoretical derivation in Figure 10a.

As shown in Figure 16, experiments were carried out at grid points, and the transmission power of each point was measured to obtain the forward transmission power characteristics. D and D_φ were varied from 0.1 to 0.9 and 0 to 1, respectively, with equal steps of 0.1. By comparing the experimental transmission power curve in Figure 16 with the theoretical transmission power curve in Figure 6b, it was found that the correctness of the transmission power equations for different modes was verified.

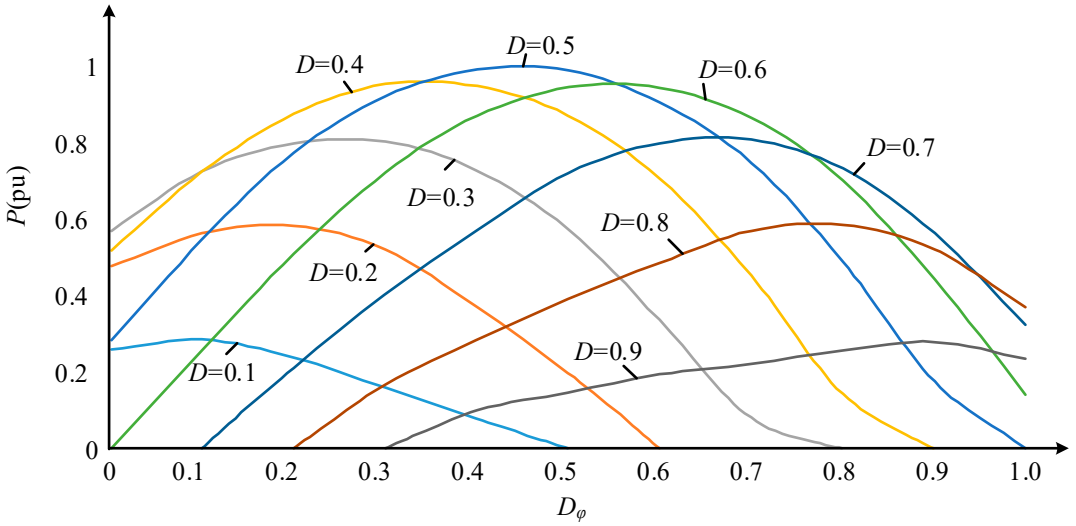

Figure 16. Curves of transmission power under ADM control.

Based on Figures 13–15, when the duty cycle or phase shift ratio is the same, DAB converters under the ADM based on DC blocking capacitors can transmit different powers. To obtain the power reverse characteristic, only input and output ports need to be exchanged. Furthermore, the curves for forward and backward power transmissions are symmetric, indicating that the experimental curve is consistent with the theory.

5.2. Experimental Verification of OADM

To verify the correctness of the theory, the OADM is compared with SPS control and DPS control with the same transmission power. Figure 17 compares the experimental waveforms at m = 0.1, m = 0.2, m = 0.3, and m = 0.4.

Figure 17 demonstrates that the controller can obtain the optimal operating point for different working states by referencing the lookup table. The OADM is effective in reducing current stress when m is relatively low, and the power devices S_2 and S_3 on the primary side are somewhat limited by parasitic parameters. However, the current approaches zero when the soft switch turns on. For the other voltage ratios in the experiment, the same transmission power as those of SPS and DPS control is achieved while ensuring ZVS for all power devices and effectively controlling current stress.

As shown in Figure 17, the converter has difficulty realizing ZVS for the full power range with SPS. Since there are no additional control degrees of freedom for optimization, the current stress is large and appears as a near triangle when the voltage ratio $m \leq 0.5$. Under this condition, such a current makes it difficult to achieve ZVS, which cannot quickly reverse the current between switching. DPS control, compared to SPS control, has an additional control degree of freedom and lighter current stress. However, due to the lack of multi-objective consideration in the optimization, the ZVS is hard to achieve at a light load. The OADM control proposed in this paper also has two control degrees of freedom, which optimizes the current stress and takes ZVS into account at the same time. It is a multi-objective optimization. Compared with DPS under light load conditions of $m \leq 0.5$, it has advantages in the realization of current stress reduction and full ZVS. In contrast to DPS, the inductor current of OADM has unequal positive and negative peaks, making it

less intuitive to compare with DPS control. To address this, the root mean square (RMS) of the inductor current is added to this experiment. The experimental results confirm the effectiveness of the proposed OADM.

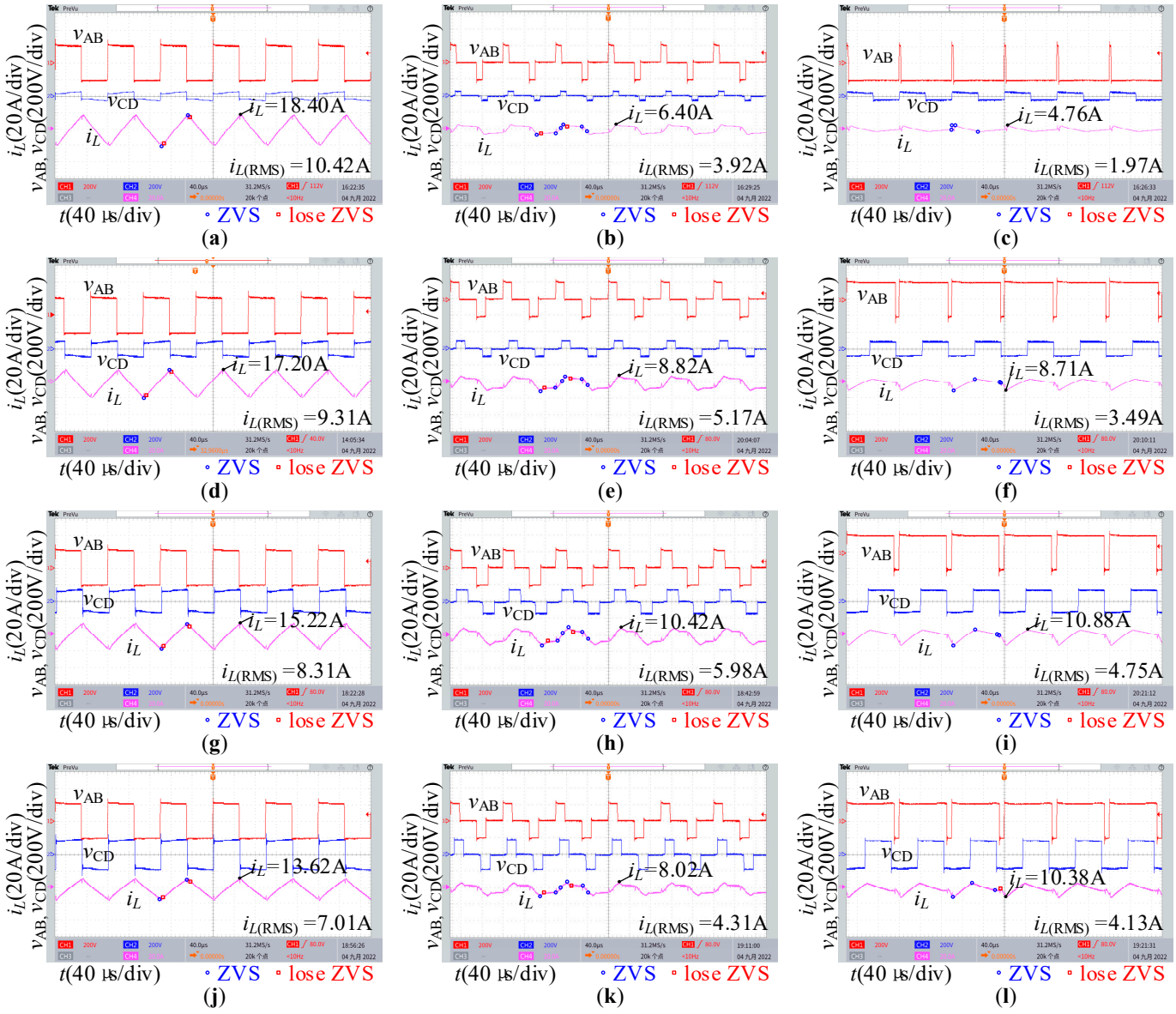

Figure 17. Waveforms of three different strategies: (**a**) SPS (m = 0.1, P = 0.11); (**b**) DPS (m = 0.1, P = 0.11); (**c**) OADM (m = 0.1, P = 0.11); (**d**) SPS (m = 0.2, P = 0.22); (**e**) DPS (m = 0.2, P = 0.22); (**f**) OADM (m = 0.2, P = 0.22); (**g**) SPS (m = 0.3, P = 0.31); (**h**) DPS (m = 0.3, P = 0.31); (**i**) OADM (m = 0.3, P = 0.31); (**j**) SPS (m = 0.4, P = 0.18); (**k**) DPS (m = 0.4, P = 0.18); (**l**) OADM (m = 0.4, P = 0.18).

Figure 18 shows the efficiency curves under SPS control, DPS current stress optimization control, and the OADM at different m with P = 0.36. As shown, the two-degrees-of-freedom modulation provides flexibility for efficiency optimization, resulting in greater efficiency improvements compared to SPS control. Moreover, the proposed OADM is even more efficient than DPS with the same degrees of control freedom.

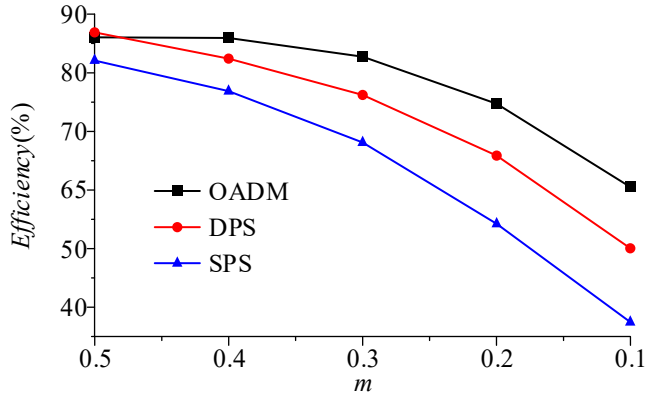

Figure 18. Efficiency curves of three different strategies.

It is worth noting that the efficiency of the DAB converter is low when there is a significant voltage deviation. The proposed OADM can improve efficiency under these conditions, thus enhancing adaptability to a wide range of voltages.

6. Conclusions

By applying DC bias to the DC blocking capacitors, the proposed ADM provides a new method of optimization. With a detailed derivation of the operation of a DAB converter with DC blocking capacitors under ADM, the eight operating modes of the converter are analyzed based on theoretical considerations, and the relationship between the control variables and the transmission power is investigated for each mode. By studying the boundary conditions of ZVS for each power device of the converter, an OADM is proposed that ensures full ZVS in the range of voltage ratio $m \leq 0.5$ and effectively reduces the current stress of the system. The proposed OADM is optimized using numerical methods, and experimental results confirm its effectiveness. Specifically, when the voltage ratio is low, the OADM can modify the bias to compensate for it, allowing the DAB to maintain consistent performance. It can increase efficiency by 3.58%, 6.57%, 8.81%, and 10.33% compared with DPS when P is equal to 0.36 and m is equal to 0.4, 0.3, 0.2, and 0.1, respectively.

Overall, this approach provides greater flexibility and robustness for DAB, which may be especially valuable in applications where voltage levels can vary widely. With the increasing demand for high-efficiency photovoltaic converters and on-board chargers (OBCs), the OADM proposed in this paper offers more opportunities for pursuing higher efficiency.

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