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# A Fault-Tolerant Control Strategy for Three-Level Grid-Connected NPC Inverters after Single-Arm Failure with Optimized SVPWM

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**Abstract:** Three-level NPC inverters have been widely used in grid-connected systems due to their superior performance compared with two-level inverters, but more switches lead to high fault probability. Meanwhile, the neutral point potential (NPP) fluctuation of the DC link is an inherent problem of three-level NPC inverters. To keep the three-level NPC inverter running stably after single-arm failure, a fault-tolerant control strategy based on an optimised space vector pulse width modulation (SVPWM) is proposed in this paper. Firstly, the common-mode voltage (CMV) of the postfault three-level NPC inverter is analysed and then the preliminary synthesis principles of the reference voltage vector are determined. Then, in order to ensure the NPP balance and the quality of the grid-connected currents, the reference voltage vector synthesis rules are optimised, a low-pass filter (LPF) and a hysteresis comparator are designed, respectively, to ensure the quality of grid-connected currents and effectively decrease the DC link NPP deviation. Finally, the simulation results show that the proposed fault-tolerant control strategy can realize the stable and reliable operation of the grid-connected three-level NPC inverter after single-arm failure, and the CMV can be reduced significantly, the quality of grid-connected currents is also improved. The proposed fault-tolerant strategy also shows good performance when the grid-connected currents change.

**Keywords:** NPC inverter; fault-tolerant control; neutral point potential (NPP) fluctuation; SVPWM optimisation compensation; low pass filter; hysteresis comparator



**Citation:** Huang, J.; Bai, F.; Yang, Q.; Ren, S. A Fault-Tolerant Control Strategy for Three-Level Grid-Connected NPC Inverters after Single-Arm Failure with Optimized SVPWM. *Energies* **2023**, *16*, 7863. https://doi.org/10.3390/en16237863

Academic Editor: Ahmed Abu-Siada

Received: 21 September 2023
Revised: 23 November 2023
Accepted: 28 November 2023
Published: 30 November 2023



## 1. Introduction

The three-phase three-level neutral point clamped (NPC) grid-connected inverters can simplify the design of filter because their outputs are close to sine waves compared with the two-level inverters. Therefore, they have been widely used in grid-connected systems [1,2]. However, the failure probability of the three-level NPC inverters increases with the multiplied number of power semiconductor devices [3–5]. To ensure sustainable operation of the three-level NPC grid-connected inverters when there is a short-circuit or open-circuit on the bridge arm of a certain phase, it is crucial to conduct thorough research on grid-connected control of the inverters after single-arm failure.

When the single-arm of inverter is failure, fault-tolerant control proves to be an efficient method to ensure uninterrupted operation of the system. In the case of three-level NPC inverters, common fault-tolerant topologies include three-phase four-bridge arm fault-tolerant topologies [6,7], switching redundancy topologies [8,9], ANPC fault-tolerant topologies [10,11], and eight-switch three-phase fault-tolerant topologies [12,13], etc. In this paper, considering the cost, volume and control complexity, the eight-switch three-phase inverters (ESTPIS) are the topology for postfault three-phase three-level NPC grid-connected inverters.

For three-level NPC grid-connected inverters, the fluctuation of neutral point potential (NPP) can be a source of concern. This problem will not only increase the content of low-order harmonics in grid-connected currents, but also cause distortion in the inverter's

output voltage and create additional stress on the switch. When the NPP fluctuation is particularly severe, it can even impact the lifespan of DC-link capacitors, as noted in [14]. As a result, ESTPI as the fault-tolerant topology still has the issue of NPP fluctuation. For three-level NPC inverters, the virtual voltage vector pulse width modulation technique (VSVPWM) is utilized to synthesize the virtual vector to restrain the fluctuation of the NPP. In [15,16], the distribution coefficients of each basic vector in the virtual vector are recalculated to suppress the fluctuation of the NPP. However, the space voltage vectors of ESTPI no longer contain redundant voltage vectors [17], therefore the multi-vector method of suppressing NPP fluctuation is limited. It is also possible to control the NPP by setting the cost function through model predictive control, but there are challenges in selecting the NPP error weight factor, the filtering complexity, and high sampling frequency requirements [18,19]. For ESTPI, the space vector pulse width modulation (SVPWM) technology can be used to control the NPP. In [20], the control effect of two different SVPWM strategies on NPP is analysed under different voltage vector selections. In [21], the SVPWM avoids using the voltage vectors with high CMV and reduces the CMV while suppressing NPP fluctuation. In [22], due to the lack of redundant vectors, a proportional moving average filter controller is used to extract the DC component of the neutral voltage to modify the duty cycle of the basic voltage vector and achieve the balance of the NPP. As described above, the traditional SVPWM must be improved to suppress the NPP fluctuation of the ESTPI. Hence, this study focuses on fault-tolerant control of three-level NPC inverters after single-arm failure based on SVPWM. The research examines the mechanism of NPP fluctuation of DC-link bus capacitors after a single-arm failure, optimises space vector modulation to decrease the common-mode voltage (CMV) and adequately compensates for the distortion of the grid-connected currents caused by NPP fluctuation.

In summary, this paper analyses the fault-tolerant control based on space vector modulation technology for the ESTPI. Firstly, the research selects a vector synthesis order rule to minimise the CMV. Moreover, the mechanism of NPP fluctuation is analysed and a compensation value for the reference voltage vector synthesis link is designed through a low-pass filter and hysteresis controller. Thus, the quality of the grid-connected currents of ESTPI is improved. Finally, the effectiveness of the proposed control strategy is verified by simulation.

## 2. ESTPI Fault Topology and Mechanism of NPP Fluctuation

### *2.1. The Space Voltage Vector of ESTPI Topology*

This work discusses the fault-tolerant topology of three-level NPC inverters, which is shown in Figure 1. The system comprises a DC-link voltage ($V_{dc}$), as well as two capacitors $C_1$ and $C_2$, whose voltages are $u_p$ and $u_n$, respectively. Point O denotes the neutral point of the DC bus, and $i_{la}$, $i_{lb}$, and $i_{lc}$ are the output currents of three-level NPC inverters. For three-level NPC inverters, there are four power semiconductor devices ($S_{x1}$, $S_{x2}$, $S_{x3}$, $S_{x4}$), two clamped diodes, a bidirectional thyristor ($T_1$, $T_2$, $T_3$) and two fast-acting fuses (FU) on each phase bridge arm.

Due to the three-phase symmetry, only phase A faults are analysed as an example. As shown in Figure 1, when phase A fails, the fast-acting fuse on phase A is disconnected, and the bidirectional thyristor on phase A is activated, thus, the output current of phase A is the NP current of the DC bus. The other two normal arms of ESTPI have three states, including *P*, *O*, and *N*. The switching function is defined as follows:

$$S_x = \begin{cases} 1(P), S_{x1}, S_{x2}\ on, S_{x3}, S_{x4}\ off \\ 0(O), S_{x2}, S_{x3}\ on, S_{x1}, S_{x4}\ off \quad (x = a, b, c) \\ -1(N), S_{x3}, S_{x4}\ on, S_{x1}, S_{x2}\ off \end{cases} \tag{1}$$

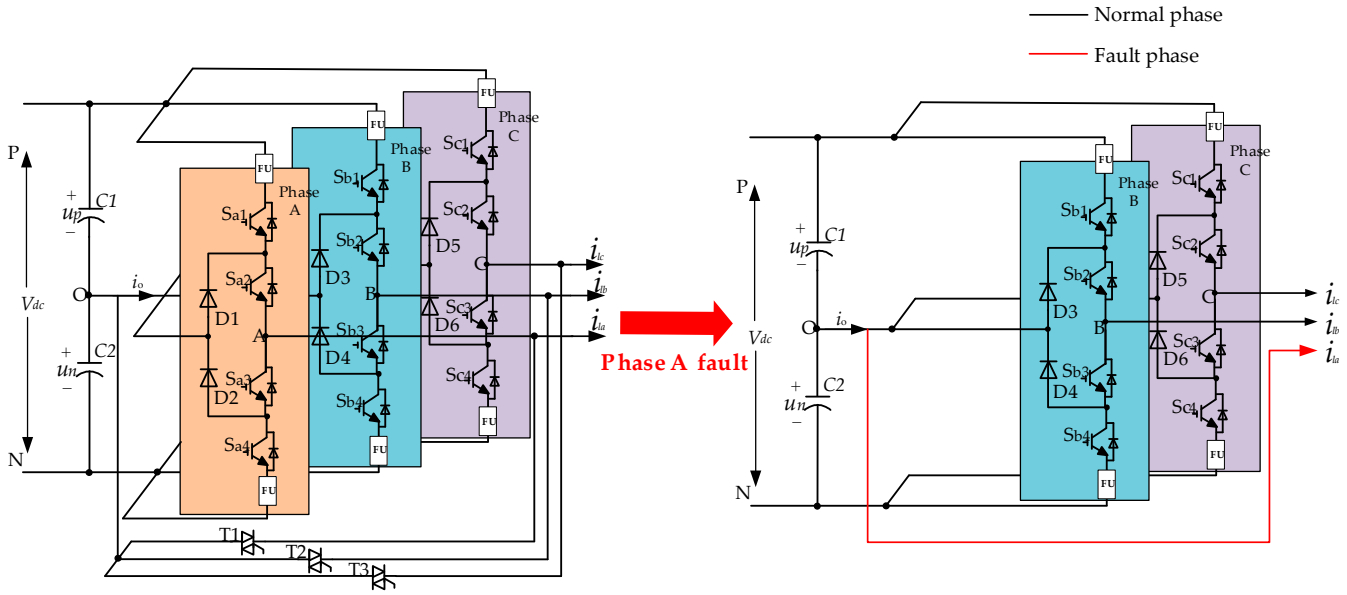



**Figure 1.** Fault-tolerant topology of three-level NPC inverter.

Due to phase A failure, it can only output *O* state. The operating modes of the three-phase three-level NPC inverters have 27 combinations, the failure of phase A restricts it to only nine combinations, as shown in Figure 2. In Figure 2b, the ESTPI topology space vector diagram can be divided into six sectors, labelled as I to VI. Sectors II and V contain medium voltage vectors that can be further divided into two subsectors. The overall space voltage vector distribution still satisfies the synthesis conditions of the reference voltage vector.

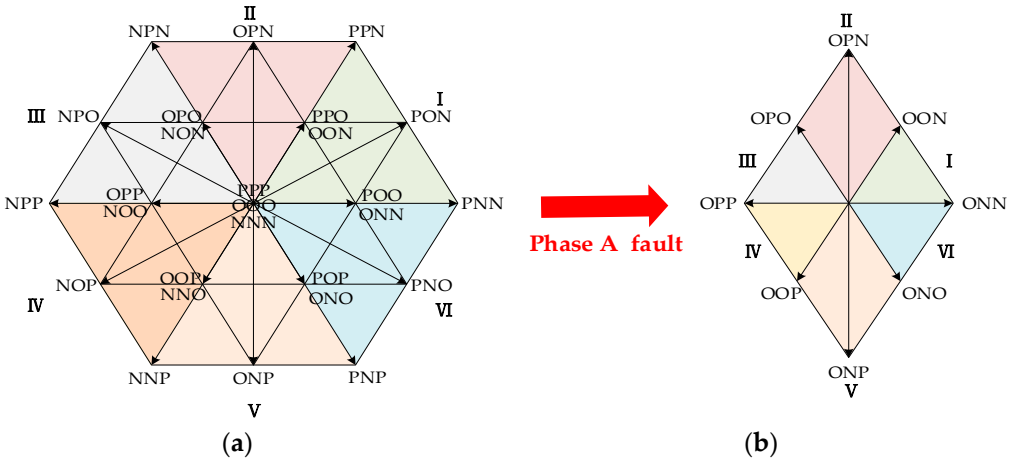



**Figure 2.** The space voltage vector distribution: (**a**) The space voltage vector distribution of a three-level NPC inverter; (**b**) The space voltage vector distribution of ESTPI.

Due to the change in space voltage vector distribution, there are only nine available vectors to ensure the operation of ESTPI, the reference voltage synthesis method must be redesigned. To minimize the low-frequency oscillation caused by the CMV, it is necessary to analyse the CMV generated by each voltage vector.

The output voltage of the ESTPI can be obtained as follows:

$$\begin{cases} u_{ao} = 0 \\ u_{bo} = S_b \times \frac{V_{dc}}{2} \\ u_{co} = S_c \times \frac{V_{dc}}{2} \end{cases} \tag{2}$$

where $S_b$, $S_c$ are defined by Formula (1). The CMV is expressed as follows:

$$u_{cm} = \frac{u_{ao} + u_{bo} + u_{co}}{3} \tag{3}$$

From Formulas (1)–(3), the CMV of each basic voltage vector is shown in Table 1.

**Table 1.** The CMV corresponds to the space vectors.

| Voltage Vector Type | Voltage Vector | Common-Mode Voltage |
|---|---|---|
| Zero voltage vector | OOO | 0 |
| Small voltage vectors | OPP | $V_{dc}/3$ |
| | ONN | $-V_{dc}/3$ |
| | OPO, OOP | $V_{dc}/6$ |
| | OON, ONO | $-V_{dc}/6$ |
| Medium voltage vectors | OPN, ONP | 0 |

As indicated in Table 1, small voltage vectors will generate the CMV, and the CMV of zero voltage vector and medium voltage vectors are zero. Traditional SVPWM relies solely on small voltage vectors to synthesize reference voltage vectors for ESTPI, so the CMV is great. In this paper, the medium voltage vectors in sectors II and V are incorporated into the synthesis of reference voltage vectors to reduce CMV. This approach of introducing medium voltage vectors effectively reduces the proportion of the small voltage vectors in the reference voltage vector synthesis, ultimately leading to the decrease in CMV.

In order to optimize computational efficiency, the synthesis of the reference voltage vector and the calculation of the duration time of the voltage vector are executed within the 60° (g-h) coordinate systems. In sector I, the duration time can be computed by the following means.

In Figure 3, $V_{ref}$ is the reference voltage vector synthesized by $V_0$, $V_1$, and $V_2$, $a_1$ is the equivalent vector of $V_2$ with duration $t_2$ in one modulation cycle. $b_1$ is the equivalent vector of $V_1$ with duration $t_1$ in one modulation cycle. The modulation index is defined as follows:

$$m = \frac{\sqrt{3} \times V_{ref}}{V_{dc}} \tag{4}$$

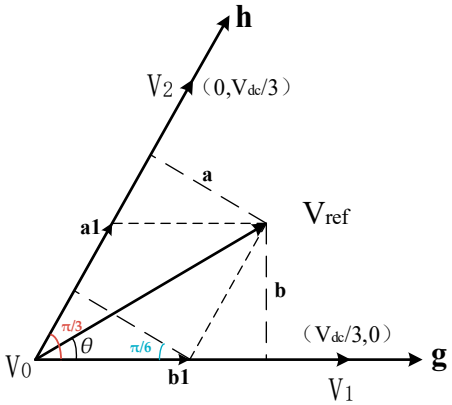



**Figure 3.** Synthesis of $V_{ref}$ in Sector I.

The vector duration time $t_1$ and $t_2$ can be obtained as follows:

$$\begin{cases} b_1 = V_1 \times \frac{t_1}{T_s} \\ V_1 = V_{dc}/3 \\ a = V_{ref} \times \sin\left(\frac{\pi}{3} - \theta\right) \\ a/b_1 = \cos\left(\frac{\pi}{6}\right) \end{cases} \Rightarrow t_1 = \frac{b_1 T_s}{V_1} = \frac{aT_s}{V_1 \times \cos\left(\frac{\pi}{6}\right)} = \frac{2T_s V_{ref} \times \sin\left(\frac{\pi}{3} - \theta\right)}{\sqrt{3} \times \frac{V_{dc}}{3}} = 2mT_s \sin\left(\frac{\pi}{3} - \theta\right) \tag{5}$$

$$\begin{cases} a_1 = V_2 \times \frac{t_2}{T_s} \\ V_2 = V_{dc}/3 \\ b = V_{ref} \times \sin(\theta) \\ b/a_1 = \sin\left(\frac{\pi}{3}\right) \end{cases} \Rightarrow t_2 = \frac{a_1 T_s}{V_2} = \frac{bT_s}{V_2 \times \sin\left(\frac{\pi}{3}\right)} = \frac{2T_s V_{ref} \times \sin(\theta)}{\sqrt{3} \times \frac{V_{dc}}{3}} = 2mT_s \sin(\theta) \quad (6)$$

The calculation of the vector duration time of other sectors is similar. The vector duration time and the synthesis rules for reference voltage are shown in Tables 2 and 3.

**Table 2.** Vector duration time and corresponding NP current.

| N | n | $t_1$ (s) | Vector $V_1$ | $i_{o1}$ (A) | $t_2$ (s) | Vector $V_2$ | $i_{o2}$ (A) |
|---|---|---|---|---|---|---|---|
| I | / | $2mT_s\sin(\pi/3-\theta)$ | ONN | $i_{la}$ | $2mT_s\sin(\theta)$ | OON | $-i_{lc}$ |
| II | 1 | $2\sqrt{3}mT_s\cos(\theta)$ | OON | $-i_{lc}$ | $-2mT_s\sin(\pi/3-\theta)$ | OPN | $i_{la}$ |
| II | 2 | $-2\sqrt{3}mT_s\cos(\theta)$ | OPO | $-i_{lb}$ | $2mT_s\sin(\pi/3+\theta)$ | OPN | $i_{la}$ |
| III | / | $2mT_s\sin(\theta)$ | OPO | $-i_{lb}$ | $-2mT_s\sin(\pi/3+\theta)$ | OPP | $i_{la}$ |
| IV | / | $-2mT_s\sin(\pi/3-\theta)$ | OPP | $i_{la}$ | $-2mT_s\sin(\theta)$ | OOP | $-i_{lc}$ |
| V | 1 | $-2\sqrt{3}mT_s\cos(\theta)$ | OOP | $-i_{lc}$ | $2mT_s\sin(\pi/3-\theta)$ | ONP | $i_{la}$ |
| V | 2 | $2\sqrt{3}mT_s\cos(\theta)$ | ONO | $-i_{lb}$ | $-2mT_s\sin(\pi/3+\theta)$ | ONP | $i_{la}$ |
| VI | / | $-2mT_s\sin(\theta)$ | ONO | $-i_{lb}$ | $2mT_s\sin(\pi/3+\theta)$ | ONN | $i_{la}$ |

N, n, $T_s$, and $m$ represent the large sector in the basic voltage vector diagram, the subsector within the large sector, the modulation period, and the modulation index. The maximum linear modulation range corresponds to $m$ = 1. In this paper, $m = \sqrt{3}V_{ref}/V_{dc}$, $V_{ref}$ is the reference voltage produced by the grid-connected controller, and $V_{dc}$ is the DC bus voltage. $t_1$ and $t_2$ are the duration of vectors $V_1$ and $V_2$, respectively. $i_{o1}$ and $i_{o2}$ are the corresponding NP currents with $V_1$ and $V_2$, respectively, and the current flowing out of the NP is considered to be in the positive direction. The reference voltage vector can be synthesized with $V_1$, $V_2$, and the zero vector ($V_0$). The duration time of $V_0$ is $t_0 = T_S - t_1 - t_2$.

**Table 3.** Vector sequences of the SVPWM strategy.

| N | N | Vector Sequences | |
|---|---|---|---|
| I | / | OOO-OON-ONN-OON-OOO | $V_0$-$V_2$-$V_1$-$V_2$-$V_0$ |
| II | 1 | OOO-OON-OPN-OON-OOO | $V_0$-$V_1$-$V_2$-$V_1$-$V_0$ |
| II | 2 | OOO-OPO-OPN-OPO-OOO | $V_0$-$V_1$-$V_2$-$V_1$-$V_0$ |
| III | / | OOO-OPO-OPP-OPO-OOO | $V_0$-$V_1$-$V_2$-$V_1$-$V_0$ |
| IV | / | OOO-OOP-OPP-OOP-OOO | $V_0$-$V_2$-$V_1$-$V_2$-$V_0$ |
| V | 1 | OOO-OOP-ONP-OOP-OOO | $V_0$-$V_1$-$V_2$-$V_1$-$V_0$ |
| V | 2 | OOO-ONO-ONP-ONO-OOO | $V_0$-$V_1$-$V_2$-$V_1$-$V_0$ |
| VI | / | OOO-ONO-ONN-ONO-OOO | $V_0$-$V_1$-$V_2$-$V_1$-$V_0$ |

### *2.2. The NPP Fluctuant Mechanism of DC Bus*

According to Tables 2 and 3, it is possible to obtain synthesis rules for the reference voltage vector. Therefore, the NP current during one fundamental period can be analysed. Assuming three-phase symmetry,

$$\begin{cases} i_{la} = I_m \cos(\theta - \varphi) \\ i_{lb} = I_m \cos(\theta - \varphi - \frac{2\pi}{3}) \\ i_{lc} = I_m \cos(\theta - \varphi + \frac{2\pi}{3}) \end{cases} \quad (7)$$

where $i_{la}$, $i_{lb}$, and $i_{lc}$ are the output current of ESTPI, $I_m$, and $\varphi$ denotes the amplitude of the phase current and the power factor angle, respectively. Due to the modulation period being short, it is assumed that the current remains constant in a modulation period. Moreover, since the NP current is not affected by the zero voltage vector, the NP current during each modulation period can be represented by the NP current with $V_1$ and $V_2$. The principle of area equivalence is expressed as follows:

$$i_o \times T_s = i_{o1} \times t_1 + i_{o2} \times t_2 \quad (8)$$

where $i_o$, $T_S$ are the NP current of the DC bus and the modulation period, respectively. $i_{o1}$, $i_{o2}$ are the corresponding NP current with $V_1$ and $V_2$. $t_1$, $t_2$ are the duration time of $V_1$ and $V_2$, respectively. $i_{o1}$, $i_{o2}$, $t_1$ and $t_2$ can be obtained in Table 2.

Combine Table 2, Formulas (7) and (8), the NP current of the DC bus is expressed as follows:

$$i_o = \begin{cases} \sqrt{3}mI_m\cos\varphi & 0 \leqslant \theta < \frac{\pi}{3}, \text{(Sector I)} \\ mI_m[2\sin(2\theta-\varphi)-\sin(\varphi)] & \frac{\pi}{3} \leqslant \theta < \frac{\pi}{2}, \text{ (Sector II)} \\ mI_m[2\sin(2\theta-\varphi)-\sin(\varphi)] & \frac{\pi}{2} \leqslant \theta < \frac{2\pi}{3}, \text{(Sector II)} \\ -\sqrt{3}mI_m\cos(\varphi) & \frac{2\pi}{3} \leqslant \theta < \pi, \text{ (Sector III)} \\ -\sqrt{3}mI_m\cos(\varphi) & \pi \leqslant \theta < \frac{4\pi}{3}, \text{ (Sector IV)} \\ -mI_m[2\sin(2\theta-\varphi)-\sin(\varphi)] & \frac{4\pi}{3} \leqslant \theta < \frac{3\pi}{2}, \text{(Sector V)} \\ -mI_m[2\sin(2\theta-\varphi)-\sin(\varphi)] & \frac{3\pi}{2} \leqslant \theta < \frac{5\pi}{3}, \text{(Sector V)} \\ \sqrt{3}mI_m\cos(\varphi) & \frac{5\pi}{3} \leqslant \theta \leqslant 2\pi, \text{(Sector VI)} \end{cases} \tag{9}$$

Formula (9) shows that the NP current has half-wave symmetry, that is $i_o(\theta) = -i_o(\theta+\pi)$. This means that the average value of NP current is zero during one fundamental cycle, and the NPP of the DC bus can remain balance. Further, by using Fourier decomposition on Formula (9) can obtain:

$$\begin{cases} a_0 = 0 \\ a_1 = \frac{mI_m\sqrt{16+384\cos^2(\varphi)}}{3\pi} \\ a_2 = 0 \\ a_3 = \frac{8\sqrt{3}mI_m\cos(\varphi)}{3\pi} \\ \vdots \end{cases} \tag{10}$$

where $a_0$, $a_1$, $a_2$, and $a_3$ correspond to the DC component, the fundamental component, the second harmonic component, and the third harmonic component, respectively. As shown in Formula (10), the NP current only contains odd harmonic waves. Thus, the NPP variation can be succinctly expressed as follows:

$$\begin{aligned} \frac{\Delta u}{V_{dc}} &= \frac{(u_p-u_n)}{2V_{dc}} = \frac{\int i_o dt}{V_{dc}\times 2C} \\ &= \frac{2mI_m\sqrt{1+24\cos^2(\varphi)}}{V_{ref}3\pi C\omega}\sin(\omega t-\zeta_1) + \sum_{n=3,5,7}^{\infty}\frac{A_n}{2V_{dc}Cn\omega}\sin(n\omega t-\zeta_n) \end{aligned} \tag{11}$$

where $\Delta u = \frac{(u_p-u_n)}{2}$ is the NPP fluctuation of the DC bus, and $\zeta_n$ ($n = 3, 5, 7\ldots$) is the initial phase of the NPP corresponding to the $n$th harmonic current. C is the DC-link capacitance, and $A_n$ is the $n$th harmonic current component. Combined with Formulas (9) and (11), under the condition of ESTPI, it can be seen that the NPP of the DC bus fluctuates with the fundamental wave frequency. The fluctuation primarily stems from the capacitance of the DC-link capacitor, as well as the amplitude and phase of the grid-connected currents, and modulation depth.

## 3. SVPWM Compensation and Optimization

### *3.1. SVPWM Compensation Strategy Considering NPP Fluctuation*

By analysing the output level status of the ESTPI, the ESTPI output voltage considering the fluctuation of the NPP can be obtained as follows:

$$\begin{cases} u_{ao} = 0 \\ u_{bo} = S_b \times \frac{V_{dc}}{2} + |S_b| \times \Delta u \\ u_{co} = S_c \times \frac{V_{dc}}{2} + |S_c| \times \Delta u \end{cases} \tag{12}$$

where, $u_{ao}$, $u_{bo}$, and $u_{co}$ are the ESTPI output voltages of phases A, B, and C, respectively. $\Delta u$ is the NPP fluctuation of the DC bus. Therefore, the space voltage vector is expressed as follows:

$$u_s = \frac{2}{3}\left(u_{ao} + u_{bo}e^{j\frac{2}{3}\pi} + u_{co}e^{-j\frac{2}{3}\pi}\right) \tag{13}$$

The basic voltage vectors coordinate considering NPP fluctuation can be obtained by combining Formulas (1), (12) and (13), as shown in Table 4.

**Table 4.** Coordinate of basic voltage vector considering NPP fluctuation (α-β coordinate systems).

| Voltage Vector | Coordinate | Voltage Vector | Coordinate |
|---|---|---|---|
| $V_{ONN}$ | $\left(\frac{V_{dc}-2\Delta u}{3}, 0\right)$ | $V_{OPP}$ | $\left(-\frac{V_{dc}+2\Delta u}{3}, 0\right)$ |
| $V_{OON}$ | $\left(\frac{V_{dc}-2\Delta u}{6}, \frac{\sqrt{3}(V_{dc}-2\Delta u)}{6}\right)$ | $V_{OOP}$ | $\left(-\frac{V_{dc}+2\Delta u}{6}, -\frac{\sqrt{3}(V_{dc}+2\Delta u)}{6}\right)$ |
| $V_{OPN}$ | $\left(-\frac{2\Delta u}{3}, \frac{\sqrt{3}V_{dc}}{3}\right)$ | $V_{ONP}$ | $\left(-\frac{2\Delta u}{3}, -\frac{\sqrt{3}V_{dc}}{3}\right)$ |
| $V_{OPO}$ | $\left(-\frac{V_{dc}+2\Delta u}{6}, \frac{\sqrt{3}(V_{dc}+2\Delta u)}{6}\right)$ | $V_{ONO}$ | $\left(-\frac{V_{dc}-2\Delta u}{6}, -\frac{\sqrt{3}(V_{dc}-2\Delta u)}{6}\right)$ |

As can be seen in Table 4 and Figure 4, it is clear that the NPP fluctuation will result in an uneven distribution of space voltage vectors, which will cause imbalances of ESTPI output. This will affect the grid-connected power quality and narrow the linear modulation area, and the NPP fluctuation is an inherent phenomenon. Unfortunately, there are no redundant vectors available for NPP control in ESTPI. Imbalance of ESTPI output is inevitable.

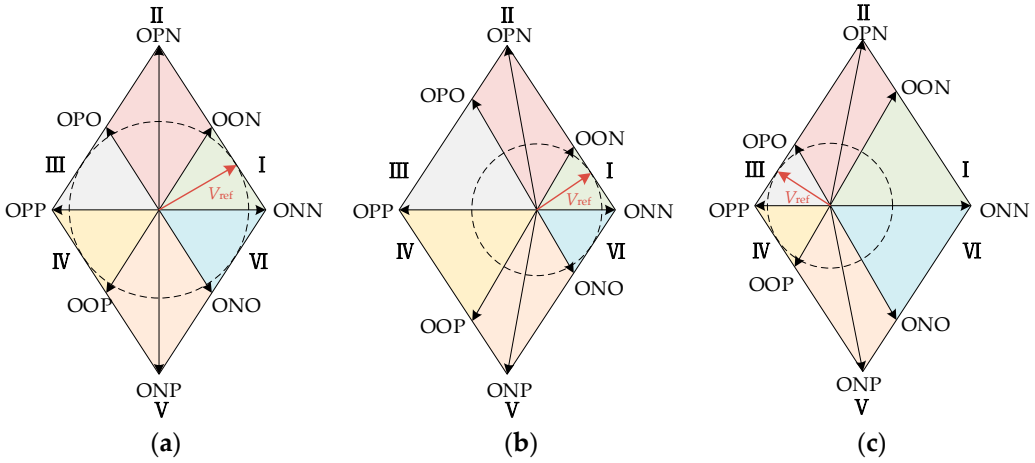



**Figure 4.** The basic voltage vector distribution of ESTPI: (**a**) $u_p = u_n$; (**b**) $u_p > u_n$; (**c**) $u_p < u_n$.

It is obvious that the NPP fluctuation of the DC bus will change the distribution of basic voltage vectors. If the method in Table 2 is still used to synthesize the reference voltage vector, the grid-connected power quality will deteriorate. At the same time, choosing the DC-link capacitor's capacity according to the lowest limitation is a common cost-saving measure in practical industrial applications, which will worsen the fluctuation of NPP and further deteriorate the power quality. Therefore, it is necessary to consider the impact of NPP fluctuation on the synthesis of the reference voltage vector. Based on the volt-second balancing principle, the reference voltage vector synthesis should be compensated when the NPP fluctuates.

The duration time of the fundamental vector is recalculated considering NPP fluctuation. The calculation method remains the same as presented in Formulas (5) and (6), with the exception that the vector coordinates need to incorporate variations in NPP. The reference voltage vector synthesis rules are outlined in Table 5.

**Table 5.** Vector duration time and corresponding NP current after compensation.

| N | n | $t_1$ (s) | Vector $V_1$ | $i_{o1}$ (A) | $t_2$ (s) | Vector $V_2$ | $i_{o2}$ (A) |
|---|---|---|---|---|---|---|---|
| I | / | $2mT_s\sin(\pi/3-\theta)/(1-2\Delta u/V_{dc})$ | ONN | $i_{la}$ | $2mT_s\sin(\theta)/(1-2\Delta u/V_{dc})$ | OON | $-i_{lc}$ |
| II | 1 | $2mT_s\sin(\pi/3+\theta)/(1-2\Delta u/V_{dc})+2mT_s\sin(\pi/3-\theta)/(1+2\Delta u/V_{dc})$ | OON | $-i_{lc}$ | $-2mT_s\sin(\pi/3-\theta)/(1+2\Delta u/V_{dc})$ | OPN | $i_{la}$ |
| II | 2 | $-2mT_s\sin(\pi/3-\theta)/(1+2\Delta u/V_{dc})-2mT_s\sin(\pi/3+\theta)/(1-2\Delta u/V_{dc})$ | OPO | $-i_{lb}$ | $2mT_s\sin(\pi/3+\theta)/(1-2\Delta u/V_{dc})$ | OPN | $i_{la}$ |
| III | / | $2mT_s\sin(\theta)/(1+2\Delta u/V_{dc})$ | OPO | $-i_{lb}$ | $-2mT_s\sin(\pi/3+\theta)/(1+2\Delta u/V_{dc})$ | OPP | $i_{la}$ |
| IV | / | $-2mT_s\sin(\pi/3-\theta)/(1+2\Delta u/V_{dc})$ | OPP | $i_{la}$ | $-2mT_s\sin(\theta)/(1-2\Delta u/V_{dc})$ | OOP | $-i_{lc}$ |
| V | 1 | $-2mT_s\sin(\pi/3+\theta)/(1+2\Delta u/V_{dc})-2mT_s\sin(\pi/3-\theta)/(1-2\Delta u/V_{dc})$ | OOP | $-i_{lc}$ | $2mT_s\sin(\pi/3\text{-}\theta)/(1-2\Delta u/V_{dc})$ | ONP | $i_{la}$ |
| V | 2 | $2mT_s\sin(\pi/3-\theta)/(1-2\Delta u/V_{dc})+2mT_s\sin(\pi/3+\theta)/(1+2\Delta u/V_{dc})$ | ONO | $-i_{lb}$ | $-2mT_s\sin(\pi/3+\theta)/(1+2\Delta u/V_{dc})$ | ONP | $i_{la}$ |
| VI | / | $-2mT_s\sin(\theta)/(1-2\Delta u/V_{dc})$ | ONO | $-i_{lb}$ | $2mT_s\sin(\pi/3+\theta)/(1-2\Delta u/V_{dc})$ | ONN | $i_{la}$ |

To examine the compensation effect of reference voltage vector synthesis considering the NPP fluctuation, the grid-connected currents and voltages of the DC-link capacitors are tested. The main circuit parameters are shown in Table 6, with the grid-connected currents at 6A and the capacitances of the DC-link are 820 μF. The simulation results are illustrated in Figure 5.

**Table 6.** Parameters of the inverter.

| | |
|---|---|
| DC bus voltage ($V_{dc}$) | 400 V |
| Grid voltage ($U_{a,b,c}$) | 380 V |
| DC-link capacitance (C1, C2) | 820/2200 μF |
| Bridge arm side filter inductance ($L_C$) | 2.4 mH |
| The capacitance of filter (C) | 10 μF |
| Grid-side filter inductance ($L_g$) | 0.6 mH |
| Frequency of sampling ($f$) | 15 kHz |

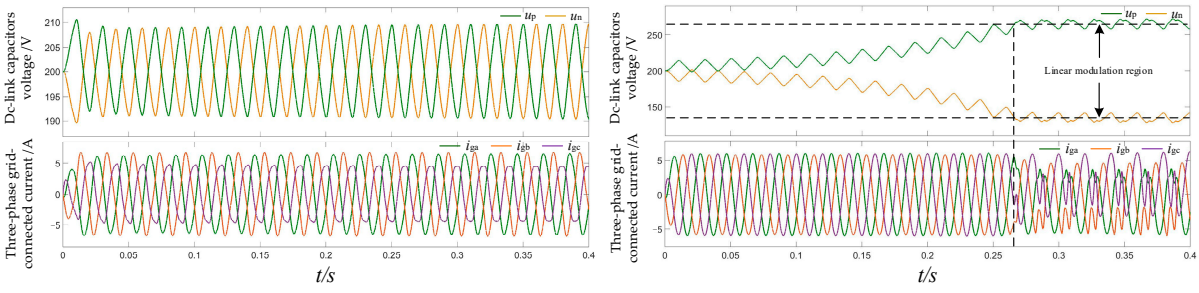



**Figure 5.** DC bus capacitor voltage and grid-connection currents. (**a**) Uncompensated (synthesis rules in Table 2); (**b**) Considering the NPP fluctuation (synthesis rules in Table 5). The dashed lines are the linear modulation region border.

As shown in Figure 5a, if the NPP fluctuation is not considered in the synthesis of the reference voltage vector, the NPP fluctuation can remain balanced, but the distortion of the grid-connected currents is severe. As shown in Figure 5b, when NPP fluctuation is taken into account in the synthesis of the reference voltage vector, the grid-connected currents have good sine waves at the beginning, but the NPP gradually deviates from the equilibrium point until exceeding the linear modulation region. Then, the reference voltage vector no longer satisfies the principle of volt-second balancing and results in a serious distortion of the grid-connected currents. In summary, considering the NPP fluctuation can improve the quality of three-phase grid-connected currents at the beginning, but NPP will still deviate from the equilibrium point. Thus, it is necessary to investigate the reasons for the NPP fluctuation increasing and optimize the compensation of the space vector modulation.

### *3.2. Optimization of SVPWM*

To ensure the inverter is still running and providing power to the grid after the single bridge arm fault, it is necessary to find the reasons for the NPP's significant fluctuation, then design the effective control strategy. Combine Table 5, Formulas (5) and (6), and the NP current of the DC bus with NPP fluctuation can be expressed as Formula (14):

$$i_o = \begin{cases} \frac{\sqrt{3}mI_m\cos\varphi}{(1-2\Delta u/V_{dc})} & 0 \leqslant \theta < \frac{\pi}{3}, \text{(Sector I)} \\ K_{21}\times(-I_m\cos(\theta-\varphi+\frac{2\pi}{3}) - \frac{I_m\cos(\theta-\varphi)\times 2m\sin(\pi/3-\theta)}{(1+2\Delta u/V_{dc})} & \frac{\pi}{3} \leqslant \theta < \frac{\pi}{2}, \text{(Sector II)} \\ K_{22}\times(-I_m\cos(\theta-\varphi-\frac{2\pi}{3}) + \frac{I_m\cos(\theta-\varphi)\times 2m\sin(\pi/3+\theta)}{(1-2\Delta u/V_{dc})} & \frac{\pi}{2} \leqslant \theta < \frac{2\pi}{3}, \text{(Sector II)} \\ \frac{-\sqrt{3}mI_m\cos\varphi}{(1+2\Delta u/V_{dc})} & \frac{2\pi}{3} \leqslant \theta < \pi, \text{(Sector III)} \\ \frac{-\sqrt{3}mI_m\cos\varphi}{(1+2\Delta u/V_{dc})} & \pi \leqslant \theta < \frac{4\pi}{3}, \text{(Sector IV)} \\ K_{51}\times(-I_m\cos(\theta-\varphi+\frac{2\pi}{3}) + \frac{I_m\cos(\theta-\varphi)\times 2m\sin(\pi/3-\theta)}{(1-2\Delta u/V_{dc})} & \frac{4\pi}{3} \leqslant \theta < \frac{3\pi}{2}, \text{(Sector V)} \\ K_{52}\times(-I_m\cos(\theta-\varphi-\frac{2\pi}{3}) - \frac{I_m\cos(\theta-\varphi)\times 2m\sin(\pi/3+\theta)}{(1+2\Delta u/V_{dc})} & \frac{3\pi}{2} \leqslant \theta < \frac{5\pi}{3}, \text{(Sector V)} \\ \frac{\sqrt{3}mI_m\cos\varphi}{(1-2\Delta u/V_{dc})} & \frac{5\pi}{3} \leqslant \theta \leqslant 2\pi, \text{(Sector VI)} \end{cases} \tag{14}$$

where, $K_{21}$, $K_{22}$, $K_{51}$, $K_{52}$ are defined as Formula (15).

$$\begin{cases} K_{21} = 2m\sin(\pi/3+\theta)/(1-2\Delta u/V_{dc}) + 2m\sin(\pi/3-\theta)/(1+2\Delta u/V_{dc}) \\ K_{22} = -2m\sin(\pi/3-\theta)/(1+2\Delta u/V_{dc}) - 2m\sin(\pi/3+\theta)/(1-2\Delta u/V_{dc}) \\ K_{51} = -2m\sin(\pi/3+\theta)/(1+2\Delta u/V_{dc}) - 2m\sin(\pi/3-\theta)/(1-2\Delta u/V_{dc}) \\ K_{52} = 2m\sin(\pi/3-\theta)/(1-2\Delta u/V_{dc}) + 2m\sin(\pi/3+\theta)/(1+2\Delta u/V_{dc}) \end{cases} \tag{15}$$

Comparing Formulas (9) and (14), it is evident that the addition of compensation ($\Delta u/V_{dc}$) causes the NP current to no longer satisfy the half-wave symmetry in Formula (14). Therefore, the NPP of the DC bus deviates from the equilibrium point. To maintain Formula (14) to satisfy $i_o(\theta) + i_o(\theta+\pi) = 0$, the following relationship should be maintained, as shown in Formula (16):

$$\Delta u(\theta)/V_{dc} + \Delta u(\theta+\pi)/V_{dc} = 0 \tag{16}$$

For Equation (16) to hold true, the voltage deviation of the DC link ($\Delta u$) should not contain the DC component. Thus, the space vector modulation of adding the NPP fluctuation should be further refined.

To eliminate the DC component of $\Delta u$, the DC component should be extracted first. A first-order low-pass filter is designed to obtain the DC component in this work. In the s-domain, the first-order low-pass filter can be expressed as follows:

$$G(s) = \frac{1}{1+s/\omega_c} \tag{17}$$

where $\omega_c$ is its cutoff frequency. According to Formula (11), it can be seen that the main AC component in the NPP fluctuation of the DC bus is the fundamental component with an angular frequency of approximately 314 rad/s. To extract the DC component, the cutoff frequency of the low-pass filter must be lower than the fundamental angular frequency. According to low-pass filter phase-frequency characteristics, when the signal passes through the filter, a large phase shift will be generated at a lower cutoff frequency, which will affect the filtering accuracy of the DC component. In this paper, the cutoff frequency is selected as 80 rad/s.

To prevent the DC bus NPP from deviating too much from the equilibrium point, a hysteresis comparator is designed to further adjust the space vector modulation compensation. The NP current is obtained by Formula (18):

$$i_o = \begin{cases} \sqrt{3}mI_m\cos\varphi/(1-2\Delta u/V_{dc}) & \text{sector I, VI} \\ -\sqrt{3}mI_m\cos\varphi/(1+2\Delta u/V_{dc}) & \text{sector III, IV} \end{cases} \tag{18}$$

According to Formula (18), in sector I, III, IV, and VI, if the value of the grid-connection system parameters ($I_m$ and $\varphi$) is determined, $\sqrt{3}mI_m\cos\varphi$ can be considered as a constant,

and cos$\varphi$ is greater than or equal to 0 within a range of $\varphi$ between $-90°$ and $90°$. According to Formulas (11) and (18), NPP fluctuation can be controlled by adjusting the compensation value of the reference voltage vector synthesis in sectors I, III, IV and VI. However, it is important to note that the modulation can be considered as a proportional link throughout the entire grid-connected control, and $V_{ref}$ is the output of the grid-connected controller that converts into the switch driver signal via space vector modulation. Consequently, the hysteresis comparator is designed to adjust the compensation value, only when the NPP of the DC bus contains the DC component and deviates large enough from the equilibrium point, the hysteresis comparator will compensate the voltage vector. The compensation value in Formula (18) is adjusted to prevent the NPP of the DC bus from deviating from the equilibrium point, achieving the synthesis of the reference voltage vector lying in the linear modulation region.

Given $0.5u_{\max} \leq \Delta u \leq u_{\max}$, the output of the hysteresis comparator should be a suitable value that can compensate for the NPP fluctuation, otherwise 0, $u_{max}$ is the maximum allowable voltage of NPP fluctuation in the linear modulation area. Since the DC component increases as the NPP deviates from the equilibrium point, the output of the hysteresis comparator also increases, and more robust control of the NPP of the DC bus can be realised. Therefore, the output of the hysteresis comparator can be designed according to the DC component of NPP fluctuation, which can be represented as follows:

$$\tau = -K \times \mathrm{sgn}(A_0) \text{sector I, III, IV, VI} \tag{19}$$

where, $K = |A_0| + 1$, $A_0$ is the DC component of NPP fluctuation.

In conclusion, the optimised compensation value is shown in Formula (20):

$$\Delta u' = \Delta u - A_0 + \tau = \frac{u_p - u_n}{2} - A_0 + \tau \tag{20}$$

Based on the above analysis, a fault-tolerant control strategy with SVPWM compensation optimisation is constructed, as shown in Figure 6.

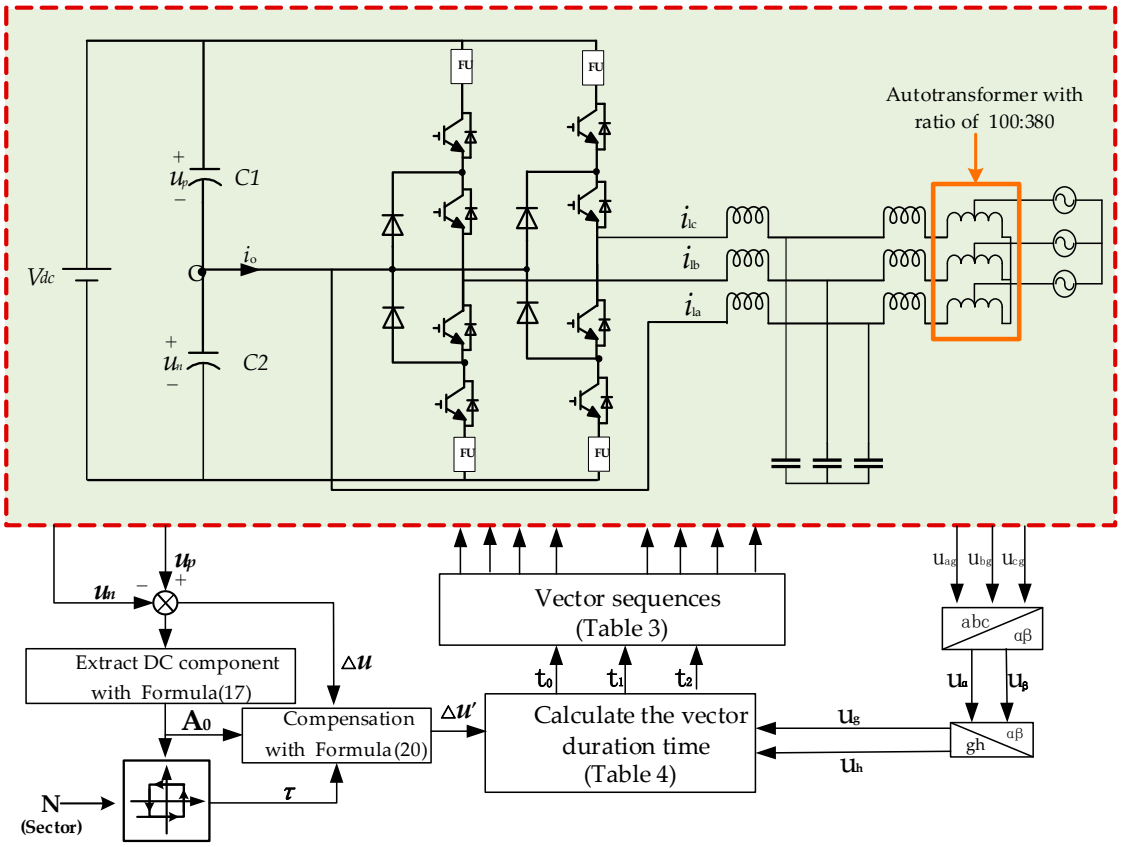



**Figure 6.** Fault-tolerant control with SVPWM compensation optimisation.

## 4. Simulation and Results Analysis

To verify the effect of the fault-tolerant control strategy proposed in this paper, a three-level NPC grid-connected inverter experimental device is simulated and analysed using MATLAB/Simulink. The topology of postfault three-phase three-level NPC grid-connected inverters is shown in Figure 7. The LCL filter in the rear stage of the inverter connects to the power grid through the autotransformer and isolation transformer. The ratio of the autotransformer is 100:380. The main parameters of the inverter are shown in Table 6.

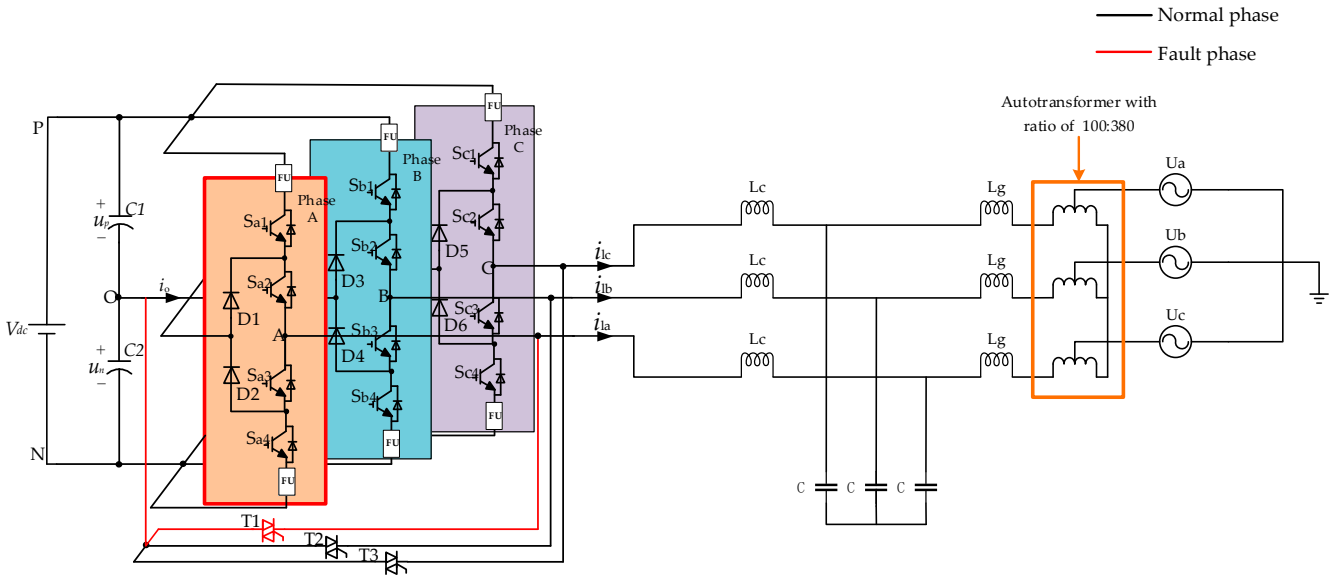


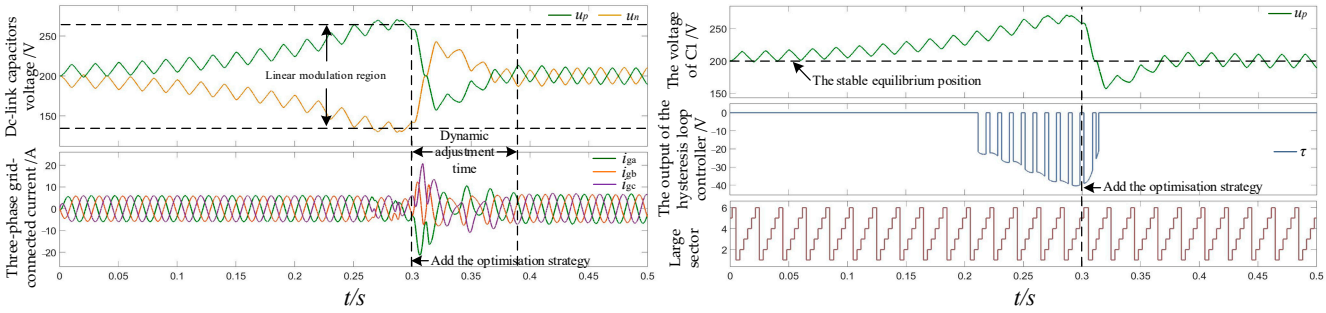

**Figure 7.** The inverter topology in simulation (Phase A failure).

To verify the effectiveness of the proposed strategy, the simulation is carried out as follows. The system runs with the control strategy of considering NPP fluctuation not extracting the DC component at the beginning, and NPP will deviate from the balance. When NPP exceeds the linear modulation region, the grid-connection current will distort severely. At this time, the proposed strategy is applied to the system to confirm the suppression effect on the NPP fluctuation. In this way, the grid-connected currents are compared between the traditional SVPWM and our proposed optimized strategy. To verify the performance when the load changes, the simulation is carried out with a grid-connected current step from 6A to 12A. Finally, the improvement in CMV is verified by comparing the proposed method with the traditional SVPWM method.

### *4.1. The Compensation Optimization Strategy Control Effect*

Firstly, the correctness of the fault-tolerant control strategy proposed is verified. The grid-connection currents are 6A and the capacitances of DC-link are 820 μF. To evaluate the compensation optimisation strategy, the grid-connected currents and DC-link capacitors' voltage are tested, respectively. Figure 8 displays the simulation results.

In Figure 8a, $i_{ga}$, $i_{gb}$, and $i_{gc}$ are the three-phase grid-connected currents. If the SVPWM is not optimised, the grid-connected currents experience significant distortion over time due to the DC bus NPP deviating from the equilibrium point. Even if the sine waves of grid-connected currents are good at first, they will distort when $V_{ref}$ exceeds the linear modulation range. However, by implementing the SVPWM compensation optimisation strategy at 0.3 s, the NPP of the DC bus can be effectively controlled. The NPP and grid-connected currents tend to be stable at 0.39 s. The dynamic processing is less than 0.1 s and the quality of grid-connected currents have noticeable improvement.

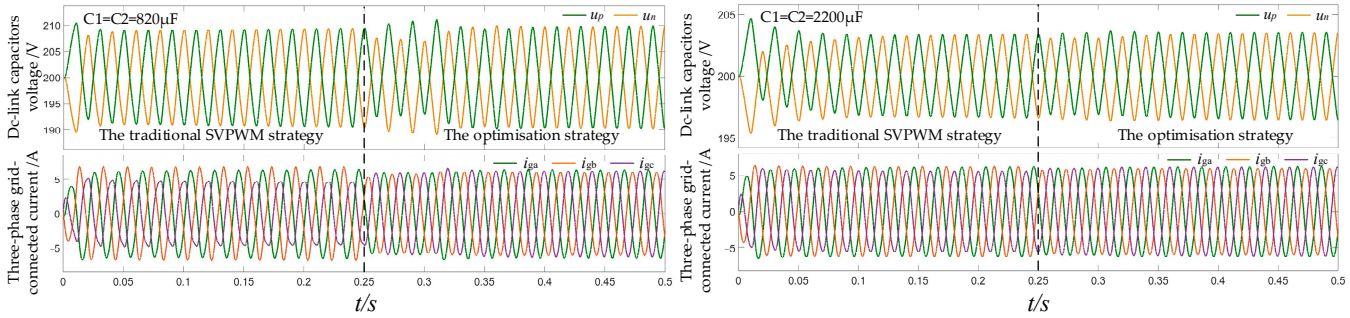



(**a**) (**b**)

**Figure 8.** Control effect of the SVPWM compensation optimisation strategy: (**a**) The dynamic adjustment process; (**b**) The output of the hysteresis comparator.

Figure 8b shows the increase output of the hysteresis comparator with the increasing of NPP deviation. When the SVPWM compensation optimisation strategy is applied at 0.3 s, the reference voltage vector is in sector V this moment. The output of hysteresis comparator is zero and has no effect on the control loop. When the reference voltage vector changes to sector VI, the NPP decreases rapidly due to the proposed strategy, then the output of the hysteresis comparator returns to zero when the NPP deviation is less than 20 V.

According to Formula (11), there is a correlation between NPP fluctuation and the DC bus's capacitance. To verify the control ability of the fault-tolerant control strategy with different capacitances, capacitances of 820 μF and 2200 μF are tested, respectively. The simulation involved both traditional SVPWM and the proposed SVPWM compensation optimisation strategy, and the results are shown in Figure 9.




(**a**) (**b**)

**Figure 9.** Fault-tolerant control results with different capacitances of the DC capacitor: (**a**) DC bus capacitance 820 μF; (**b**) DC bus capacitance 2200 μF.

As shown in Figure 9, as the capacitance increases from 820 μF to 2200 μF, the voltage fluctuation of the DC bus capacitor and the distortion of the grid-connected currents decrease. The currents behave distortion significantly with traditional SVPWM, especially when the capacitance is small (820 μF). At 0.25 s, the SVPWM compensation optimisation strategy is applied in both capacitance cases, and the degree of grid-connected current distortion gets improvement drastically. When the DC-link capacitance is 820 μF, the total harmonic content analysis (THD) of the grid-connected currents before and after the SVPWM compensation optimisation strategy are shown in Figure 10.

As shown in Figure 10, when the DC-link capacitances are 820 μF, we can see a remarkable reduction in the THD of the grid-connected currents from 10.41% to 2.03% by implementing the SVPWM compensation optimisation strategy. This improvement significantly enhances the quality of the grid-connected currents, meeting the requirement for grid connection (THD $\leq$ 5%). These findings indicate that even when the capacitances of the DC-link are small, the compensation optimisation strategy can effectively compensate the grid-connected currents, the hardware costs and volume can be reduced.

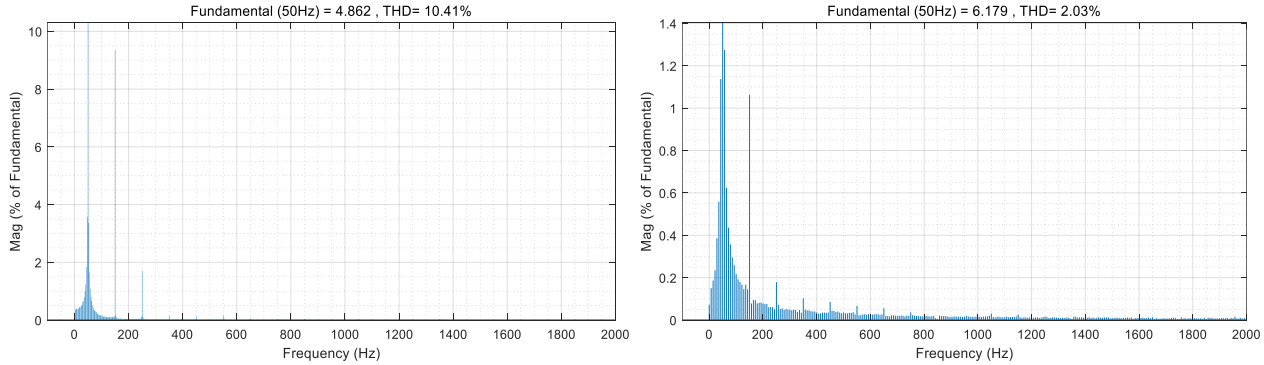



**Figure 10.** THD analysis of grid-connected currents (C1 = C2 = 820 μF): (**a**) Traditional SVPWM strategy; (**b**) SVPWM compensation optimisation strategy.

To further validate the efficacy of the compensation optimization strategy when the grid-connected power changes, the simulations are carried out with the amplitude of grid-connected currents varying from 6 A to 12 A. As shown in Figure 11, when the grid-connected currents increase, the NPP fluctuation also increases, which is consistent with the theoretical analysis in Formula (11). The grid-connected currents remain in the form of smooth sine waves, despite abrupt change in the amplitude of grid-connected currents.

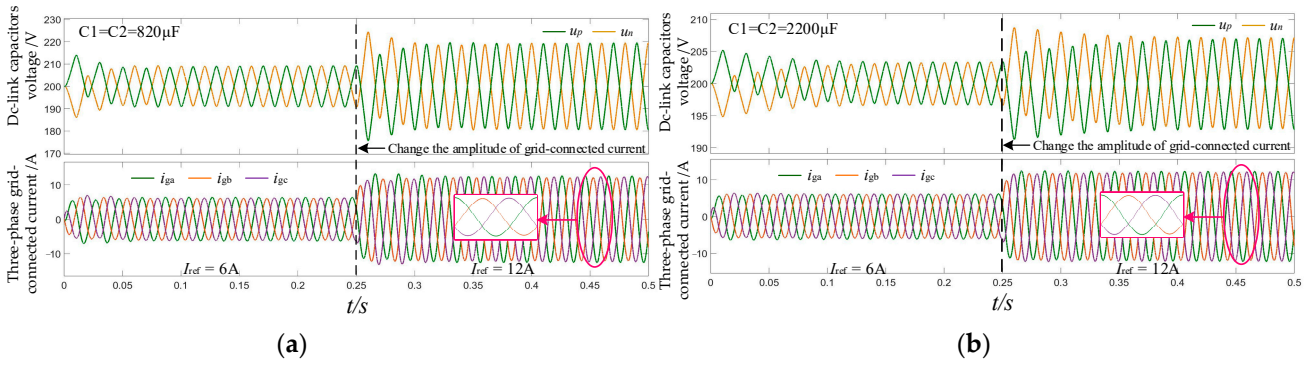
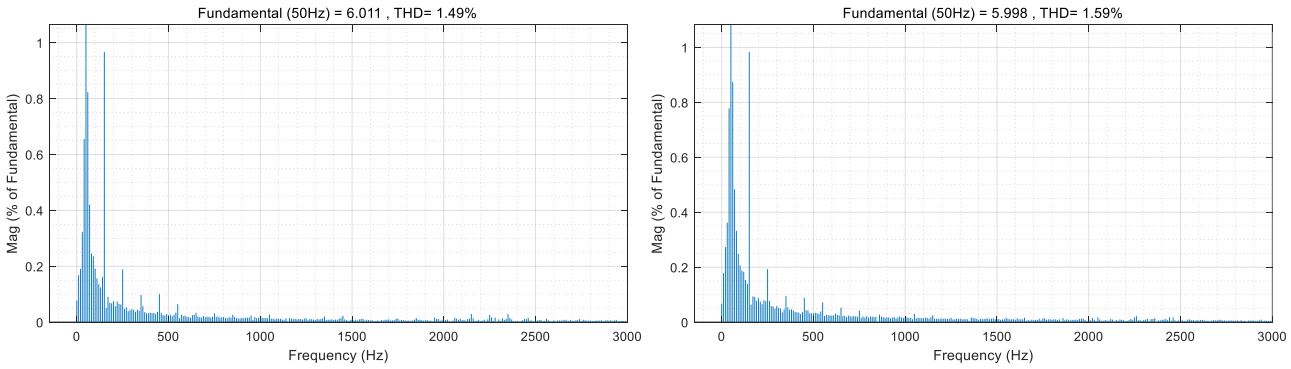



**Figure 11.** Fault-tolerant control results with the sudden change in the amplitude of grid-connected currents: (**a**) DC bus capacitance 820 μF; (**b**) DC bus capacitance 2200 μF.

In Figure 11a, the NPP deviation amplitude is greater than that in Figure 11b, as described in Formula (11). When the amplitude of the grid-connected currents changes suddenly, the half-wave symmetry of the NP current is destroyed in a fundamental period, leading to the NPP fluctuation containing the DC component. Therefore, the NPP and the grid-connected currents need to be dynamically adjusted to restore balance. When the DC bus capacitances are 2200 μF, the maximum rms deviation percentage of steady-state three-phase grid-connected currents is 2.66%. When DC bus capacitances are 820 μF, the maximum rms deviation percentage of the steady-state three-phase grid-connected currents is 4.33%. In both situations, the maximum rms deviation percentage of steady-state three-phase grid-connected currents are relatively small. When the amplitude of the grid-connected currents changes and the DC bus capacitances are 820 μF, the maximum NPP fluctuation is 24 V, and the maximum DC bus NPP deviation tolerated within the linear modulation region is 63 V. Despite the NPP's significant fluctuation amplitude under these conditions, the ESTPI can operate properly. Thus, the SVPWM compensation optimisation strategy designed in this paper can ensure the continuous operation of the three-level NPC inverter after a single-arm failure.

### *4.2. The Improvement of Common Mode Voltage*

In the SVPWM compensation optimization strategy, the medium vector is employed for the space vector synthesis in sector II and V. This results in reduction in the proportion of the small vector, leading to a decrease in the CMV. To evaluate the impact of the approach, the THD of the currents with the vector synthesis method only using small vectors and introducing medium vectors are analysed, respectively, and the results are shown in Figure 12.




(**a**) (**b**)

**Figure 12.** THD analysis of grid-connected currents (C1 = C2 = 2200 μF): (**a**) Use only small voltage vectors; (**b**) Introduce medium voltage vectors.

According to the data presented in Figure 12, when introducing medium vectors in vector synthesis, the THD of grid-connected currents is 1.59%, which is slightly higher than the 1.49% only using small vectors. This is because the switch sequence is unable to meet the three-phase symmetry requirement within one-third of one fundamental period when incorporating medium vectors. Thus, the content of the third harmonic and its multiples harmonics of the ESTPI output currents will increase. The THD of grid-connected currents is still less than 5% in both cases, with only a 0.10% difference between the two methods, but the vector synthesis method introducing medium vectors can effectively reduce CMV. As shown in Figure 13:

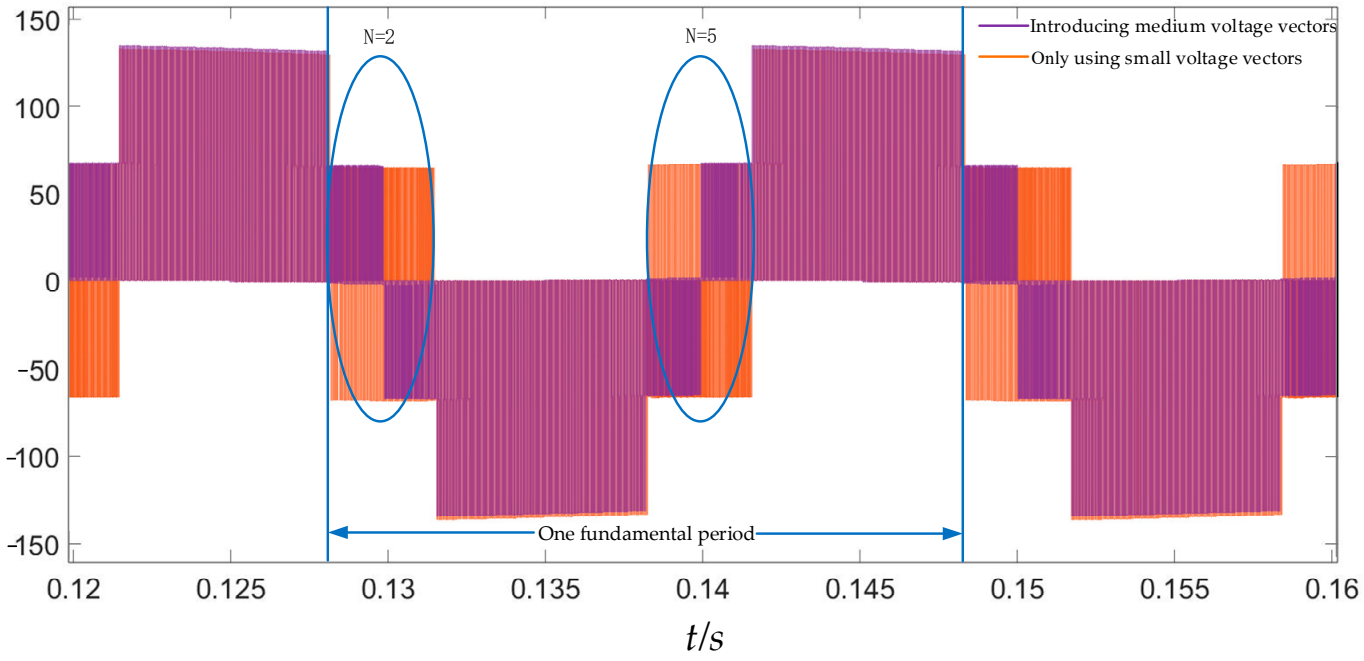



**Figure 13.** The CMV with difference reference voltage vector synthesis strategy.

The method with the medium-voltage vector is used to synthesize the reference voltage vector. When the reference voltage vector is in subsector 1 of sector II, the CMV changes from $-V_{dc}/6$ to 0, the CMV changes from $V_{dc}/6$ to 0 in subsector 2. When the reference voltage vector is in subsector 1 of sector V, the CMV changes from $V_{dc}/6$ to 0, and the CMV changes from $-V_{dc}/6$ to 0 in subsector 2. This indicates that the proposed fault-tolerant control strategy not only can guarantee exceptional grid-connection control after a single-arm fault, but also can significantly reduce the CMV for one-third of the time within each fundamental wave period, with the CMV decreasing accordingly throughout the entire cycle, which is conducive to grid-connection operation.

## 5. Conclusions

This paper proposed a fault-tolerant control strategy for three-level NPC grid-connected inverters based on SVPWM. First, after the single-arm of the NPC grid-connected inverter failure, the CMV is improved by repartitioning the sectors and subsectors and selects a new reference voltage vector synthesis sequence. Then, based on the NPP migration mechanism of the DC bus, the low-pass filter and hysteresis controller are designed to optimise and compensate for the reference voltage vector synthesis, which can restrict the reference voltage vector in the linear modulation area. The optimised SVPWM algorithm can effectively suppress NPP migration and improve the quality of grid-connected currents. When the amplitude of the grid-connected currents suddenly changes, the improved fault-tolerant control strategy can also realise the three-phase balance of the inverter output and maintain good grid-connected power quality.

With the proposed fault-tolerant control strategy, the THD of grid-connected currents decreases from 10.41% to 2.03%, and the amplitude of CMV decreases in one-third of one fundamental period. The simulation results verify the effectiveness of the proposed fault-tolerant control strategy and provide a guarantee for the continuous stable operation of the three-level NPC grid-connected inverters after a single-arm fault.

**Author Contributions:** Conceptualization, J.H.; formal analysis, J.H.; funding acquisition, J.H.; investigation, F.B.; methodology, J.H. and F.B.; project administration, J.H.; software, Q.Y.; validation, Q.Y. and S.R.; visualization, F.B. and S.R.; writing—original draft, F.B.; writing—review and editing, J.H. and Q.Y. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by National Natural Science Foundation of China (U1504617) and University-Industry Collaborative Education Program, China (202101222007).

**Data Availability Statement:** Data are contained within the article.

**Conflicts of Interest:** The authors declare no conflict of interest.

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