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Active Disturbance Rejection Control of an Interleaved High Gain DC-DC Boost Converter for Fuel Cell Applications

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Abstract: In this paper, a simplified and robust control strategy of an interleaved high gain DC/DC boost converter (IHGBC) is proposed in order to enhance DC bus voltage regulation in proton exchange membrane fuel cell (PEMFC) applications. The fluctuation of the energy source voltage and external load, and the change in system parameters lead to the instability of output voltage. Based on the creation of an average state space model of the DC/DC boost converter, the proposed controller is designed based on a linear active disturbance rejection control (LADRC), which has an external voltage loop and an internal current loop to meet the output voltage requirements under parameters uncertainties and disturbances. The effectiveness of the proposed approach strategy and its superiority were examined under different operating conditions and scenarios. Simulation and experiment results showed the efficiency and robustness of the suggested approach and the great effectiveness in the reference tracking and disturbance rejection.

Keywords: linear active disturbance rejection control (LADRC); proton exchange membrane fuel cell (PEMFC); robust control; DC-DC boost converter



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1. Introduction

With the increasing search for new non-polluting renewable energy resources that can replace fossil fuels to reduce greenhouse gas emissions, PEMFC presents itself as a serious solution as clean, highly efficient and reliable energy [1,2]. Fuel cells are used in transport, and stationary and portable applications [3,4]. In these applications and due to the low output voltage of the PEMFC system, the DC-DC converter associated to the PEMFC plays a very important role in transferring the generated power to the load (motor, auxiliaries or resistive load on the DC bus side) [5,6]. These converters require specific characteristics of PEMFC applications such as [7,8]: a high voltage gain ratio, minimal input current ripple and good efficiency.

In this context, studies have largely addressed many different structures of DC/DC converters categorized into non-isolated, isolated and soft-switched structures for PEMFC applications based on current issues of volume and weight reduction, input current ripple reduction or fault tolerance [9–13].

In accordance with the requirements of fuel cell applications, an interleaved non-isolated high gain boost converter is proposed in this work. This converter is a combination of a passive switched inductor cell with an additional step-up capacitor [14]. This combination provides high voltage gain with reduced voltage stress on the switches and diodes, which reduces conduction and switching losses of the diodes and thus improves converter efficiency. Furthermore, the converter is improved by adding a passive switching inductor cell in parallel with the first cell at the input of the converter with the control signals shifting on switches S1 and S2 to reduce input current ripples. Regarding the latter, the

literature [7,15–17] has explored the effects of low frequency and high frequency current ripple on the fuel cell.

Studies have revealed that compared to high frequency current ripple (i.e., >1 kHz), low frequency current ripple (i.e., 100–120 Hz) has a greater impact on efficiency, hydrogen consumption and FC lifetime.

Furthermore, the impact on the FC is highly dependent on the amplitude of the current ripple. If the current ripple amplitude is too high, it could cause much greater degradation, especially on the lifetime of platinum catalysts [16,17]. It has been suggested in the literature [7,15] that the current ripple should be limited to less than 10% of the nominal FC current.

In fact, the proposed topology offers a high voltage conversion gain. Additionally, interleaving helps reduce the input current ripple compared to existing conventional converters (e.g., Boost, Cascade Boost, Three Level Boost), which makes it appropriate for FC applications [13].

Regulating the output voltage and meeting the power demanded in fuel cell systems requires a high-performance DC-DC boost converter with high efficiency and a fast response. However, since the DC-DC boost converter is a non-minimum phase system that is very sensitive to uncertainties and disturbances, such as fluctuations in the load impedance and input voltage, and disturbance of the system parameters, it causes limitations in the control bandwidth [18,19]. For this purpose, many different strategies for the control design of DC-DC converters have been developed.

In [20], the adaptive sliding mode control (SMC) system is designed to regulate the output voltage and reduce the inductance current ripple of a three phase direct coupled interleaved boost converter (TP-DIBC).

Based on the concept of differential flatness, the author in [21] proposes a non-linear single-loop control strategy for a multiphase interleaved converter in order to achieve efficient reference tracking without using a complex algorithm. To ensure good voltage tracking and good performance of an interleaved boost converter, the author in [22] proposes a control strategy based on the H-infinity mixed sensitivity approach. The strategy was validated under different operating conditions, but such algorithms are complex and difficult to implement.

Considering the previous techniques applied to a DC-DC converter, a particular control technique can improve the DC-DC converter's operation to achieve better efficiency and robustness. The control technique is selected based on the priority of the application requirements, so some converter topology can be considered most suitable for a particular control technique [23]. Several control techniques are available each with different advantages, including response time, efficiency and robustness [24–26]. For example, classical PI control is widely used due to its easier design and low control complexity compared to other control techniques [27]. However, this technique has a slow dynamic response and a limited performance.

In recent years, many fields of control engineering have turned to the use of an emerging control technology designed for robust disturbance tolerance known as linear active disturbance rejection control (LADRC) as a candidate for classical controllers (PID) and modern model-based control strategies [27,28].

Based on the LADRC design, all internal uncertainties and external disturbances are estimated and compensated by extended state observer (ESO) law and feedback control. In order to simplify the non-linear structure and facilitate the tuning of complex parameters, Gao et al. in [29] simplified the control design into a linear active disturbance rejection control (LADRC). In contrast to many control strategies, LADRC is an independent method that does not depend on the exact mathematical model of the controlled system [30], which qualifies it for wide use in many practical applications and theoretical studies [31–36].

The authors in [32] proposed an LADRC strategy for independent electric vehicle control. Their results showed that the LADRC controller significantly reduces the driver's steering effort, and can also perform better in terms of tracking accuracy, compared to

the PID controller. In [33], the LADRC method was incorporated into the control loop of a standalone inverter with the aim of improving the system immunity and extending the virtual impedance range. In [35], the hydrogen generation produced by the water electrolyzer is controlled by relying on the LADRC to maintain the gas pressure in the hydrogen tank. The control system was developed and designed and the superiority of LADRC was proven by comparing its performance with a PI controller. In [36], a robust LADRC-based damping method against disturbances and parametric changes was proposed for an LCL filter. The results showed good dynamic performance and high power quality.

Based on the previous analysis, to address the issues of varying system parameters, the external load voltage and the power source fluctuation that causes output voltage instability in fuel cell applications, the authors of this paper present:

- A robust dual-loop control application and design based on a linear active disturbance rejection control that controls the external voltage loop and the internal current loop of an interleaved DC-DC boost converter.
- This converter provides high efficiency and high voltage gain with reduced voltage stress on switches and diodes.

2. PEMFC Modelling

In the literature, several electrochemical reaction models have been developed to predict the PEMFC supplied voltage. The purpose of this modeling is to obtain the PEMFC polarization characteristics, which are deduced from the current and voltage of the fuel cell. In this section, a cell voltage model is presented as follows [37]:

$$V_{FC} = E_N - V_{Act} - V_{Ohm} - V_{Conc} \quad (1)$$

where E_N is the fuel cell open circuit potential [37,38].

$$E_N = 1.229 - 0.85 \times 10^{-3}(T_{FC} - 298.15) + 4.3085 \times 10^{-5}T_{FC} \left[\ln\left(\frac{P_{H_2}}{1.01325}\right) + \frac{1}{2}\ln\left(\frac{P_{O_2}}{1.01325}\right) \right] \quad (2)$$

V_{Act} are the activation losses expressed as a function of the constants V_a , C_1 and the voltage drop V_O .

$$V_{Act} = V_O + V_a \left(1 - e^{-C_1 i}\right) \quad (3)$$

V_{Ohm} is the ohmic voltage drop and is calculated based on the temperature, membrane thickness of fuel cell and constants b_1 , b_2 [37].

$$V_{Ohm} = \frac{i \cdot t_m}{b_1 \exp\left(b_2 \left(\frac{1}{303} - \frac{1}{T_{FC}}\right)\right)} \quad (4)$$

The concentration losses V_{Conc} are given as a function of constants i_{Max} , C_2 and C_3 [37].

$$V_{Conc} = i \left(C_2 \frac{i}{i_{Max}}\right)^{C_3} \quad (5)$$

3. Modelling of the Proposed Converter

The interleaved high gain DC-DC boost converter (IHGBC) is shown in Figure 1. The circuit consist of two active switches (S1, S2), four inductors (L1, L2, L3, L4) and two boost capacitors (CB1, CB2) with equal values, one input capacitor (Cin), four passive switched inductor diodes (D1, D2, D3, D4), two output diodes (Ds1, Ds2) and one output capacitor (C0).

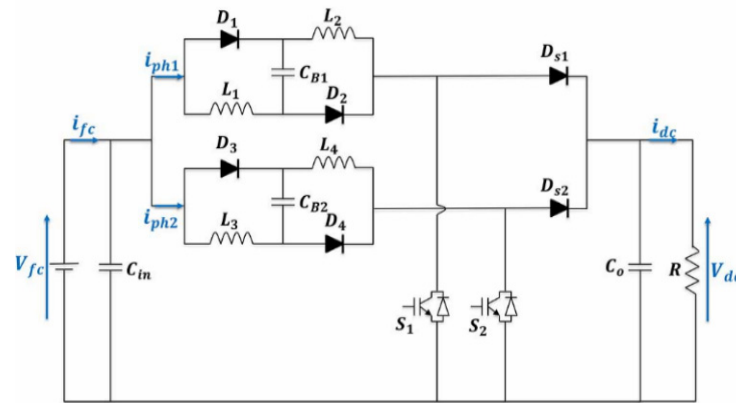


Figure 1. Structure of the proposed interleaved high gain DC-DC boost converter.

The interleaving concept used in this configuration is ensured by the parallel connection of two passive switched inductor cells at the input of the converter and the shifting of the control signals for the switches S1 and S2.

The interleaved topology reduces input current ripple. Moreover, this topology makes it possible to provide a high voltage gain and to reduce the electrical stresses (i.e., voltage and current) on the power semiconductors. The gain ratio of this topology is given by the following relationship:

$$\frac{V_{dc}}{V_{FC}} = \frac{2}{1-d} \tag{6}$$

The power switches (S1, S2) are controlled by switching each PWM gate control signal from each other by an angle of 180°.

When the switches (S1, S2) are turned on, diodes D1, D2, D3 and D4 are forward biased and L1, L2, L3, L4 and CB1, CB2 charge in parallel. When the switches (S1, S2) are turned off, then D1, D2, D3 and D4 are reverse biased and (L1, CB1 and L2), (L3, CB2 and L4) discharge in series.

The converter average model can be described by the equation:

$$\begin{cases} L \frac{dI_L}{dt} = V_{in} - \frac{(1-d)}{2} V_{dc} \\ C \frac{dV_{dc}}{dt} = (1-d)i_{L1} + (1-d)i_{L2} + i_{dc} \end{cases} \tag{7}$$

The small-signal model makes it possible to consider the transient and permanent state of the converter [39]. Therefore, we write:

$$x(t) = X(t) + \tilde{x} \tag{8}$$

where x represents the variable, X represents the steady state and, finally, \tilde{x} represents the small variation around this steady state.

The average small-signal model of the converter is given below:

$$\begin{cases} Ls\hat{i}_L = \hat{V}_{in} - \frac{(1-d)}{2}\hat{V}_{dc} + \frac{V_o}{2}\hat{d} \\ Cs\hat{V}_{dc} = (1-d)\hat{i}_{L1} - I_{L1}\hat{d} + (1-d)\hat{i}_{L2} - I_{L2}\hat{d} + \hat{i}_{dc} \end{cases} \tag{9}$$

Assuming that the duty cycles (d_1, d_2) are identical, the different transfer functions of this converter with a resistive load R are given below.

$$\frac{\hat{V}_{dc}}{\hat{d}} = \frac{-2RLI_Ls + RV_{dc}(1-d)}{2RLCs^2 + 2Ls + R(1-d)^2} \tag{10}$$

$$\frac{\hat{i}_L}{\hat{d}} = \frac{V_{dc}RCs + R(1-d)I_L + V_{dc}}{2RLCs^2 + 2Ls + R(1-d)^2} \tag{11}$$

4. LADRC-Based Control Design

This work presents the application of a linear active disturbance rejection control on a DC-DC converter in order to ensure a good reference tracking of the DC bus voltage reference and improve the performance and stability of the control system.

The LADRC design is based on the effective estimation and compensation of internal and external disturbances. LADRC is an independent technique of the controlled system, which gives it an important advantage over traditional control methods.

LADRC contains a linear state error feedback (LSEF) control law, and a linear extended state observer (LESO). The structure is shown in Figure 2. The LADRC is composed of two main control loops: the inner loop, also called the disturbance rejection loop, and the outer loop, also called the feedback control loop. The total disturbances of the system are estimated in advance by the LESO and eliminated by the inner loop, which is combined with the feedback control loop to achieve the desired signal and improve the system stability.

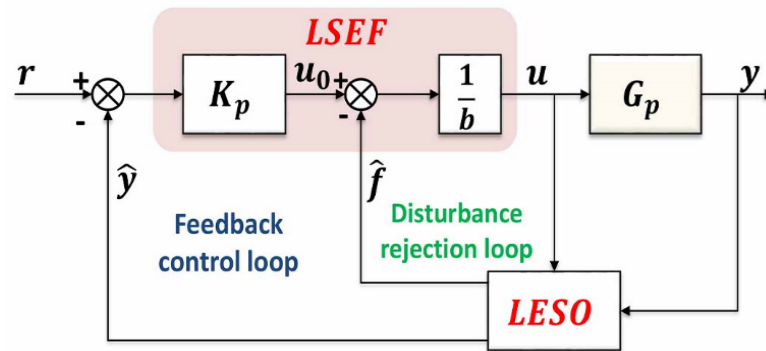


Figure 2. Structure diagram of the LADRC.

Assuming that the exact mathematical model of the system is not known, and the external perturbation is ignored, the dynamics of the IHGBC system can be reformulated based on the approximate model in the LADRC framework as follows [27,36]:

$$\dot{y} = bu + f(y, u) \tag{12}$$

where y is the system output, f represents the total disturbance, u is the controlled quantity, and b is the system gain.

Let $x_1 = y, x_2 = \dot{y}$ then

$$\begin{cases} \dot{x} = Ax + Bu + Ef \\ y_1 = Cx \end{cases} \tag{13}$$

where $A = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}; B = \begin{bmatrix} b \\ 0 \end{bmatrix}; E = \begin{bmatrix} 0 \\ 1 \end{bmatrix}; x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}; C = [1 \ 0]$

The corresponding second-order LESO is then written as follows:

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + Bu + L_0(y - \hat{y}) \\ \hat{y} = C\hat{x} \end{cases} \tag{14}$$

where $L_0 = \begin{bmatrix} \beta_1 \\ \beta_2 \end{bmatrix}$ is the observer gain vector.

The total disturbance is estimated by properly designing the LESO and configuring the observer bandwidth ω_0 . To obtain the total perturbation compensation, the final control law is written as [27]:

$$u = \frac{u_0 - \hat{f}}{b} \tag{15}$$

where \hat{f} is the estimated value of the total disturbance, and u_0 is the control quantity before compensation.

Substitute Equation (15) into Equation (12) to obtain:

$$\dot{y} = f - \hat{x}_2 + u \approx u \tag{16}$$

For first-order system, proportional control is adopted:

$$u_0 = K_p(r - \hat{x}_1) \tag{17}$$

where K_p is the controller parameter and r is the input reference (see Figure 2).

By applying Laplace transform to (14) we can obtain [36]:

$$\hat{x}_1 = \frac{\beta_1 y s + k_p r s}{s(s + \beta_1 + k_p)} \tag{18}$$

$$\hat{x}_2 = \frac{\beta_2 y s + \beta_2 k_p y + \beta_2 k_p r}{s(s + \beta_1 + k_p)} \tag{19}$$

To simplify the parameter tuning process, the setting of K_p and L_0 is converted into the observer's bandwidth ω_0 and the controller's bandwidth ω_c .

The needed settling time determines the controller parameter so $K_p = \omega_c$ with $\omega_c \approx \frac{4}{T_{settl}}$ [36].

The observer bandwidth is often selected in an effort to balance the sensitivity to noise and the rapidity of state estimation. All of the observer poles are put at $-\omega_0$ by carefully choosing the observer gains, and the equation is found as $\beta_1 = 2\omega_0$; $\beta_2 = \omega_0^2$.

There is a general rule based on selection $\omega_0 = 3 \sim 10\omega_c$.

Finally, the value of b is required to be increased incrementally until the desired performance is reached [36].

The DC-DC converter control loop is designed with a linear active disturbance rejection control that contains two cascaded loops (Figure 3): an outer loop for DC bus voltage control and an inner loop for phase current control. The DC bus voltage controller produces an $i_{ph.ref}$ by the error between the desired voltage value and the observed DC bus voltage, then the inner current loop allows the control signals (d_1, d_2) to be generated.

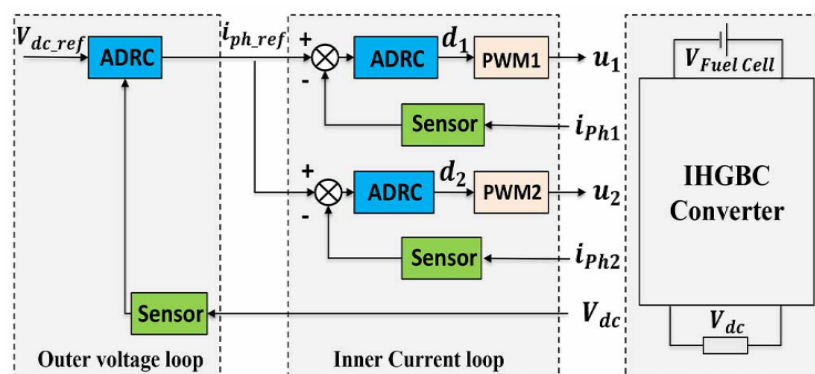


Figure 3. Cascaded control scheme for IHGBC.

The current controller parameters are designed using the transfer function given by Equation (7) as follows:

$$\frac{dI_L}{dt} = -\frac{(1-d)U_{dc}}{2L} + \frac{U_{in}}{L} \tag{20}$$

Let $I_L = y_1, d = u_1$ then:

$$\dot{y}_1 = \frac{U_{dc}}{2L} u_1 + \frac{U_{in}}{L} - \frac{U_{dc}}{2L} = b_1 u_1 + f_1(y_1, u_1) \tag{21}$$

where $b_1 = \frac{U_{dc}}{2L}$ is the object gain, u_1 is the system input, $f_1 = \frac{2U_{in}-U_{dc}}{2L}$ is the total disturbance and y_1 is the system output.

Let $x_1 = y_1, x_2 = \dot{y}_1$ then:

$$\begin{cases} \dot{x} = A_1x + B_1u_1 + E_1\dot{f}_1 \\ y_1 = C_1x \end{cases} \quad (22)$$

where $A_1 = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}; B_1 = \begin{bmatrix} b_1 \\ 0 \end{bmatrix}; E_1 = \begin{bmatrix} 0 \\ 1 \end{bmatrix}; x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}; C_1 = [1 \ 0]$

Second-order LESO is [30]:

$$\begin{cases} \dot{\hat{x}} = A_1\hat{x} + B_1u_1 + L_1(y_1 - \hat{y}_1) \\ \hat{y}_1 = C_1\hat{x} \end{cases} \quad (23)$$

where $L_1 = \begin{bmatrix} \beta_{11} \\ \beta_{12} \end{bmatrix}$

The final control law is designed to achieve aggregate compensation for disturbance as follows [30]:

$$u_1 = \frac{u_0 - \hat{x}_2}{b_1} \quad (24)$$

Substituting Equation (24) into Equation (21):

$$\dot{y}_1 = f_1 - \hat{x}_2 + u_1 \approx u_1 \quad (25)$$

Considering the controlled plant as a first-order system, a linear proportional controller can be used of the form:

$$u_0 = K_{pi}(r_1 - \hat{x}_1) \quad (26)$$

Based on the concept of bandwidth, the tuning of L_1 and K_{pi} is simplified.

$$\beta_{11} = 2\omega_{01}; \beta_{12} = \omega_{01}^2; K_{pi} = \omega_{c1}$$

In the same way as the study of the design of the current controller, the voltage controller parameters are designed using the transfer function given by Equation (7) as follows:

$$\frac{dU_{dc}}{dt} = \frac{(1-d)I_L}{C} - \frac{U_{dc}}{RC} \quad (27)$$

Let $U_{dc} = y_2, I_L = u_2$ then:

$$\dot{y}_2 = \frac{(1-d)}{C}u_2 - \frac{y_2}{RC} = b_2u_2 + f_2(y_2, u_2) \quad (28)$$

where $b_1 = \frac{(1-d)}{C}$ is the system gain, u_2 is the system input, $f_1 = -\frac{y_2}{RC}$ is the total disturbance of the system and y_2 is the system output.

Let $x_1 = y_2, x_2 = \dot{y}_2$ then:

$$\begin{cases} \dot{x} = A_2x + B_2u_2 + E_2\dot{f}_2 \\ y_2 = C_2x \end{cases} \quad (29)$$

where $A_2 = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}; B_2 = \begin{bmatrix} b_2 \\ 0 \end{bmatrix}; E_2 = \begin{bmatrix} 0 \\ 1 \end{bmatrix}; x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}; C_2 = [1 \ 0]$.

Second-order LESO is:

$$\begin{cases} \dot{\hat{x}} = A_2\hat{x} + B_2u_2 + L_2(y_2 - \hat{y}_2) \\ \hat{y}_2 = C_2\hat{x} \end{cases} \quad (30)$$

where $L_2 = \begin{bmatrix} \beta_{21} \\ \beta_{22} \end{bmatrix}$

The control law is designed to compensate the disturbances as follows:

$$u_2 = \frac{u_0 - \hat{x}_2}{b_2} \tag{31}$$

Thus, Equation (28) becomes:

$$\dot{y}_2 = f_2 - \hat{x}_2 + u_2 \approx u_2 \tag{32}$$

and the controlled plant is easily regulated using a proportional controller:

$$u_0 = K_{pv}(r_2 - \hat{x}_2) \tag{33}$$

The parameter setting for L_2 and K_{pv} is simplified as follows:

$$\beta_{21} = 2\omega_{02}; \beta_{22} = \omega_{02}^2; K_{pv} = \omega_{c2}$$

Figure 4 shows the block diagram of the proposed control for one phase. From Figure 4, the gain of the internal current loop is equal to:

$$G_i(s) = \frac{G_{ci}(s)H_i(s)}{1 + G_{ci}(s)G_{pi}(s)} \tag{34}$$

and the gain of the external voltage loop is obtained as:

$$G_v(s) = \frac{G_{cv}(s)H_v(s)G_{ci}(s)H_i(s)G_{pv}(s)G_{pi}(s)}{1 + G_{ci}(s)G_{pi}(s)} \tag{35}$$

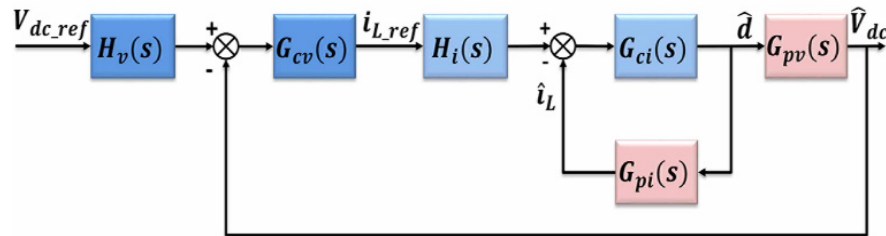


Figure 4. Control structure of IHGBC for one phase.

In Figure 4, $H_v(s)$ and $G_{cv}(s)$ represent the outer voltage loop of the LADRC to obtain the phase current reference from the difference between the measured DC bus voltage and the reference DC bus voltage, and $H_i(s)$ and $G_{ci}(s)$ represent the LADRC inner current loop, which allows the duty cycle from the difference between the measured current and the reference current to be obtained.

$G_{pv}(s)$ and $G_{pi}(s)$ are the transfer functions defined, respectively, with the following equations.

$$G_{pv}(s) = \frac{\hat{V}_{dc}}{\hat{d}} = \frac{-2RLI_Ls + DRV_{dc}}{2RLCs^2 + 2Ls + DR} \tag{36}$$

$$G_{pi}(s) = \frac{\hat{i}_L}{\hat{d}} = \frac{V_{dc}RCs + DRI_L + V_{dc}}{2RLCs^2 + 2Ls + DR} \tag{37}$$

where R is the load, and $D = 1 - d$.

By combining (18), (19), (24), (26), (31) and (33), the LADRC transfer functions-based control law can be expressed as:

$$H_v(s) = \frac{k_{pv}(s^2 + \beta_{21}s + \beta_{22})}{(k_{pv}\beta_{21} + \beta_{22})s + k_{pv}\beta_{22}} \tag{38}$$

$$G_{cv}(s) = \frac{1}{b_2} \frac{(k_{pv}\beta_{21} + \beta_{22})s + k_{pv}\beta_{22}}{s(s + \beta_{21} + k_{pv})} \quad (39)$$

$$H_i(s) = \frac{k_{pi}(s^2 + \beta_{11}s + \beta_{12})}{(k_{pi}\beta_{11} + \beta_{12})s + k_{pi}\beta_{12}} \quad (40)$$

$$G_{ci}(s) = \frac{1}{b_1} \frac{(k_{pi}\beta_{11} + \beta_{12})s + k_{pi}\beta_{12}}{s(s + \beta_{11} + k_{pi})} \quad (41)$$

5. Simulation Results

The simulations of the IHGBC converter and the proposed LADRC control were performed using MATLAB/SIMULINK. The performance and stability of the system are checked under different operating scenarios and the proposed controller is compared with the classical PI controller and sliding mode control (SMC) to prove the advantage of the proposed strategy. Table 1 shows the simulation parameters used for the IHGBC converter and controller.

Table 1. Simulation parameters.

| Parameters | Specifications |
|--|--------------------|
| DC bus voltage V_{bus} | 80–200 V |
| Switching frequency, f_s | 10 KHz |
| Inductors, L_1, L_2, L_3, L_4 | 440 μ H |
| Boost capacitors CB_1, CB_2 | 47 μ F /100 V |
| Input capacitor, C_{in} | 4.7 mF/400 V |
| Output capacitor, C_o | 330 μ F /400 V |
| $\omega_{c1}, \omega_{01}, b_1$ | 1200, 6000, 21,000 |
| $\omega_{c2}, \omega_{02}, b_2$ | 50, 450, 490 |
| PI parameters (voltage loop), $Kp1, Ki1$ | 0.4, 4.5 |
| PI parameters (current loop), $Kp2, Ki2$ | 0.5, 30 |

First, the performance of the proposed converter is evaluated in an open loop by performing tests at different duty cycle values. The obtained results are shown in Figure 5a–d. During the entire operation, the input voltage is fixed at 20 V with a load resistance of 100 Ω .

Figure 5a–c show the input current, phase currents and inductor currents at duty cycle values of 0.3, 0.5, 0.67, respectively, while Figure 5d represents the obtained output voltage values. The output voltage ranges from 57 V to 121 V with a duty cycle change from 0.3 to 0.67.

These results confirm the ability of the proposed converter to achieve high voltage gain with less current ripple. Moreover, the evolution of the output voltage and the duty cycle correspond to Equation (6).

Second, the output voltage reference was increased from 100 to 120 volts and then decreased from 120 to 100 volts in order to test the robustness of the proposed controller.

Figure 6 shows the output voltage response of the conventional PI, sliding mode control and the proposed LADRC controller. As can be seen, the proposed LADRC controller provides better performance with a fast response and perfect traceability of the output voltage reference compared to PI control and sliding mode control.

To further verify the efficiency of the IHGBC converter, and the proposed LADRC control, the converter is controlled in a closed loop in order to regulate the DC bus voltage to multiple values, between 80 and 200 volts. The input voltage is set to 20 V with a 150 Ω resistance load.

Figure 7 confirms that the proposed converter has the ability to provide good efficiency and high voltage gain. The results also confirmed, once again, the efficiency of the LADRC to deliver the DC bus voltage to the desired value faster.

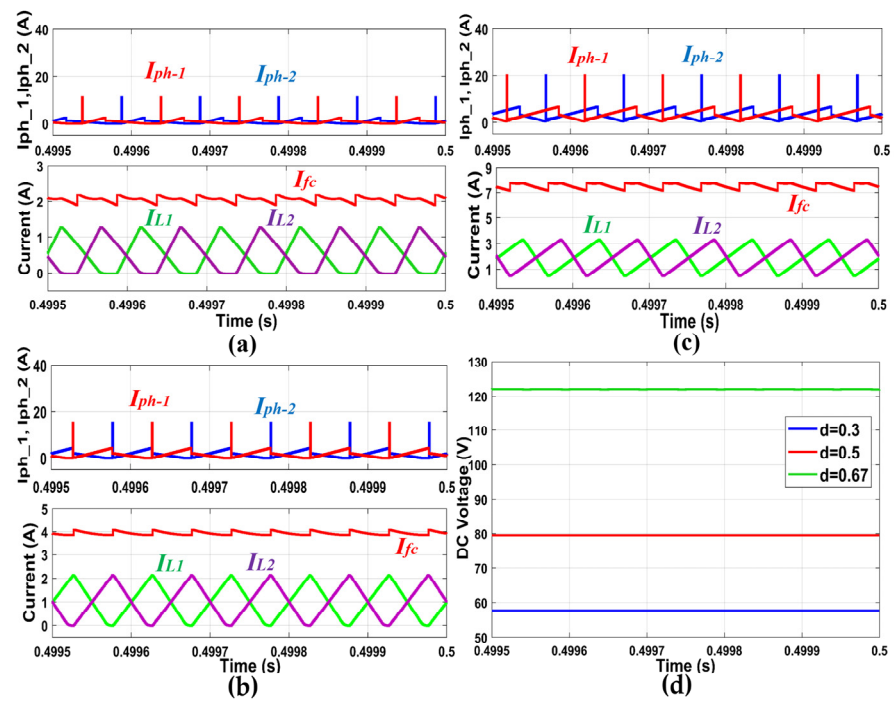


Figure 5. IHGBC simulation results: (a–c) show the input current, phase currents and inductor currents at duty cycle values of 0.3, 0.5, and 0.67, respectively. While (d) the obtained output voltage values.

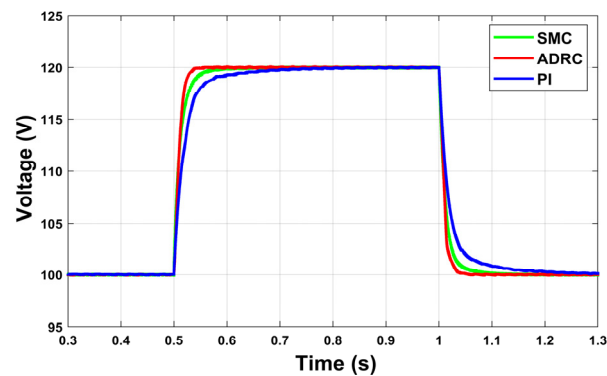


Figure 6. Output voltage responses.

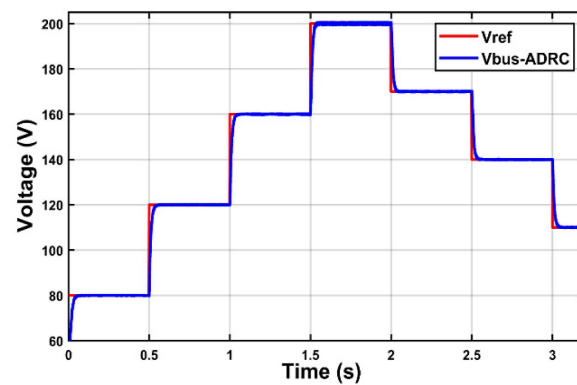


Figure 7. Output voltage response for different voltage reference.

The output voltage reference is fixed at a value of 100 and then 120 volts, then the stability of the system is tested under different operating points (different input voltage values and load resistance are selected).

Figure 8 shows the converter performance of the proposed LADRC controller, sliding mode control and the PI controller. By comparing the results of the three methods under similar conditions, the LADRC controller provides optimum performance with voltage stability at different operating points. In contrast, the performance of the SMC and PI controller records overshoots and deviations from the output voltage reference as operating points change.

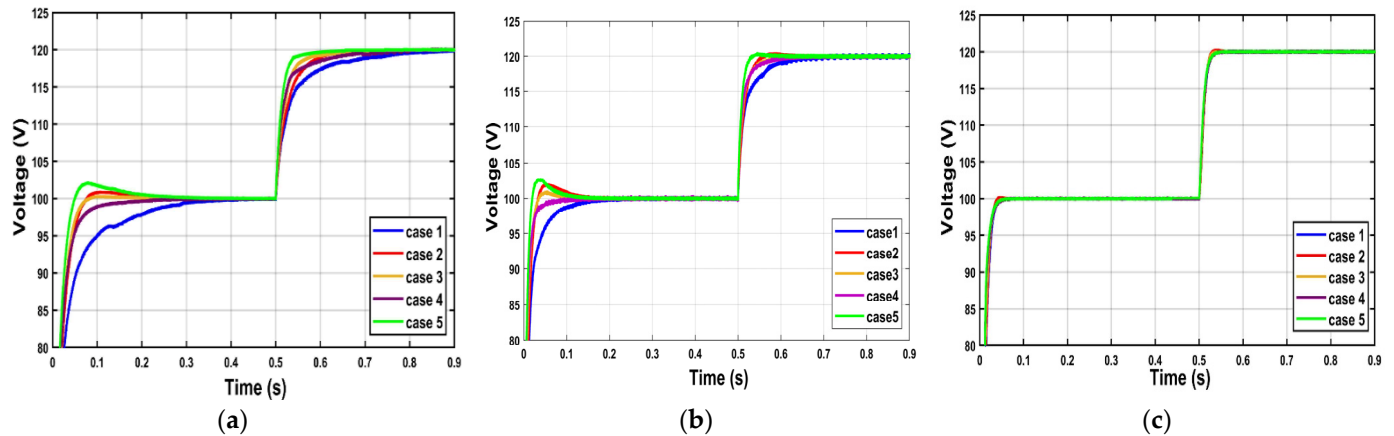


Figure 8. Output voltage responses with different operation points, (a) PI control (b) SMC (c) proposed LADRC. Case 1: $V_{fc} = 15$ V, $R = 100 \Omega$; case 2: $V_{fc} = 15$ V, $R = 200 \Omega$; case 3: $V_{fc} = 20$ V, $R = 150 \Omega$; case 4: $V_{fc} = 25$ V, $R = 100 \Omega$; case 5: $V_{fc} = 25$ V, $R = 200 \Omega$.

6. Experimental validation

In order to test and verify the robustness and the efficiency of the proposed LADRC dual-loop control, tests were carried out on an experimental prototype of the interleaved gain high DC-DC boost converter, as shown in Figure 9.

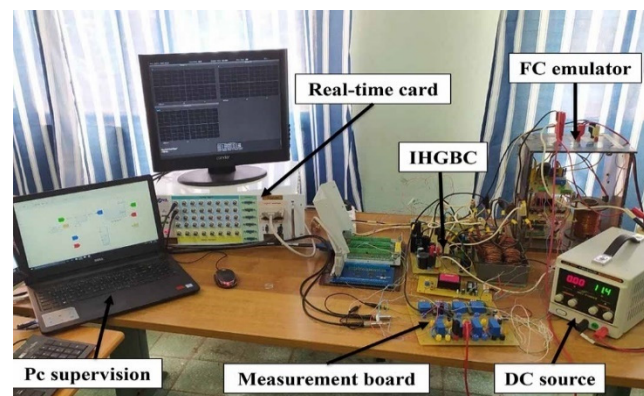


Figure 9. Experimental test bench.

The experimental test bench consists of a real-time PEMfc system emulator to reproduce the same characteristics of a real PEMfc, an IHGBC DC/DC converter, a resistive load, a measurement card, a development real-time card and, finally, a PC to save the data obtained using MATLAB software.

The fuel cell model presented in Section 2 and the DC/DC converter control methods are implemented on a real-time board, the latter being used for the control and data acquisition of the IHGBC converter and FC emulator.

The operation principle of the PEMFC emulator is presented in Figure 10; it consists mainly of a DC/DC buck converter. The output current of this converter is used as input to the fuel cell model. The model allows the reference voltage to be used, which is compared to the measured voltage, and regulated using a PI regulator, to generate the PWM control signals, so the buck converter is controlled in the voltage.

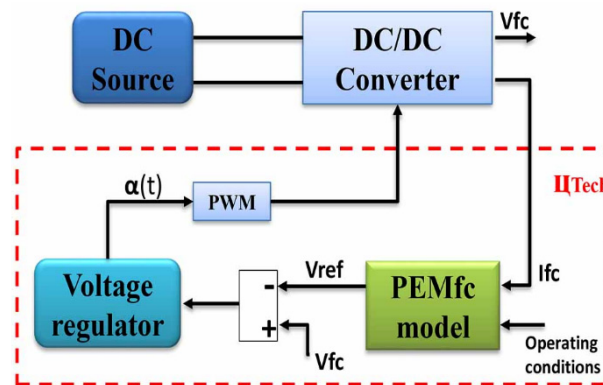


Figure 10. Architecture of PEMFC emulator.

The PWM gate control signals are generated by a PWM signal generator block provided by the real-time board library in the MATLAB Simulink environment. The IHGBC converter and controller's parameters are summarized in Table 2.

Table 2. Experimental parameters.

| Parameters | Specifications |
|--|-----------------------|
| Switching frequency, f_s | 10 KHz |
| Inductors, L_1, L_2, L_3, L_4 | 440 μ H |
| Boost capacitors C_{B1}, C_{B2} | 47 μ F/100 V |
| Input capacitor, C_{in} | 4.7 mF/400 V |
| Output capacitor, C_o | 330 μ F/400 V |
| Switch 'S1', 'S2' | IRFP260 (200 V, 50 A) |
| Diodes D_1, D_2, D_3, D_4, D_o | RHRG3060 |
| Diodes $Ds1, Ds2$ | RHRG3060 |
| $\omega_{c1}, \omega_{01}, b_1$ | 500, 1750, 1600 |
| $\omega_{c2}, \omega_{02}, b_2$ | 30, 270, 851 |
| PI parameters (voltage loop), $Kp1, Ki1$ | 0.05, 0.5 |
| PI parameters (current loop), $Kp2, Ki2$ | 0.01, 10 |

Various operating modes are made to check the behavior of the considered system and the proposed controller.

The superiority of the proposed method was first demonstrated by comparing the proposed LADRC controller with the classical PI controller. The main purpose is to make the DC bus voltage follow its reference and provide a disturbances rejection.

Figures 11–13 show the system response for a reference change in the output voltage from 100 V to 120 V between moment 4 s and 6 s.

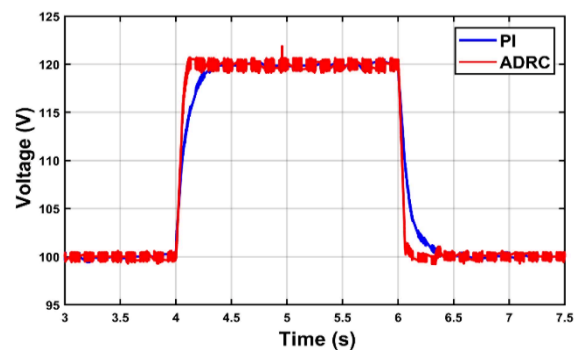


Figure 11. Output voltage responses.

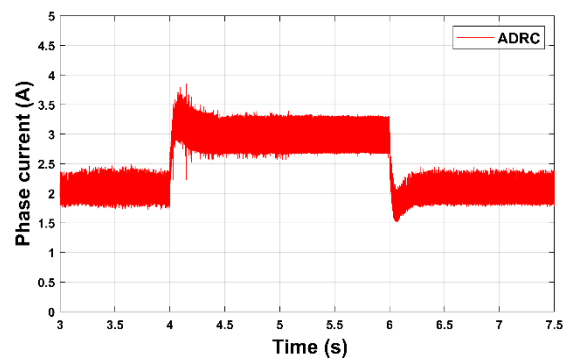


Figure 12. IHGBC phase current.

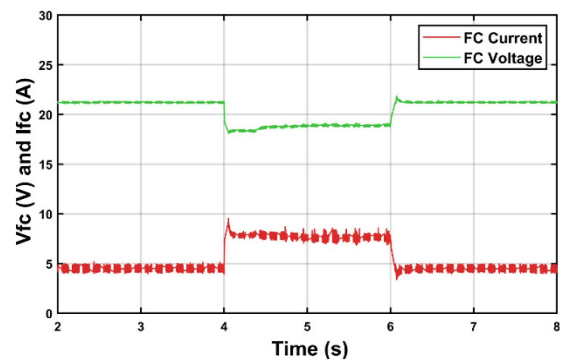


Figure 13. PEMFC emulators current and voltage.

As can be seen from Figure 11, the two controllers can reach the desired value, but the proposed LADRC proves its superiority by perfect tracking of the output voltage reference with a fast response and without any overshoot during rise or fall. The phase current response after the reference change in the output voltage is shown in Figure 12.

An increase in output voltage leads to an increase in phase current and PEMFC emulator current, and, consequently, the PEMFC emulator voltage decreases depending on the fuel cell nature, as shown in Figure 13.

Second, to check how well the controller can ensure a stable output voltage under different loads, a variable load current is applied, by abruptly changing the load resistance from 150Ω to 100Ω . The phase current rises from 2 A to 3 A during this period (Figure 14) to meet the load requirements, while the proposed control algorithm reacts instantly in order to maintain the output voltage constant at the desired reference, as shown in Figure 15. At the same time, Figure 16 shows that the controller PI takes a long response time and with greater deflection.

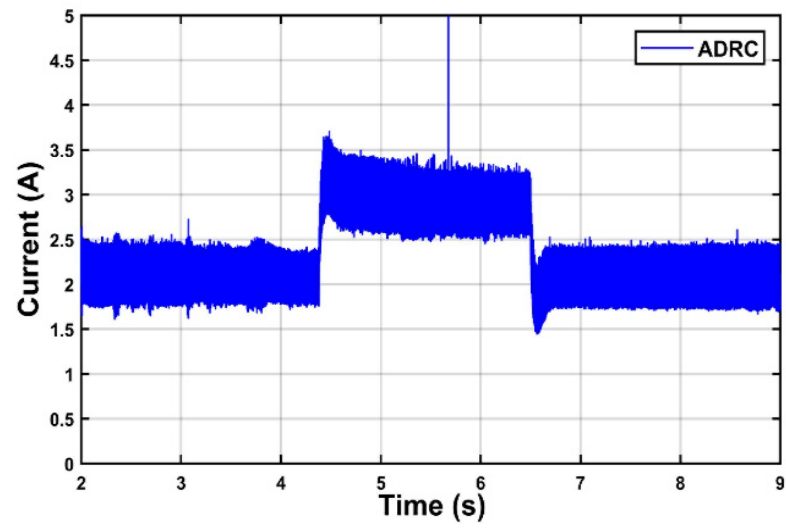


Figure 14. IHGBC phase current.

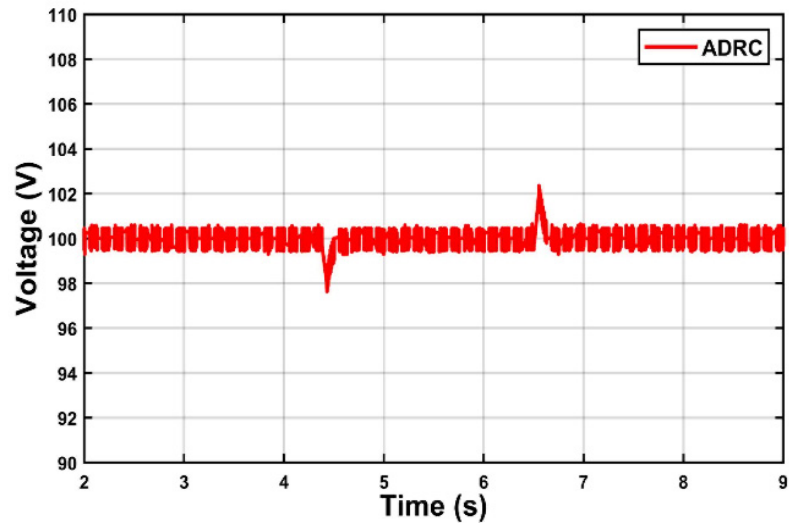


Figure 15. Output voltage response.

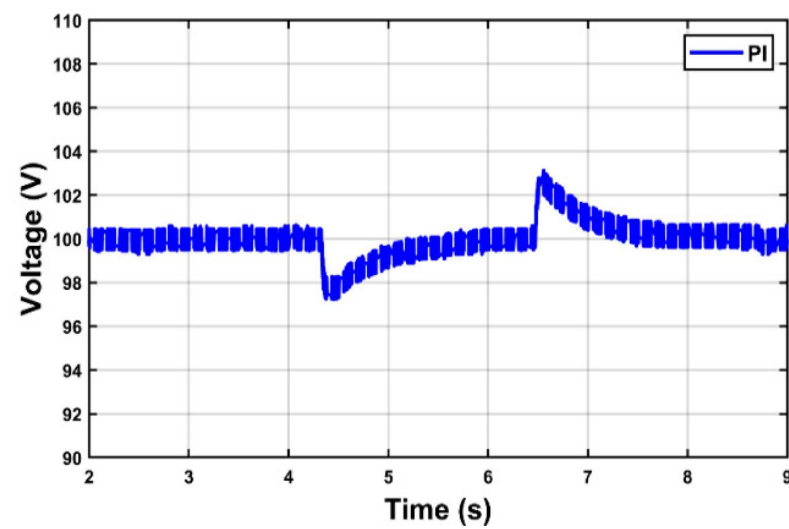


Figure 16. Output voltage response.

Figure 17 shows the PEMFC emulator current and voltage, respectively.

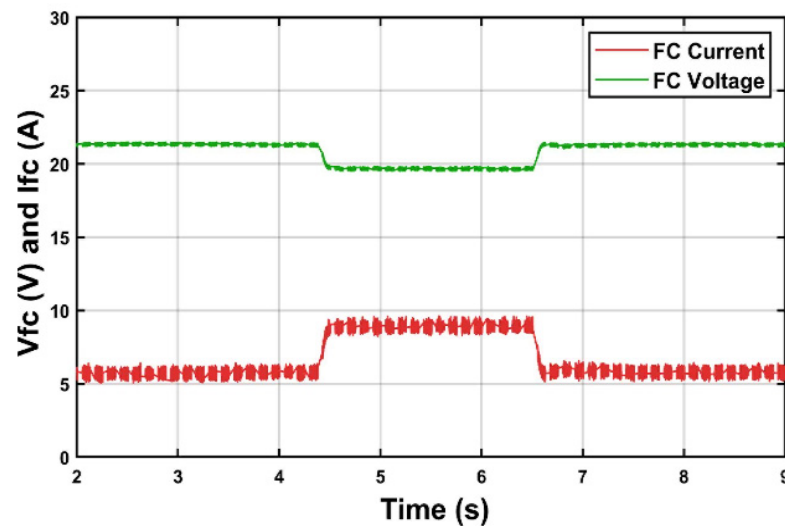


Figure 17. PEMFC emulator's current and voltage.

7. Conclusions

To improve the control performance and ensure the stability and fast response of the DC/DC boost converter under parameter uncertainties and disturbances, a robust two-loop control based on a linear active disturbance rejection control is proposed in this paper. It includes an internal current control loop and an external voltage control loop of an interleaved high gain DC/DC boost converter associated with the proton exchange membrane fuel cell system. This converter provides high efficiency and high voltage gain with reduced voltage stress on the switches and diodes. In addition, the interleaving technique and the parallel structure of the converter guarantee low input current ripple and reduce the size of the passive components and its modularity also offers fault tolerant capabilities.

The robustness and effectiveness of the proposed controller have been confirmed by simulations and experimental results. The results showed that the proposed control unit provides good dynamic performance and stability under different operating conditions. Moreover, the performance of the proposed control still needs to be verified against other advanced control techniques. Additionally, a number of ongoing research studies show that strong robustness can be provided by relying on a hybrid control between LADRC and other control algorithms, and this will be one of the directions of our future research.

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