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Brief Report

A Compact Five-Level Single-Stage Boost Inverter

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Abstract: This article presents a single-stage five-level boost inverter (5L-SBI) topology with reduced power components. The proposed topology falls under the self-balanced switch-capacitors (SCs) type and combines both a DC/DC boost converter and inverter with a switched-capacitor cell. The advantages of proposed topologies include the following: the number of switch counts is reduced, the maximum voltage gain is two times higher than the input voltage, and the capacitor's charging current is suppressed. Further, the proposed topology cascaded, and three-phase extensions are presented. To attest, the advantages of the proposed topology are thoroughly compared with other recent SCI topologies. The proposed topology is verified under dynamic loading conditions, and the results are presented, considering a 600 W laboratory prototype model.

Keywords: boost inverter; reduced component; cascaded; five-level

1. Introduction

Distributed power generation increases every day because of the increasing electricity demand. The power electronics interface is major equipment that can support producing highly reliable and efficient power generation. However, the cost of the power electronics interfaces is high, and it operates in two-stage power conversion [1]. The multilevel inverters (MLIs) are well-matured and promising power converter technology. The MLIs are widely used in several applications such as AC drives, large-scale grid-tied PV or wind systems, heavy track electric vehicles, etc. However, the conventional MLIs have several drawbacks such as a high component count, multiple DC sources and voltage balancing problems in DC-link capacitors. The continuous effort and contribution to research yield new promising power converter topologies that are highly efficient for broad applications, including distributed power generation. In recent years, switched-capacitor multilevel inverter (SCMLIs) topologies with boosting abilities are quite famous due to their features such as self-voltage balancing, high voltage gain and reduction in power components [2]. The studies [3–5] propose a new five-level switched-capacitor inverter topology. The voltage gain of these topologies is two times higher than the input voltage (v_{in}). However, the total power component count is high, and the source current will be high during the capacitor charging current, which limits the several applications including the PV system. Further, these SCMLI topologies require high current rating switches and DC sources to charge the capacitor [6], and this is a remarkable drawback of SCMLI topologies. To suppress the high charging current (also known as inrush current), the current limiting component can be used between the DC source and switched-capacitors (SCs). Here, the inductor is used as a current limiting component and can act as a boost converter with a combination of switches and SCs. Moreover, the design of the current limiting inductor is not yet well defined and the validation of inverter with current limiting inductor is still under study. Several studies have taken an alternative approach in their research: In [7], the cascaded H-bridge, MLI is presented with a front DC/DC boost converter for each module. Each module required the addition of a full bridge in the capacitor, inductor

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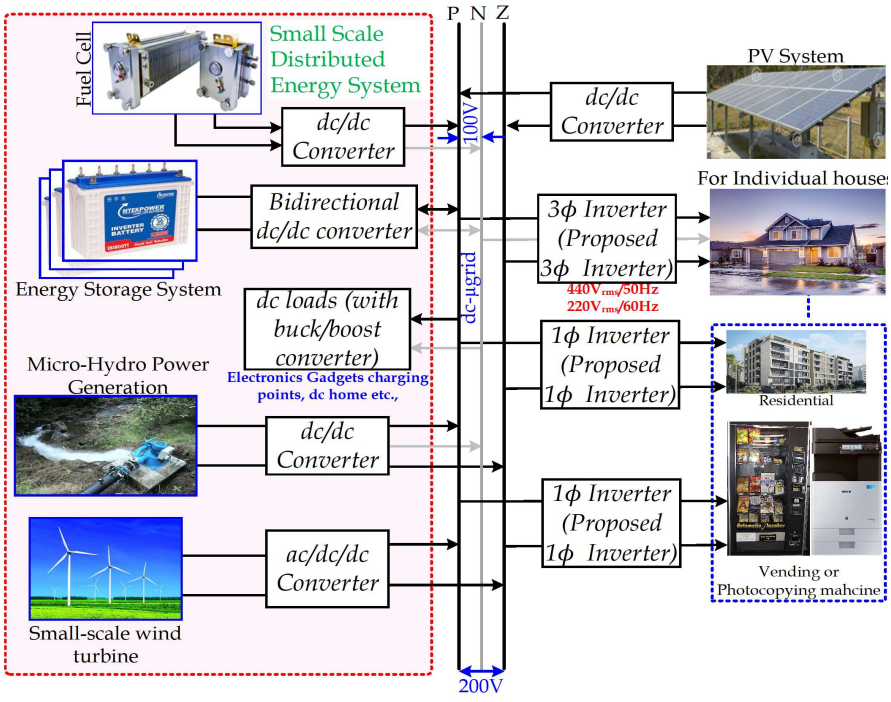
and diode. So, the number of power components is high, but with reduced voltage stress. The single DC source quasi-Z-boost inverter topology is presented in [8,9], with higher voltage gain than [7], but both topologies require a higher number of passive and active components. The integrated DC/DC converter with the inverter is proposed in [8]. In this study, the DC decoupling technique is used to suppress the leakage current. Moreover, this topology needs more power components. In [10], a five-level diode-clamped inverter topology with a boost converter circuit is recommended for AC load. The boost circuit is combined with an auxiliary component to balance the DC-link capacitor. A dual-mode interleaved multilevel inverter is presented in [11]. The topology operates in buck and boost mode, but the number of passive and active components is high. More than five-level output waveforms are generated with switched capacitor circuits [12,13]. Moreover, in [12], the inductor reduces the charging current, and the [13] produces an asymmetrical output voltage waveform which produces a high total harmonic distortion and leads to a complex filter design. Another topology with a single DC source and less passive component is proposed in [14], but this topology needs more active devices and a complex pulse generation scheme. Cassiano et al. developed a new SC-based five-level inverter topology which has the voltage boosting ability [15]. However, the suppression of the high capacitor charging current is not discussed and the required number of active switches are high. Another five-level, grid-tied inverter without voltage boosting ability is presented in [16] with common ground to suppress the leakage current.

The existing topologies have various drawbacks, such as drawing high input current, increasing the DC source count, and increasing passive components and semiconductor devices count. Furthermore, the proposed topology can extend "*n*" by a simple cascading of the basic unit. Figure 1a presents the typical schematic of the DC microgrid. The various power sources with regulated outputs are connected to the bipolar DC-microgrid (0 V–100–200 V). Further, to connect with AC applications, the inverter with boost converter is necessary. This paper introduces a new single-stage boost inverter, as shown in Figure 1b, with a reduced component count, which overcomes the existing topologies drawbacks as discussed above.



(**a**)

Figure 1. *Cont.*

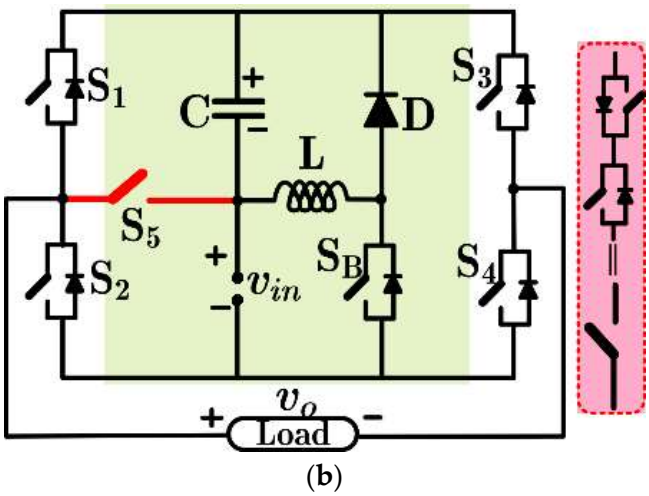


Figure 1. (**a**) Schematic diagram of microgrid system for small scale DES; (**b**) proposed 5L-SB inverter topology (L—inductor, D—diode, C—capacitor, v_{in}—input voltage, v_o—output voltage, S_1-S_5, S_B—switches).

2. Proposed 5L-Single Stage-Boost Inverter (SBI) Topology

2.1. Description of Proposed Topology

The proposed 5L-SBI topology is shown in Figure 1b. It uses one capacitor, inductor, diode, and seven switches to generate the 5L output voltage with a double voltage gain, and uses a single DC source that is connected to series with the SC. One end of the inductor is connected to the mid-point of the DC source and SC in the proposed topology, whereas the other is connected to the switch S_B. The boost switch (S_B) works independently and can be controlled by changing the duty cycle (d). The S_5 is a bidirectional switch, and it can be two switches with an anti-series connection or four diodes with one switch. However, both switches can be used, and there are no changes in the performance of the inverter.

2.2. Steady-State Operation

Each mode of operation for five-level is depicted in Figure 2a–e. In each mode of operation, the S_B is independent of the other switches, which is one of the advantages of the proposed topology. The switch S_5 is turned on and off for both ±1st level, and S1 and S2 switches are turned on the +2nd and −2nd level, respectively, but the S3 and S4 the turned on both +1st, +2nd and −1st, −2nd level. The switch S_B is adjusted to meet the load requirement during source voltage variation. In [14], the duty cycle of the boost switch is combined with the inverter switching sequence, which is complex to the precious voltage regulation.

Level +1: As shown in Figure 2a, the inductor is charging during the S_B turned ON and discharge when the S_B is turned OFF and charge the capacitor C, i.e., the capacitor voltage is equal to inductor voltage $V_C = V_L$. Simultaneously, the switches S_5 and S_3 are turned on to tap the capacitor voltage across the load.

Level +2: During the positive half cycle second level, the S_B is operated separately i.e., irrespective of S_B operation, the switches S_2 and S_3 are turned on to produce the sum of the v_{in} + V_C across the load, as shown in Figure 2b.

Level 0: As discussed earlier, the boost operation is independent to the inverter operation and the inductor continuously charges and discharges to charge the capacitor. Simultaneously, the switches S_2 and S_4 are turned ON to produce the zero level as illustrated in Figure 2c.

Level −1: As shown in Figure 2d, in first negative half cycle, the inductor charges during the S_B is turned ON and discharges when the S_B is turned OFF and charges the capacitor C, i.e., the capacitor voltage is equal to inductor voltage $V_C = V_L$. Simultaneously, the switches S_5 and S_4 are turned on to tap the source voltage across the load i.e., $v_o = v_{in}$.

Level −2: During the negative half cycle second level, the S_B is operated separately i.e., irrespective of S_B operation the switches S_1 and S_4 are turned to produce the sum of the $-(v_{in} + V_C)$ across the load, as shown in Figure 2e.

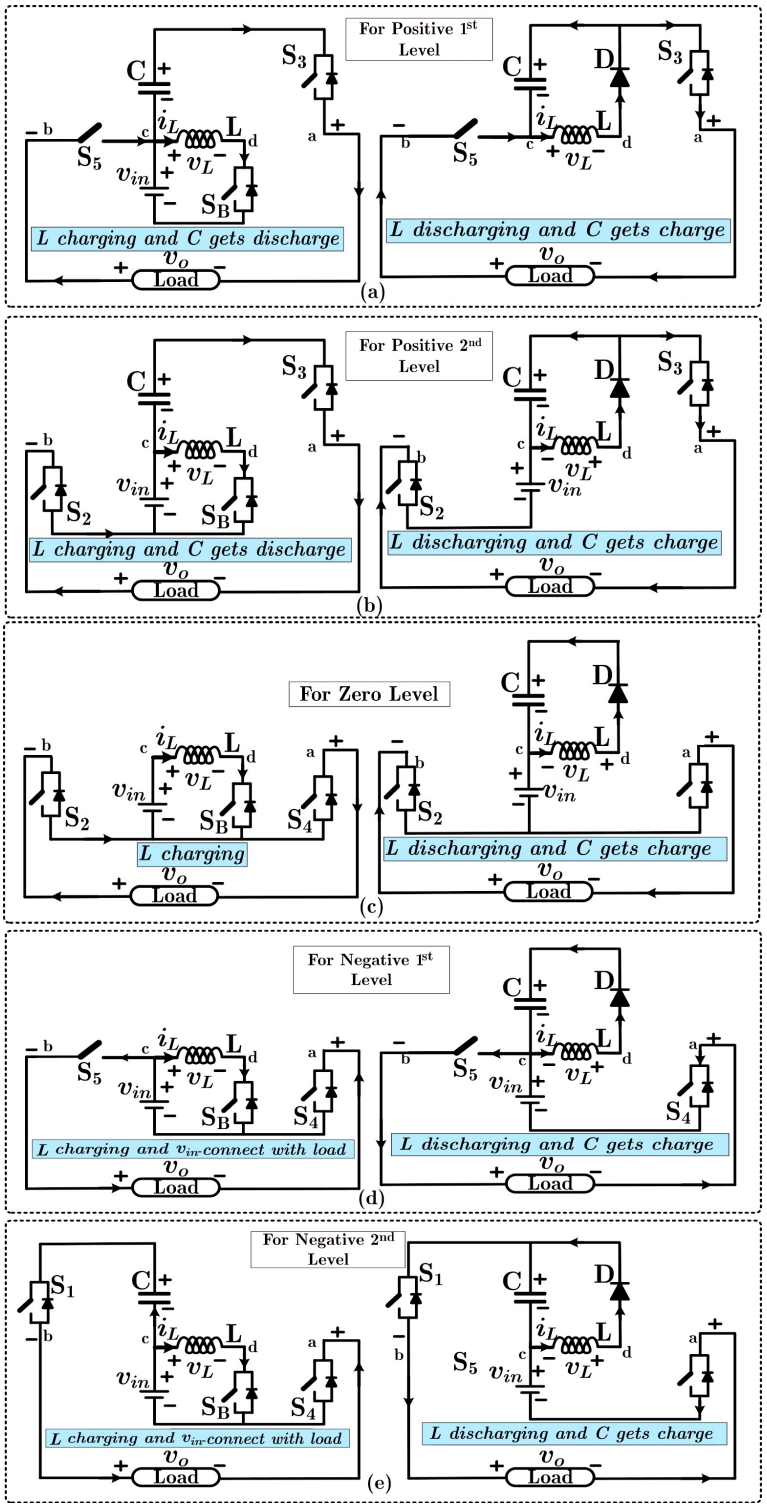


Figure 2. Modes of operation of proposed 5L-SB inverter topology with inductor charging and discharging for (**a**) +Level −1, (**b**) +Level −2, (**c**) Zero level, (**d**)−Level −1, (**e**) −Level −2. (v_L-inductor voltage, i_L-inductor current, L—inductor, D—diode, C—capacitor, v_{in}—input voltage, v_o—output voltage, S_1-S_5, S_B—switches).

2.3. Analysis and Design of Passive Components

Given that the proposed inverter topology operates in a symmetric output voltage waveform, the duty cycle of the S_B is kept at 50%, which gives two times voltage gain. Further, by operating at 50% of the duty cycle, the voltage stress on the capacitor is reduced to 50%. Figure 2 shows that the capacitor charged to ($v_o - v_{in}$) through the inductor (L). The mathematical expression for the various current and voltage parameters is given as follows: The maximum output voltage is two times higher than the input voltage, and the corresponding voltage gain (G) is given in Equation (1). Because the load is resistive-inductive, the output voltage is obtained from Equation (2)

$$G = Mv_{in}/(1-d) = 2Mv_{in} \tag{1}$$

$$v_o = R_o i_o + L_o(di_o/dt) \tag{2}$$

where M is the modulation index of the inverter, and d- is the duty cycle. The average current of the inductor is zero at steady-state conditions. So, the capacitor voltage is given in Equation (3)

$$V_C = v_o - v_{in} \tag{3}$$

Due to variation in the duty cycle, the voltage across the capacitor also varies, and it can be obtained from Equation (4)

$$V_C = (v_{in}/(1-d)) - v_{in} \tag{4}$$

Here, it is worth mentioning that the capacitor voltage is reduced to 50% compared to a conventional boost DC/DC converter. The current flow of the inductor at 50% of the duty cycle, the average power (P_{avg}) flowing into the C is

$$P_{C,avg} = 0.5 \times i_L \times v_{in} \tag{5}$$

The inductor and capacitor ripple voltage is

$$\Delta V_C = \frac{0.5(v_o - v_{in})}{R_o f_s C} \tag{6}$$

$$\Delta i_L = \frac{v_o d(1-d)}{f_s L} = \frac{0.25 \times v_o}{f_s L} \tag{7}$$

Existing SCMLI topologies suffer due to a high charging current, also known as inrush current. To avoid the high charging current, the inductor is inserted between the DC source and capacitors.

The series connection of the capacitor to the source leads to producing pulsated DC current, and the source RMS current ($i_{Sou,rms}$) is a sum of the capacitor RMS current ($i_{C,rms}$) and inductor RMS current ($i_{L,rms}$).

$$i_{Sou,rms} = i_{L,rms} \tag{8}$$

$$i_{Sou,rms} = i_o\left(\frac{1}{1-d}\right) = 2i_o \tag{9}$$

Further, the stress on the boost switch (S_B) is given in Equation (10)

$$i_{SB} = \left(\frac{i_o}{1-d}\right) + \left(\frac{\Delta i_L}{2}\right) = (2i_o + 0.5\Delta i_L) \tag{10}$$

It is confirmed that the maximum current stress across the circuit has not exceeded two times the load current ($i_{sou} = 2i_o$) with voltage boosting, but in the case of the SCMLI topologies, the inrush current is $5v_{in} > v_{in}$. The pulse generation scheme is shown in

Figure 3. In this *reference signal (v_{ref})* is compared with triangle carrier signals *(v_{tr1}, v_{tr2}) for inverter operation,* and constant signal (v_{con}) for boost operation. The v_{con} compared output is given to the $S_{B,}$ and the rest of the comparator output is given to the inverter operation.

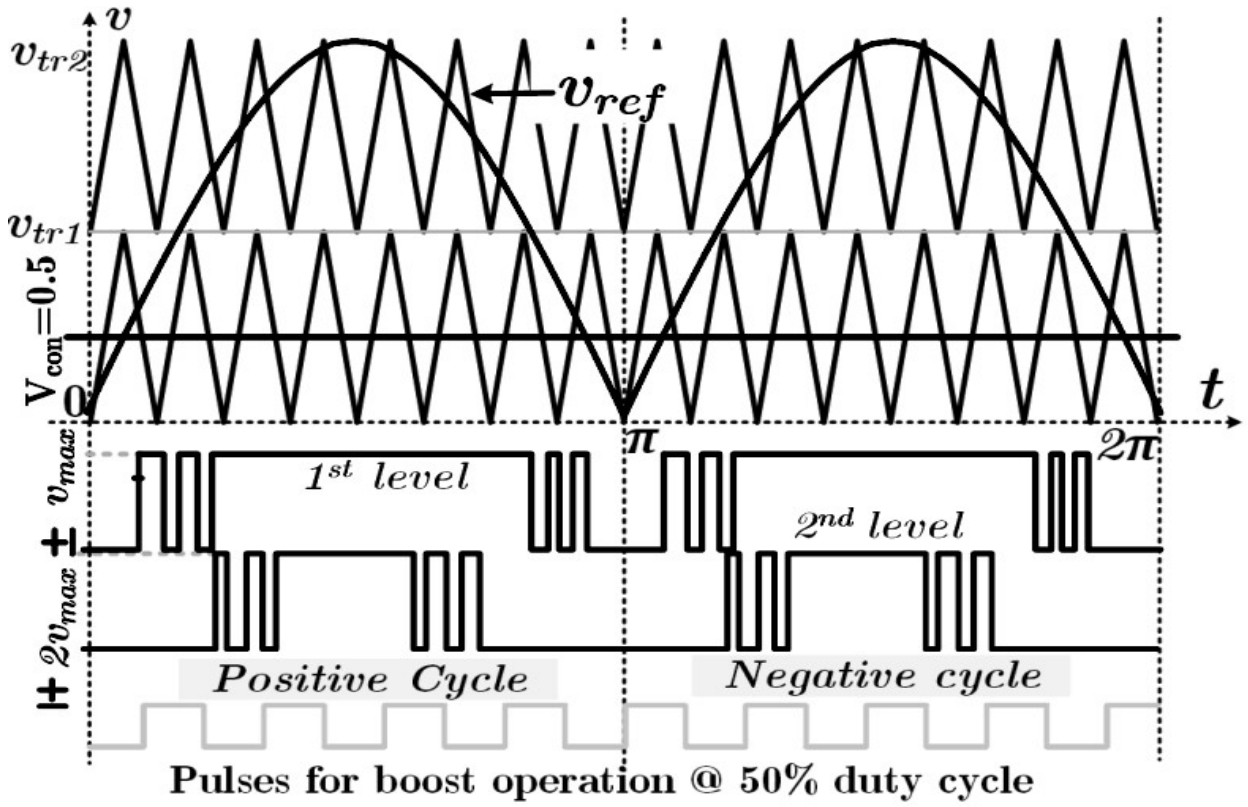


Figure 3. Pulse Width Modulation Scheme (v_{tr1},v_{tr2}—Triangle carrier signal, v_{ref}—reference signal, v_{con}—constant signal, v_{max}—maximum voltage, v—amplitude, t—time scale for one cycle (20 ms)).

2.4. Cascaded Extension

The proposed topology can be extended to the "n" number by cascading each module, as shown in Figure 4a. The cascaded topology has symmetric DC source magnitude i.e., $v_1 = v_2 = v_3 = \ldots = v_n = v_{in}$. The proposed cascaded topology produces a higher voltage level than the cascaded H-bridge (CHB) topology in a symmetric configuration. The proposed topology can be configured in an asymmetric configuration by keeping the non-symmetric DC source magnitude. Here, the voltage gains and determination of the magnitude of the DC source are obtained from Equations (11)–(13).

$$v_1 = v_{in}, v_2 = 5v_{in}, \ldots, v_n = 5^{n-1}v_{in} \tag{11}$$

$$N_{Level} = 5^n \tag{12}$$

$$G = 2\sum_{x=1}^{n}(v_1 + v_2 + v_3 + \ldots + v_x)v_{in} = 2v_{in}\sum_{i=1}^{n} v_i \tag{13}$$

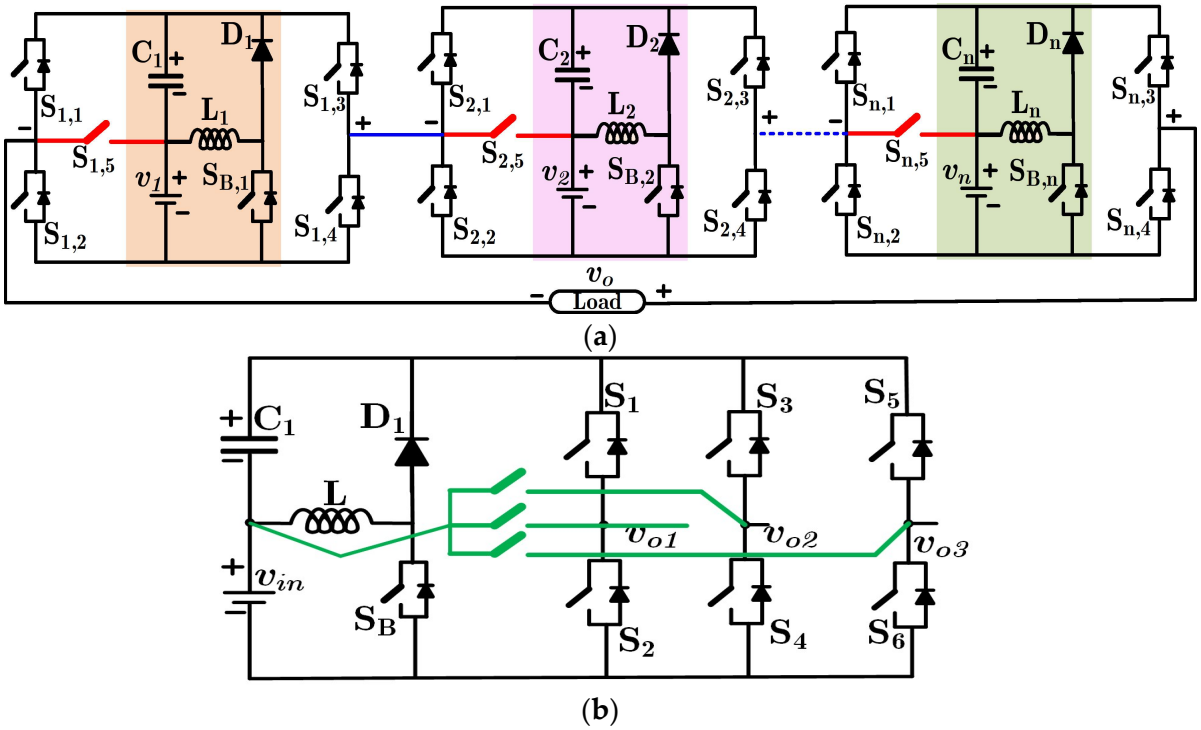


Figure 4. Extended Structures of proposed topology (**a**) cascaded extension and (**b**) 3ϕ- extension. (L_n—inductor, D_n—diode C_n—capacitor, v_n—input voltage v_o, n—output voltage, $S_{n,1}$-$S_{n,5}$, $S_{n,B}$—switches, where n = 1,2,3 . . .).

2.5. 3ϕ(Three Phase)-Extension

Another advantage of the proposed topology is it can be extended as a 3ϕ inverter, as shown in Figure 4b. Further, the required number of switches, driver circuits and passive components are given in Table 1.

Table 1. Comparison of proposed topology and [14].

Description	For 1ϕ Inverter			For 3ϕ Inverter	
	[14]	Pro. Symmetric	Pro. Asymmetric	[14]	Proposed
N_{Level}	4n + 1	4n + 1	5n	5	
N_{IGBT}	10n/9n	7n	7n	24	18
N_{Driver}	8n/7n	6n	6n	18	15
N_{Diode}	n	n	n	1	1
N_{Ind}	n	n	n	1	1
N_{DC}	n	n	n	1	1
Gain	$2nv_{in}$	$2nv_{in}$	$2v_{in}\sum_{i=1}^{n} v_i$	$2v_{in}$	
MVS	$2v_{in}$	$2v_{in}$	$2 \times 5n - 1v_{in}$		
TVS	$14nv_{in}$	$12nv_{in}$	$12v_{in}\sum_{i=1}^{n} v_i$	$24v_{in}$	$18v_{in}$

3. Results and Discussions

The proposed topology's performance and feasibility were simulated, and the prototype model was developed for 600 W. The simulation results show that the proposed topology gain is two times higher than the v_{in} with a lagging power factor of 0.85, and the corresponding waveforms are shown in Figure 5. The maximum source current is 8 A. The capacitor current is limited to 5 A. Here, it is worth mentioning that the source current is minimized in 5L-SBI, whereas in SCMLI topologies, the i_C is five times higher than the i_o.

The input voltage of 100 V is taken from the 200 V/100 A three-phase rectifier unit, and the output voltage is 200 V/50 Hz. The variable resistor and inductor coil is used as a load. The Texas instrument TMS320F28739D is used to generate the gate pulses.

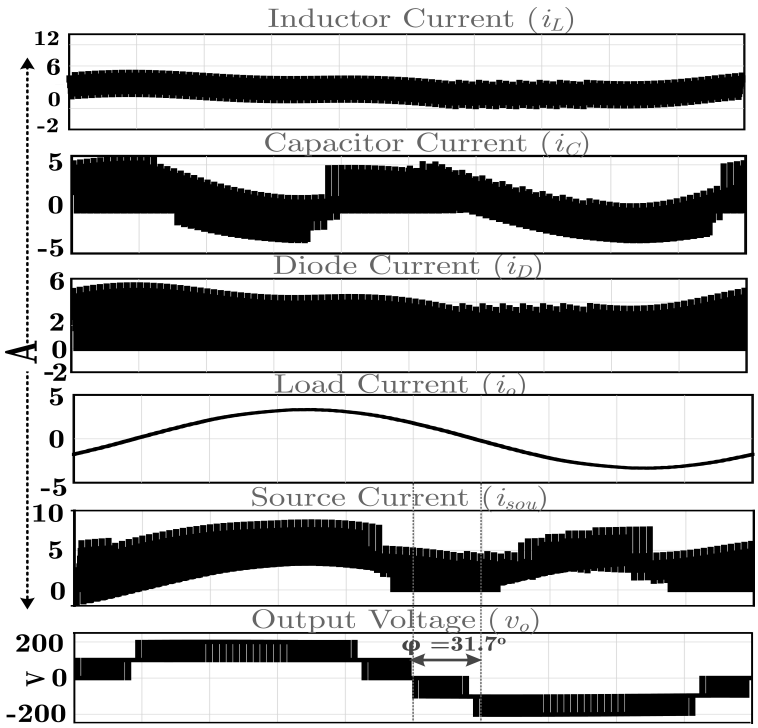
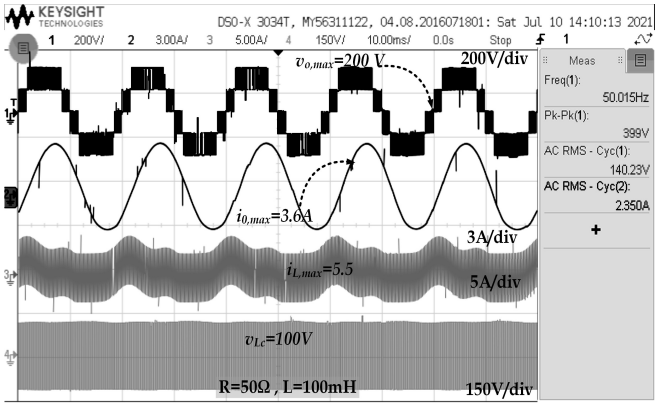


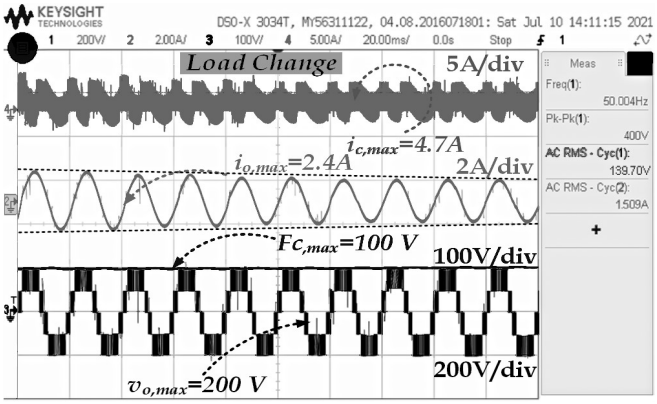
Figure 5. Simulation results for R = 50 Ω and L = 100 mH.

The capacitor PG-6DI is used at 150 V/470 µF and a ferrite core type inductor with a value of 2 mH for both simulation and prototype. The SKM75GB63D Semikron IGBTs are used, and the gating signals are driven by TLP 250. The power diode MUR1520G is used. The switching frequency is 20 kHz, and the fundamental frequency is 50 Hz. However, this type of circuit suffers from the pulsated DC source current due to the series connection of the capacitor. The experimental results are shown in Figure 6. In Figure 6, the output voltage and current are measured. Because the 5L-SBI is a boost-type inverter, it is necessary to measure the voltage and current of the inductor, as presented in Figure 6a. It confirms that the inductor voltage is equal to the source voltage.

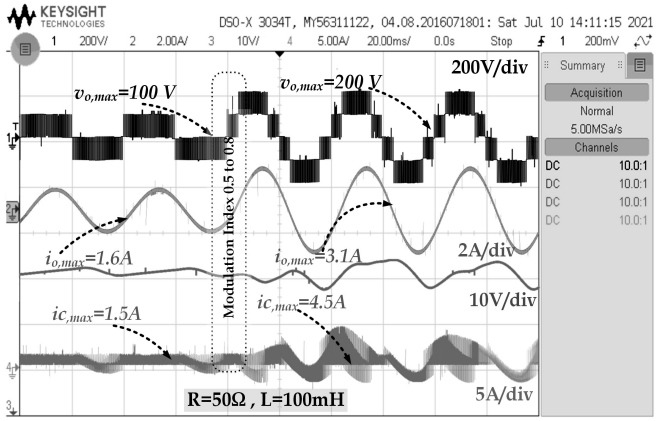


(**a**)

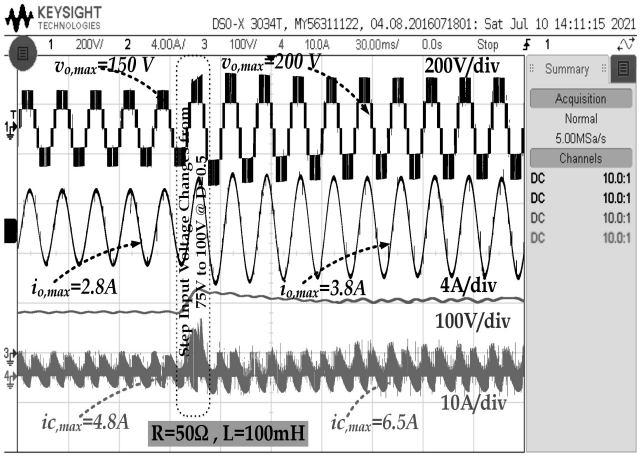
Figure 6. *Cont.*



(**b**)



(**c**)



(**d**)

Figure 6. Experimental results of proposed 5L-SBI (**a**) v_o, i_o and V_L, i_L, (**b**) output voltage with load change, (**c**) changing of modulation index, and (**d**) step input change. ($v_{o,max}$—maximum output voltage, $i_{o,max}$—maximum output current, $i_{o,max}$—maximum capacitor current, v_L—inductor voltage, FC_{max}—maximum capacitor voltage).

The result of transient operation during the load changing from unity (R = 100 Ω) to non-unity (R = 50 Ω to L = 100 mH) power factor (0.85) is shown in Figure 6b. It is demonstrated that the load voltage is not deteriorating, and the current is exhibiting dynamic performance. The maximum output power is 592 W in simulation and 580 W in experimental results for the unity power factor. The variation in the modulation index is shown in Figure 6c. It is apparent that the magnitude of the voltage is changing, and its corresponding current amplitude is varied. The modulation index virtually does not

have any influence on the capacitor operations. Therefore, the proposed topology is more suitable for any dynamic load application. The sudden change in source voltage further validates the effectiveness of the circuit, and the measured results are shown in Figure 6d. Once again, the results show a good outcome of the proposed topology.

The power loss distribution and efficiency of the proposed topology are presented in Figure 7a,b, and the scaled-down prototype is shown in Figure 7c. Here, simulation efficiency and power loss distribution for each component are calculated using PLECS simulation software. The maximum simulation efficiency is 98.3%, and the experimental efficiency is ~97.0% for a 600 W load. Upon initial examination, the proposed topology appears to be a straightforward integrated boost inverter. Therefore, it is necessary to show the advantage of the proposed topology over other recent 5L boost inverters. Table 2 shows a detailed comparison with respect to the components, and obviously, the proposed topology is superior to the other topologies presented in the literature.

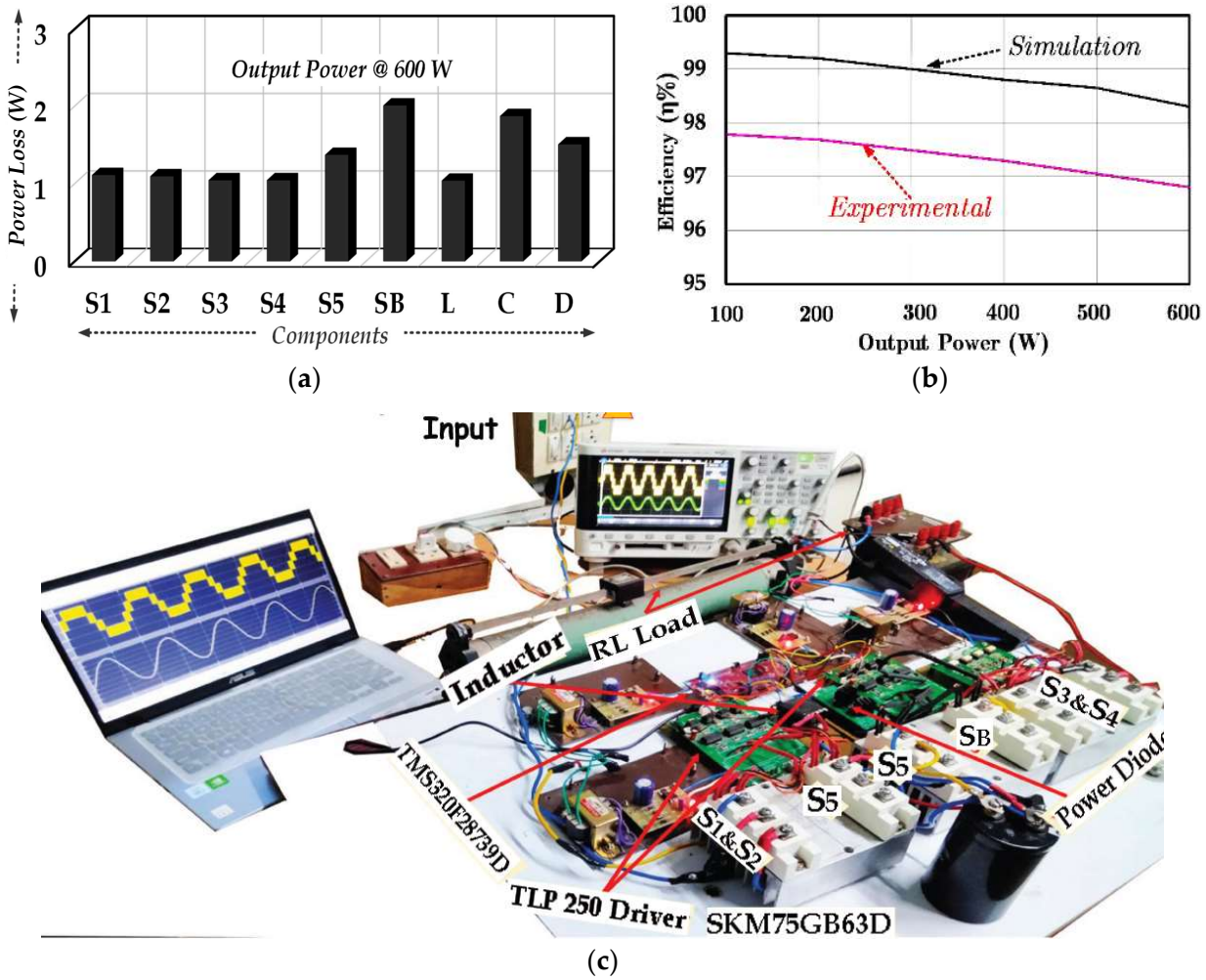


Figure 7. The proposed 5L-SDBI @ 600 W (**a**) power loss distribution, (**b**) the efficiency curve, and (**c**) prototype model. (S_1-S_5, S_B—Switches, L/C/D— Inductor/Capacitor/Diode, RL—Resistive -Inductive).

Table 2. Comparison of proposed 5L-SBI with other boost type inverters.

Top.	N_{Switch}	N_{Driver}	N_{Diode}	N_{Cap}	N_{DCS}	N_{Ind}	TC	Charging
[3]	7	7	2	2	1	-	19	Hard
[4]	7	7	4	2	1	-	21	Hard
[5]	7	7	2	1	1	-	18	Hard
[6]	9	9	8	2	1	-	23	Hard
[7]	10	10	2	2	2	2	28	Soft
[8]	8	8	3	4	1	2	26	Soft
[9]	8	8	4	3	2	2	27	Soft
[10]	12	12	4	4	1	3	36	Soft
[11]	9	9	1	2	1	1	23	Soft
[12]	9	9	3	2	1	1	25	Hard
[13]	12	11	2	4	1	2	32	Soft
[14]	9	7	1	1	1	1	20	Soft
Pro.	7	6	1	1	1	1	17	Soft

4. Conclusions

A new, five-level inverter topology with voltage boosting was presented, and the topology adopted the soft charging technique. Brief theoretical analyses were discussed, and the same is validated by using simulation and experimental setup. The results verified that the proposed topology generated the five-level output voltage with voltage boosting. Further, the soft charging technique confirms the suppression of the inrush current in the proposed topology, which is a major problem in recent SCMLI circuits. Moreover, the number of components count is less than the other recent topology. The proposed DC microgrid architecture has constant DC voltage, where there are no major variations in the duty cycle. Therefore, the proposed 5L-SBI is the best candidate for DC/AC power conversion in AC microgrid applications.

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