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Design of Uninterruptible Power Supply Inverters for Different Modulation Techniques Using Pareto Front for Cost and Efficiency Optimization

Edemar O. Prado [1,2,*], Pedro C. Bolsi [1,2], Hamiltom C. Sartori [2] and José R. Pinheiro [1,2]

[1] Energy Efficiency Lab, LABEFEA, Federal University of Bahia, Salvador 40170-110, BA, Brazil
[2] Power Electronics and Control Research Group, GEPOC, Federal University of Santa Maria, Santa Maria 97105-900, RS, Brazil
* Correspondence: edemar.prado@ufba.br

Abstract: This work presents a design for uninterruptible power supply inverters using Pareto front optimization for improved cost and efficiency. Three PWM modulation techniques applied to the full-bridge inverter are analyzed. As a result, the best MOSFET design solution in terms of the cost and efficiency of the inverter is evaluated based on a database with 47 power MOSFETs. Using the Pareto front, the optimal and sub-optimal solutions are compared, considering the three modulation techniques and the characteristics of MOSFETs manufactured for different voltage levels. Thermal and electrical measurements are used to validate the models.

Keywords: database; modulation technique; Pareto front analysis; power MOSFET; optimization; UPS SOHO

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1. Introduction

Uninterruptible power supplies (UPSs) are electronic systems capable of supplying high quality power to critical loads [1–7]. These are used for a wide range of applications, from systems rated at less than 1 kVA (single phase), to systems rated at more than 1000 kVA (three phase). High-power UPSs are used as temporary backup sources for large equipment and data centers, supplied by battery banks with hundreds of volts [8–10]. Lower-power UPSs are used in small office or home office (SOHO) applications, including converters that generally operate on battery voltages equal to or below 24 V, and are mainly classified as offline or line-interactive type [8,9,11].

In SOHO UPSs, the batteries can be connected to the load using a full-bridge converter. It is often necessary to raise the output voltage of the inverter to the AC output voltage using a low frequency transformer [8,9,11,12]. These topologies are known as ferroresonant-based UPSs [13–16]. Due to the use of the step-up transformer, the current drawn from the batteries and flowing through the inverter is higher than the load current, which causes high current stress on the inverter [12].

In order to lower harmonic distortions caused by converter switching, three-level modulations are employed [17–20]. Three modulation techniques are frequently utilized in the full bridge converter [11,17,20]:

- Discontinuous modulation (DM): the converter legs alternate switching within a carrier period. One converter leg is switched at high frequency during half of the fundamental (50 or 60 Hz) cycle, and the other converter leg is switched in the remaining half of the cycle [17] (Figure 1a);
- Phase-shifted modulation (PS): both converter legs switch at high frequency [17] (Figure 1b);
- Discontinuous single-phase leg switched modulation (DSPLS): one converter leg switches at high frequency, while the other switches at the rate of the fundamental cycle [17] (Figure 1c).

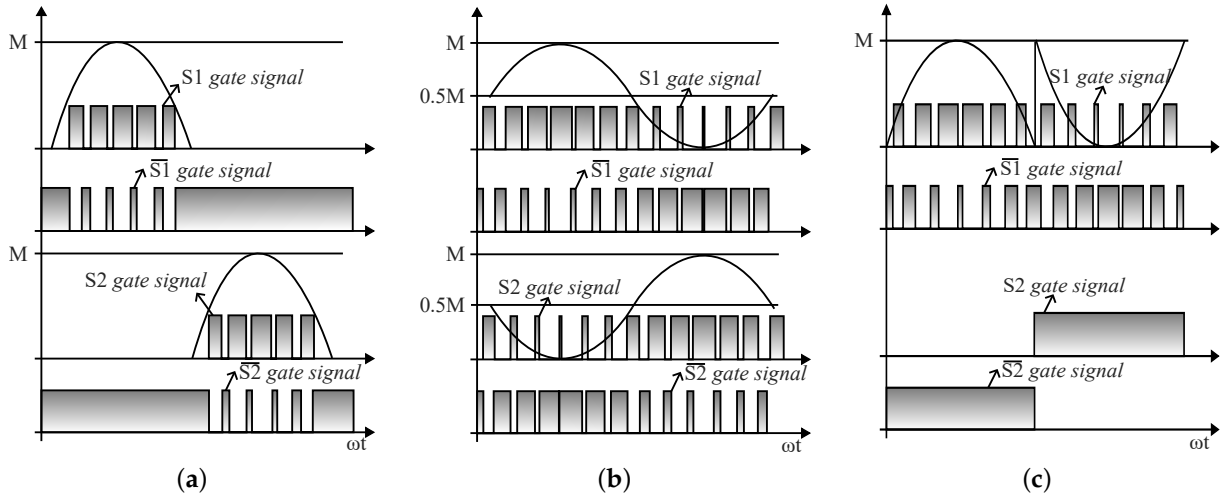


Figure 1. Three-level modulations applied to single-phase full-bridge inverter. (**a**) DM. (**b**) PS. (**c**) DSPLS.

Different modulation techniques will have different influences on the voltage and current of the semiconductors, which affects losses directly. To reduce losses and improve efficiency, optimization techniques are used [21–26]. In low-voltage full-bridge applications, converter optimization faces the challenge of selecting the part number of the MOSFETs of the inverter, considering their relation to efficiency and cost. These two metrics are often conflicting, and the Pareto front optimization is used as a tool to determine the compromise among them. Limits of the Pareto front are considered optimal for one or the other objective, or both [27,28]. The analysis of this front can be used by designers to guide the decision, according to the design requirements.

Based on the outlined discussions, this work evaluates the cost × efficiency relationship in full-bridge inverters applied to SOHO UPSs using Pareto front optimization, considering three modulation techniques and a database with 47 MOSFET part numbers (Appendix A). The analysis is performed for UPS operations in backup mode with a battery bank of 24 V, an RMS output voltage of 120 V/60 Hz, and a rated power of 1 kW. The main contributions of this work are as follows:

- Comparison of cost and efficiency in three PWM modulation techniques applied to full-bridge inverters in SOHO UPSs.
- Evaluation of power MOSFETs in the design of full-bridge inverters using Pareto fronts, while also comparing optimal and sub-optimal solutions based on a database of 47 devices.
- Comparison of the internal characteristics of MOSFETs manufactured for different voltage rating levels, presenting the part numbers selected in each design.

This paper is organized as follows. In Section 2, the experimental validation of losses and temperature models is presented. These models are used in Section 3 to determine the efficiency of the converter and build the Pareto fronts. The MOSFETs of the database are evaluated, and the Pareto fronts are used to select the optimal and sub-optimal solutions. The influence of individual MOSFET characteristics in the cost and efficiency of the inverter is discussed in Sections 3 and 4. Section 5 concludes the paper.

2. Experimental Validation of Computational and Thermal Models

2.1. Computational Models and UPS Waveforms

The developed methodology is applied to a commercial 1 kW line-interactive ferroresonant-based UPS, shown in Figure 2a. The backup mode equivalent circuit is shown in Figure 2b. The RMS output voltage is 120 V (60 Hz), and a pair of series-connected 12 V/7 Ah batteries (24 V) is used, with the possibility of adding external batteries to

increase the current (Ah) capacity. The default MOSFET part number of the product is STP220N6F7 [29], with two devices used in parallel in order to reduce the current.

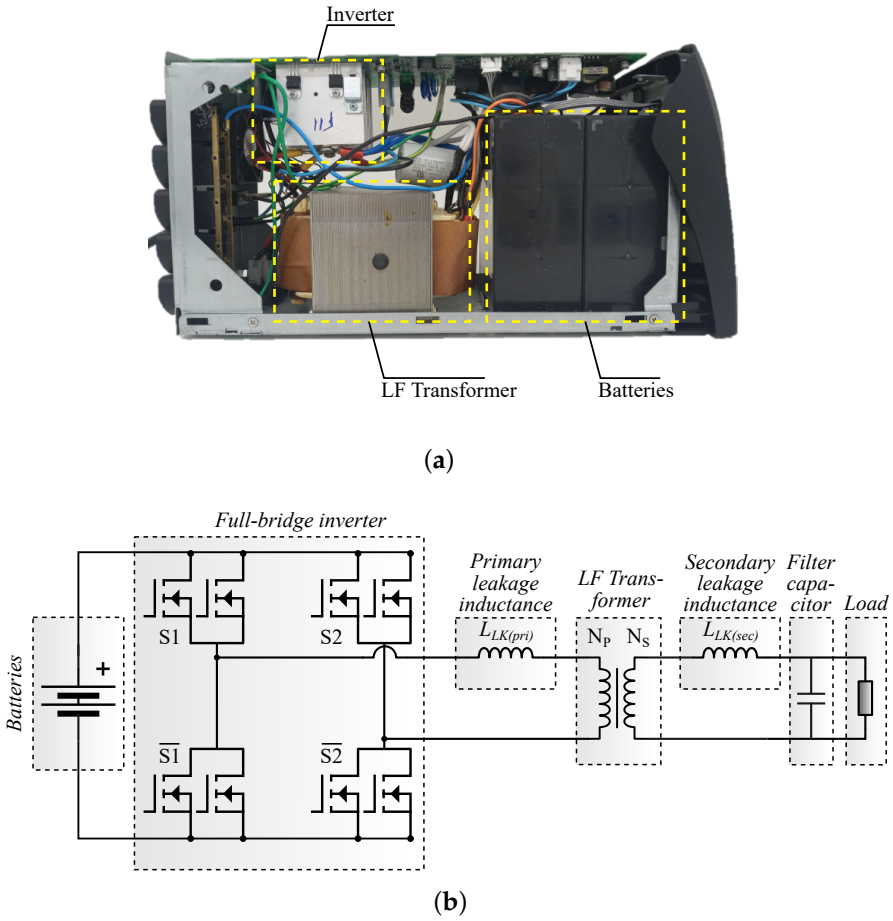


Figure 2. (**a**) Commercial line-interactive ferroresonant-based UPS of 1 kW. (**b**) Offline or line-interactive ferroresonant-based UPS equivalent circuit of operation in backup mode [11].

The three modulation techniques (DM, PS, and DSPLS) are implemented using a dSpace MicroLabBox equipment, base board DS1202. The original microcontroller and control circuits of the commercial UPS are disconnected and replaced by dSpace Micro-LabBox via an RJ45 connection to the gate drivers. The use of this equipment allows for alteration of the control and modulation parameters in real time using MATLAB Simulink and Controldesk software. The connection of signals from dSpace via RJ45 is shown in Figure 3.

The UPS is simulated in Simulink, including the inverter topology, the modulation techniques, a model for the transformer impedance, and the resistances of the battery, connectors, and cables. To validate the simulated UPS, Figure 4a,b present the experimental waveforms of current and voltage at the inverter output, with loads of 100 W and 400 W, respectively. Figure 4c,d present the simulated waveforms for the same operation point. In this example, DM is used. The simulated and measured RMS values of voltage and current at the load and at the output of the inverter are compared in Table 1.

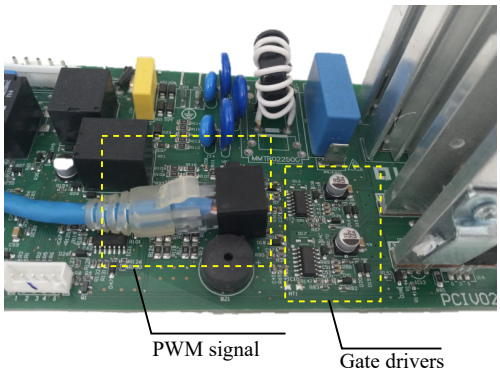


Figure 3. Connection of signals from dSpace via RJ45 to modify UPS modulation [11].

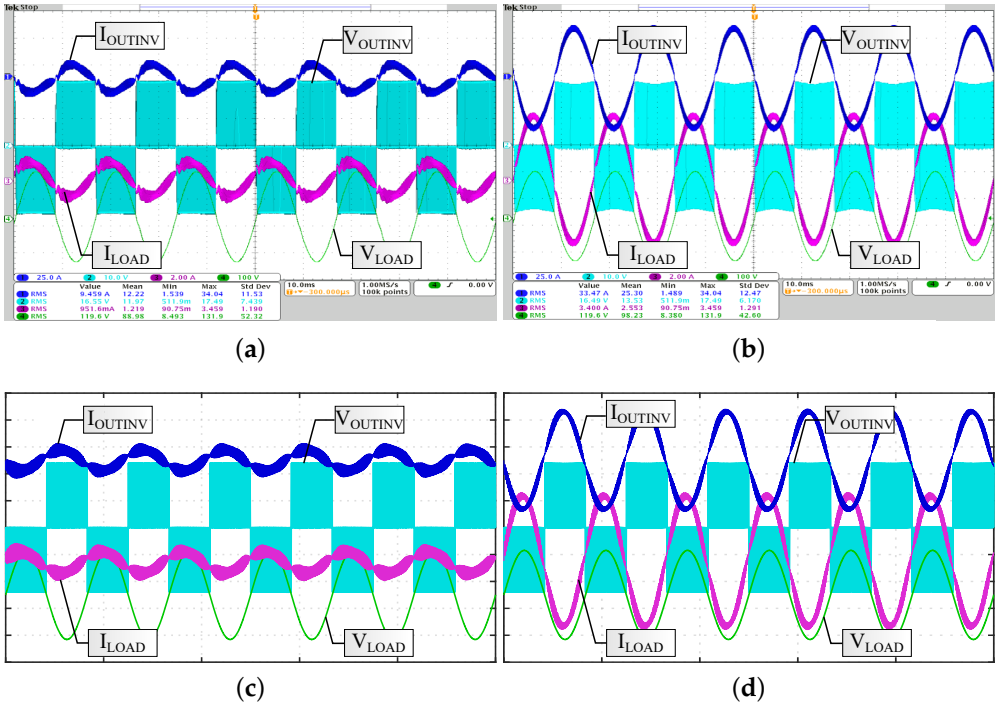


Figure 4. Waveforms for DM. (**a**) Experimental 100 W load. (**b**) Experimental 400 W load. (**c**) Simulation 100 W load. (**d**) Simulation 400 W load.

Table 1. Experimental and simulation RMS voltage and current values, with loads of 100 W and 400 W.

	Experimental 100 W	**Simulation 100 W**	**Experimental 400 W**	**Simulation 400 W**
Current at the inverter output	9.46 A	10.2 A	33.47 A	33 A
Voltage at the inverter output	16.55 A	16.47 A	16.49 V	16.44 V
Current at the load	0.95 A	1.02 A	3.4 A	3.38 A
Voltage at the load	119.6 A	120.1 A	119.6 V	120 V

2.2. Losses and Thermal Models

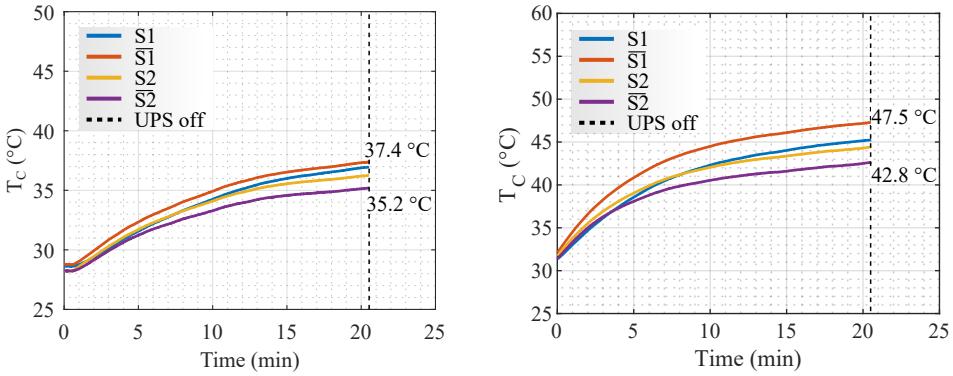
In order to implement the Pareto front analysis, device losses are estimated. MOSFET losses and temperature are mutually dependent, because the drain-source on-state

resistance (R_{DSon}) of the MOSFET is dependent on junction temperature (T_J) [30–34]. Thus, accurate models for both are necessary.

Power MOSFET losses may be calculated by analytical methods, SPICE models, or finite element analysis [34–37]. The use of analytical models is preferable when reduced computational time is desired [32,33,36,37]. In this work, the model presented in [34] is used to estimate conduction and switching losses. Among the models presented in [30,31,34,38–41], only those presented in [34,38] consider the internal gate resistance, and [34] also takes into account characteristics of the gate driver and the variation of Miller capacitance to determine overlap times. For reverse recovery losses, the model presented in [31] is used.

Device temperature can be estimated using thermal models, which are particular for each application. To obtain the thermal model for the case study UPS, MOSFET temperature variation over time is measured using a Keysight DAQ970A data logger. Thermocouples are placed on the case of the transistor of each pair. The thermocouples used are of the K-type (±2% accuracy).

With the default battery bank of the commercial UPS (7 Ah),the batteries are discharged before the temperature of the MOSFETs reaches a steady-state condition. In order to increase the autonomy of the UPS, an Itech IT7900 programmable voltage source was used to emulate an external battery bank. The resulting MOSFET case temperatures (T_C) are shown in Figure 5a,b for the operating points of 400 W and 600 W, respectively.



(**a**) (**b**)

Figure 5. Temperatures measured in the MOSFETs [11]. (**a**) 400 W. (**b**) 600 W.

The behavior of temperature over time is modeled by a parallel RC circuit of equivalent thermal resistance and capacitance [42–46]. The equivalent thermal resistance (R_{TH}) is determined using the measured temperature after thermal steady is reached,

$$R_{TH} = \frac{T_\infty - T_A}{P} \tag{1}$$

at which T_∞ is the steady state temperature, T_A is the ambient temperature, and P is the device power loss (according to the switching frequency and the power level).

The equivalent thermal capacitance (C_{TH}) describes the behavior of temperature as a function of time before a thermal steady-state is reached. This value is determined by extracting an instant in time (t) from the temperature transient,

$$C_{TH} = \frac{-t}{R_{TH} \ln\left(\frac{PR_{TH} - T_{(t)} + T_A}{PR_{TH}}\right)} \tag{2}$$

The values of R_{TH} and C_{TH} obtained from Figure 5 using $T_{(t)} = 5$ min are shown in Table 2. Due to the small difference between the values, the average was used. It is observed that in the case that different hardware is used or there are changes in the heat

transfer system, R_{TH} and C_{TH} will be different, and thus must be recalculated following the same methodology.

Table 2. Thermal coefficients calculated [11].

	R_{TH} (°C/W)			C_{TH} (J/°C)		
	400 W	**600 W**	**Average**	**400 W**	**600 W**	**Average**
S1	10.5	10.5	10.5	0.85	0.85	0.85
$\overline{S1}$	7.2	7.2	7.2	1.1	1.1	1.1
S2	9.7	10.2	10	0.8	0.75	0.77
$\overline{S2}$	5.6	5.8	5.7	1.4	1.3	1.35

Based on the results presented in Table 2, for the following analysis, the R_{TH} and C_{TH} used for all transistors are 8.4 °C/W and 1 J/°C, corresponding to the respective averages of S1, $\overline{S1}$, S2, and $\overline{S2}$. Thus, only the effect of the modulations on temperatures is analyzed, disregarding the influence of the heat transfer system.

3. Optimization Methodology Considering a Mosfet Database

To evaluate the best cost × efficiency relationship in the full-bridge converter, different part numbers were evaluated. A database with 47 transistors was created (Appendix A), including MOSFETs with rated voltages of 40, 55, and 60 V. All MOSFETs in the database operate safely at the rated power of the UPS system, and two power levels (500 W and 800 W) were used to evaluate the behavior of cost and efficiency in each modulation technique. For the following analysis, all components are compared to the part number that is used in the commercial UPS under study (STP220N6F7). The efficiency of STP220N6F7 is $\eta_{ref} = 98.89\%$ at 500 W and $\eta_{ref} = 98.23\%$ at 800 W, and the component costs are normalized with respect to the cost of STP220N6F7 ($C_{ref} = 1$).

3.1. Discontinuous Modulation

In the Pareto front analysis for DM, two scenarios are considered: (1) all MOSFETs have the same part number, and (2) there are different part numbers for each switching pattern, that is, the transistors in the upper positions are of part number X and the lower ones are of part number Y. Figure 6 depicts these two scenarios.

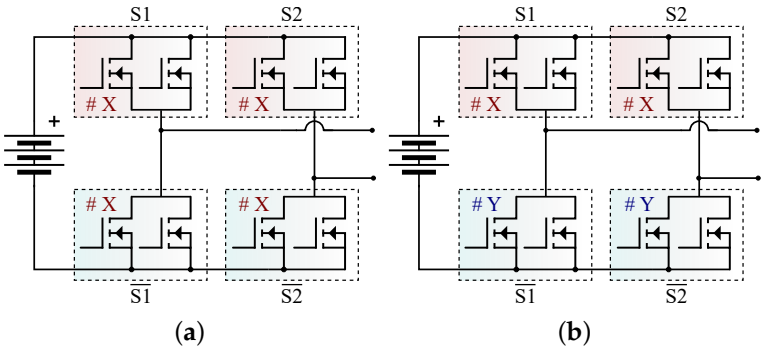


Figure 6. Inverter part number configuration for DM. (**a**) Scenario where all MOSFETs have the same part number. (**b**) Scenario where different part numbers are considered for the different switching patterns.

Figure 7 shows the Pareto front solutions for both scenarios considering the load powers of 500 W and 800 W. The points in red represent the designs relative to scenario 1, and the gray points represent the designs of scenario 2.

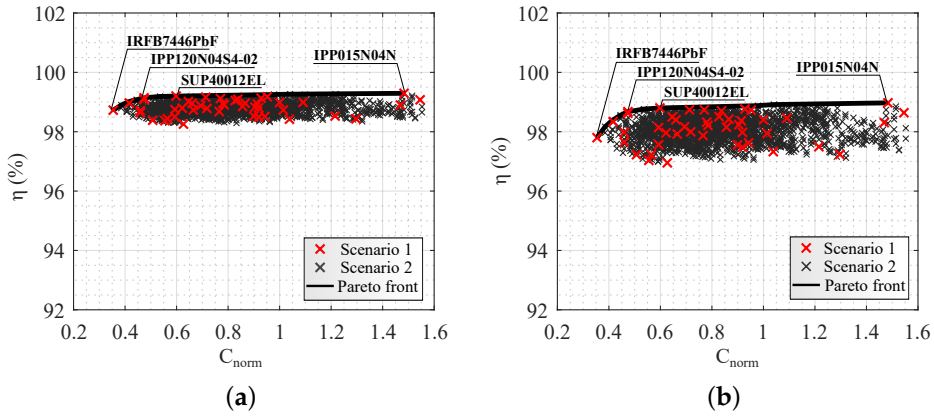


Figure 7. Pareto front for DM. (**a**) 500 W. (**b**) 800 W.

In these, 2209 MOSFET combinations were evaluated. The Pareto front contains the optimal solutions for cost × efficiency. The part numbers on the front are shown in Tables 3 and 4 for the powers of 500 W and 800 W, respectively, identifying the normalized cost (C_{norm}), efficiency (η) and junction temperature (T_J) for each transistor. The highlighted rows identify the solutions of scenario 1, which uses the same part number in all MOSFETs. These part numbers are presented in Figure 7.

Table 3. Design details for DM with 500 W.

C_{norm}	η	T_J S1	T_J $\overline{S1}$	T_J S2	T_J $\overline{S2}$	# S1 and S2	# $\overline{S1}$ and $\overline{S2}$
0.354067	**98.7%**	**40.2 °C**	**49.9 °C**	**40.2 °C**	**49.9 °C**	**IRFB7446PbF**	**IRFB7446PbF**
0.385167	98.9%	40.2 °C	45.3 °C	40.2 °C	45.3 °C	IRFB7446PbF	IRFB7440PbF
0.413876	99%	40.2 °C	42.6 °C	40.2 °C	42.6 °C	IRFB7446PbF	IPP120N04S4-02
0.444976	99.1%	38.4 °C	42.6 °C	38.4 °C	42.6 °C	IRFB7440PbF	IPP120N04S4-02
0.473684	**99.1%**	**37 °C**	**42.6 °C**	**37 °C**	**42.6 °C**	**IPP120N04S4-02**	**IPP120N04S4-02**
0.535885	99.2%	37 °C	41.5 °C	37 °C	41.5 °C	IPP120N04S4-02	SUP40012EL
0.598086	**99.2%**	**36.8 °C**	**41.5 °C**	**36.8 °C**	**41.5 °C**	**SUP40012EL**	**SUP40012EL**
0.978469	99.3%	37 °C	39.8 °C	37 °C	39.8 °C	IPP120N04S4-02	IPP015N04N
1.04067	99.3%	36.8 °C	39.8 °C	36.8 °C	39.8 °C	SUP40012EL	IPP015N04N
1.48325	**99.3%**	**36 °C**	**39.8 °C**	**36 °C**	**39.8 °C**	**IPP015N04N**	**IPP015N04N**

Table 4. Design details for DM with 800 W.

C_{norm}	η	T_J S1	T_J $\overline{S1}$	T_J S2	T_J $\overline{S2}$	# S1 and S2	# $\overline{S1}$ and $\overline{S2}$
0.354067	**97.7%**	**63.4 °C**	**92.6 °C**	**63.4 °C**	**92.6 °C**	**IRFB7446PbF**	**IRFB7446PbF**
0.385167	98.2%	63.4 °C	75.7 °C	63.4 °C	75.7 °C	IRFB7446PbF	IRFB7440PbF
0.413876	98.4%	63.4 °C	66.9 °C	63.4 °C	66.9 °C	IRFB7446PbF	IPP120N04S4-02
0.444976	98.5%	56.7 °C	66.9 °C	56.7 °C	66.9 °C	IRFB7440PbF	IPP120N04S4-02
0.473684	**98.6%**	**52.6 °C**	**66.9 °C**	**52.6 °C**	**66.9 °C**	**IPP120N04S4-02**	**IPP120N04S4-02**
0.535885	98.7%	52.6 °C	63.6 °C	52.6 °C	63.6 °C	IPP120N04S4-02	SUP40012EL
0.598086	**98.8%**	**51.4 °C**	**63.6 °C**	**51.4 °C**	**63.6 °C**	**SUP40012EL**	**SUP40012EL**
0.978469	98.9%	52.6 °C	58.5 °C	52.6 °C	58.5 °C	IPP120N04S4-02	IPP015N04N
1.04067	98.9%	51.4 °C	58.5 °C	51.4 °C	58.5 °C	SUP40012EL	IPP015N04N
1.48325	**99%**	**49 °C**	**58.5 °C**	**49 °C**	**58.5 °C**	**IPP015N04N**	**IPP015N04N**

The lowest cost solution on the Pareto front for 500 W and 800 W represents 35% of the MOSFET reference cost using the part number IRFB7446PbF. For 500 W, the efficiency achieved is 98.7%, or 0.2% smaller than the reference part number, and for 800 W, $\eta = 97.7\%$ or 0.5% smaller than the reference. The best efficiency condition is obtained with part number IPP015N04N, that being 99.3% in 500 W and 99% in 800 W, with efficiency increases of 0.4% and 0.7% respectively. The cost of this solution is 148% of C_{ref}. The remaining optimal solutions may be selected according to the desired cost × efficiency relationship.

When analyzing T_J, in scenario 1 there is thermal imbalance between the transistors that are off during a half of the fundamental cycle (S1 and S2) and the transistors that are on during a half of the fundamental cycle ($\overline{S1}$ and $\overline{S2}$). This occurs because DM presents asymmetry in the conduction losses and can result in a reduction in autonomy time according to the operation point [11]. In the optimal designs in scenario 2, the part numbers of the transistors are different, as presented in Figure 6b. The different combinations of MOSFETs result in different losses and consequently differences in T_J behavior. Although $\overline{S1}$ and $\overline{S2}$ are on during a half of a fundamental cycle, specific combinations of part numbers may result in lower thermal imbalance in the inverter. The lowest difference in T_J is obtained in the design using part number X = IRFB7446PbF and Y = IPP120N04S4-02, where T_J of IRFB7446PbF is 63.4 °C and T_J of IPP120N04S4-02 is 66.9 °C in 800 W.

3.2. Phase-Shifted Modulation

For this modulation technique, the evaluated scenarios are: (1) considering all MOSFETs with the same part number and (2) considering each leg with different part number. Even with symmetric modulation, this scenario is considered in order to evaluate the different combinations of cost × efficiency. Figure 8 shows the configuration of these scenarios for PS modulation: transistors S1 and $\overline{S1}$ with part number X and S2 and $\overline{S2}$ with part number Y.

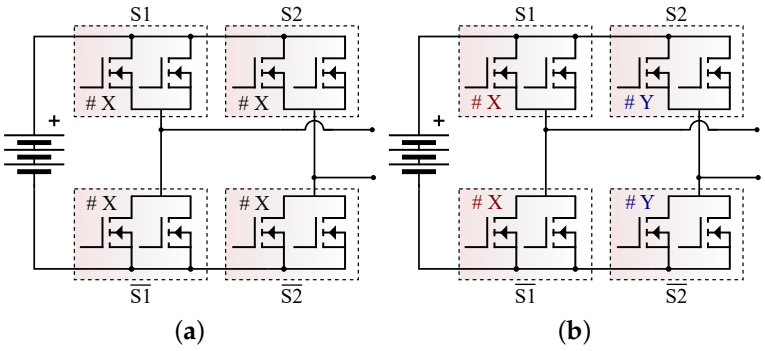


Figure 8. Inverter part number configuration for PS. (**a**) Scenario where all MOSFETs have the same part number. (**b**) Scenario using two different part numbers.

Pareto fronts for PS are shown in Figure 9. The red points represent the designs corresponding to scenario 1, and the green points represent the designs for scenario 2. The part numbers of the optimal solutions are shown in Tables 5 and 6 for 500 W and 800 W, respectively. The highlighted rows represent the optimal solutions that use the same part number in all MOSFETs.

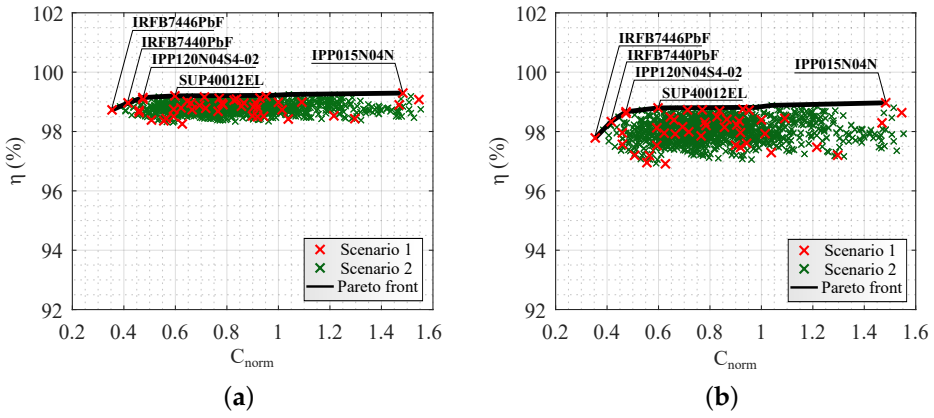


Figure 9. Pareto front for PS. (**a**) 500 W. (**b**) 800 W.

Table 5. Design details for PS with 500 W.

C_{norm}	η	T_J S1	T_J $\overline{S1}$	T_J S2	T_J $\overline{S2}$	# S1 and S2	# $\overline{S1}$ and $\overline{S2}$
0.354067	**98.7%**	**44.9 °C**	**44.9 °C**	**44.9 °C**	**44.9 °C**	**IRFB7446PbF**	**IRFB7446PbF**
0.385167	98.8%	44.9 °C	44.9 °C	41.8 °C	41.8 °C	IRFB7446PbF	IRFB7440PbF
0.416268	**99%**	**41.8 °C**	**41.8 °C**	**41.8 °C**	**41.8 °C**	**IRFB7440PbF**	**IRFB7440PbF**
0.444976	99%	41.8 °C	41.8 °C	39.7 °C	39.7 °C	IRFB7440PbF	IPP120N04S4-02
0.473684	**99.1%**	**39.7 °C**	**39.7 °C**	**39.7 °C**	**39.7 °C**	**IPP120N04S4-02**	**IPP120N04S4-02**
0.535885	99.2%	39.1 °C	39.1 °C	39.7 °C	39.7 °C	SUP40012EL	IPP120N04S4-02
0.598086	**99.2%**	**39.1 °C**	**39.1 °C**	**39.1 °C**	**39.1 °C**	**SUP40012EL**	**SUP40012EL**
0.978469	99.2%	39.7 °C	39.7 °C	37.9 °C	37.9 °C	IPP120N04S4-02	IPP015N04N
1.04067	99.2%	39.1 °C	39.1 °C	37.9 °C	37.9 °C	SUP40012EL	IPP015N04N
1.48325	**99.3%**	**37.9 °C**	**37.9 °C**	**37.9 °C**	**37.9 °C**	**IPP015N04N**	**IPP015N04N**

Table 6. Design details for PS with 800 W.

C_{norm}	η	T_J S1	T_J $\overline{S1}$	T_J S2	T_J $\overline{S2}$	# S1 and $\overline{S1}$	# S2 and $\overline{S2}$
0.354067	**97.8%**	**77.1 °C**	**77.1 °C**	**77.1 °C**	**77.1 °C**	**IRFB7446PbF**	**IRFB7446PbF**
0.385167	98%	77.1 °C	77.1 °C	65.9 °C	65.9 °C	IRFB7446PbF	IRFB7440PbF
0.416268	**98.3%**	**65.9 °C**	**65.9 °C**	**65.9 °C**	**65.9 °C**	**IRFB7440PbF**	**IRFB7440PbF**
0.444976	98.5%	65.9 °C	65.9 °C	59.4 °C	59.4 °C	IRFB7440PbF	IPP120N04S4-02
0.473684	**98.6%**	**59.5 °C**	**59.5 °C**	**59.5 °C**	**59.5 °C**	**IPP120N04S4-02**	**IPP120N04S4-02**
0.535885	98.7%	57.3 °C	57.3 °C	59.4 °C	59.4 °C	SUP40012EL	IPP120N04S4-02
0.598086	**98.8%**	**57.3 °C**	**57.3 °C**	**57.3 °C**	**57.3 °C**	**SUP40012EL**	**SUP40012EL**
0.978469	98.8%	59.5 °C	59.5 °C	53.7 °C	53.7 °C	IPP120N04S4-02	IPP015N04N
1.04067	98.9%	57.3 °C	57.3 °C	53.7 °C	53.7 °C	SUP40012EL	IPP015N04N
1.48325	**99%**	**53.7 °C**	**53.7 °C**	**53.7 °C**	**53.7 °C**	**IPP015N04N**	**IPP015N04N**

The lowest cost solution for 500 W and 800 W is the same as DM, which has 35% of the cost in semiconductors. The best performance condition is also the same as obtained with DM, using part number IPP015N04N. As with the analysis of DM, the remaining optimal solutions may be selected according to the desired cost × efficiency relation.

For the T_J analysis, it is shown in Tables 5 and 6 that the optimal designs for scenario 1 present thermal balance between the T_J values of S1, S2, $\overline{S1}$, and $\overline{S2}$. When different part numbers are used in scenario 2, there is thermal imbalance between the legs.

3.3. Discontinuous Single-Phase Leg Switched Modulation

For DSPLS modulation in scenario 1, all MOSFETs are considered with the same part number, and in scenario 2, different part numbers for each switching pattern (Figure 10). Scenario 2 uses part number X for positions S1 and $\overline{S1}$, which are the transistors that work at the switching frequency (30 kHz), and part number Y for S2 and $\overline{S2}$, which are the transistors that work at the grid frequency.

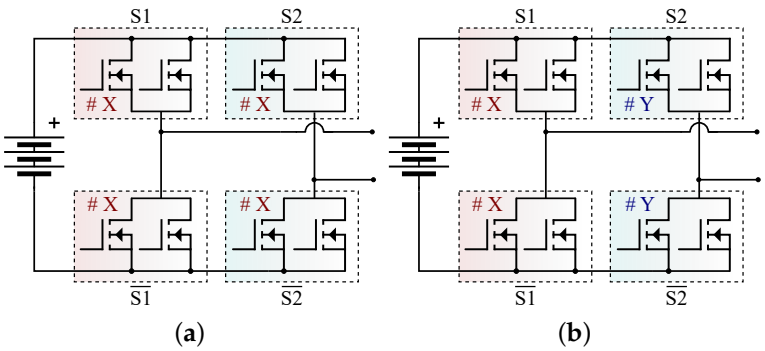


Figure 10. Inverter part number configuration for DSPLS. (**a**) Scenario where all MOSFETs have the same part number. (**b**) Scenario where different part numbers are considered for the different switching patterns.

The Pareto front for DSPLS modulation is shown in Figure 11. The points in red represent the designs corresponding to scenario 1, and the points in blue represent the designs for scenario 2.

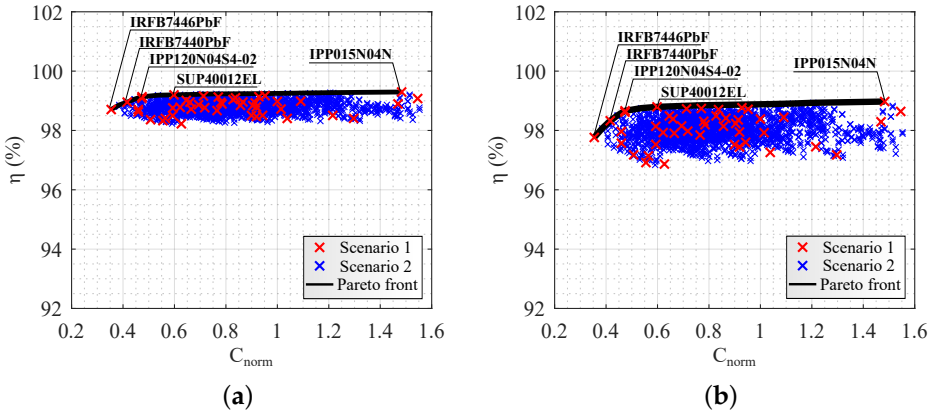


Figure 11. Pareto front for DSPLS. (**a**) 500 W. (**b**) 800 W.

All part numbers of the optimal solutions are shown in Tables 7 and 8 for the powers of 500 W and 800 W, respectively, identifying the C_{norm}, η and T_J obtained with each transistor configuration. The highlighted rows represent the optimal solutions that use only 1 part number in all MOSFETs. These same part numbers are highlighted in Figure 11.

Table 7. Design details for DSPLS with 500 W.

C_{norm}	η	T_J S1	T_J $\overline{S1}$	T_J S2	T_J $\overline{S2}$	# S1 and $\overline{S1}$	# S2 and $\overline{S2}$
0.354067	**98.7%**	**45.8 °C**	**46 °C**	**44 °C**	**44.4 °C**	**IRFB7446PbF**	**IRFB7446PbF**
0.385167	98.9%	45.8 °C	46 °C	40.3 °C	40.4 °C	IRFB7446PbF	IRFB7440PbF
0.416268	**98.9%**	**43.4 °C**	**43.5 °C**	**40.3 °C**	**40.4 °C**	**IRFB7440PbF**	**IRFB7440PbF**
0.444976	99%	41 °C	41.1 °C	40.3 °C	40.4 °C	IPP120N04S4-02	IRFB7440PbF
0.473684	**99.1%**	**41 °C**	**41.1 °C**	**38.5 °C**	**38.6 °C**	**IPP120N04S4-02**	**IPP120N04S4-02**
0.535885	99.2%	41 °C	41.1 °C	37.3 °C	37.4 °C	IPP120N04S4-02	SUP40012EL
0.598086	99.2%	40.9 °C	40.9 °C	37.3 °C	37.4 °C	SUP40012EL	SUP40012EL
0.62201	99.2%	41 °C	41.1 °C	36.7 °C	36.8 °C	IPP120N04S4-02	PSMN1R9-40PL
0.684219	99.2%	40.7 °C	40.9 °C	36.7 °C	36.8 °C	SUP40012EL	PSMN1R9-40PL
0.70095	99.2%	41 °C	41.1 °C	36.4 °C	36.4 °C	SUP40012EL	PSMN1R5-40PS
0.763158	99.2%	40.9 °C	40.9 °C	36.4 °C	36.4 °C	SUP40012EL	PSMN1R5-40PS
0.940191	99.2%	40.3 °C	40.4 °C	36.4 °C	36.4 °C	SUP50010EL	PSMN1R5-40PS
1.04067	99.3%	40.9 °C	40.9 °C	36 °C	36 °C	SUP40012E	IPP015N04N
1.20574	99.3%	39.7 °C	39.7 °C	36.4 °C	36.4 °C	IPP015N04N	PSMN1R5-40PS
1.48325	**99.3%**	**39.7 °C**	**39.7 °C**	**36 °C**	**36 °C**	**IPP015N04N**	**IPP015N04N**

Table 8. Design details for DSPLS with 800 W.

C_{norm}	η	T_J S1	T_J $\overline{S1}$	T_J S2	T_J $\overline{S2}$	# S1 and $\overline{S1}$	# S2 and $\overline{S2}$
0.354067	**97.8%**	**79 °C**	**78.6 °C**	**76 °C**	**75.7 °C**	**IRFB7446PbF**	**IRFB7446PbF**
0.385167	98.1%	79 °C	78.6 °C	63.5 °C	63.3 °C	IRFB7446PbF	IRFB7440PbF
0.416268	**98.3%**	**68.8 °C**	**68.4 °C**	**63.5 °C**	**63.3 °C**	**IRFB7440PbF**	**IRFB7440PbF**
0.444976	98.5%	61.8 °C	61.4 °C	63.5 °C	63.3 °C	IPP120N04S4-02	IRFB7440PbF
0.473684	**98.7%**	**61.8 °C**	**61.4 °C**	**57.5**	**57.4**	**IPP120N04S4-02**	**IPP120N04S4-02**
0.535885	98.8%	61.8 °C	61.4 °C	54.4 °C	54.3 °C	IPP120N04S4-02	SUP40012EL
0.598086	**98.8%**	**60.3 °C**	**60 °C**	**54.4 °C**	**54.3 °C**	**SUP40012EL**	**SUP40012EL**
0.684219	98.8%	60.3 °C	60 °C	52.9 °C	52.7 °C	SUP40012EL	PSMN1R9-40PL
0.763158	98.9%	60.3 °C	60 °C	52 °C	51.9 °C	SUP40012EL	PSMN1R5-40PS
1.04067	98.9%	60.3 °C	60 °C	50.7 °C	50.6 °C	SUP40012EL	IPP015N04N
1.12679	98.9%	56.9 °C	56.4 °C	52.9 °C	52.7 °C	IPP015N04N	PSMN1R9-40PL
1.20574	98.9%	56.9 °C	56.4 °C	52 °C	51.9 °C	IPP015N04N	PSMN1R5-40PS
1.48325	**99%**	**56.9 °C**	**56.4 °C**	**50.7 °C**	**50.1 °C**	**IPP015N04N**	**IPP015N04N**

The lowest cost MOSFET in the optimal solutions for 500 W and 800 W is the same as the previous modulation techniques, IRFB7446PbF. The highest efficiency optimal solution is obtained with the same part number of DM and PS, IPP015N04N.

For T_J in scenario 1, the lowest thermal imbalance between the high- and low-frequency converter legs at 800 W is 3.3 °C with IRFB7446PbF ($\eta = 97.8\%$). The highest difference in temperature is 6.8 °C with IPP015N04N, even though this is the highest efficiency (99%) optimal solution.

The high efficiency achieved with IPP015N04N is due to its relatively smaller drain-source on-state resistance (R_{DSon}). To reduce R_{DSon}, manufacturers increase the carrier density and die size, which as a consequence increases internal capacitances. The increase in internal capacitances results in higher switching losses [33], and consequently, there is more thermal imbalance between the legs (only one leg works at high frequency).

In scenario 2 the lowest difference in temperatures between the legs at 800 W is 2.1 °C with part number X = IPP120N04S4-02 and Y = IRFB7440PbF ($\eta = 98.5\%$), and the highest is 15.1 °C with part number X = IRFB7446PbF and Y = IRFB7440PbF ($\eta = 98.1\%$).

4. Comparison of Pareto Front Solutions for the Three Evaluated Modulation Techniques

In the previous sections, the Pareto fronts for each modulation technique were presented as well as several solutions with better efficiencies and attractive costs when compared to the reference. Figure 12 shows the designs and Pareto fronts with the three evaluated modulations together.

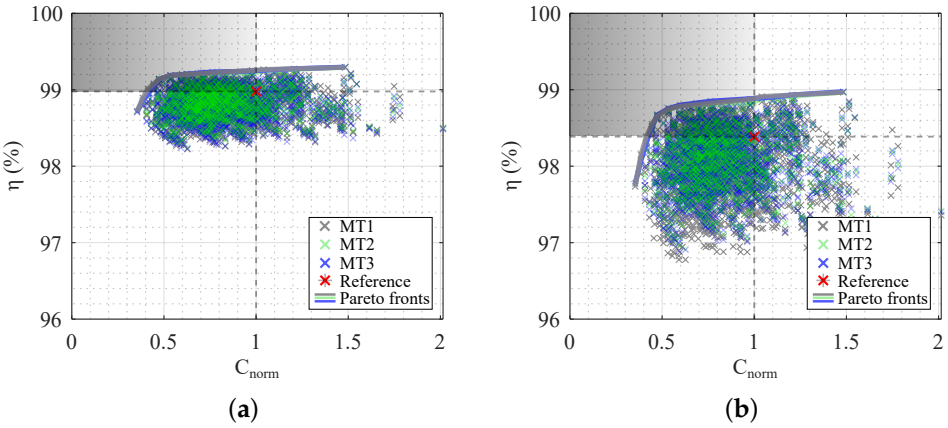


Figure 12. Pareto front considering all modulation techniques. (**a**) 500 W. (**b**) 800 W.

The shaded area contains 403 designs with $\eta \geq \eta_{ref}$ and $C_{norm} \leq C_{ref}$. As can be seen in the results of the previous sections, the part numbers found on the front as well as the efficiencies were similar for the three evaluated modulation techniques. However, the analysis of T_J should be used by designers to select the best modulation technique according to the required application. Each modulation technique and part number combination can be exploited according to the heat transfer system used in the converter. For example, thermal imbalance can be desirable if the heat transfer system is asymmetric due to layout constraints.

However, industry applications in general use the same part number in all transistors because of possible advantages in cost (buying in bulk) and uniformity of manufacturing processes. Thus, in this section the analysis of scenario 1 (use of the same part numbers for both converter legs) is emphasized.

In Table 9, the designs with same part numbers in all MOSFETs are shown, detailing the characteristics of voltage rating (V_{DSb}), input capacitance (C_{ISS}), R_{DSon}, η, and C_{norm}. The cost is lower than the reference for 80% of selected MOSFETs, being higher only for IPP015N04N. It is possible to identify that as cost increases, $R_{DSon(25)}$ decreases and C_{ISS}

rises. In this evaluation, only transistors with rated voltages of 40 V were selected, instead of 55 V or 60 V transistors. The lower breakdown voltage rating enables smaller die sizes and higher carrier densities in the drift region, which in turn increases electron mobility and reduces the R_{DSon}. Thus, the 40 V transistors tend to present higher efficiency and a smaller cost in comparison to 55 V and 60 V transistors. In order to increase the number of solutions, the sub-optimal designs, which are the solutions that are near the Pareto front, are included.

Table 9. Comparison of optimal solutions with same part number for all MOSFETs with each modulation technique, with 800 W. Reference values: C_{ref} = 1, η_{ref} = 98.23.

C_{norm}	Part Number	V_{DSb}	C_{ISS} (pF)	$R_{DSon(25)}$ (mΩ)	η (%)		
					DM	PS	DSPLS
0.35	IRFB7446PbF	40	3183	3.3	97.7	97.8	97.8
0.41	IRFB7440PbF	40	4730	2.5	98.3	98.3	98.3
0.47	IPP120N04S4-02	40	8260	2.1	98.6	98.6	98.7
0.59	SUP40012EL	40	10,930	1.8	98.8	98.8	98.8
1.48	IPP015N04N	40	15,000	1.5	99	99	99

Figure 13 shows the designs selected under these conditions, with the center point to the dashed lines being the reference design. The remaining points marked in red are the optimal and sub-optimal designs for scenario 1. Table 10 shows the selected part numbers, detailing the characteristics of V_{DSb}, C_{ISS}, and R_{DSon}. The highlighted rows are the sub-optimal solutions, and the other rows are the optimal solutions that were previously presented.

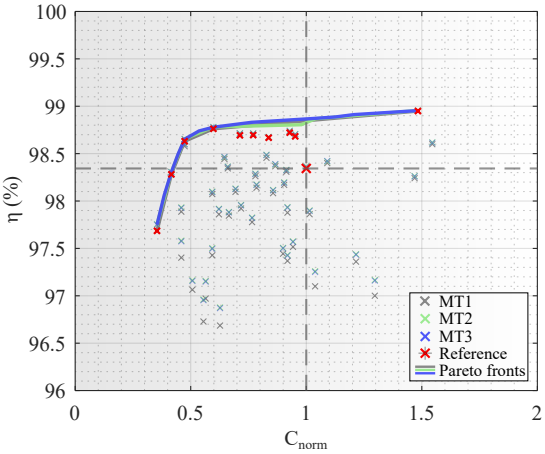


Figure 13. Pareto front for 800 W considering optimal and sub-optimal designs for scenario 1.

Table 10. Comparison of optimal and sub-optimal solutions with same part number for all MOSFETs with each modulation technique, for 800 W. Reference values: C_{ref} = 1, η_{ref} = 98.23.

C_{norm}	Part Number	V_{DSb}	C_{ISS} (pF)	$R_{DSon(25)}$ (mΩ)	Efficiency (%)		
					DM	PS	DSPLS
0.35	IRFB7446PbF	40	3183	3.3	97.7	97.8	97.8
0.41	IRFB7440PbF	40	4730	2.5	98.3	98.3	98.3
0.47	IPP120N04S4-02	40	8260	2.1	98.6	98.6	98.7
0.59	SUP40012EL	40	10,930	1.8	98.8	98.8	98.8
0.71	**AOT2142L**	**40**	**8320**	**1.7**	**98.7**	**98.7**	**98.7**
0.77	**PSMN1R9-40PL**	**40**	**13,200**	**1.6**	**98.7**	**98.7**	**98.7**
0.84	**SUP40010EL**	**40**	**11,165**	**1.8**	**98.7**	**98.7**	**98.7**
0.92	**PSMN1R5-40PS**	**40**	**9710**	**1.9**	**98.7**	**98.7**	**98.7**
0.95	**SUP50010E**	**60**	**10,895**	**2**	**98.7**	**98.7**	**98.7**
1.48	IPP015N04N	40	15,000	1.5	99	99	99

For this evaluation, there are 10 solutions, with 9 having a voltage rating of 40 V, and only one, with the part number SUP50010E, having a voltage rating of 60 V. The normalized cost of this solution is 95% of C_{ref} and improves the efficiency from 98.23% to 98.6%. The 40 V part numbers again were superior in terms of cost × efficiency, as they are manufactured for a lower voltage rating. Among the ten solutions found, once again only the part number IPP015N04N presented a cost higher than C_{ref}.

To evaluate the use of MOSFETs with higher voltage ratings, Figure 14 shows the solutions that use transistors with $V_{DSb} > 40$ V. The center point of the dashed lines represents the reference design, and the red line identifies the Pareto front for the transistors with $V_{DSb} > 40$ V. All solutions presented a lower normalized cost than the reference. Table 11 shows the selected part numbers.

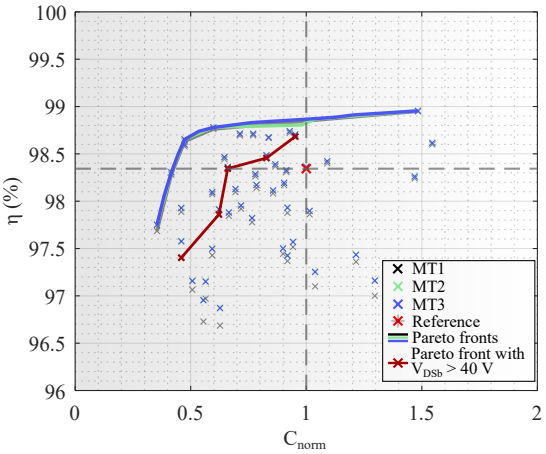


Figure 14. Pareto front considering MOSFETs with $V_{DSb} > 40$ V, for 800 W.

Table 11. Comparison of solutions with the same part number in all positions considering only MOSFETs with $V_{DSb} > 40$ V for all modulation techniques for 800 W. Reference values: $C_{ref} = 1$, $\eta_{ref} = 98.23$.

C_{norm}	Part Number	V_{DSb}	C_{ISS} (pF)	$R_{DSon(25)}$ (mΩ)	Efficiency (%)		
					DM	PS	DSPLS
0.46	BUK653R5-55C	55	11,516	2.9	97.5	97.5	97.5
0.62	IRFB3206PbF	60	6540	3	97.9	97.9	97.9
0.66	IPP024N06N3	60	17,000	2.4	98.4	98.4	98.4
0.83	SUP50020E	60	11,150	2.4	98.5	98.5	98.5
0.95	SUP50010E	60	10,895	2	98.7	98.7	98.7

The part numbers BUK653R5-55C and IRFB3206PbF showed efficiencies of 0.73% and 0.33% lower than the reference. The normalized costs were 46% and 62%, respectively, which could be an attractive alternative for reducing the cost of semiconductors. The part number IPP024N06N3 showed efficiency similar to the reference value at a cost of 66%. The part numbers SUP50020E and SUP50010E showed a small improvement in efficiency, costing 83% and 95% of the cost, respectively.

5. Conclusions

In this paper, a design of uninterruptible power supply inverters using Pareto front optimization for cost and efficiency was presented. With the use of a MOSFET database, Pareto front analyses were developed considering two different MOSFET combinations in the full-bridge inverter. These were selected according to the switching pattern in DM and DSPLS and considering each leg with a part number in PS in order to evaluate the different combinations of cost × efficiency. In these analyses, the optimal solutions for each modulation technique and its junction temperatures in the MOSFETs were discussed. Based

in these results, the designers may select the MOSFET according to the cost, efficiency, and thermal behavior required by the application.

Analysis of scenario 1 (same part numbers for both convert legs) was emphasized in the comparison of the three modulation techniques, because in industry applications, it is the same part number is generally used in all transistors due to advantages in the cost (buying in bulk) and uniformity of the manufacturing processes. The results have showed superior cost × efficiency for MOSFETs manufactured for V_{DSb} of 40 V. In order to increase the number of available solutions, sub-optimal solutions were analyzed. Under these conditions, 10 part numbers were selected, where 90% presented V_{DSb} of 40 V. In the third analysis, only transistors with $V_{DSb} > 40$ V were selected, providing options for applications where there is a demand to use components in this voltage range. Among the three evaluated scenarios and all the solutions found, only the one that uses the IPP015N04N MOSFET has a higher cost than the reference.

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Appendix A

Part numbers in the database are listed: (1) AOT2142L, (2) AUIRF1404Z, (3) AUIRFB8405, (4) DMNH4005SCTQ, (5) STP185N55F3, (6) STP190N55LF3, (7) STP260N6F6, (8) STP220N6F7, (9) FDP020N06-D, (10) FDP025N06-D, (11) FDP030N06B-F102-D, (12) AUIRF1404, (13) IPP120N06S4-H1, (14) IPP015N04N, (15) IPP120N04S4-02, (16) IPP024N06N3, (17) IPP032N06N3, (18) IRFB3206GPbF, (19) IRFB7440PbF, (20) IRFB7446PbF, (21) IRFB3206PbF, (22) IRFB3306PbF, (23) IRL40B215, (24) IPP120N04S3-02, (25) IPP120N04S4-02, (26) AUIRL1404Z, (27) AUIRF3805L, (28) IRL1404PbF, (29) IXTP160N04T2, (30) BUK653R2-55C, (31) BUK653R5-55C, (32) BUK652R6-40C, (33) BUK652R3-40C, (34) PSMN2R1-40PL, (35) PSMN1R5-40PS, (36) PSMN1R9-40PL, (37) PSMN2R0-60PS, (38) PSMN2R5-60PL, (39) PSMN2R6-60PS, (40) PSMN3R9-60PS, (41) PSMN4R2-60PL, (42) SQP120N06-3m5L, (43) SUP40010EL, (44) SUP40012EL, (45) SUP50010E, (46) SUP50020E, (47) SUP50020EL.

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