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Analysis of Asymmetric Hybrid Modular Multilevel Topology for Medium-Voltage Front-End Converter Applications

Muhammad Ali [1,*], Ajmal Farooq [1], Muhammad Qasim Khan [2], Muhammad Mansoor Khan [2] and Lucian Mihet-Popa [3,*]

[1] Department of Electrical Engineering, University of Engineering and Technology, Mardan 23200, Pakistan
[2] Department of Electrical Engineering, SEIEE, Shanghai Jiao Tong University, Shanghai 200240, China
[3] Faculty of Electrical Engineering, Ostfold University College, 1757 Halden, Norway
* Correspondence: ali@uetmardan.edu.pk (M.A.); lucian.mihet@hiof.no (L.M.-P.)

Abstract: Modular multilevel converters (MMCs) have been conceived as an alternative in front-end converter applications to enhance the converter system's reliability, minimize total harmonic distortion, and improve power quality. These converters utilize several DC-link capacitors and power electronic switches, along with switches operating with high switching frequencies, to attain the desired characteristics. Thereby, this paper systematically proposes a novel three-phase asymmetric hybrid modular multilevel converter (AHMMC) for front-end converters used in lower-medium-voltage applications. The AHMMC configuration is based on a three-phase converter connected to a per-phase series arrangement with a cascaded converter module (CCM). The study investigates the AHMMC and proposes a control scheme, which minimizes the voltage range on switches and maintains the current to its reference value. Furthermore, the study also introduces an active balancing of voltage across DC-link capacitors based on the phase opposition disposition PWM (POD-PWM) method. Our new configuration has features such as low switching loss, reduced DC-link voltage, a wider modulation range for the unity power factor (PF), and low voltage and current harmonic distortion. The simulation results are added to verify the performance of the new AHMMC topology and the usefulness of the modular control scheme. In addition, a low-voltage laboratory prototype based on customized control and power boards is built to validate the proposed converter and its control scheme in practice.

Keywords: asymmetric hybrid converter; front-end converter; hybrid modulation; modular multilevel converter; MMC; power-factor correction; PFC; series-active filter; space-vector pulse-width modulation; SV-PWM

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1. Introduction

The pervasive use of power electronics and inductive loads highlights the need to focus on line pollution and the low power factor. Considering the power electronic system, diode and thyristor rectifiers are used commonly in front-end converters as an interface with the AC mains. However, the non-linear nature of these rectifiers produces harmonic currents in the AC mains, which result in various power quality issues. Due to these issues, some techniques, such as active, passive, and hybrid filters [1], have been developed for conventional rectifiers in existing installations; however, most use expansive and bulky filters.

To maintain power quality within acceptable limits, multilevel converters (MLCs) have recently attracted attention due to their ability to limit the current total harmonic distortion (THD) to 5%, as specified by IEEE-519. These MLCs have been extensively studied for high-power applications at medium voltages as they have several advantages, including low-stress voltage on their switches, minimum voltage harmonics, and low electromagnetic interference (EMI). Conventional MLCs can be classified as a flying capacitor (FC) [2,3],

neutral point clamped (NPC) [4,5], or cascaded H-bridge (CHB) [6,7]. However, these MLC topologies have some disadvantages, for example, the NPC and FC converters have unequal voltages across switches and complex control for balancing the DC-link voltage, and the CHB requires more DC sources. Moreover, as the output voltage levels increase, the component count and voltage balancing control complexity increase, which affects the converter system's efficiency and reliability.

Recently constructed hybrid multilevel converters using several conventional MLC topologies, which are also known as hybrid modular multilevel converters (HMMC), have been introduced. Some of these HMMCs are an H-bridge with an FC module [8], an NPC with an H-bridge converter [9], a traditional three-phase two-level converter with an H-bridge module [10], a generalized FC with an n-level and active NPC (ANPC) [11], an H-bridge with a half-bridge converter [12], an FC-based ANPC converter [13], a modular multilevel matrix converter, and a Hexverter [14]. In comparison with NPCs, FCs, and CHBs, HMMCs have the advantages of high efficiency, high reliability, and lower modulation complexity [15–17]. The modular multi-level converter (MMC) is a suitable topology for medium-power high-voltage applications such as HVDC transmission [18,19], motor-driven applications [20,21], and front-end converter applications [22–24]. Moreover, the majority of research is focused on various DC-link voltages to raise output voltage levels and lower redundancy with the same number of components. In the literature, these topologies are referred to as asymmetric converters [8,25].

This paper investigates the design and control of the proposed AHMMC topology. Improved output voltage levels with minimum components are realized using the AHMMC. To reduce the switch loss, the converter switches can be flexibly operated under the proposed hybrid modulation technique, which offers a lower switching frequency. The DC-link voltages are balanced to achieve the required output voltage level. Finally, a laboratory prototype is developed to experimentally validate the proposed converter and its control scheme. A customized control board is built, which utilizes a micro-controller unit (TMS320C28346 Delfino^{TM}), complex programmable logic device (EPM570 ALTERA®), and AD conversion to realize the control in practice.

This paper is arranged as follows. Section 2 demonstrates the proposed model configuration and its working principles. Section 3 discusses the employment of the hybrid modulation strategy and Section 4 describes a modular control scheme for tracking the current and maintaining the DC-link capacitor voltage at their respective references. Sections 5 and 6 provide the simulation and experimental validation of the AHMMC and its modular control method, respectively. Finally, Section 7 provides the conclusions.

2. Proposed Model Configuration

Figure 1 presents the proposed AHMMC topology, which is based on a per-phase series configuration of the high-voltage two-level three-phase converter (fundamental converter) with a low-voltage cascaded converter module that generates five levels at the output. The two-level three-phase converter has three legs; each leg contains two alternately active switches, which are connected to a common DC source, E. Considering the *a*-phase leg, it generates an output voltage level of 0 and E at AC terminal Y. The series connecting the CCM to the *a*-phase leg contains six power switches (S_a, S_b, and S_c and, respectively, S'_a, S'_b, and S'_c) and two DC-link capacitors C_{h1} and C_{h2}. The voltage of the DC-link capacitors is $V_{Ch1} = V_{Ch2} = V_{dc} = 0.275E$ (subscript h is either a, b, or c), which yields the maximum output voltage of five levels at the AC terminal (V_{YZ}), i.e., $\pm 2V_{dc}$, $\pm 1V_{dc}$, and $0V_{dc}$. The cascaded converter module has redundant switching-state combinations of $\pm 1V_{dc}$ and $0V_{dc}$ of the output voltage levels, which are listed in Table 1.

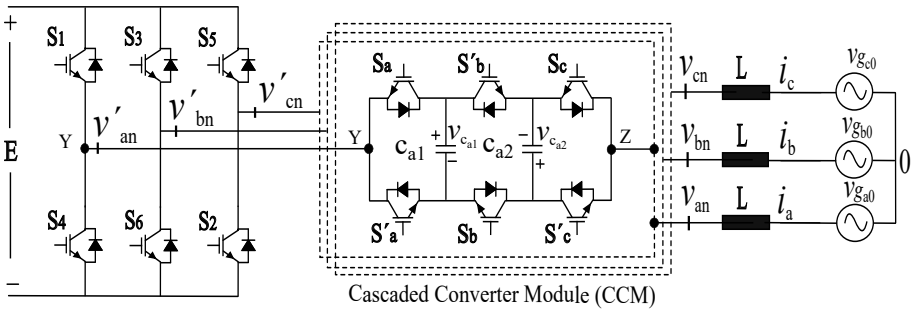

Figure 1. AHMMC topology.

Table 1. Switching modes of CCM.

Modes	Switching States			Capacitor	Capacitor	CCM V_{out}
	S_a	S_b	S_c	C_1	C_2	$V_{(YZ)}$
		Table (a)			when $i_a > 0$	
1	1	1	1	charge	charge	$2V_{dc}$
2	1	1	0	discharge	bypass	V_{dc}
3	0	1	0	bypass	by pass	0
4	1	0	0	bypass	charge	$-V_{dc}$
5	0	0	0	charge	charge	$-2V_{dc}$
		Table (b)			when $i_a > 0$	
1	1	1	1	charge	charge	$2V_{dc}$
2	0	0	1	bypass	discharge	V_{dc}
3	1	0	1	bypass	bypass	0
4	0	1	1	charge	bypass	$-V_{dc}$
5	0	0	0	charge	charge	$-2V_{dc}$

The AC-side dynamics of the AHMMC system in Figure 1 are expressed by a switched equivalent circuit in (1)–(3):

$$\frac{di_h}{dt} = \frac{1}{L}(S_x V_{Ch1} + S_y V_{Ch2} \mp S_z E \pm V_{gho}) \tag{1}$$

$$\frac{dV_{Ch1}}{dt} = \frac{S_x i}{C_{h1}} \tag{2}$$

$$\frac{dV_{Ch2}}{dt} = \frac{S_y i}{C_{h2}} \tag{3}$$

where $V_{gho} = Esin(wt)$ is a grid voltage with a frequency of 50Hz, S_{zh} is the switching sequence for the different phases to neutral voltage of the three-phase two-level converter [26], and S_{xh} and S_{yh} are the switching functions of the AHMMC (subscript h is either a, b, or c), which can be expressed by (4) and (5):

$$S_{xh} = \mathrm{S_a S_b} - \mathrm{S'_a S'_b} \tag{4}$$

$$S_{yh} = \mathrm{S_b S_c} - \mathrm{S'_b S'_c} \tag{5}$$

3. Hybrid Modulation Strategy

For any given topology, the strategy used for pulse-width modulation (PWM) plays a decisive role in the switch loss. For the PWM method, the number of voltage pulses at the output is achieved by reference voltage approximation. The present study's emphasis is on

the modulation scheme, which should be designed so that the switches with the highest voltage stresses operate at low switching frequencies and the low-stress switches operate at high frequencies. The PWM modulation strategy is divided into two parts: a PWM strategy for the three-phase converter and a PWM strategy for the per-leg CCM. Since the switches of the three-phase inverter are under higher voltage stress, they should be operated at the lowest frequency with the fewest pulses possible in each fundamental cycle. The CCM's switches are classified according to their voltage stresses, followed by the elaboration of the middle-leg switches and the outer-leg switches in a section (III-C). The approach used to determine the timing of these pulses is to alternate the PWM techniques [17,18]. In the literature, the modulation methods studied for MMCs include fundamental switching-frequency PWM [27], carrier-based PWM [28,29], space-vector PWM [30–32], and selective harmonic elimination (SHE) PWM [13]. The SV-PWM-based technique is widely used in applications, such as motor control, electric vehicles, and grid interfacing, due to its many advantages [33–35].

3.1. Three-Phase Converter Modulation

Since the stress on the three-phase converter is higher, SHE-PWM and SV-PWM are studied as low-frequency-switching modulation techniques. The increased switching transitions per fundamental cycle increase the zero crossing requirements in the harmonic reference signal, which are compensated for by the per-leg CCM. In SHE-PWM, the switching transitions of five angles ($\alpha 1$–$\alpha 5$) in the first-quarter cycle of the fundamental period are optimally chosen to eliminate the first four lower-order non-triplen harmonics [36]. As a result, the switching losses associated with the middle leg of the cascaded converter increase. Figure 2 depicts a fundamental signal comparison of the phase voltage of the three-phase converter, which is achieved using the SHE-PWM and SV-PWM methods, for the harmonic compensation reference signal calculation. To target minimum switching effort, SV-PWM operating at 150 Hz is suggested.

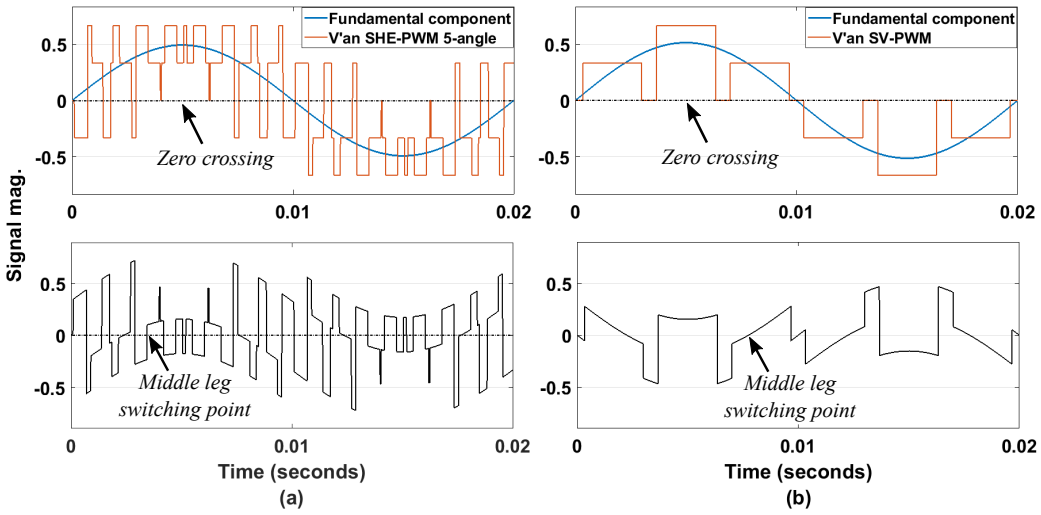

Figure 2. Signal comparison for harmonic compensation reference signal calculation. (**a**) SHE-PWM as a modulation strategy for 3-phase converter. (**b**) SV-PWM as a modulation strategy for 3-phase converter.

Referring to Figure 3, for different switch combinations of the three-phase converter in Figure 1, the output state voltage vector is mapped to distinct active vectors V_1–V_6 in the alpha-beta coordinates. Additionally, the space vectors V_0 and V_7 are zero vectors with zero magnitudes located at the center of the hexagon. In the proposed SV-PWM method, a hexagon is split into three sectors: sector I, which contains two active vectors V_1 and V_2; sector II (V_3 and V_4), and sector III (V_5 and V_6). Considering sector I, V_1 and V_2 are applied to the on-time interval T1, and the zero vectors V_0 and V_7 are applied to the off-time

interval T0, where the vector application time T1 and T0 are calculated in terms of angles and can be equated as:

$$T_1 = 120^o \times M_f \quad (6)$$

$$T_0 = 120^o \times (1 - M_f) \quad (7)$$

where M_f is the modulation index of the two-level three-phase converter. In this method, the active vectors are placed in the center between the symmetric zero vectors. For this modulation strategy, as an example of a particular vector at a modulation index m = 0.9, the waveform appears as depicted in Figure 3b. The converter's fundamental component is kept in phase with the grid voltage and only the time interval (on and off time intervals) changes, which varies according to the modulation depth.

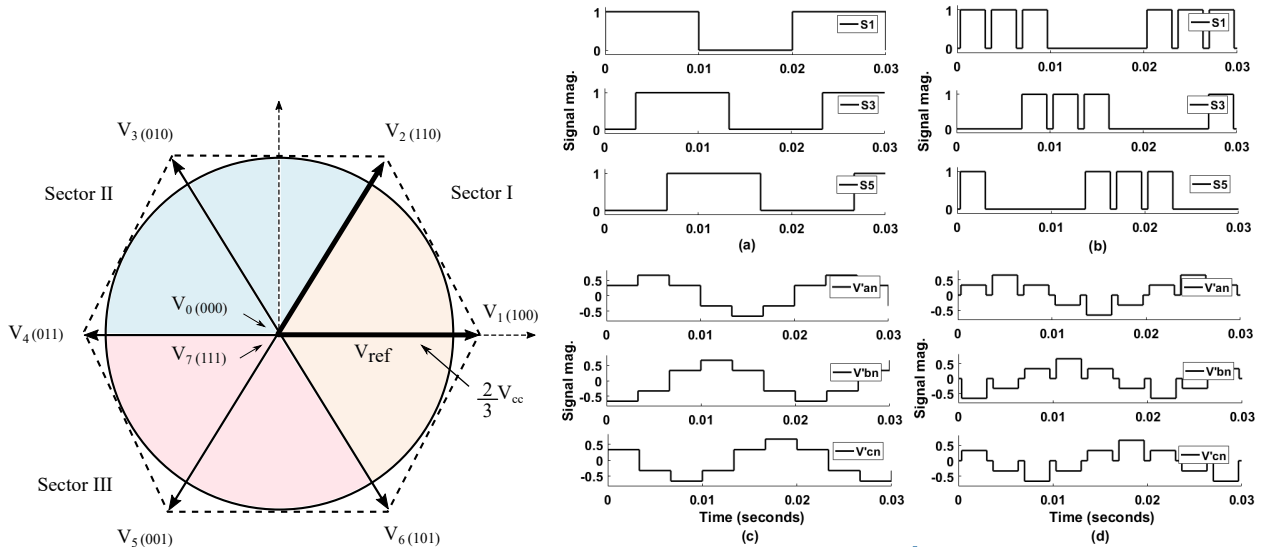

Figure 3. SVM technique for three-phase converter. (**a**) Pole voltages of upper switches (S_1, S_3, S_5) at m = 1. (**b**) Pole voltages of upper switches (S_1, S_3, S_5) at m = 0.9. (**c**) Phase voltages at m = 1. (**d**) Phase voltages at m = 0.9.

The maximum voltage requirement of the summated DC-link voltage (V_{C1} + V_{C2}) for harmonic compensation also depends on the modulation strategy of the fundamental converter. To compare the DC-link requirement, SHE-PWM is considered another possible candidate to operate the fundamental converter switches with 500 Hz low-frequency switching. For different modulation depths, the results in Figure 4 show the DC-link capacitors' voltage (in the CCM) to compensate for the harmonics. However, the selection of the SHE-PWM technique as the modulation strategy for the fundamental converter requires a higher DC-link capacitor voltage than the SV-PWM technique. Based on the above discussions, the SV-PWM technique (150 Hz switching frequency) is chosen as the modulation technique for the fundamental three-phase converter.

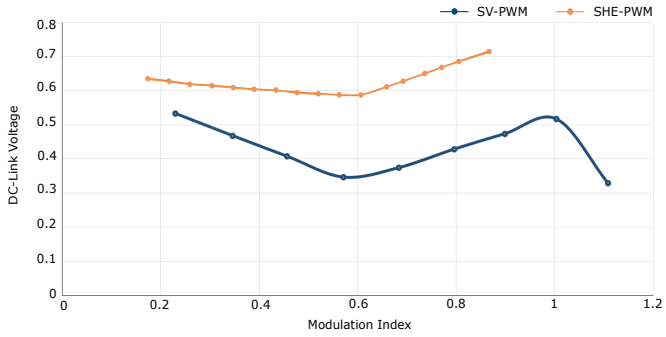

Figure 4. SHE-PWM vs. SV-PWM DC-link requirements at different modulation indexes (m).

3.2. Modulation Range

Considering the SV-PWM modulation strategy, the maximum output voltage of the cascaded converter module also relies on the modulation index M_f of the two-level three-phase converter, as expressed by Equation (8):

$$M_f = \frac{\sqrt{3}(|\ \overline{V}_{an_{(ref)}}\ |)}{\mathrm{E}} \tag{8}$$

where $\overline{V}_{an_{(ref)}}$ is the reference voltage vector and E is the magnitude of the DC bus. Slightly modifying the modulation index range results in a high impact on the DC-link voltage requirement for harmonic minimization. Figure 4 depicts the maximum CCM modulation index (m) of 10% that can be achieved. The maximum modulation index m = 1.10 requires a DC-link capacitor voltage of $(\frac{1}{3})$E (DC-bus voltage). As the modulation index of the fundamental converter decreases to m = 0.88, the sum of the DC-link voltages of 0.47E is required to minimize the harmonics produced by the fundamental converter, as shown in Figure 4. Reducing the DC-link voltage requirements for harmonic compensation minimizes the voltage stress on the semiconductor switches, which provides an advantage over varying the switching frequency according to the system design.

3.3. Cascaded Converter Module Modulation

The switches used in cascaded converter modules are classified into two groups: (i) high-voltage low-frequency switches, and (ii) low-voltage high-frequency switches. For the design aspect, the middle-leg switches S_b and S'_b of the cascaded converter module in Figure 1 handle high-voltage stress, i.e., $2V_{dc}$. As the third harmonic forms a zero sequence, the resulting zero crossing frequency of these switches is 550 Hz, resulting in reduced switch loss. The outer-leg switches of the cascaded converter module are under low stress, i.e., V_{dc}, and as a result, they are switched at four times the frequency of the middle-leg switches. To generate all the levels and fulfill the requirements of balancing the DC-link capacitor voltages, a phase opposition disposition (POD) PWM method is employed in the cascaded converter module, as shown in Figure 5. In this method, the carrier signals have a level shift and a phase shift across the zero references. The resulting equivalent frequency using this method is 3.2 kHz, with the highest effective frequency being 1.6 kHz, which results in further distribution of losses in the system.

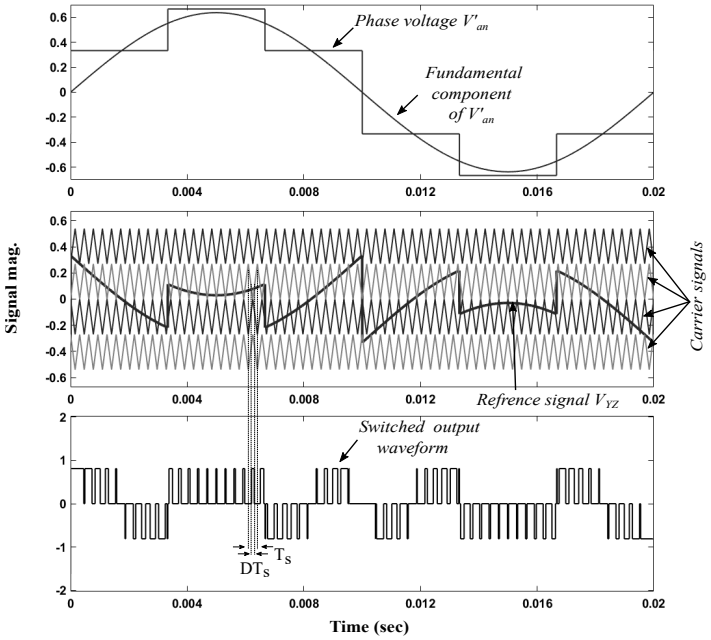

Figure 5. POD-PWM control method.

The complete modulation strategy for the AHMMC is as follows: (i) the high-voltage three-phase converter offers fundamental component support and is run at a low switching frequency, and (ii) the CCM as a series-active filter compensates the high harmonics generated by the fundamental converter. The output of the CCM depends on the magnitude of the reference modulating signal, as shown in Figure 4. As the CCM acts as a series filter, the reference modulating signal for this module is obtained from the phase output voltage by subtracting its fundamental component. Here, the maximum modulation index is considered for the three-phase converter. Therefore, the resulting reference modulating signal for the CCM generates an output voltage of three levels, as shown in Figure 5. Figure 6 depicts the output voltage of the *a*-phase leg V_{an} of the AHMMC at different switching angles, as shown in Table 2.

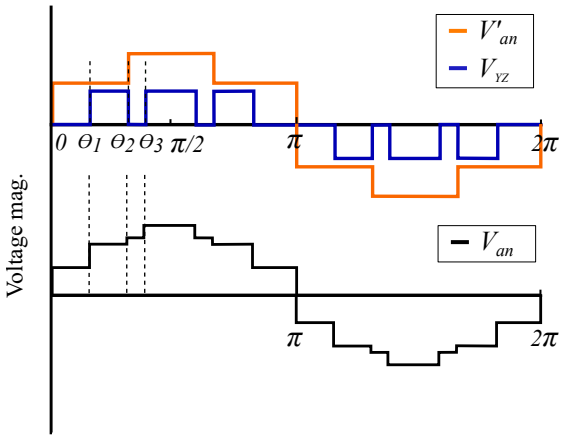

Figure 6. Phase-output voltage of the AHMMC operating at a different angle.

Table 2. AHMMC output phase voltage (V_{an}).

Angle	V_{YZ}	V'_{an}	$V_{an} = V_{YZ} + V'_{an}$
$0 \leq \theta \leq \theta_1$	0	$\frac{1}{3}$E	$\frac{1}{3}$E
$\theta_1 \leq \theta \leq \theta_2$	V_{dc}	$\frac{1}{3}$E	$\frac{1}{3}$E+ V_{dc}
$\theta_2 \leq \theta \leq \theta_3$	0	$\frac{2}{3}$E	$\frac{2}{3}$E
$\theta_3 \leq \theta \leq \pi/2$	V_{dc}	$\frac{2}{3}$E	$\frac{2}{3}$E+ V_{dc}

The overall output phase voltage of the *a*-phase V_{an} is mathematically expressed by Equations (9)–(11):

$$V_{an} = V'_{an} + V_{YZ} \tag{9}$$

$$V'_{an} = \frac{4}{3\pi}\mathrm{E}\sum_{r}^{\infty}\frac{1}{r}(\cos(\frac{\pi}{3}r + \theta_f) + M_f)(\sin(r\omega t)) \tag{10}$$

$$V_{YZ} = V'_{an} - (\frac{4}{3\pi}\mathrm{E}(\cos(\frac{\pi}{3} + \theta_f) + M_f)(\sin(\omega t))) \tag{11}$$

where θ_f is calculated from the off-time interval T_0 of SV-PWM applied to the fundamental converter, which varies with the modulation depth M_f of the fundamental converter, and r is the harmonic component.

4. Control Scheme

Despite the aforementioned merits, MMCs require many DC-link capacitors to generate a multi-level output. A challenge for MMCs irrespective of the module type used is the voltage balancing [37,38] needed to enhance the converter's reliability. In order to tackle this issue, various methods have been proposed in the literature. Voltage balancing techniques among phase clusters are proposed in [39]. One method for voltage balancing

is the independent control of each phase cluster's active power [40]. Another proposed method involves DC-link voltage balancing using negative-sequence currents [41].

To track the proposed converter current and regulate the DC-link capacitor voltage to their respective reference values, a control algorithm is employed, which consists of decoupled, current-control, and voltage-control techniques. The decoupled voltage-control technique is further classified into control objectives, which are (i) the average voltage control between the three-phase converter and the CCM, (ii) inter-module energy balancing among the CCMs, and (iii) individual capacitor voltage balancing in the CCM. The functions of blocks A, B, C, and D shown in Figure 7 are summarized as follows: (i) block A: feed-forward fundamental component support, (ii) block B: harmonic signal extraction for the CCM, (iii) block C: zero-sequence voltage calculation, and (iv) block D: controlled current signal from the decoupled control loop.

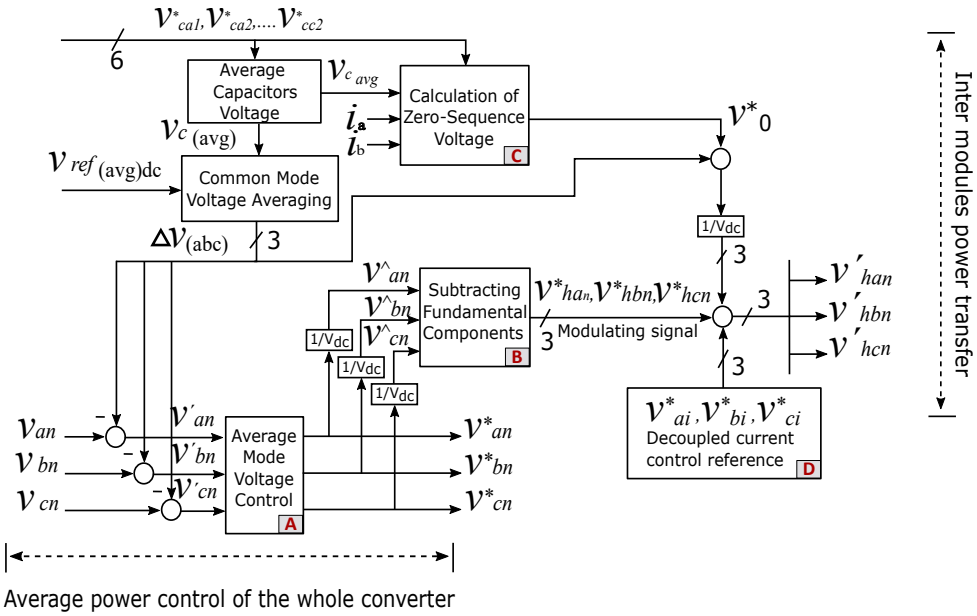

Figure 7. General block diagram of the AHMMC's control.

4.1. Decoupled Current Control Loop

The effectiveness of a converter system is determined by the performance of current control; therefore, the current control is required to respond fast to transients and exhibit satisfactory steady-state behavior. Current control in the synchronous reference frame (SRF) (*dq* coordinates) offers attractive features, which are widely known and applied in most PWM schemes [42,43].

In this study, the output voltage generated by each phase-cascaded converter module determines the converter current control that is in use. This control strategy's primary goal is to provide the required voltage for the needed output current. The current control has two main paths: the feed-forward fundamental component support, which is provided by the three-phase converter, and the harmonic and fast current control support, which is provided by the cascaded converter module, as depicted in Figure 7. The decoupled current control loop in Figure 8 is applied to the cascaded converter modules, as these converter modules provide high-frequency support. Thus, the reaction will be faster if the grid voltages change abruptly.

Referring to Figure 1, the following current-voltage equation (12) is deduced by ignoring the resistive components.

$$\begin{bmatrix} Vg_{a0} \\ Vg_{b0} \\ Vg_{c0} \end{bmatrix} - \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (12)$$

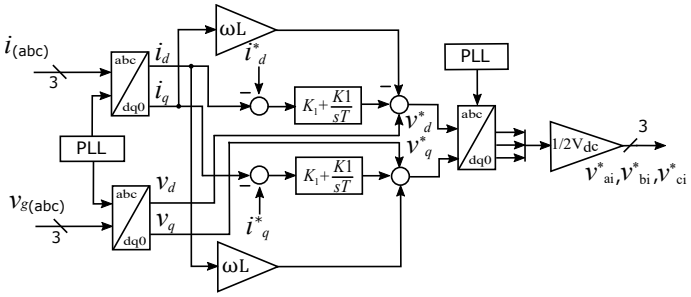

Figure 8. Current control implementation in the SRF.

The Park transformation matrix attaining the d-q components of the three-phase currents i_a, i_b, and i_c, and voltages V_{an}, V_{bn}, and V_{cn} is provided in [42] and in (13) and (15) as follows:

$$T_P = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - \frac{2}{3}\pi) & \sin(\omega t + \frac{2}{3}\pi) \\ \cos(\omega t) & \cos(\omega t - \frac{2}{3}\pi) & \cos(\omega t + \frac{2}{3}\pi) \end{bmatrix} \tag{13}$$

Therefore

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = T_P \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{14}$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = T_P \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{15}$$

Considering a balanced three-phase voltage, v_q will be zero as $\vec{V}$g is aligned with the d-axis. Applying the d-q transformation, the three-phase active and reactive power can be expressed by (16) and (17), respectively, as follows:

$$P = \frac{3}{2}\left[(v_d i_d) + (v_q i_q)\right] \tag{16}$$

$$Q = \frac{3}{2}\left[(v_q i_d) - (v_d i_q)\right] \tag{17}$$

which shows that by controlling i_d and i_q independently, the control of active/reactive power will be achieved. The current commands i^*_d and i^*_q of their respective axes are expressed by (18) and (19) as follows:

$$i^*_d = \frac{p^*}{v_d} \tag{18}$$

$$i^*_q = \frac{q^*}{v_q} = 0 \tag{19}$$

where p^* and q^* are the active and reactive power commands, respectively. Here, a strictly unity power factor is considered. $q^* = 0$ guarantees the system operation at a unity power factor. The controlled reference signal is achieved by the inverse d-q transformation, as expressed in (20).

$$\begin{bmatrix} v^*_d \\ v^*_q \end{bmatrix} = \begin{bmatrix} v_d \\ 0 \end{bmatrix} + \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + K_1 \begin{bmatrix} i^*_d - i_d \\ i^*_q - i_q \end{bmatrix} + \frac{K_1}{T_1} \int \begin{bmatrix} i^*_d - i_d \\ i^*_q - i_q \end{bmatrix} dt \tag{20}$$

Applying the d-q to abc transformation gives the decoupled current controlled signals V_{ai}^{*}, V_{bi}^{*}, and V_{ci}^{*} shown in Figure 8, which are applied to the cascaded converter modules shown in Figure 7.

The current control loop bandwidth relies on the PWM's frequency in order to lessen the effect of distortion in the current resulting from abrupt voltage dips or swells in the grid. Equation (21) describes how the PWM is changed in the DC voltage feed-forward control loop to lessen the influence of DC-link voltage ripples:

$$d = \left(a_1 \frac{|V_{out}|}{V_{c1}} + a_2 \frac{|V_{out}|}{V_{c2}} + a_3 \frac{|V_{out}| - V_{c1}}{V_{c2}} + a_4 \frac{|V_{out}| - V_{c2}}{V_{c1}} \right) \times Sign(V_{out}) \tag{21}$$

where the duty ratio for the cascaded module output voltage levels is denoted by d and, a_1, a_2, a_3, and a_4 are the PWM output conditions given in Table 3. The output direction of the PWM is determined by $Sign(V_{out})$ in (22):

$$Sign(V_{out}) = \begin{cases} 1 & \text{if } V_{out} \geq 0 \\ -1 & \text{if } V_{out} < 0 \end{cases} \tag{22}$$

Table 3. PWM Operating Conditions.

Operating Condition	a_1	a_2	a_3	a_4
V_{c1} is a lower capacitor				
$\mid V_{out} \mid \leq V_{c1}$	1	0	0	0
$V_{c1} < \mid V_{out} \mid < (V_{c1} + V_{c2})$	0	0	1	0
V_{c2} is a lower capacitor				
$\mid V_{out} \mid \leq V_{c2}$	0	1	0	0
$V_{c2} < \mid V_{out} \mid < (V_{c1} + V_{c2})$	0	0	0	1

4.2. Decoupled Voltage Control Loop

The imbalance of voltage in the DC-link capacitors in the per-phase cascaded module arises mainly due to the inaccuracy of the PWM gating signal over a cycle and the real component produced by the non-linearity of the semiconductor devices. To mitigate this balancing issue, a decoupled voltage balancing control is employed with the control objectives that are classified and discussed below.

4.2.1. Average Voltage Control

The sum of the charge across the average-mode DC-link capacitor (V_{c1} and V_{c2}) in each phase of the cascaded module is finite. An energy exchange is required between the three-phase leg/inverter or grid to compensate for the total energy. The total sum of all the charges across these cascaded modules will decide the amount of energy that is required to be absorbed from the AC main or three-phase converter. As the fundamental component of the voltage is a positive sequence and the current is sinusoidal, the sign of the positive-sequence voltage will decide the direction of the energy exchange between the cascaded modules and the grid or three-phase converter. If the sum of the capacitors' energies in the cascaded modules is less than the reference value, the energy will be absorbed from the three-phase converter or grid. If the energy is higher, it will transfer to the three-phase converter or grid. Therefore, average DC-link capacitor voltage balancing is attained through positive-sequence voltage. Figure 9a shows the average-mode DC-link

capacitor voltage control loop. The reference signal for controlling the average-mode DC-link capacitor voltages per phase is given in (23):

$$\begin{bmatrix} \triangle V_a \\ \triangle V_b \\ \triangle V_c \end{bmatrix} = \triangle V \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2}{3}\pi) \\ \sin(\omega t + \frac{2}{3}\pi) \end{bmatrix} \tag{23}$$

To keep the sum of the capacitors' energies in the cascaded modules balanced at the required value, the average sum of all the DC-link voltages of the cascaded modules is compared with the reference DC value. The error signal is given to a PI controller to attain a compensated $\triangle V$ reference signal, which is deduced in (24)–(26):

$$E_c = \frac{1}{2} C \left(\frac{dVc_{avg}}{dt} \right)^2 \tag{24}$$

$$Vc_{avg} = \frac{1}{3} \sum_{h=a,b,c} \sum_{l=1,2} Vc_{hl} \tag{25}$$

$$\triangle V = \left(Vref_{(avg)(dc)} - Vc_{avg} \right)^* \left(K_2 + \frac{K_2}{sT_2} \right) \tag{26}$$

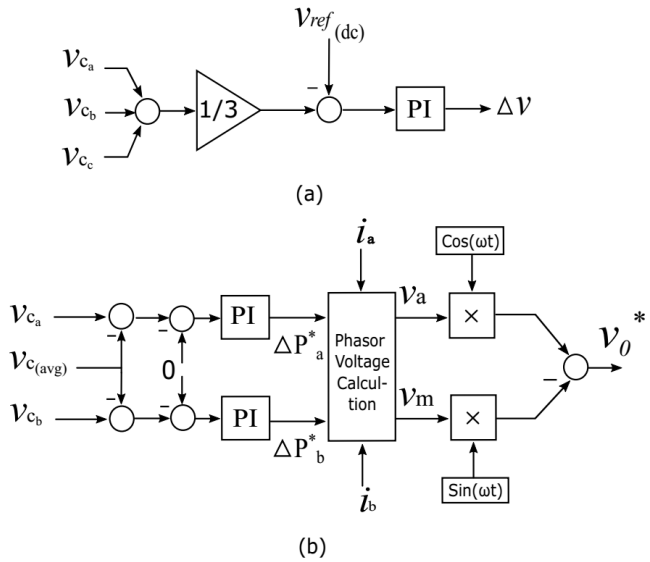

Figure 9. Voltage control loop. (**a**) Average-mode DC-link capacitor voltage control loop. (**b**) Difference-mode DC-link capacitor voltage control loop.

4.2.2. Inter-Module Power Balancing

In practice, after transferring the average power, the AHMMC cannot be naturally balanced because of component parametric variances or different control signal delays, which inevitably cause unbalanced power among the cascaded modules. Redistributing the power among the cascaded module converters is carried out to address the uneven energy distribution. A corrective voltage control, i.e., difference-mode voltage control, is realized, which is dependent on injecting zero-sequence voltage. By implementing the difference-mode DC-link capacitor voltage control, power among the cascaded modules is exchanged by zero-sequence voltage injection, ensuring that the power will not appear at the output of the cascaded converter modules. Hence, the power is exchanged equally among the cascaded modules. The analysis of the difference-mode DC-link capacitor

voltage control is shown in Figure 9b. The average active power due to the zero-sequence voltage can be calculated by (27) and (28):

$$P_{a0} + P_{b0} + P_{c0} = 0 \tag{27}$$

where

$$P_{a0} = V_0 e^{j0} I e^{j0} \tag{28}$$

Similarly, the change in the power commands for the *a*-phase, *b*-phase, and *c*-phase can be expressed by (29):

$$\begin{bmatrix} \triangle P_a^* \\ \triangle P_b^* \\ \triangle P_c^* \end{bmatrix} = V_0 e^{j0} I \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2}{3}\pi) \\ \sin(\omega t + \frac{2}{3}\pi) \end{bmatrix} \tag{29}$$

The controlled converter currents, which are in phase with the grid voltage, are assumed to contain positive-sequence currents, and the power command in phasor form by the zero-sequence voltage is given by (30) and (31):

$$\triangle P_a^* = Re\Big[(V_a - jV_m) I_a\Big] \tag{30}$$

$$\triangle P_b^* = Re\Big[(V_a - jV_m) I_b\Big] \tag{31}$$

The zero-sequence voltage is calculated by comparing (30) and (31) and is given as follows:

$$V_0 = \big(V_a - jV_m\big) \tag{32}$$

4.2.3. Individual Capacitor Voltage Balancing

Once the power is distributed equally among the cascaded modules, it is essential to balance each DC-link capacitor's voltage to the desired reference, which is accomplished by the voltage swapping approach, which utilizes the redundant switching states shown in Table 1. Based on the relationship, redundant switching states are used for charge swapping:

- When $(i_{(hdc)} \times V_{Ch1}) < 0$, if $V_{Ch1} < V_{Ch2}$, Table 1 (b) will subsequently be chosen.
- When $(i_{(hdc)} \times V_{Ch2}) > 0$, if $V_{Ch1} > V_{Ch2}$, Table 1 (a) will subsequently be chosen.

where $i_{(hdc)}$ is the DC reference current direction (subscript h is either a, b, or c). The voltage balancing of the capacitors is accomplished using the relation of the selected tables mentioned above.

5. Simulation Results

A simulation of the AHMMC configuration shown in Figure 1 is performed in MATLAB/Simulink. Using the specifications mentioned in Table 4, the simulated findings from the research were scaled to the experimental results.

Table 4. Proposed system's parameters.

Parameter	Symbol	Value
Inductance	L	0.7 mH
DC-link Capacitor	C	20 mF
Cascaded Converter	PWM_{freq}	3.2 kHz
Three-phase Converter	SW_{freq}	150 Hz
Capacitor Voltage	Vc	110 V_{dc}
Grid Voltage(rms)	Vg_0	110 V
Grid Current(rms)	I_s	15 A
DC-bus Voltage	E	300 V

Extensive simulations were conducted to choose the components. Capacitors were chosen based on a peak–peak voltage ripple of 2%, whereas inductors were chosen for a peak–peak current ripple of 0.5% at the maximum rated current. A switching frequency of 3.2 kHz was chosen because the outer-leg switches on the cascaded converter module were under minimal voltage stress (1.6 kHz effective switching frequency). By operating the outer-leg switches of the cascaded converter modules S_a and S_c at a switching frequency of 3.2 kHz, the current ripple, inductor size, and overall system costs were minimized.

Figure 10 demonstrates the simulation waveforms of the single-leg phase-output voltage of the AHMMC topology. The output voltage V_{an} was obtained by adding the *a*-phase output voltage of the fundamental converter to the output voltage of the cascaded converter module. It is clear that the fundamental converter with high-voltage stress on the semiconductor devices was switched at a low frequency, whereas the cascaded converter module was switched at a high frequency to compensate for the harmonics produced by the fundamental converter.

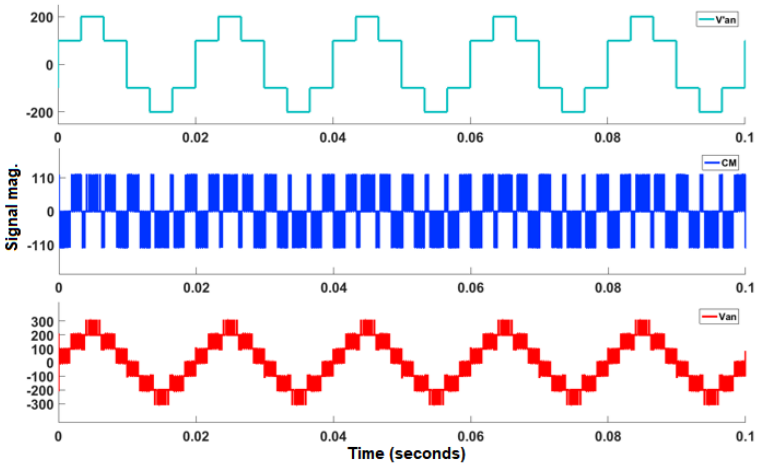

Figure 10. Single-leg phase-voltage of AHMMC (V_{an}).

Figure 11 shows the simulation results of the three-phase phase voltages. At the maximum modulation index M_f = 1 of the fundamental converter, the AHMMC topology generated an output voltage of seven levels. When the modulation index value was reduced to M_f = 0.9, the converter fundamental component was in phase with the grid voltage and only the sampling time changed, which varied with the modulation depth, as shown in Figure 12. Figure 13 shows the simulation results of the three-phase line voltages. The output line voltage of the AHMMC topology was $\sqrt{3}V_{an}$, and at M_f = 1, it generated

an output voltage of nine levels. Figure 14 shows the output line voltages when the modulation index value was reduced to $M_f = 0.9$.

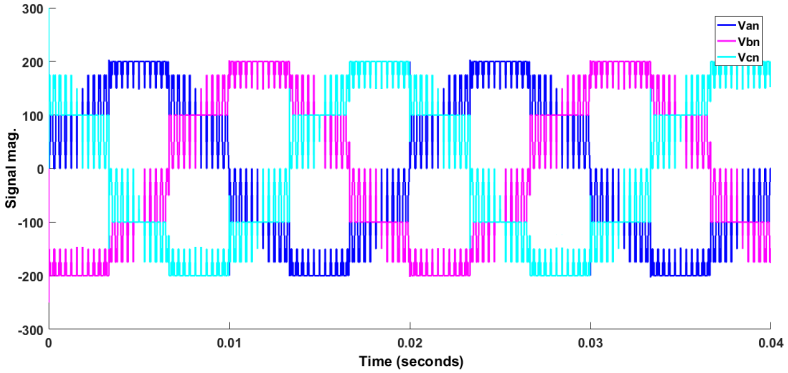

Figure 11. AHMMC output phase voltages at $M_f = 1$.

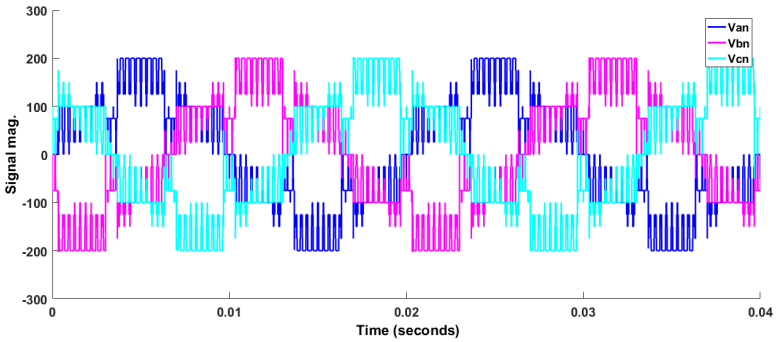

Figure 12. AHMMC output phase voltages at $M_f = 0.9$.

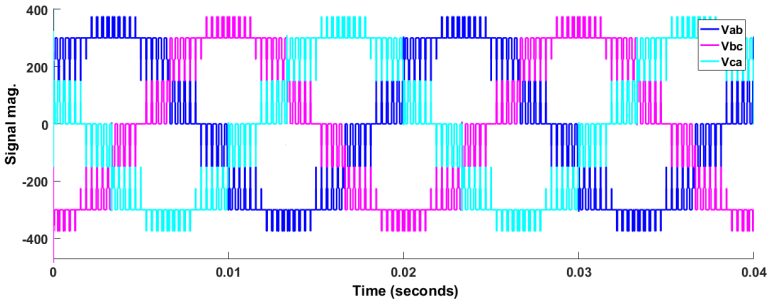

Figure 13. AHMMC output line voltages at $M_f = 1$.

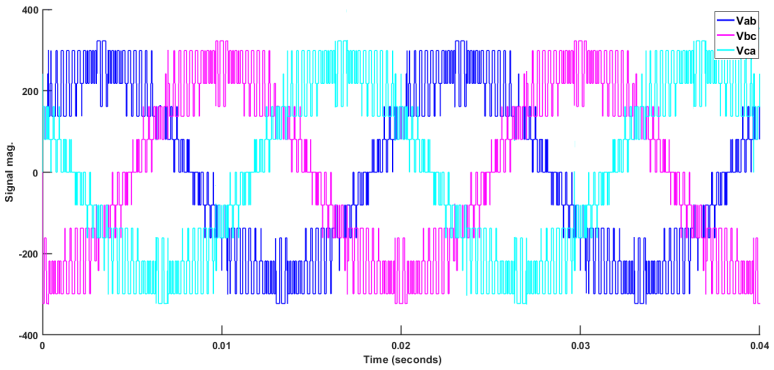

Figure 14. AHMMC output line voltages at $M_f = 0.9$.

Figure 15 shows the waveform of the proposed converter current. It is clear that the converter tracked its reference current, which was realized in the *dq* reference coordinates. The current tracked the reference value I_{ref}, even when it changed direction (180° out of phase with the grid voltage) to ensure a bidirectional active power flow. Figure 16 shows the simulation results of the converter phase voltage and current with variations in the power transfer (when the amplitude of the reference current was changed from a 50% to a 100% converter rating).

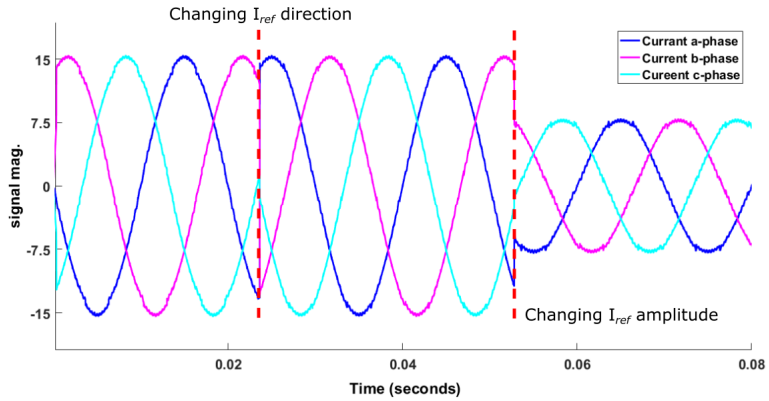

Figure 15. AHMMC current waveform.

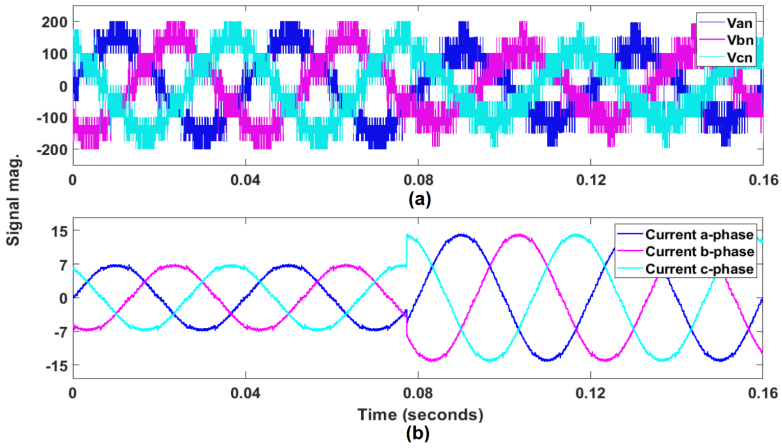

Figure 16. AHMMC phase voltage and current with variations in the power transfer: (**a**) phase voltages, (**b**) converter current.

A decoupled voltage control technique was applied to maintain the balance of the summated DC-link capacitor voltage in the cascaded module to its reference value. However, the DC-link capacitor voltage of the cascaded modules was not naturally balanced and was affected when the output terminal is connected through one of the DC-link capacitor terminals. The DC-link capacitor voltage in each cascaded converter module, V_{cn1} and V_{cn2} (subscript n is either a, b, or c), diverged from its reference value and entered into an over-charging/under-charging state, respectively. The individual DC-link capacitor voltage balancing in the cascaded converter modules was realized by the charge-swapping technique using the redundant switching-state selection, which converged the capacitor voltages to their respective reference values. Figure 17 depicts the simulation results of the balanced DC-link capacitor voltages of the cascaded converter modules. The balancing of the summated DC-link capacitor voltage, which was achieved by redistributing the power among the cascaded converter modules, is shown in Figure 17a. Initially, swapping was enabled that converged the DC-link capacitor voltage to its reference value. When the swapping of the cascaded converter module was disabled, the DC-link capacitor voltage deviated from its reference value, as shown in Figure 17b.

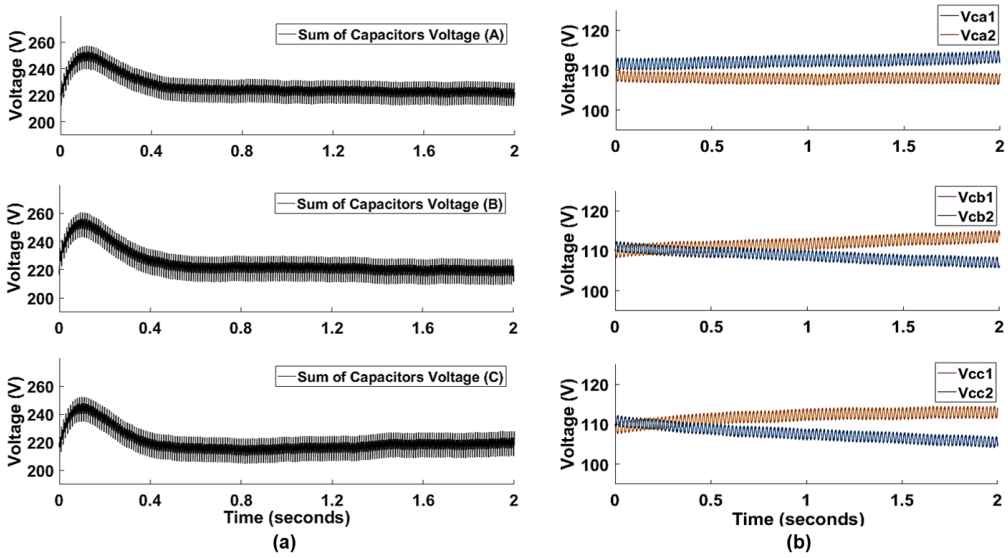

Figure 17. Balanced DC-link capacitors: (**a**) balanced summated DC-link capacitor voltage, (**b**) deviation of the DC-link capacitor voltage from its reference value when voltage swapping is disabled.

6. Experimental Results

Using a low-voltage laboratory prototype, as illustrated in Figure 18, the proposed converter and its modular control strategy were experimentally validated. A customized control board was built, which utilized a micro-controller unit (TMS320C28346 Delfino^{TM}), complex programmable logic device (EPM570 ALTERA$^{®}$), and AD conversion to realize the control in practice. It can be observed that all the experimental results are in good agreement with the results achieved in the simulation.

Figure 19 demonstrates the experimental results of the single-leg phase-output voltage of the AHMMC topology. The converter output voltage V_{an} was obtained by adding the *a*-phase output voltage of the fundamental converter to the output voltage of the cascaded converter module. Figure 20 shows the experimental results of the three-phase phase voltages. At the maximum modulation index $M_f = 1$ of the fundamental converter, the proposed AHMMC topology generated an output voltage of seven levels. Figure 21 depicts the experimental waveform of the output phase voltages at $M_f = 0.9$ in which the fundamental component of the converter was in phase with the grid voltage, and due to the variation in the sampling time, the modulation depth changed.

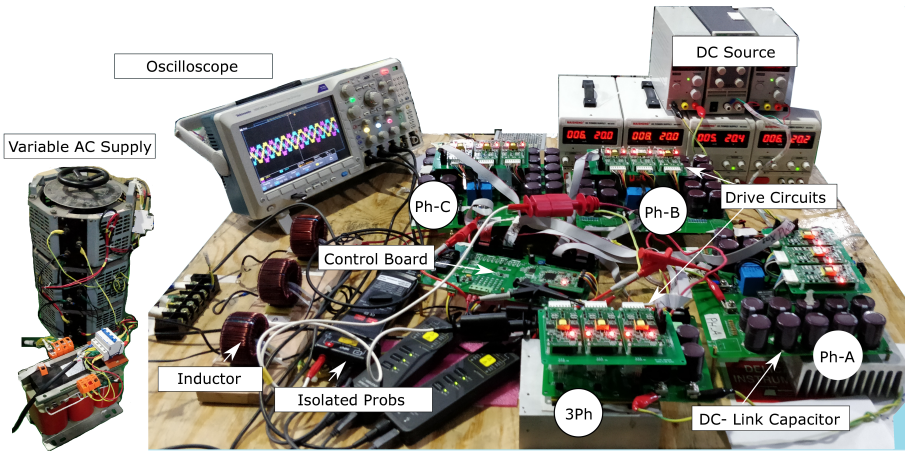

Figure 18. Low-voltage laboratory prototype.

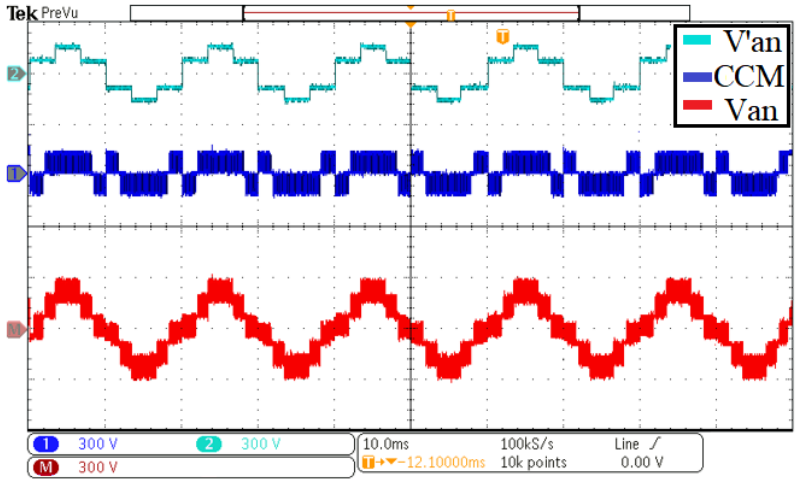

Figure 19. Experimental waveform of single-leg phase-voltage of AHMMC (V_{an}) tracing channels 1, 2, 3 (300 V/div).

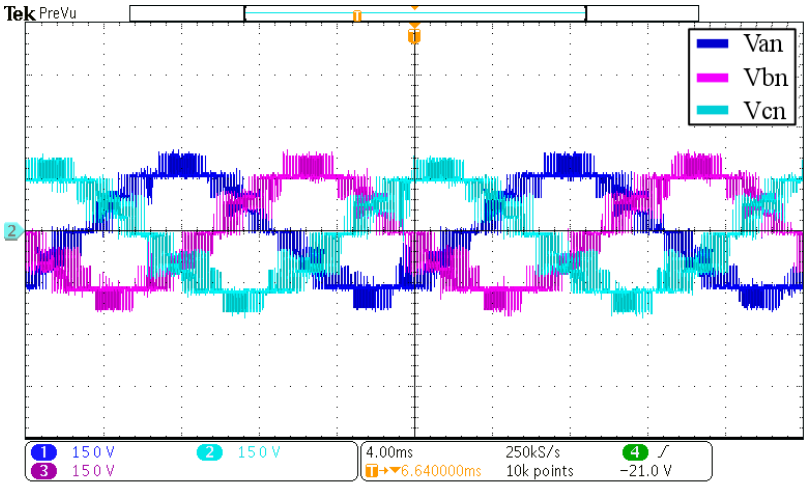

Figure 20. Experimental waveform of AHMMC output phase voltages at M_f = 1 tracing channels 1, 2, 3 (150 V/div).

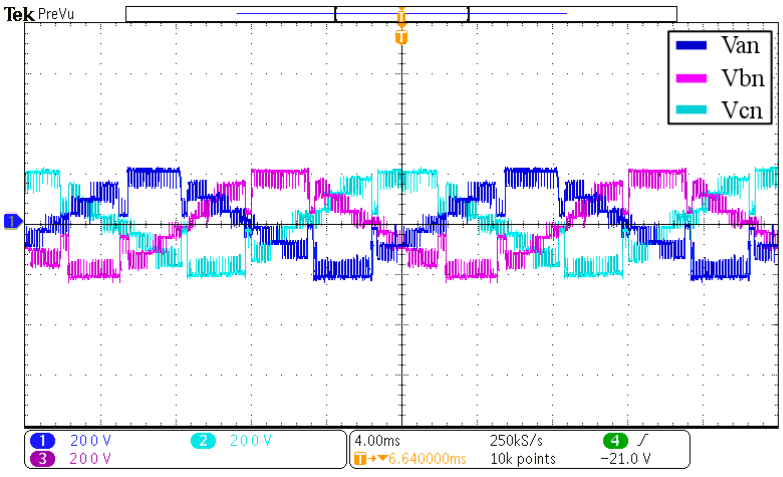

Figure 21. Experimental waveform of AHMMC output phase voltages at M_f = 0.9 tracing channels 1, 2, 3 (200 V/div).

Figure 22 shows the experimental results of the three-phase line voltages. The output line voltage of the AHMMC topology was $\sqrt{3}V_{an}$; therefore, at M_f = 1, it generated an output voltage of nine levels.

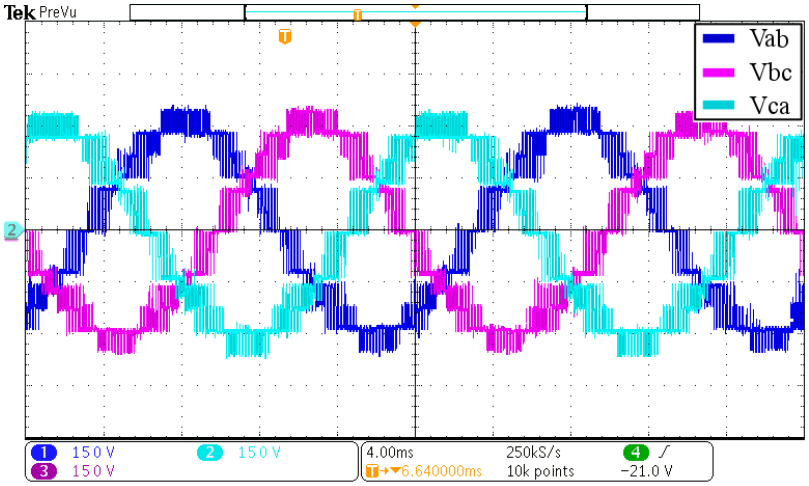

Figure 22. Experimental waveform of AHMMC output line voltages at M_f = 1 tracing channels 1, 2, 3 (150 V/div).

Figure 23 shows the experimental waveform of the proposed converter current. It can be seen that the converter tracked its reference value I_{ref}, even when it changed direction (180° out of phase with the grid voltage) to ensure the bidirectional active power flow.

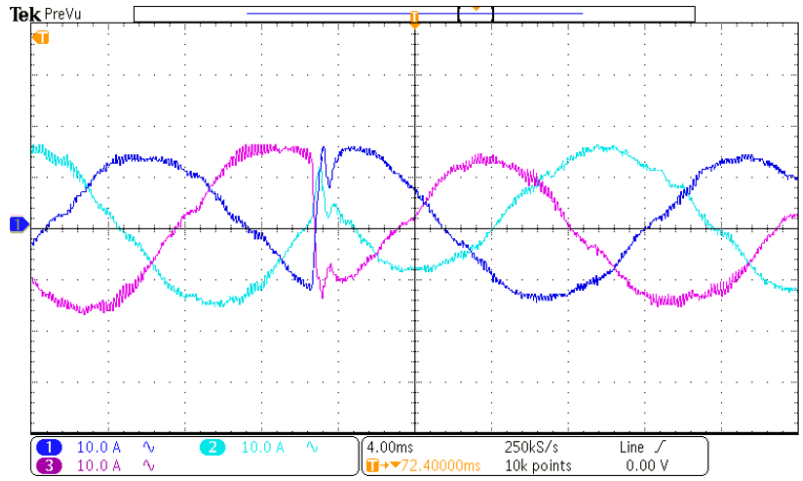

Figure 23. Experimental waveform of AHMMC current tracing channels 1, 2, 3 (10A /div).

Figure 24 depicts the experimental waveforms of the DC-link capacitor voltages of the CCMs connected to the *a*- and *b*-phase legs of the three-phase converter. Initially, the swapping in the *a*-phase cascaded converter module was disabled, which resulted in the deviation of the DC-link capacitor voltage from its reference value. When the swapping was enabled, the DC-link capacitor voltage converged to its reference value.

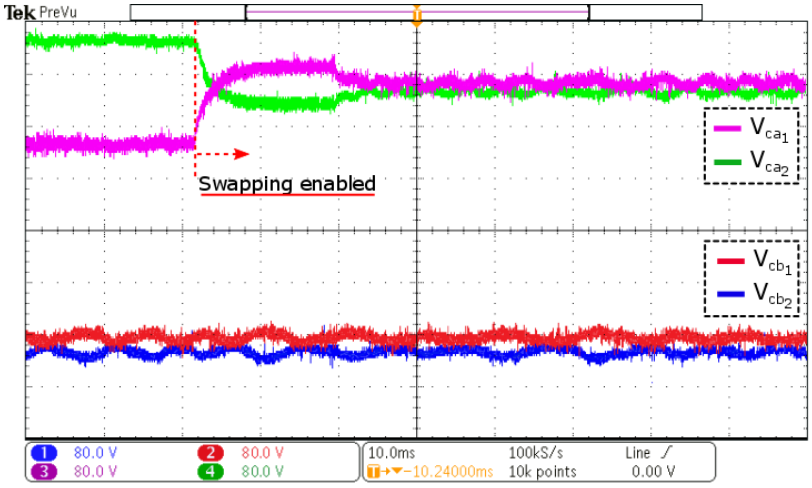

Figure 24. Experimental waveform of the balanced DC-link capacitor voltage tracing channels 1, 2, 3, 4 (80 V/div).

Figure 25 shows the experimental results of the converter phase voltage and current with variations in the power transfer (when the amplitude of the reference current was changed to a 100% converter rating). Table 5 presents the simulated and experimental current total harmonic distortion (THD) at various power ratings.

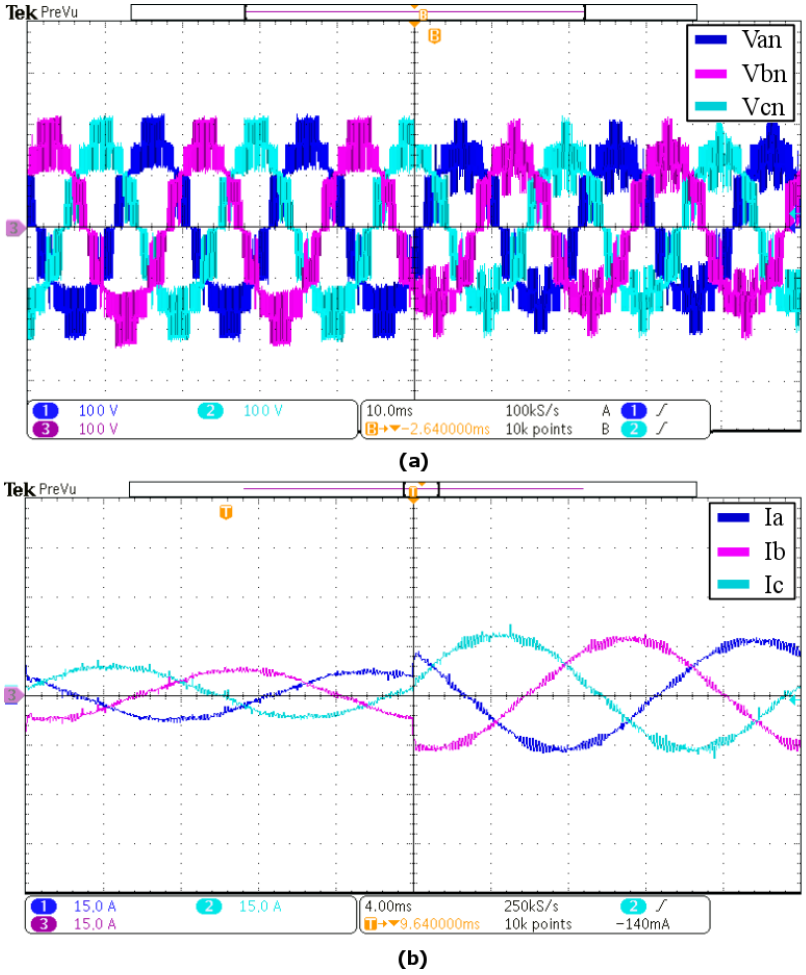

Figure 25. Variations in power transfer. (**a**) Experimental waveform of phase voltages tracing channels 1, 2, 3 (100 V/div). (**b**) Experimental validation of converter current tracing channels 1, 2, 3 (15A/div).

Table 5. Converter current THD.

Current THD	Power Rating		
Simulation	25%	50%	100%
	5.31	2.83	1.38
Experimental	7.2	5.33	4.21

The proposed converter was compared with similar works in [44,45] in terms of the output voltage levels, required number of components, and THD percentage of harmonic content. The comparison is provided in Table 6.

Table 6. Comparative analysis of converter topologies.

Converter System	Parameters					
	V-Level	Switch	Diode	DC Source	Capacitor	Current THD
AHMMC	9	8	0	1	2	4.21%
MLI [44]	8	6	4	2	6	1.25%
MLI [45]	19	12	1	2	2	4.30%

It is evident from Table 6 that the performance of the proposed AHMMC is better than that in [45] in terms of the THD and those in [44,45] in terms of the component count.

7. Conclusions

A new topology for a three-phase AHMMC for a medium-voltage high-power front-end converter is proposed, which is a per-phase series arrangement of a high-voltage three-phase half-bridge converter with a low-voltage cascaded converter module. The proposed modular control scheme, which is a combination of control techniques, i.e., SV-PWM, POD-PWM, inter-module energy balancing through zero-sequence voltage, and active swapping, is employed to decrease the voltage stress on the converter, keep the DC-link voltage balanced, and track the current to its reference value. Furthermore, the active switches' categorization of the proposed topology is performed according to the voltage stress: (i) high-voltage low-frequency switching, and (ii) low-voltage high-frequency switching. The features of the AHMMC topology include the minimization of the harmonic contents injected into the AC mains, a wider modulation range for the unity power factor, reduced conduction and switching losses, low DC-link capacitor voltage requirements for harmonic compensation, and the elimination of a bulky transformer. The detailed topology design and effectiveness of the modular control scheme are thoroughly examined. The efficiency and usefulness of the proposed topology are verified through simulation results, and experimental results via a customized laboratory prototype based on control and power boards are presented to validate the system in practice.

Author Contributions: Conceptualization, M.A. and M.M.K.; methodology, A.F.; software, M.A. and M.M.K.; validation, M.A. and M.Q.K.; formal analysis, M.A. and M.Q.K.; investigation, A.F.; resources, M.M.K.; data curation, M.A.; writing–original draft preparation, M.A.; writing–review and editing, M.A. and A.F.; visualization, A.F. and M.Q.K.; supervision, M.M.K. and L.M.-P.; writing–review and editing, project administration, funding acquisition, M.M.K. and L.M.-P. All authors have read and agreed to the published version of the manuscript.

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References

1. Singh, B.; Singh, B.N.; Chandra, A.; Al-Haddad, K.; Pandey, A.; Kothari, D.P. A review of single-phase improved power quality AC-DC converters. *IEEE Trans. Ind. Electron.* **2003**, *50*, 962–981. [CrossRef]
2. Khazraei, M.; Sepahvand, H.; Corzine, K.A.; Ferdowsi, M. Active Capacitor Voltage Balancing in Single-Phase Flying-Capacitor Multilevel Power Converters. *IEEE Trans. Ind. Electron.* **2012**, *59*, 769–778. [CrossRef]
3. He, L.; Cheng, C. A Flying-Capacitor-Clamped Five-Level Inverter Based on Bridge Modular Switched-Capacitor Topology. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7814–7822. [CrossRef]
4. Lee, J.; Kwak, R.; Lee, K. Novel Discontinuous PWM Method for a Single-Phase Three-Level Neutral Point Clamped Inverter with Efficiency Improvement and Harmonic Reduction. *IEEE Trans. Power Electron.* **2018**, *33*, 9253–9266. [CrossRef]
5. Dekka, A.; Fuentes, R.L.; Narimani, M.; Wu, B. Voltage Balancing of a Modular Neutral-Point-Clamped Converter with a Carrier-Based Modulation Scheme. *IEEE Trans. Power Electron.* **2018**, *33*, 8208–8212. [CrossRef]
6. Sepahvand, H.; Liao, J.; Ferdowsi, M.; Corzine, K.A. Capacitor Voltage Regulation in Single-DC-Source Cascaded H-Bridge Multilevel Converters Using Phase-Shift Modulation. *IEEE Trans. Ind. Electron.* **2013**, *60*, 3619–3626. [CrossRef]
7. Zhang, Y.; Wu, X.; Yuan, X. A Simplified Branch and Bound Approach for Model Predictive Control of Multilevel Cascaded H-Bridge STATCOM. *IEEE Trans. Ind. Electron.* **2017**, *64*, 7634–7644. [CrossRef]
8. Ali, M.; Khan, M.M.; Yi, Z.; Yang, Y.J.; Tang, H. 7-Level asymmetrical hybrid cascaded multilevel converter topology for traction system. In Proceedings of the 2017 International Conference on Electrical Engineering (ICEE), 2017; pp. 1–6. [CrossRef]
9. Veenstra, M.; Rufer, A. Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives. *IEEE Trans. Ind. Appl.* **2005**, *41*, 655–664. [CrossRef]
10. Konstantinou, G.S.; Pulikanti, S.R.; Agelidis, V.G. Harmonic elimination control of a five-level DC-AC cascaded H-bridge hybrid inverter. In Proceedings of the 2nd International Symposium on Power Electronics for Distributed Generation Systems, Hefei, China, 16–18 June 2010; pp. 352–357. [CrossRef]
11. Pulikanti, S.R.; Konstantinou, G.S.; Agelidis, V.G. Generalisation of flying capacitor-based active-neutralpoint- clamped multilevel converter using voltage-level modulation. *IET Power Electron.* **2012**, *5*, 456–466. [CrossRef]
12. Jung, J.; Cui, S.; Lee, J.; Sul, S. A New Topology of Multilevel VSC Converter for a Hybrid HVDC Transmission System. *IEEE Trans. Power Electron.* **2017**, *32*, 4199–4209. [CrossRef]
13. Pulikanti, S.R.; Agelidis, V.G. Hybrid Flying-Capacitor-Based Active-Neutral-Point-Clamped Five-Level Converter Operated with SHE-PWM. *IEEE Trans. Ind. Electron.* **2011**, *58*, 4643–4653. [CrossRef]
14. Karwatzki, D.; Mertens, A. Generalized Control Approach for a Class of Modular Multilevel Converter Topologies. *IEEE Trans. Power Electron.* **2018**, *33*, 2888–2900. [CrossRef]
15. Li, P.; Adam, G.P.; Holliday, D.; Williams, B. Controlled Transition Full-Bridge Hybrid Multilevel Converter with Chain-Links of Full-Bridge Cells. *IEEE Trans. Power Electron.* **2017**, *32*, 23–38. [CrossRef]
16. Perez, M.A.; Bernet, S.; Rodriguez, J.; Kouro, S.; Lizana, R. Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters. *IEEE Trans. Power Electron.* **2015**, *30*, 4–17. [CrossRef]
17. Kolb, J.; Kammerer, F.; Gommeringer, M.; Braun, M. Cascaded Control System of the Modular Multilevel Converter for Feeding Variable-Speed Drives. *IEEE Trans. Power Electron.* **2015**, *30*, 349–357. [CrossRef]
18. Saeedifard, M.; Iravani, R. Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System. *IEEE Trans. Power Deliv.* **2010**, *25*, 2903–2912. [CrossRef]
19. Flourentzou, N.; Agelidis, V.G.; Demetriades, G.D. VSC-Based HVDC Power Transmission Systems: An Overview. *IEEE Trans. Power Electron.* **2009**, *24*, 592–602. [CrossRef]
20. Hagiwara, M.; Nishimura, K.; Akagi, H. A Medium-Voltage Motor Drive with a Modular Multilevel PWM Inverter. *IEEE Trans. Power Electron.* **2010**, *25*, 1786–1799. [CrossRef]
21. Korn, A.J.; Winkelnkemper, M.; Steimer, P. Low output frequency operation of the Modular Multi-Level Converter. 2010 IEEE Energy Conversion Congress and Exposition, Atlanta, GA, USA, 12–16 September 2010; pp. 3993–3997. [CrossRef]
22. Wiechmann, E.P.; Burgos, R.P.; Holtz, J. Active front-end converter for medium-voltage current-source drives using sequential-sampling synchronous space-vector modulation. *IEEE Trans. Ind. Electron.* **2003**, *50*, 1275–1289. [CrossRef]
23. Song, Z.; Tian, Y.; Chen, W.; Zou, Z.; Chen, Z. Predictive Duty Cycle Control of Three-Phase Active-Front-End Rectifiers. *IEEE Trans. Power Electron.* **2016**, *31*, 698–710. [CrossRef]
24. Prakash, P.S.; Kalpana, R.; Singh, B.; Bhuvaneswari, G. Power Quality Improvement in Utility Interactive Based AC–DC Converter Using Harmonic Current Injection Technique. *IEEE Trans. Ind. Appl.* **2018**, *54*, 5355–5366. [CrossRef]
25. Malinowski, M.; Gopakumar, K.; Rodriguez, J.; Perez, M.A. A Survey on Cascaded Multilevel Inverters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2197–2206. [CrossRef]
26. Dowruang, S.; Theeranan, J.; Bumrungsri, P.; Jeraputra, C. Optimal voltage vector sequences on model predictive control for a grid connected three-phase voltage source inverter. In Proceedings of the 2016 13th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), Chiang Mai, Thailand, 28 June–1 July 2016; pp. 1–5. [CrossRef]
27. Odeh, C.I. Enhanced three-phase multilevel inverter configuration. *IET Power Electron.* **2013**, *6*, 1122–1131. [CrossRef]
28. Chaturvedi, P.K.; Jain, S.; Agarwal, P. Reduced switching loss pulse width modulation technique for three-level diode clamped inverter. *IET Power Electron.* **2011**, *4*, 393–399. [CrossRef]

29. Banaei, M.R.; Kazemi, F.M.; Oskuee, M.R.J. New mixture of hybrid stacked multicell with half-cascaded converter to increase voltage levels. *IET Power Electron.* **2013**, *6*, 1406–1414. [CrossRef]
30. Sirisha, B.; Kumar, P.S. A simplified space vector PWM for cascaded H-Bridge inverter including over modulation operation. In Proceedings of the 2016 IEEE Annual India Conference (INDICON), Bangalore, India, 16–18 December 2016; pp. 1–6. [CrossRef]
31. Mehrizi-Sani, A.; Filizadeh, S. An Optimized Space Vector Modulation Sequence for Improved Harmonic Performance. *IEEE Trans. Ind. Electron.* **2009**, *56*, 2894–2903. [CrossRef]
32. López, .; Álvarez, J.; Freijedo, F.D.; Yepes, A.G.; Malvar, J.; Fernández-Comesaña, P.; Doval-Gandoy, J.; Nogueiras, A.; Lago, A.; Peñalver, C.M. Multilevel multiphase space vector PWM algorithm with switching state redundancy applied to three-phase four-leg converters. In Proceedings of the IECON 2010—36th Annual Conference on IEEE Industrial Electronics Society, Glendale, AZ, USA, 7–10 November 2010; pp. 568–575. [CrossRef]
33. Jacob, B.; Baiju, M.R. Vector-Quantized Space-Vector-Based Spread Spectrum Modulation Scheme for Multilevel Inverters Using the Principle of Oversampling ADC. *IEEE Trans. Ind. Electron.* **2013**, *60*, 2969–2977. [CrossRef]
34. Gu, L.; Jin, K. A Three-Phase Isolated Bidirectional AC/DC Converter and its Modified SVPWM Algorithm. *IEEE Trans. Power Electron.* **2015**, *30*, 5458–5468. [CrossRef]
35. Das, S.; Narayanan, G. Novel Switching Sequences for a Space-Vector-Modulated Three-Level Inverter. *IEEE Trans. Ind. Electron.* **2012**, *59*, 1477–1487. [CrossRef]
36. Flourentzou, N.; Agelidis, V.G. Harmonic performance of multiple sets of solutions of SHE-PWM for a 2-level VSC topology with fluctuating DC-link voltage. In Proceedings of the 2007 Australasian Universities Power Engineering Conference, Perth, WA, Australia, 9–12 December 2007; pp. 1–8. [CrossRef]
37. Salinas, F.; Gonzalez, M.A.; Escalante, M.F. Voltage balancing scheme for flying capacitor multilevel converters. *IET Power Electron.* **2013**, *6*, 835–842. [CrossRef]
38. Pulikanti, S.R.; Agelidis, V.G. Control of neutral point and flying capacitor voltages in five-level SHE-PWM controlled ANPC converter. In Proceedings of the 2009 4th IEEE Conference on Industrial Electronics and Applications, Xi'an, China, 25–27 May 2009; pp. 172–177. [CrossRef]
39. Betz, R.E.; Summers, T.J. Using a cascaded H-bridge STATCOM for rebalancing unbalanced voltages. In Proceedings of the 2007 7th International Conference on Power Electronics, Daegu, Republic of Korea, 22–26 October 2007; pp. 1219–1224. [CrossRef]
40. Akagi, H.; Inoue, S.; Yoshii, T. Control and Performance of a Transformerless Cascade PWM STATCOM with Star Configuration. *IEEE Trans. Ind. Appl.* **2007**, *43*, 1041–1049. [CrossRef]
41. Hatano, N.; Ise, T. A configuration and control method of cascade H-bridge STATCOM. In Proceedings of the 2008 IEEE Power and Energy Society General Meeting—Conversion and Delivery of Electrical Energy in the 21st Century, Pittsburgh, PA, USA, 20–24 July 2008; pp. 1–8. [CrossRef]
42. Kesler, M.; Kisacikoglu, M.C.; Tolbert, L.M. Vehicle-to-Grid Reactive Power Operation Using Plug-In Electric Vehicle Bidirectional Offboard Charger. *IEEE Trans. Ind. Electron.* **2014**, *61*, 6778–6784. [CrossRef]
43. Debnath, S.; Qin, J.; Bahrani, B.; Saeedifard, M.; Barbosa, P. Operation, Control, and Applications of the Modular Multilevel Converter: A Review. *IEEE Trans. Power Electron.* **2015**, *30*, 37–53. [CrossRef]
44. Khoun Jahan, H.; Eskandari, R.; Rahimi, T.; Shalchi Alishah, R.; Ding, L.; Bertilsson, K.; Sabahi, M.; Blaabjerg, F. A Limited Common-Mode Current Switched-Capacitor Multilevel Inverter Topology and Its Performance and Lifetime Evaluation in Grid-Connected Photovoltaic Applications. *Energies* **2021**, *14*, 1915. [CrossRef]
45. Fahad, M.; Tariq, M.; Faizan, M.; Ali, A.; Sarwar, A.; Dehghani Tafti, H.; Ahmad, S.; Shah Noor Mohamed, A. A Dual Source Switched-Capacitor Multilevel Inverter with Reduced Device Count. *Electronics* **2022**, *11*, 67. [CrossRef]