*energies*

MDPI

*Article*

# A High Frequency Multiphase Modular Hybrid Transformerless DC/DC Converter for High-Voltage-Gain High-Current Applications

**Hu Xiong [1], Jiayuan Li [1], Bin Xiang [1], Xiaoguang Jiang [1] and Yuan Mao [2,*]**

[1] State Grid Hubei Electric Power Research Institute, No.227 Xudong Avenue, Wuhan 430077, China
[2] College of Information Engineering, The Zhejiang University of Technology, Hangzhou 310023, China
* Correspondence: maoyuan@zjut.edu.cn; Tel.: +86-17133387919

**Abstract:** In order to meet the demands of desirable efficiency, transformerless DC/DC equipment with great voltage step-down are inevitable needed. This research offers a unique type of high-frequency, high-voltage-gain DC/DC converter, which comprises a switched capacitor (SC) converter and a buck converter. Thanks to the transformation of a two-stage converter to a single-stage converter, it has a considerable ratio of step-down voltage transformation and a reasonable duty cycle. In addition, it can permit low voltage stress on the switches. The simple control method and easy driving circuit implementation makes it scalable for high-power-level devices. Low cost can be realized as fewer components are needed. Under all operational circumstances, total soft-charging and low equipment voltage stresses are accomplished. Compared to those classic high-voltage-gain converters, the proposed converter exhibits merits of higher efficiency, higher flexibility, lower ripples, and lower costs. A comprehensive analysis is carried out for the converter's steady-state operations. With a 1 MHz switching frequency, a 900 W prototype of a 20-time converter is constructed, with a peak efficiency of 92.5%. Simulations and experiments verify the effectiveness of the theoretical investigation of the converter's operation.

**Keywords:** high-frequency hybrid converter; DC microgrids; high efficiency; low-voltage-stress; high-voltage conversion ratio; cost-effective



**Citation:** Xiong, H.; Li, J.; Xiang, B.; Jiang, X.; Mao, Y. A High Frequency Multiphase Modular Hybrid Transformerless DC/DC Converter for High-Voltage-Gain High-Current Applications. *Energies* **2023**, *16*, 2518. https://doi.org/10.3390/en16062518

Academic Editor: Salvatore Musumeci

Received: 20 January 2023
Revised: 25 February 2023
Accepted: 2 March 2023
Published: 7 March 2023



## 1. Introduction

In an inter-grid scenario with a lot of distributed generation (DG), the traditional power grid architecture, which is made up of numbers of power stations, transmission, and distribution networks, will be displaced by a number of microgrids [1]. For instance, DC microgrids are well used in car, airplane, data center, and boat systems [1–7]. In many applications, a DC bus is used to distribute power so that lighting systems, motor drives, and devices that store energy can work together. A high-gain converter is needed to ensure that the DC voltage buses feed low-voltage loads, such as those in records centers, in a way that is both efficient and good for the power quality.

Step-down conversion is often carried out using DC/DC buck converters since they have fewer active switches and passive components. However, for high-duty cycle operation, the energy efficiency of the converter decreases substantially. Traditional buck DC/DC converters have a limited voltage gain as they lose a lot of power when the voltage goes very high [4,5]. They are not good for applications that need a lot of voltage gain. To get a huge voltage gain, a two-stage converter consisting of two cascaded buck converters has been suggested [8]. To stop the beat-frequency effect, a set of controllers that work together would have to be used to control the active switches. The controller's design would become more challenging as a result [8]. Additionally, if the input voltage and load value vary, instability is quite probable [9].

The switched capacitor (SC) converter belongs to a non-isolated DC/DC converter that may boost voltage while preserving efficiency [10–18]. SC converters without magnetic components would be tiny and powerful. Dickson, Fibonacci (FIB), series–parallel, and other high-voltage-gain SC converters have been studied previously [19–27]. Generally, the SC converter cannot achieve both high efficiency and sufficient line and load regulation [28–31]. Efficiency will suffer greatly if precision control is sought [28–30]. A two-stage DC/DC converter may improve control and voltage gain. The standard buck converter is utilized in the second stage, owing to regulatory considerations and the necessity for high-voltage-gain with few components. Additionally, multi-phase buck converters may provide a significant current capacity for high-power applications. The regulation issue is often solved and voltage gain is increased by using two-stage DC/DC conversion [32]. Figure 1 depicts the system diagram for this two-stage converter topology. A multiphase buck converter with regulation makes up the second stage, whereas the first stage is made up of an uncontrolled SC converter. Most of the high-voltage-gain is produced by the first-stage converter, while precise control is produced by the second stage. The design has two downsides, despite its advantages: (a) the two-stage design has a larger bill of materials (BOM) cost since it has more circuit components; and (b) the efficiency may drastically decrease with two switching stages and large switching losses by the relative components.

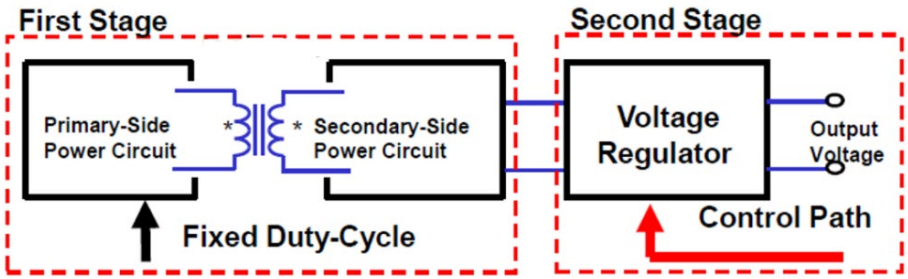



**Figure 1.** Conventional two-stage DC/DC converter with high-voltage-gain.

For high-voltage and high-current devices, a hybrid transformerless DC/DC converter with great efficiency is discussed in this article. With substantially less switches as well as y control. It has a reasonable duty cycle, and low cost because it combines a two-stage into one stage, which minimizes the number of components needed. To reduce current ripple, the recommended converter employs interleaving control. The principle of the suggested converter is validated, and the improved performance is shown in both simulations and experiments. Fair comparisons among the proposed converter and other popular single-stage converters are given in Table 1. Here, the star symbols (i.e., "*") indicate the polarities of the transformer. It is exhibited that even with a larger voltage gain, the suggested circuit can implement a higher efficiency.

**Table 1.** Comparisons among different single-stage converters.

| The Converter Topology in | Voltage Gain (Times) | Output Power (W) | Switching Frequency (kHz) | Peak Efficiency (%) |
|---|---|---|---|---|
| [33] | 15 | 2000 | 100 | 90 |
| [34] | 15 | 2000 | 100 | 92 |
| [35] | 16.6 | 100 | 100 | 90 |
| [36] | 16.6 | 300 | 100 | 92.5 |
| Proposed | 20 | 900 | 100 | 92.5 |

## 2. Operation Principle and Configuration for the Designed DC/DC Converter

This section describes the suggested DC/DC SC-buck converter's system architecture and modular design. The suggested converter's operating theory is then described.

### *2.1. System Topology and Modular Scheme*

The suggested SC-buck converter is depicted in Figure 2. On the basis of the aforementioned theories, some assumptions are completed first.

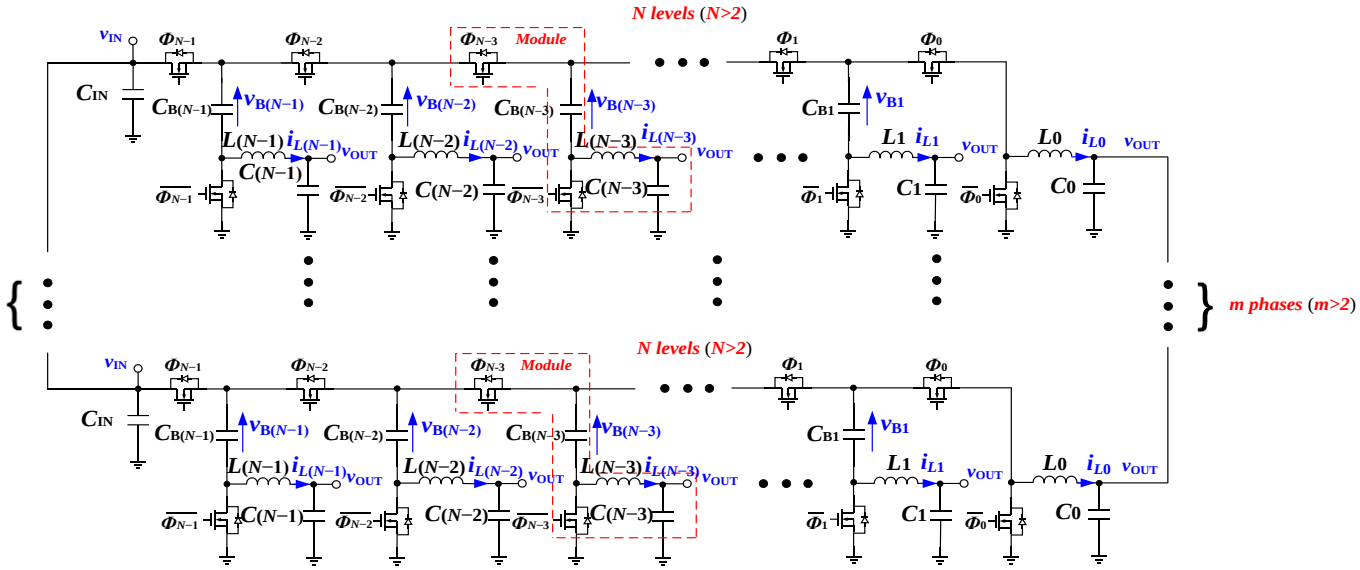



**Figure 2.** Configuration of the suggested converter at the system level.

a. Each switching component in the recommended converter is perfect.
b. Voltage variation between the capacitors is ignored; therefore, all capacitors have ideal values to maintain virtually constant holding voltages throughout operation. As a result, the capacitors are assumed as ideal voltage sources.
c. The dead-time between activating one switch and deactivating a complimentary switch is minimal compared to the conduction time of each switch, and may therefore be ignored. The dead-time is excluded from the examination of circuit structure in order to make it simpler.
d. Every switch within the modules has equal switching frequency while the suggested converter is working in steady-state.

The suggested $M$-phase converter contains $N$ programmable modules of SC-buck circuits in each of its phases. With the exception of the first module, which is devoid of a flying capacitor, $C_{B0}$, each phase is made up of two complementary MOSFETs, a flying MOSFET $\Phi_i$ ($i = 0, 1, 2, \ldots, -1$) and a bottom MOSFET $\overline{\Phi_i}$ ($i = 0, 1, 2, \ldots, N-1$), a flying capacitor $C_{B(i)}$ ($i = 1, 2, \ldots, N-1$), and an input capacitor $C_i$ ($i = 0, 1, 2, \ldots, N-1$). The design of each module in the proposed converter's switched-capacitor-buck circuit is shown in Figure 3.

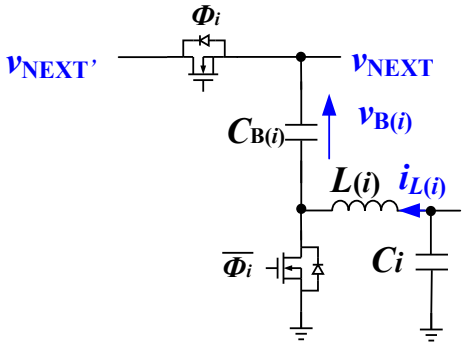


**Figure 3.** Configuration of the SC-circuit model.

The proposed converter's input and output voltages are represented by $v_{\mathrm{IN}}$ and $v_{\mathrm{OUT}}$, respectively; the inductor currents on $L_i$ ($i = 0, 1, 2, \ldots, N-1$) and the voltages acros $C_{\mathrm{B}(i)}$ ($i = 1, 2, \ldots, N-1$) are represented by $i_{Li}$ ($i = 0, 1, 2, \ldots, N-1$) and $v_{\mathrm{B}(i)}$ ($i = 1, 2, \ldots, N-1$). Additionally, $\overline{d_i}$ ($i = 0, 1, 2, \ldots, N-1$) is used to denote the duty ratios of the MOSFETs. The bottom MOSFETs' complementary duty ratios $d_i$ ($i = 0, 1, 2, \ldots, N-1$) are shown as $\Phi_i$ ($i = 0, 1, 2, \ldots, N-1$). Evidently, $d_i + \overline{d_i} = 1$.

The steady-state functioning of $L_i$ ($i = 0, 1, 2, \ldots, N-1$) is given by the following expressions to achieve voltage-second balance.

$$\begin{cases} V_{\mathrm{OUT}} = \left[V_{\mathrm{B}(i+1)} - V_{\mathrm{B}(i)}\right] \\ V_{\mathrm{B}(N)} = V_{\mathrm{IN}} \\ V_{\mathrm{B0}} = 0 \end{cases} (i = 0, 1, 2, \ldots, N-1) \tag{1}$$

On the basis of (1), the voltage gain $M$ can be obtained as

$$M = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} (i = 1, 2, 3, \ldots, N) \tag{2}$$

To achieve charge equilibrium across all $C_{\mathrm{B}(i)}$, the following expression is derived:

$$I_{L0}D_0 = I_{L1}D_1 = I_{L2}D_2 = I_{L(N-1)}\, D_{N-1} \tag{3}$$

According to (3), each inductor's steady-state current will be the same because the flying MOSFET's duty ratios are equal.

The benefits that the modular design can reduce the intricacy of the power converter system and provide uniform thermal distribution are realized in the majority of applications by spreading the inductor currents evenly. It is desirable for the converter to maintain a constant temperature throughout with no hot areas. This means that all devices will experience the same power stress distribution. It allows the converter to provide the most power at the required temperature.

Consequently, the duty ratios, $D_i$, of each flying MOSFET are all adjusted to the same value.

$$D_0 = D_1 = D_2 = \ldots = D_{N-1} = D \tag{4}$$

where $D$ stands for the flying MOSFETs' consistent duty ratio to ensure equitable current sharing.

Substitute (4) into (1) and (2),

$$M = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{D}{N} (i = 1, 2, 3, \ldots, N) \tag{5}$$

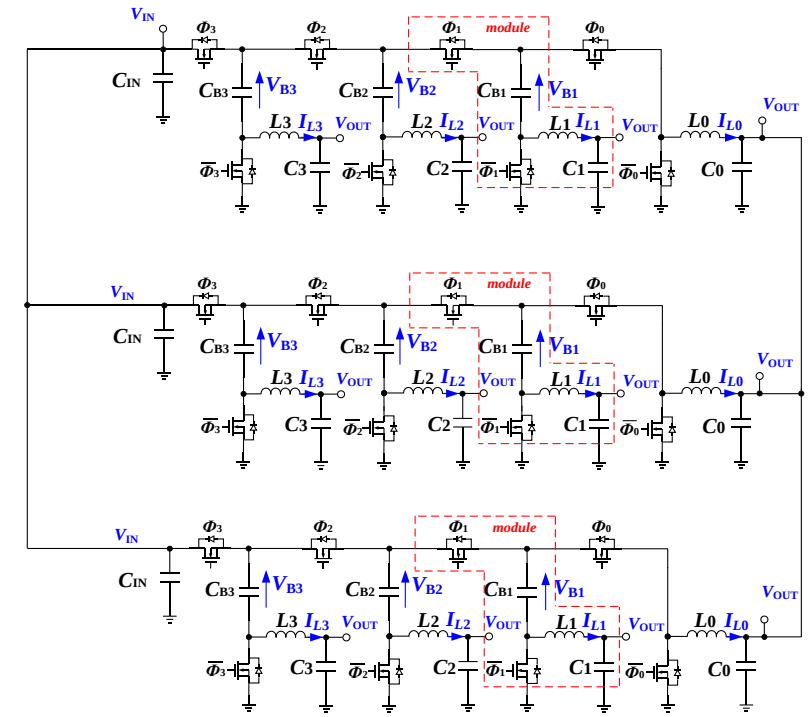
The $M$ in (5) is equivalent to that of an $N$-phase buck converter with a $N$:1 ratio SC converter that is duty-cycle-regulated. It should be noted that the duty ratios are designed for the proposed circuit operating at the continuous current mode (CCM).

### *2.2. Operating Principle*

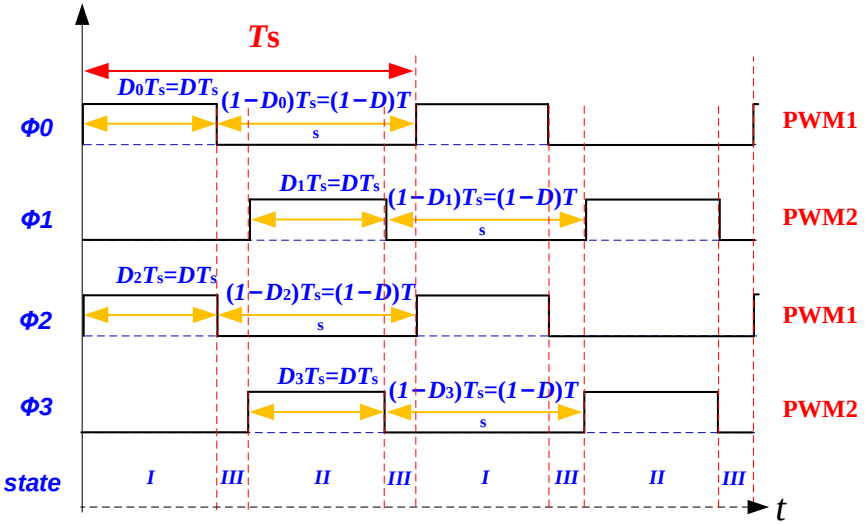
The duty cycle should be near to 1/2 for optimal efficiency in typical buck converters [4]. Based on the design procedure in [33], both the maximum and lowest duty cycles must be constrained to optimize the converter in terms of efficiency, cost, and size. Consequently, the value of $N$ can be obtained from (5). In this research, a three-phase converter with four modules in each phase is used to show the working concept.

Figure 4a depicts the converter in steady-state operation with three phases and four modules working in each phase. The flying MOSFET 0 and 2 are controlled by signal PWM-1, while MOSFET 3 and MOSFET 4 are controlled by PWM-2 that is in reverse phase with PWM-1. The converter's matching timing diagram is depicted in Figure 4b. In Figure 4a, the converter is shown operating in three phases, with four modules operating in each

phase as it would in a typical situation. Signal PWM-1 is in charge of controlling the flying MOSFETs 0 and 2. Signals in PWM-2 that are out of phase with PWM-1 are used to control components 3 and 4. Figure 4 displays the suggested converter's timing diagram, b.




(**a**)




(**b**)

**Figure 4.** (**a**) Schematic diagram of the suggested converter; and (**b**) the corresponding timing schematic.

The switches controlled through PWM-1 will "ON", whereas the switches controlled through PWM-2 will "OFF" in state I. Consequently, the switches controlled through the complement of PWM-1 will "OFF" and the switches controlled through the complement of PWM-2 will "ON". According to Figure 5a, $V_{IN}$ charges the $C_{OUT}$ and the $C_{B2}$ through $L_1$ and $L_3$, respectively. For $C_{B2}$ and $C_{OUT}$, respectively, $C_{B1}$ and $C_{B3}$ are simultaneously

discharged. Meanwhile, $V_{IN}$ charges $L_0$ and $L_2$, storing energy in $L_0$ and $L_2$. The voltage on $C_{OUT}$ powers the load.

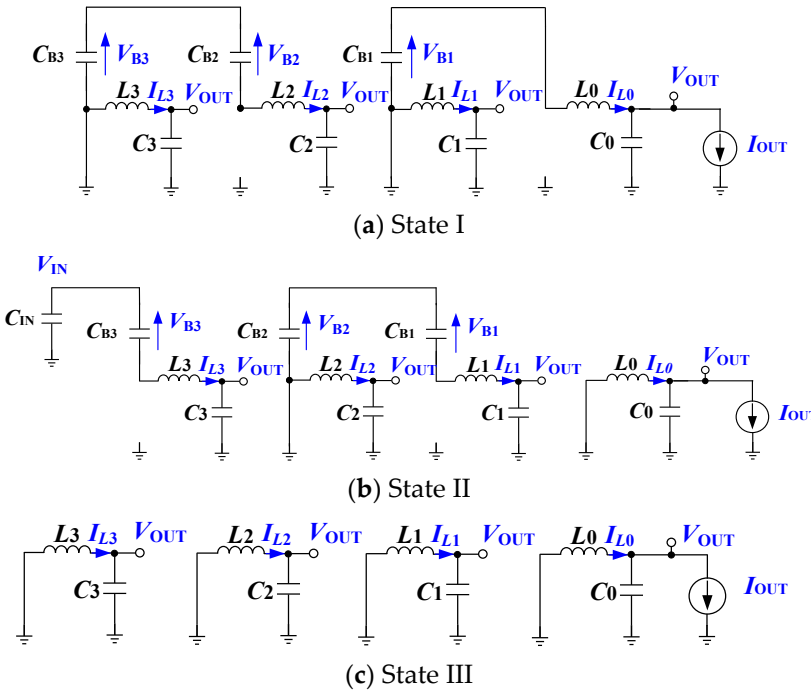



**Figure 5.** Equivalent circuit diagrams for the three distinct operational states for each phase.

Every switch controlled through PWM-1 will "OFF" and every switch controlled through PWM-2 will "ON" in state II. Consequently, the switches operated by PWM-1's complement will "ON," while the switches operated by PWM-2's complement will "OFF." According to Figure 5b, $C_{B1}$ and $C_{B3}$ are charged by the $V_{IN}$ via $L_0$ and $L_2$. The load and $C_{B3}$ are being concurrently discharged by $C_{OUT}$ and $C_{B2}$, respectively. While this is happening, $V_{IN}$ charges $L_1$ and $L_3$ and stores energy in them.

All switches under PWM-1 control will "OFF", while the switches under PWM-2 control will "OFF" in state III. The switches that are controlled by PWM-1 and PWM-2's complementary are therefore "ON". The flying capacitors do not charge or discharge, since all of the flying MOSFETs are deactivated. $V_{IN}$ charges and stores energy in inductors $L_0$–$L_3$. The simultaneous supply of the load by the voltage on $C_{OUT}$ is shown in Figure 5c.

The following equations are deduced based on (4) and the assumption that all flying MOSFETs' duty ratios $D_i$ ($i = 1,\ 2,\ 3$) are set to be the same to $D$ in order to realize an equitable current sharing condition across $L_0$–$L_3$.

$$\begin{cases} V_{B1}D = V_{OUT} \\ (V_{B2} - V_{B1})D = V_{OUT} \\ (V_{B3} - V_{B2})D = V_{OUT} \\ (V_{IN} - V_{B3})D = V_{OUT} \end{cases} \tag{6}$$

Therefore, (6) can be rewritten as

$$\begin{cases} V_{OUT} = \frac{D}{4}V_{IN} \\ V_{B1} = \frac{1}{4}V_{IN} \\ V_{B2} = \frac{2}{4}V_{IN} \\ V_{B3} = \frac{3}{4}V_{IN} \end{cases} \tag{7}$$

Based on (7), $C_{B(i)}$ ($i = 1, 2, 3$) throughout this converter owns an offset voltage $V_{B(i)}$ ($i = 1, 2, 3$) that resembles that of conventional converters.

According to (7), the steady-state voltage gain $M$ with $N = 4$ is obtained as

$$M = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{D}{4} \tag{8}$$

which matches (2) when $N$ equals to 4.

In line with the operating principle illustrated above, each flying capacitor is continually softly charged/discharged, efficiently mitigating the loss made by the flying capacitors' voltage ripple owning to the converter's hybrid architecture, which interconnects the buck inductor with the SC stage. In conventional SC-based converters, this crucial function will prevent the inrush current. This eliminates the charge-sharing losses that normally occur during charging. Because of this, the hybrid converter proposed here will always be gently charged, no matter the tolerance of the flying capacitors.

### *2.3. Interleaving Procedure*

With the right gate driving signal control, 360/4 interleaving between each module of the suggested converter might be put into practice. The timing diagram of the gate signals of $\Phi_i$ ($i = 0,\ 1\ ,2\ ,3$) is shown in Figure 6. This circuit combines a four-module switching capacitor converter with a standard four-phase interleaved buck converter. This may lead to the cancellation of four-phase current ripple and a significant decrease in current ripple. As a result, the current stress on the capacitors may be mitigated, and it would be possible to avoid using the enormous capacitor bank that is often needed to buffer the substantial current ripple. The corresponding current and voltage stresses for the switches are provided in Table 2.

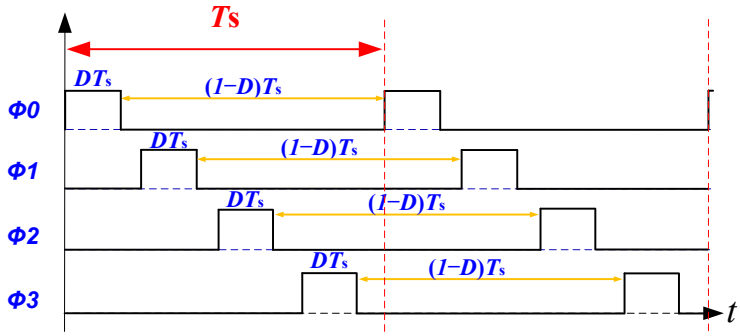



**Figure 6.** Timing schematic of the gate signals for the MOSFET $\Phi_{\mathrm{i}}$ ($i = 0,\ 1\ ,2,\ \ldots, N-1$) with flawless interleaving operation under four modules in each phase for the suggested converter.

**Table 2.** Voltage and current stresses of the switches.

| Power Switches | Voltage Stress | Current Stresss |
|---|---|---|
| $\Phi_{N-1}$ | $(V_{\mathrm{OUT}}/N)$ | Peak of $I_{L(N-1)}$ |
| $\Phi_i$ ($i = 0, 1, \ldots, N-2$) | $2(V_{\mathrm{OUT}}/N)$ | Peak of $I_{Li}$ ($i = 0, 1, \ldots, N-2$) |
| $\overline{\Phi_i}$ ($i = 0, 1, \ldots, N-1$) | $(V_{\mathrm{OUT}}/N)$ | Peak of $I_{Li}$ ($i = 0, 1, \ldots, N-1$) |

### *2.4. Circuit Design and Optimization*

Switching frequency, the number of modules in the converter, maximum output current, input voltage, and output voltage are the key parameters that need to be specially designed for optimizing the layout of the circuit.

The inductance of the inductor for each module can be calculated using

$$L = \frac{V_{\mathrm{IN}} \cdot (1 - D)}{\Delta I_L \cdot f_s} \tag{9}$$

where the inductor current ripple is $\Delta I_L = \alpha \cdot I_{O_{MAX}}$ and $\alpha$ is typically 0.2 or 0.3.

The capacitance of the flying capacitor for each module is derived using

$$C = \frac{I_{O_{MAX}} \cdot D}{\Delta V_C \cdot N \cdot f_s} \tag{10}$$

where $\Delta V_C$ is the voltage ripple across the flying capacitors. The capacitances are determined by the switching frequency, load current, duty cycles of the flying active switches, number of modules, and desired voltage ripples. The voltage ripples are required to be controlled at the lowest level for high efficiency.

For the power switches, the maximum voltages are obtained through a scaling function of $N$. All switches' current rating are obtained by the peak value of their inductor currents.

## 3. Simulation and Experimental Verifications

First, simulation was finished to confirm the facticity of the suggested converter in interleaved operation. Table 3 displays the simulated parameters. The proposed converter is regulated in the reverse mode. The input voltage of the prototype is 2.4 V, while the output voltage is 48 V, which is a typical DC bus voltage for low-voltage DC microgrids. Figure 7a represents the full-load current waveforms of $L_1$–$L_4$. The voltage waveforms of the capacitors $C_{B1}$–$C_{B3}$ are shown in Figure 7b. The average voltages on $C_{B1}$–$C_{B3}$ are 12 V, 24 V, and 36 V, respectively, with an output voltage of 48 V, as anticipated in (7). Figure 7c shows the input current and output voltage at full load. The voltage across FET $\Phi_1$ and $\overline{\Phi_1}$ is also processed, as shown in Figure 7d. Based on Table 3, the highest voltage stress for FET $\Phi_i$ ($i$ = 0, 1, 2) is 24 V. The highest voltage stress for FET $\overline{\Phi_i}$ ($i$ = 0, 1, 2, 3) and $\Phi_3$ is 12 V.

**Table 3.** Main parameters of the simulation as well as hardware.

| Depiction | Symbols | Values |
|---|---|---|
| Inductor | $L_0$–$L_3$ | 0.2 µH |
| Flying Capacitor | $C_{B1}$–$C_{B3}$ | 47 µF |
| Resistor Load | $R_{OUT}$ | 6.95 mOhm |
| Output Voltage | $V_{OUT}$ | 2.4 V |
| Output Power | $P_{OUT}$ | 900 W |
| Input Voltage | $V_{IN}$ | 48 V |

A prototype of the suggested hybrid DC/DC converter was built with $M$ = 3, meaning three phases were active, and $N$ = 4, meaning four modules were activated in each phase (see Figure 8). The hardware prototype consists of three stages. The power rating of each phase equals to 300 W, and $V_{OUT}$ equals to 2.4 V; thus, the output current of each phase equals to 125 A. Each step of the prototype model consists of four parts. With an output voltage of 2.4 V, each module's flying capacitors and power inductor will carry around 31 A of current, while each module's power inductor will carry about 31 A of current. Three different types of components are used: (a) power MOSFETs, (b) inductors, and (c) capacitors. Three PCB boards, such as a DSP control board, a power stage board, and a signal processing board, are used in each step of the setup. The power stage board also comprises six components. The board can function in a four-module configuration when four modules are active and two are deactivated. A complete list of the parts used in the setup is provided in Table 4. The DSP TMS320F28335 is used to build the digital closed-loop controller. BSC009NE2LS5 MOSFETs are being used. The MOSFET has a turn-on resistance of less than 1 mΩ and a rated voltage of 30 V. The drivers and control logic circuitry of the MOSFET would be further manufactured and combined onto a semiconductor chip to provide a more desirable way. The required ripple voltage, the flying active switches' duty cycle, the number of modules, and the output current at full-load frequency all affect the flying capacitor's capacitance. Voltage ripple should be as little as feasible to maximize efficiency. The efficiency of the flying capacitor will be enhanced by its own value. The capacitances of the flying capacitors are 47 µF, with the ripple of the

peak-to-peak capacitor voltage being lower than 1 V. Flying capacitors may be thought of as a continuous voltage source/sink because of their low voltage ripple in comparison to their DC value. Electrical properties like input impedance, power losses, etc., are often connected with capacitance levels in the most of DC-DC converters. To produce less voltage ripple than DC flying capacitors, Class-II multilayer ceramic capacitors (MLCCs) with low equivalent series resistance (ESR) would be adopted. Additionally, to achieve a higher power density, class-II MLCCs sometimes provide a high capacitance per unit area. The flying capacitors employed in this setup are Class-II (e.g., X7R, X6S, etc.) MLCC capacitors. More capacitors should be added in parallel if the current rating of the selected capacitor is insufficient. For this setup, ten 4.7 µF MLCCs in parallel connection are adopted for each module, and the total capacitance is 47 µF. The current grade for every MLCC equals 4 A. The size of the MLCC piece is 0.6 mm × 0.3 mm. According to the operating principle of our suggested design, because of the hybrid design of the suggested converter, which connects the buck inductor to the SC stage, each flying capacitor can be softly charged/discharged during all operating periods. In conventional switched capacitor-based converters, this crucial characteristic will prevent the inrush current. Therefore, complete soft-charging functioning and low device strains are accomplished under all working circumstances.

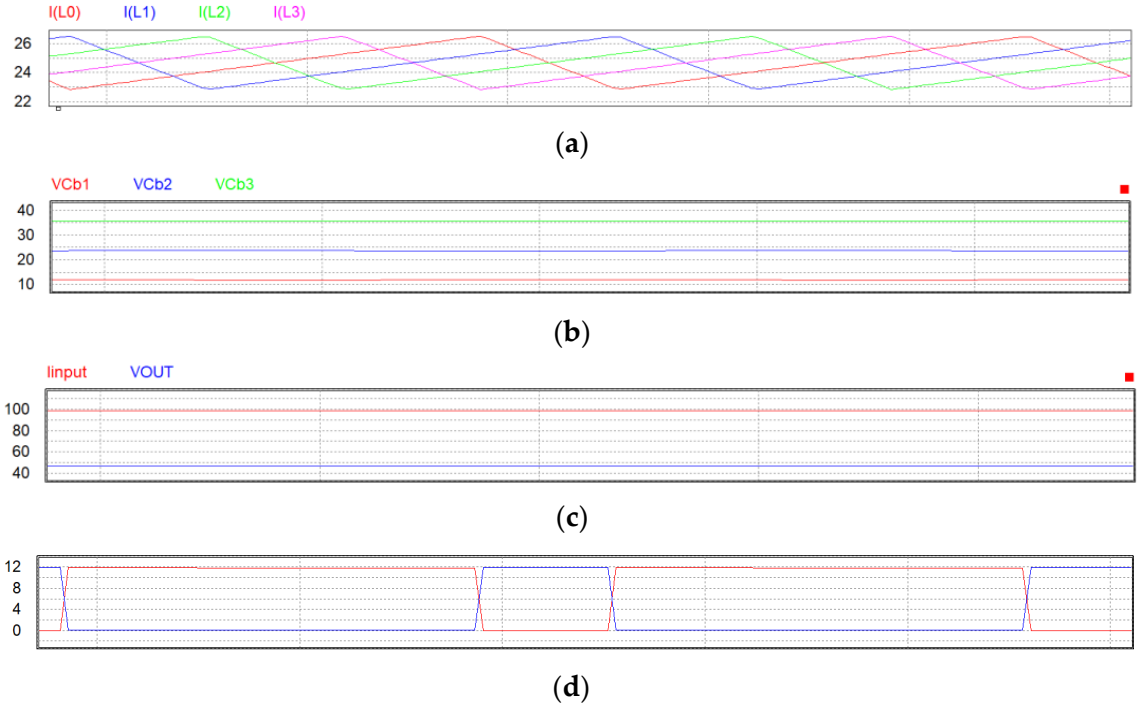
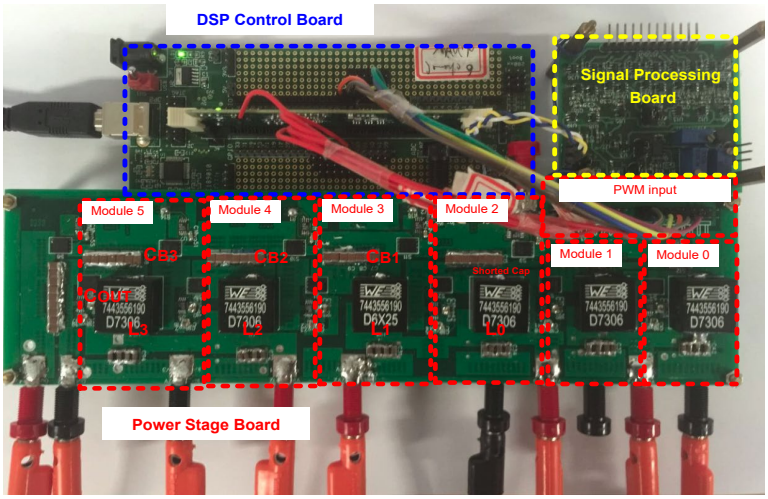


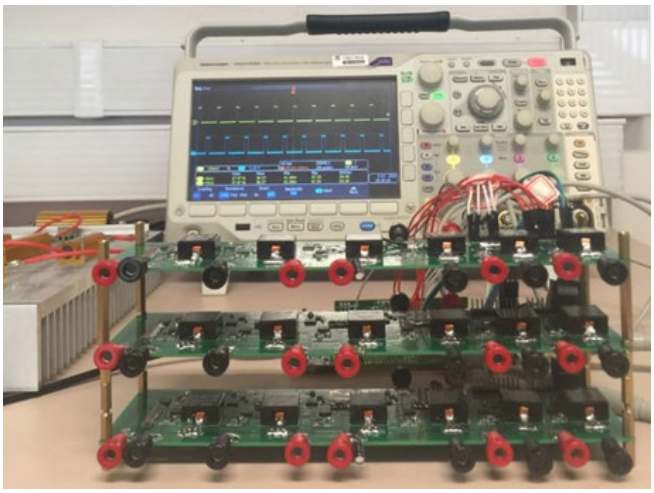

**Figure 7.** Simulated results of the suggested converter in the reverse operation mode with (**a**) inductor $L_0$–$L_3$ current (A), (**b**) voltage for the converter capacitor $C_{B1}$–$C_{B3}$ (V), (**c**) input current (A) and output voltage (V); and (**d**) device $\Phi_3$ and $\overline{\Phi_3}$ drain-to-source voltage (V).

In general, the current ratings of all power MOSFET switches may be derived from the peak inductor current. In reality, all switch current ratings are identical to power inductor current values. The power MOSFET utilized in the experimental setup is manufactured by Infineon and has the component number BSC009NE2LS5. The device's current flow under full load is substantially less than the maximum continuous drain current of 100 A. Full load current may flow via this MOSFET. This power MOSFET is put in a 4 mm × 4 mm package to power both the bottom and flying MOSFETs. The size of power MOSFETs may be decreased via system integration by further combining a pair of flying MOSFETs and a bottom MOSFET into a single package (which is not shown here to illustrate the concept). The prototype power inductor is a Wurth part with part number 744323020, based on the current that each module's power inductor conducts. The saturation current of the inductor

equals 52 A, which is a lot larger than its peak current. Its dimensions are 10.2 mm by 10.2 mm (with a height equal to 5 mm). The test condition and the simulation condition are the same, as shown in Table 3.




(**a**)



(**b**)

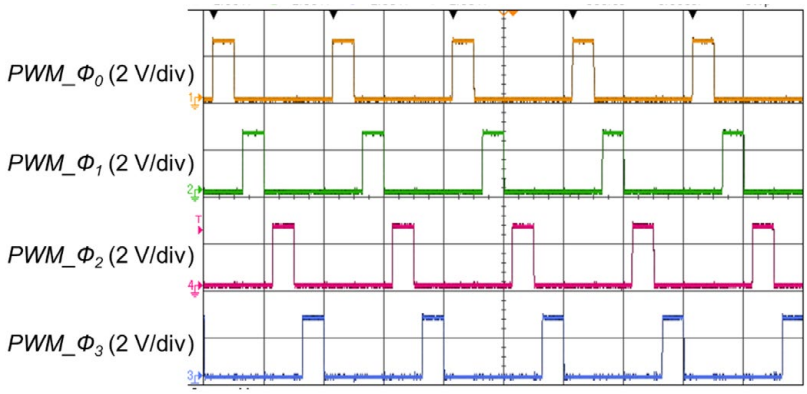
**Figure 8.** Experimental setup of the suggested converter (**a**) single-phase for a power rating of 300 W; (**b**) three-phase for a power rating of 900 W.

**Table 4.** Components for the prototype.

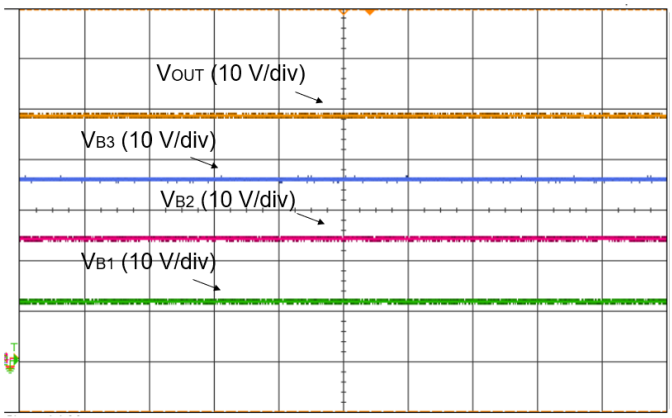
| Depiction | Part# |
|---|---|
| Inductor | 744323020 (0.2 µH) |
| Level Shifter | ADUM5240 |
| Switching Device | BSC009NE2LS5 |
| Gate Driver | LTC4440 |
| Flying Capacitor *CB*1 | C3216X7R1H475K160AC |
| Flying Capacitor *CB*2 | C3216X7R1H475K160AC |
| Flying Capacitor *CB*3 | C3216X7R1H475K160AC |
| Digital Controller | TMS320F28335 |

Figure 9 illustrates the observed waveforms of the current and voltage. Figure 9a illustrates the observed PWM signals of $\Phi_i$ ($i = 0, 1, 2, 3$), and Figure 9b represents the observed waveforms of the output voltage and capacitor voltages $C_{B1}$–$C_{B3}$. As demonstrated,

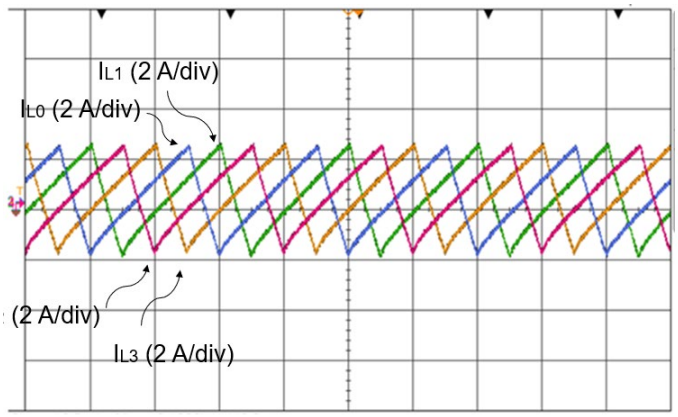
the voltage on $C_{B1}$ is 12 V, $C_{B2}$ is 24 V, and $C_{B3}$ is 36 V, which corresponds to the previous analysis. Figure 9c illustrates the current waveforms flow through $L_0$–$L_3$ under full load conditions (i.e., 900 W for 3 phases). The observed drain-to-source voltage's waveforms for $\Phi_1$ and $\overline{\Phi_1}$ are shown in Figure 9d. The aforementioned findings indicate that the suggested converter can realize a four-phase interleaved operation.




(**a**)

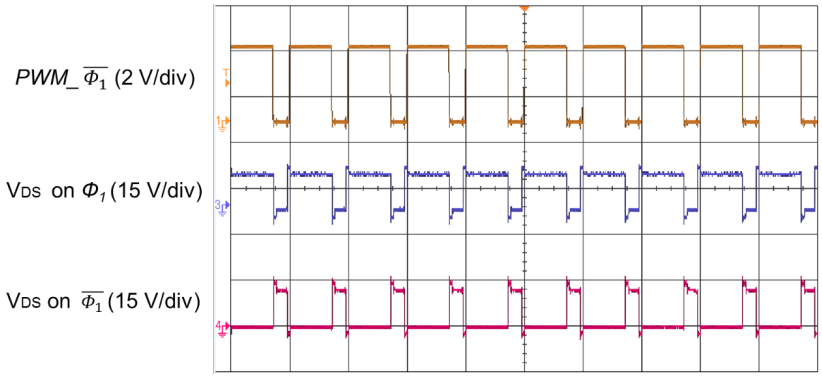



(**b**)




(**c**)

**Figure 9.** *Cont.*




**(d)**

**Figure 9.** (**a**) PWM signals on MOSFETs $\Phi_i$ ($i = 0, 1, 2, 3$) (**b**) voltages cross $C_{B1}$–$C_{B3}$ and output voltage (**c**) currents for $L_0$–$L_3$ (**d**) drain-to-source voltage on $\Phi_1$ and $\overline{\Phi_1}$.

The observed efficiency of the suggested converter switching at 1 MHz while operating in interleaved mode is shown in Figure 10. The input/output voltage are observed through the fluke multimeters under the high-resolution mode to achieve the most accurate results. The output current is tested with programmable chroma loads. The converter's measured maximum efficiency is 92.5%, as depicted in Figure 10.

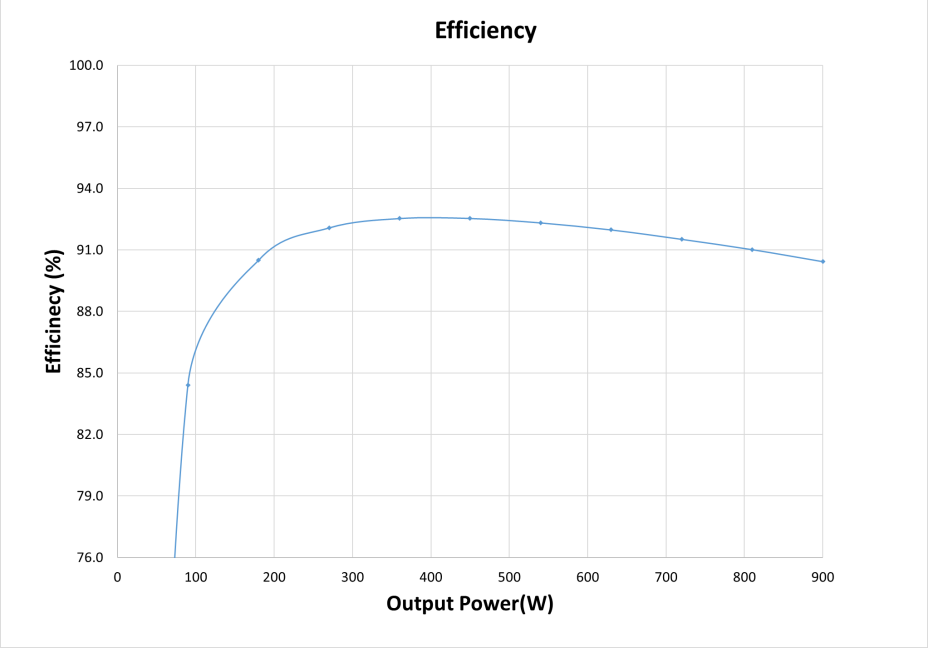



**Figure 10.** Observed efficiency for the converter under 2.4 V output voltage and 900 W output power.

Similar investigations were also conducted for the suggested circuit with $N = 5$. Four modules are with the load conditions in Table 3, and one module is load-free. The switching signals of the four modules with loads are shown in Figure 11a, while the switching signals of the rest module are shown in Figure 11b. The corresponding waveforms of $V_{OUT}$, $I_{OUT}$, and $V_{DS}$ for $\Phi_1$ are presented in Figure 12.

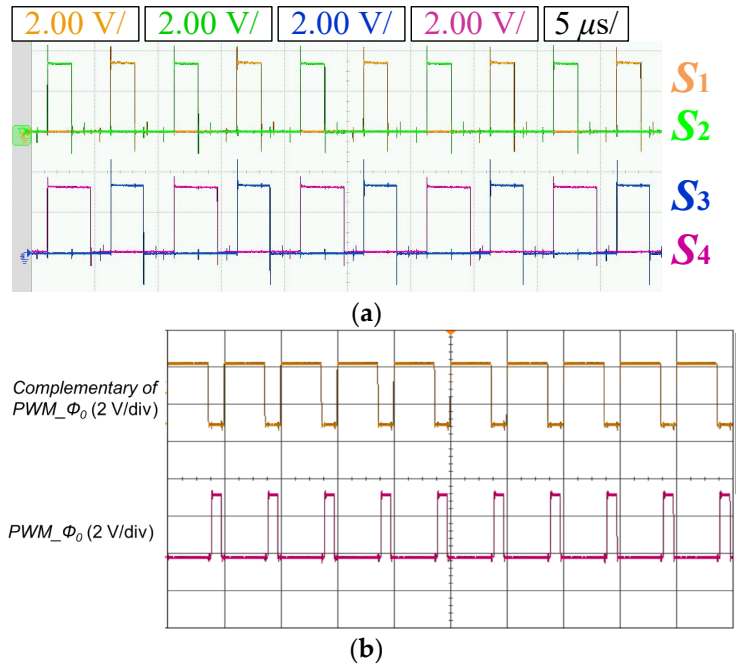



**Figure 11.** (**a**) PWM signals on MOSFETs $\Phi_i$ ($i = 1, 2, 3, 4$) and (**b**) PWM signals of MOSFETs $\Phi_0$ and $\overline{\Phi_0}$ of the studied circuit with $N = 5$.

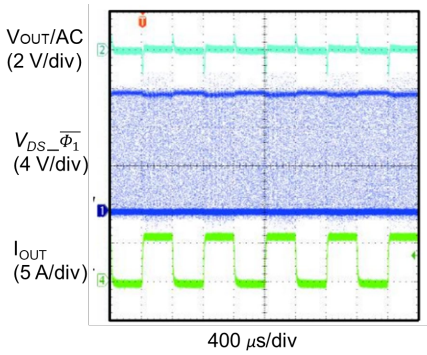



**Figure 12.** Waveforms of $V_{\text{out}}$, $I_{\text{out}}$, and $V_{\text{DS}}$ for $\Phi_1$ for the proposed circuit with $N = 5$.

## 4. A Comparison for Several Types of High-Voltage-Gain-Converters

Adopting two-stage DC/DC conversion is one common method for achieving high-current capacity, high-voltage-gain, and appropriate regulation all at the same time, as was previously described. Figure 13a shows a typical two-stage system for high-current and -power applications. A four-phase buck converter is formed as the first stage, while the second is a switched-capacitor converter with a 4:1 ratio. For applications requiring high-voltage-gain, this two-stage converter is often employed. Compared to single-phase buck operation, four-phase buck operation can achieve precise regulation with rapid reaction and readily manage high-power and high-current strains. Figure 13b shows the suggested converter acquiring the same voltage gain and power rating as the two-stage method to allow for a fair comparison. Given the same voltage gain and power rating, the two-stage system has eighteen active switches in each phase, while the suggested hybrid converter has eight active switches in each phase. All switches from the SC converter stage can be saved, resulting in a low BOM cost. With just one switching stage and fewer switching devices needed, the suggested converter may also achieve substantially greater efficiency with only one set of active switches and lower switching losses. In addition, Table 5 compares the performance of the suggested converter to converters from earlier stages. The recommended converter is proven to have a higher efficiency with the same voltage gain.

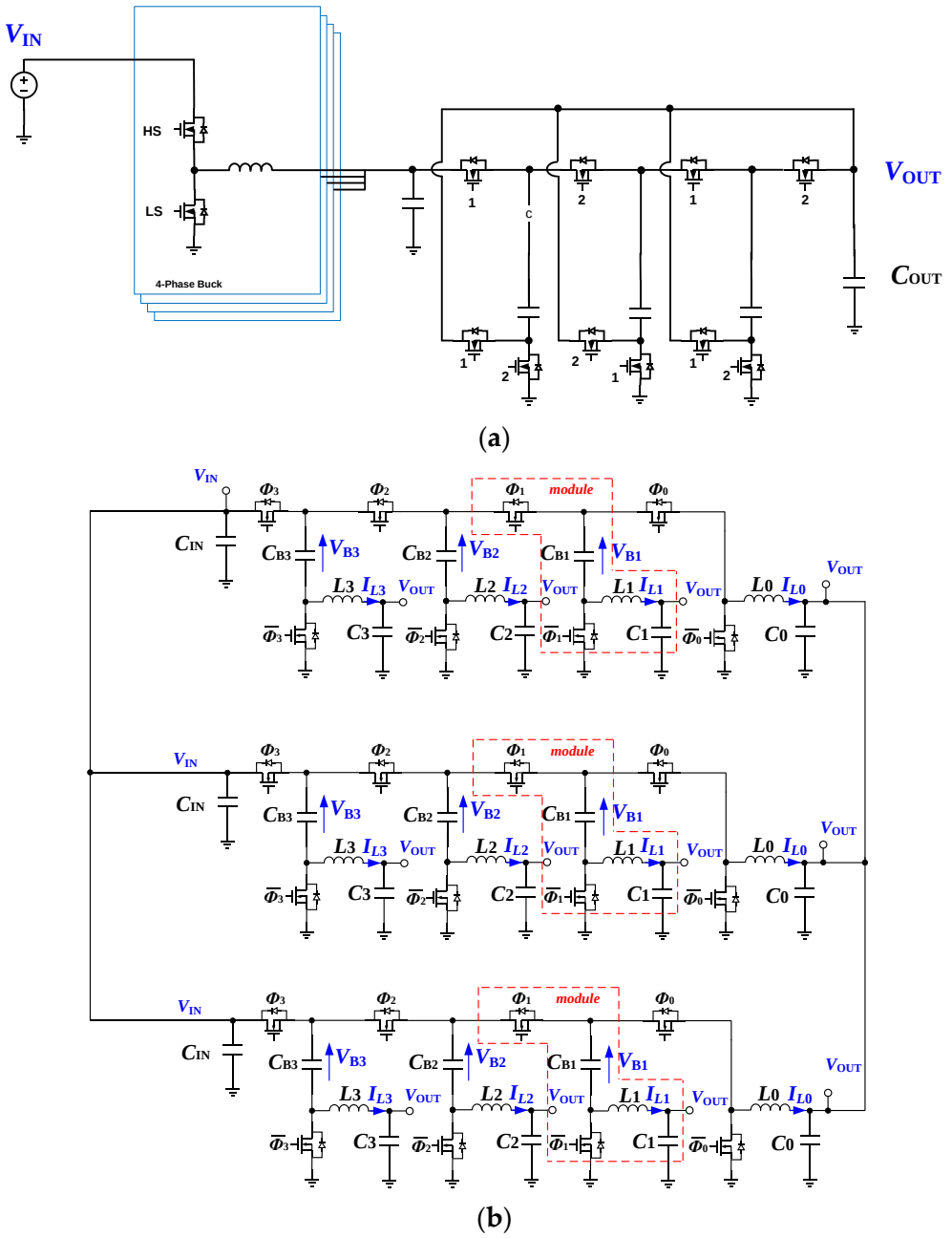



**Figure 13.** (**a**) Traditional two-stage solution with high-voltage-gain step-down conversion for high-current and -power devices. (**b**) Suggested conveter.

**Table 5.** Comparisons for the high-voltage-gain converters.

| Converter in | Voltage Gain (Times) | Scalability | Switching Frequency (kHz) | Peak Efficiency (%) |
|---|---|---|---|---|
| [33] | 20 | Poor | 1000 | 90% |
| Cascaded multi-phase buck | 20 | Medium | 1000 | 91.7% |
| Proposed | 20 | Very good | 1000 | 92.5% |

## 5. Conclusions

In this work, a novel class of high-frequency transformerless converters is presented for high-efficiency applications that need high-voltage step-down ratios. The characteristics can be summarized as follows.

a. A high-voltage step-down ratio that is adjustable and has a medium duty cycle.
b. High efficiency due to the employment of low-voltage, high-powered switching devices and the smaller number of MOSFETs in the single merging stage, making it suitable for high-frequency operation.
c. Due to the interleaved operation, there is no pulsing current and minimal current ripple.
d. The total cost is relatively low because of the hybrid design using less MOSFETs and the integration of two-stage converters to single-stage converters.
e. Inherent modularity and scalability for high-power applications.
f. Mitigation current and voltage spike issues and electro-magnetic interference (EMI) concerns as a result of the flying capacitors' soft-charging action.

The research analyzes the recommended converter's steady-state performance. A 48 V to 2.4 V, 900 W converter system was created to illustrate the benefits of the recommended topology. The highest efficiency was 92.5 percent. The validity of the theoretical analysis was determined by simulation and experimentation. Applications needing a high-current, high-voltage-gain, and high-power hold a lot of potential for the recommended converter. The suggested hybrid converter may therefore be used in power conversion applications.

**Author Contributions:** Conceptualization, H.X. and Y.M.; methodology, H.X.; software, J.L.; validation, H.X., B.X. and X.J.; formal analysis, H.X.; investigation, H.X. and J.L.; resources, Y.M.; data curation, H.X.; writing—original draft preparation, H.X.; writing—review and editing, Y.M.; visualization, J.L., B.X. and X.J.; supervision, Y.M.; project administration, Y.M. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research received no external funding.

**Data Availability Statement:** Data is unavailable due to ethical restrictions.

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

1. Guerrro, J.M.; Vasquez, J.; Matas, J.; de Vicuna, L.; Castilla, M. Hierarchical control of droop-controlled AC and DC microgrids—A general approach toward standardization. *IEEE Tran. Ind. Electron.* **2011**, *58*, 158–172. [CrossRef]
2. Yang, Y.; Mok, K.; Tan, S.; Hui, S.Y.R. Nonlinear dynamic power tracking of low-power wind energy conversion system. *IEEE Tran. Power Electron.* **2015**, *30*, 5223–5236. [CrossRef]
3. Huang, Y.; Mei, Y.; Xiong, S.; Tan, S.; Tang, C.; Hui, S.Y.R. Reverse electrodialysis energy harvesting system using high-gain step-up dc/dc converter. *IEEE Trans. Sustain. Energy* **2018**, *9*, 1578–1587. [CrossRef]
4. Huang, Y.; Xiong, S.; Tan, S.; Hui, S.Y. Non-isolated harmonics-boosted resonant DC/DC converter with high-step-up gain. *IEEE Trans. Power Electron.* **2017**, *9*, 7770–7781.
5. Yang, Y.; Tan, S.; Hui, S.Y.R. Mitigating distribution power loss of DC microgrids with DC electric springs. *IEEE Trans. Smart Grid* **2018**, *9*, 5897–5906. [CrossRef]
6. Pan, C.T.; Lai, C.M. A high-efficiency high step-up converter with low switch voltage stress for fuel-cell system applications. *IEEE Trans. Ind. Electron.* **2010**, *57*, 1998–2006.
7. Lineykin, S.; Ben-Yaakov, S. Modeling and analysis of thermoelectric modules. *IEEE Trans. Ind. Electron.* **2007**, *43*, 505–512. [CrossRef]
8. Huber, L.; Jovanovic, M.M. A design approach for server power supplies for networking applications. In Proceedings of the Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition, New Orleans, LA, USA, 6–10 February 2000; pp. 1163–1169.
9. Feng, X.G.; Liu, J.; Lee, F.C. Impedance specifications for stable dc distributed power systems. *IEEE Trans. Power Electron.* **2002**, *17*, 157–162. [CrossRef]
10. Schaef, C.; Rentmeister, J.; Stauth, J.T. Multimode Operation of Resonant and Hybrid Switched-Capacitor Topologies. *IEEE Trans. Power Electron.* **2018**, *33*, 10512–10523. [CrossRef]
11. Schaef, C.; Din, E.; Stauth, J.T. A Hybrid Switched-Capacitor Battery Management IC With Embedded Diagnostics for Series-Stacked Li–Ion Arrays. *IEEE J. Solid-State Circuits* **2017**, *52*, 3142–3154. [CrossRef]

12. Le, H.; Crossley, J.; Sanders, S.; Alon, E. A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19W/mm2 at 73% efficiency. In Proceedings of the 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, San Francisco, CA, USA, 17–21 February 2013; pp. 372–373.
13. Le, H.; Sanders, S.; Alon, E. Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters. *IEEE J. Solid-State Circuits* **2011**, *46*, 2120–2131. [CrossRef]
14. Li, K.; Hu, Y.; Ioinovici, A. Generation of the large DC gain step-up non-isolated converters in conjunction with renewable energy sources starting from a proposed geometric structure. *IEEE Trans. Power Electron.* **2017**, *32*, 5323–5340. [CrossRef]
15. Wu, G.; Ruan, X.; Ye, Z. Non-isolated high step-up DC–DC converters adopting switched-capacitor cell. *IEEE Trans. Ind. Electron.* **2015**, *62*, 383–393. [CrossRef]
16. Dickson, J. On-chip high-voltage generation in mnos integrated circuits using an improved voltage multiplier technique. *IEEE J. Solid-State Circuits* **1976**, *11*, 374–378. [CrossRef]
17. Chen, M.; Li, K.; Hu, J.; Ioinovici, A. Generation of a family of very high DC gain power electronics circuits based on switched-capacitor-inductor cells starting from a simple graph. *IEEE Trans. Circuits Syst.* **2016**, *63*, 2381–2392. [CrossRef]
18. Eguchi, K.; Ueno, F.; Zhu, H.; Tabata, T.; Fujiyoshi, A. An IC chip of a Dickson-type DC-DC converter with bootstrapped gate transfer switches. In Proceedings of the IEEE Region 10 Conference TENCON 2004, Chiang Mai, Thailand, 24 November 2004; pp. 77–80.
19. Kiratipongvoot, S.; Tan, S.; Ioinovici, A. Phase-shift interleaving control of variable-phase switched-capacitor converters. *IEEE Trans. Ind. Electron.* **2013**, *60*, 5575–5584. [CrossRef]
20. Cheung, C.K.; Tan, S.; Tse, C.; Ioinovici, A. On energy efficiency of switched-capacitor converters. *IEEE Trans. Power Electron.* **2013**, *28*, 862–876. [CrossRef]
21. Law, K.K.; Cheng, K.; Yeung, Y.P.B. Design and analysis of switched-capacitor-based step-up resonant converters. *IEEE Trans. Circuits Syst.* **2005**, *52*, 943–948. [CrossRef]
22. Ye, Y.; Cheng, K.E.; Liu, J.; Xu, C. A family of dual-phase-combined zero-current switching switched-capacitor converters. *IEEE Trans. Power Electron.* **2014**, *29*, 4209–4218. [CrossRef]
23. Ben-Yaakov, S. Behavioral average modeling and equivalent circuit simulation of switched capacitors converters. *IEEE Trans. Power Electron.* **2012**, *27*, 632–636. [CrossRef]
24. Rentmeister, J.S.; Stauth, J.T. Modeling the Dynamic Behavior of Hybrid-Switched-Capacitor Converters in State Space. In Proceedings of the 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padova, Italy, 25–28 June 2018; pp. 1–7.
25. Schaef, C.; Stauth, J.T. A 12-volt-input hybrid switched capacitor voltage regulator based on a modified series-parallel topology. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 2453–2458.
26. Farth, H.M.H.; Othman, M.; Eltamaly, A.; Al-Saud, M.S. Maximum power extraction from a partially shaded PV system using an interleaved boost converter. *Energies* **2018**, *11*, 2543. [CrossRef]
27. Farth, H.M.H.; Eltamaly, A.; Al-Saud, M.S. Interleaved boost converter for global maximum power extraction from the photovoltaic system under partial shading. *IET Renew. Power Gener.* **2019**, *13*, 1232–1238. [CrossRef]
28. Cervera, A.; Ben-Yaakov, S.; Peretz, M. Single-stage switched-resonator converter topology with wide conversion ratio for volume-sensitive applications. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 1706–1712.
29. Schaef, C.; Din, E.; Stauth, J.T. 10.2 A digitally controlled 94.8%-peak-efficiency hybrid switched-capacitor converter for bidirectional balancing and impedance-based diagnostics of lithium-ion battery arrays. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 180–181.
30. Schaef, C.; Reese, B.; Sullivan, C.; Stauth, J.T. Design aspects of multi-phase interleaved resonant switched-capacitor converters with mm-scale air-core inductors. In Proceedings of the 2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL), Vancouver, BC, Canada, 12–15 July 2015; pp. 1–5.
31. Schaef, C.; Kesarwani, K.; Stauth, J.T. 20.2 A variable-conversion-ratio 3-phase resonant switched capacitor converter with 85% efficiency at 0.91W/mm$^2$ using 1.1nH PCB-trace inductors. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference—(ISSCC) Digest of Technical Papers, San Francisco, CA, USA, 22–26 February 2015; pp. 1–3.
32. Cao, D.; Peng, F.Z. A family of zero current switching switched-capacitor dc-dc converters. In Proceedings of the 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Palm Springs, CA, USA, 21–25 February 2010; pp. 1365–1372.
33. Krismer, F.; Biela, J.; Kolar, J.W. A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range. In Proceedings of the Fourtieth IAS Annual Meeting, Conference Record of the 2005 Industry Applications Conference, Hong Kong, China, 2–6 October 2005; pp. 599–606.
34. Krismer, F.; Kolar, J.W. Closed form solution for minimum conduction loss modulation of DAB converters. *IEEE Trans. Power Electron.* **2012**, *27*, 174–188. [CrossRef]

35. Shang, F.; Krishnamurthy, M.; Isurin, A. A novel high gain step-up resonant DC-DC converter for automotive application. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 880–885.
36. Hwu, K.I.; Jiang, W.; Yau, Y.T. An isolated high step-up converter with continuous input current and LC snubber. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 2415–2421.