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Double Dual High Step-Up Power Converter with Reduced Stored Energy

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Abstract: This paper introduces a dual-switchhigh step-up DC-DC power converter. The proposed converter features a high step-up voltage gain, relatively low cumulative stored energy over its inductors, low voltage stress on the active switches, and high efficiency, even at a relatively high duty ratio. An assessment of the proposed converter against conventional boost and a high step-up power converter is presented in terms of steady-state time, voltage gain, stored energy over its inductors, and efficiency. The assessment shows a reduction of 81.25% and 62.5% of stored energy in inductors to comply with the same operational conditions. Simulation and experimental results are provided to validate the benefits of the proposed dual-switch high step-up power converter.

Keywords: DC-DC power converter; boost converter; high step-up power converter

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1. Introduction

Nowadays, DC-DC power electronic converters are among the main building blocks in various electrical applications, such as renewable energy integration systems, high-intensity lamp ballasts in automobiles, smart lighting, and small, medium, and high-scale electronic appliances [1–3]. According to the literature, in theory, a DC-DC boost power converter with synchronous rectification can be designed to achieve a high step-up voltage gain by properly managing its duty cycle (d or D) [4]. The "conventional Boost" is shown in Figure 1, where the input voltage V_g, input current i_g, and output voltage V_o are indicated. The topology consists of one inductor L, one capacitor C, and a load resistor R. Note that the switching function s is complementary to the switching function $\bar{s}$. However, in reality, the step-up voltage gain is restricted due to switching losses of semiconductors, equivalent series resistors of inductors and capacitors, and other parasitic effects of the implemented circuit [5,6]. Furthermore, it is well established in the literature that the higher the duty ratio, the higher the reverse-recovery problem. To help alleviate this issue, some topologies have been proposed [7,8]. Their objective is to provide a high step-up voltage gain while maintaining a relatively low-duty cycle. Featuring a high step-up voltage gain, other investigations include the so-called "transformerless DC-DC power converters" [9–11]. These studies include (but are not limited to) the cascade boost type power converter, the quadratic boost type [12,13], the capacitor-diode voltage multiplier type [14,15], and the boost type with switched-capacitor technique [16]. Nevertheless, all of these power converter designs are intricate and present relatively high costs. A transformerless DC-DC power converter was proposed in [17], featuring high step-up (HSU) voltage gain. The HSU converter is depicted in Figure 2 and consists of two switches s_1 and s_2, two inductors L_1 and L_2, an output diode D_1, and a capacitor C. Switches s_1

and s_2 are controlled simultaneously. The HSU power converter implements the switched-inductor technique, where two inductors with equal inductance values are charged in parallel during the switch-on state and are discharged in series during the switch-off state of the power converter. This technique enables a high step-up voltage gain while avoiding an extreme duty ratio.

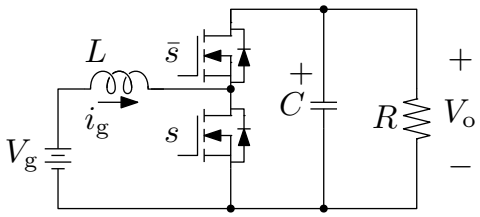

Figure 1. Conventional boost power converter.

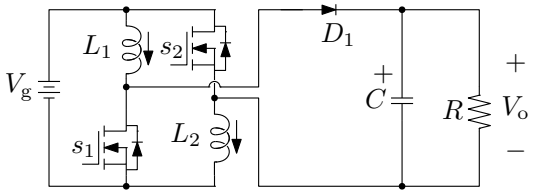

Figure 2. High step-up (HSU) power converter.

In this paper, a dual-switch high step-up power converter, termed the "Double Dual Super Boost (DDSB)", is proposed. It is depicted in Figure 3 and features a high step-up voltage gain, low voltage stress on the active switches, and high efficiency (even at a relatively high duty ratio). Additionally, when compared to the conventional boost and the so-called HSU power converters, the DDSB converter has a significantly higher voltage gain. Furthermore, in terms of stored energy over its inductors, the cumulative stored energy is substantially less.

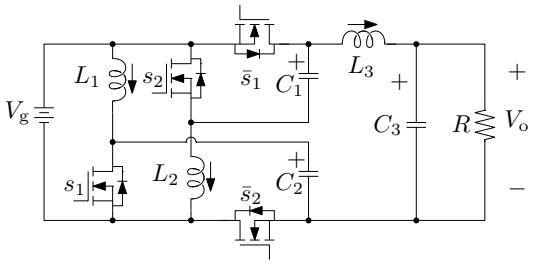

Figure 3. Proposed high step-up power converter, named the "Double Dual Super Boost (DDSB)".

Based on the discussion above, the main contributions of this article are summarized as follows:

- A new dual-switch high step-up power converter is proposed. It is identified as the "Double Dual Super Boost", featuring high step-up voltage gain;
- When compared to the conventional boost and HSU power converters, its cumulative stored energy over its inductors is significantly less;
- Lastly, the DDSB power converter outperforms the conventional boost and HSU power converters featuring significantly less voltage stress over the active switches;

This paper is organized as follows. The converter principle of operation is presented in Section 2. A comparative evaluation is developed thoroughly in Section 3. Experimental results are presented in Section 4. Finally, conclusions are summarized in Section 5.

2. Modeling

The proposed topology contains three inductors: L_1, L_2, and L_3; three capacitors: C_1, C_2, and C_3; and four transistors: s_1, s_2, $\bar{s}_1$, and $\bar{s}_2$. It is depicted in Figure 3. Switching functions of transistors s_1 and s_2 are complementary to the switching functions of transistors $\bar{s}_1$ and $\bar{s}_2$.

In the continuous conduction mode (CCM), the analysis of the switching states leads to two possible equivalent circuits depicted in Figures 4 and 5.

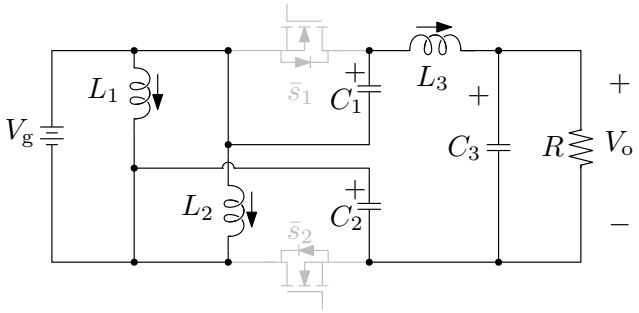

Figure 4. Equivalent circuit of switching state 1.

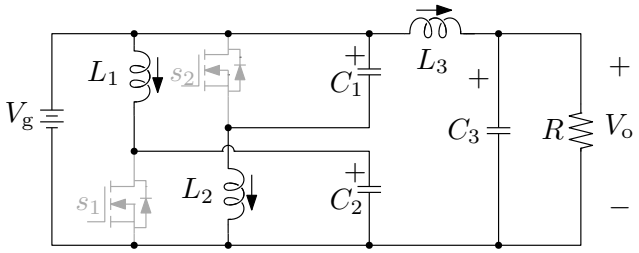

Figure 5. Equivalent circuit of switching state 2.

2.1. Mathematical Model of the Proposed DDSB Converter

Regarding the mathematical model of the DDSB power converter, it is necessary to take into account both circuits shown in Figures 4 and 5. By applying the standard averaging technique, the following mathematical model is obtained. The average voltage across inductors L_1, L_2, and L_3 during one switching cycle is expressed by Equations (1)–(3), respectively.

$$L_1 \frac{di_{L_1}}{dt} = d(V_g) + (1-d)(V_g - v_{C_2}), \tag{1}$$

$$L_2 \frac{di_{L_2}}{dt} = d(V_g) + (1-d)(V_g - v_{C_1}), \tag{2}$$

$$L_3 \frac{di_{L_3}}{dt} = d(V_g + v_{C_1} + v_{C_2} - v_{C_3}) + (1-d)(V_g - v_{C_3}), \tag{3}$$

where v_{C_1}, v_{C_2}, and v_{C_3} correspond to the voltage across each capacitor, and i_{L_1}, i_{L_2}, and i_{L_3} refer to the current through each of the inductors. Notice, the first term of each equation (multiplied by d) corresponds to the voltage across each inductor when the switches s_1 and s_2 are closed. The second term of each previous equation represents the voltage across each inductor when the switches s_1 and s_2 are open (multiplied by (1–d)). In the same fashion, the averaging technique can be applied to the current passing through each of the capacitors. By doing so, the average current through capacitors C_1, C_2, and C_3 can be expressed as (4)–(6), respectively. It should be noted that i_o corresponds to the output current and is calculated by ($i_o = -V_o/R$).

$$C_1 \frac{dv_{C_1}}{dt} = d(-i_{L_3}) + (1-d)i_{L_2}. \tag{4}$$

$$C_2 \frac{dv_{C_2}}{dt} = d(-i_{L_3}) + (1-d)i_{L_1}. \tag{5}$$

$$C_3 \frac{dv_{C_3}}{dt} = d(i_{L_3} - i_o) + (1-d)(i_{L_3} - i_o). \tag{6}$$

The set of Equations (1)–(6) is the average dynamic model of the converter. Before analyzing the model, Equations (1)–(6) can be simplified by performing some mathematical manipulations. The simplified equations are rewritten as Equations (7)–(12).

$$L_1 \frac{di_{L_1}}{dt} = V_g - (1-d)v_{C_2}, \tag{7}$$

$$L_2 \frac{di_{L_2}}{dt} = V_g - (1-d)v_{C_1}, \tag{8}$$

$$L_3 \frac{di_{L_3}}{dt} = V_g + d(v_{C_1} + v_{C_2}) - v_{C_3}, \tag{9}$$

$$C_1 \frac{dv_{C_1}}{dt} = (1-d)i_{L_2} - di_{L_3}, \tag{10}$$

$$C_2 \frac{dv_{C_2}}{dt} = (1-d)i_{L_1} - di_{L_3}, \tag{11}$$

$$C_3 \frac{dv_{C_3}}{dt} = i_{L_3} - i_o. \tag{12}$$

The average dynamic model assumes that the DDSB power converter is operating in CCM.

2.2. DC Components of State Equations or Equilibrium Operating Point

From the dynamic model of the proposed DDSB converter represented by Equations (7)–(12), the equilibrium operating point can be calculated. Considering the small ripple approximation [18], which can be summarized as variables that appear in lowercase in Equations (7)–(12). The lowercase format indicates that these are not constant values. The small ripple approximation considers that changes over the state variables are negligibly small during a single switching cycle. This can be accomplished by selecting an appropriate switching frequency and nominal values of capacitance and inductance for capacitors and inductors, respectively. In the steady state, the derivative of state variables is equal to zero. Therefore, by making Equations (7)–(12) equal to zero and considering the small ripple approximation, the equilibrium of the converter can be found. From Equations (7) and (8), the voltage across the capacitors C_1 and C_2 can be determined as follows:

$$V_{C_1} = \frac{1}{1-D} V_g, \qquad V_{C_2} = \frac{1}{1-D} V_g. \tag{13}$$

Then, the output voltage, which is the same as V_{C_3}, can be obtained from (9) as follows:

$$\begin{aligned} V_o &= V_g + D(V_{C_1} + V_{C_2}), \\ &= V_g + D\left(\frac{1}{1-D} V_g + \frac{D}{1-D} V_g\right). \end{aligned} \tag{14}$$

$$\begin{aligned} V_o &= \left(1 + \frac{D}{1-D} + \frac{D}{1-D}\right) V_g, \\ &= \left(\frac{1-D}{1-D} + \frac{D}{1-D} + \frac{D}{1-D}\right) V_g. \end{aligned} \tag{15}$$

Finally,

$$V_o = \left(\frac{1+D}{1-D}\right) V_g. \tag{16}$$

Similarly, after some mathematical manipulations, the current through each of the inductors can be derived from Equations (10)–(12) as follows:

$$I_{L_3} = I_o, \qquad I_{L_2} = \frac{D}{1-D} I_o, I_{L_1} = \frac{D}{1-D} I_o. \tag{17}$$

2.3. Selection of Components

The reactive elements of the DDSB converter can be sized following the standard procedure presented in [18], with the design specifications being the maximum current ripple allowed in inductors and the maximum voltage ripple allowed in capacitors. From the equivalent circuits shown in Figures 4 and 5, inductors L_1 and L_2 can be chosen with the following Equation (18).

$$L_1 = \frac{V_g}{2\Delta i_{L1}} DT_{sw}, \qquad L_2 = \frac{V_g}{2\Delta i_{L2}} DT_{sw}, \tag{18}$$

where Δi_{L1} and Δi_{L2} are the maximum allowed current ripples through L_1 and L_2, respectively, and can be obtained as a percentage of the DC (for example, 10% of the DC at the rated power). Equation (18) can be derived relatively simply since inductors L_1 and L_2 are connected to the input power source when the transistors are closed. Regarding L_3, we may observe that it is connected to the voltage $V_{C1} + V_g + V_{C2} - V_{C3}$ when transistors are closed (see Figures 4 and 5). Hence, their inductances can be selected with Equations (19) and (20).

$$L_3 = \left(V_{C1} + V_g + V_{C2} - V_{C3}\right) \frac{DT_{sw}}{2\Delta i_{L3}}, \tag{19}$$

$$L_3 = V_g \left(\frac{1}{1-D} + 1 + \frac{1}{1-D} - \frac{1+D}{1-D}\right) \frac{DT_{sw}}{2\Delta i_{L3}} = \frac{V_g}{\Delta i_{L3}} DT_{sw}, \tag{20}$$

where Δi_{L3} is the maximum allowable current ripple through L_3.

In the case of capacitors, from the equivalent circuits shown in Figures 4 and 5, capacitances C_1 and C_2 can be chosen with the following Equation (21).

$$C_1 = \frac{I_o}{2\Delta v_{C1}} DT_{sw}, \qquad C_2 = \frac{I_o}{2\Delta v_{C2}} DT_{sw}, \tag{21}$$

where Δv_{C1} and Δv_{C2} are the maximum allowable voltage ripple in C_1 and C_2, respectively; similar to the current ripple case in the inductors, the maximum voltage ripple can be provided as a percentage of the DC voltage (for example, 0.1% of the DC voltage at the rated power). C_3's current is continuous since it belongs to a second-order filter; similar to the Buck or the Cuk converter, the capacitance can be determined with (22),

$$C_3 = \frac{\Delta i_{L3} T_{sw}}{8\Delta v_{C3}}, \tag{22}$$

where Δv_{C3} is the maximum allowable voltage ripple in C_3, which (in this case) is the same as the output voltage ripple.

2.4. Stored Energy in Inductors

Regarding the conventional boost power converter, its input current ripple is given by Equation (23),

$$\Delta i_g = \Delta i_L = \frac{V_g D T_{sw}}{2L}. \tag{23}$$

Moreover, the energy that is stored over its pole inductor, defined as $W_{L,B}$, can be determined by Equation (24),

$$W_{L,B} = \frac{1}{2} L i_L^2 = \frac{1}{2} L \{ \frac{I_o}{1-D} + \Delta i_L \}^2. \tag{24}$$

In the case of the HSU power converter, the input current ripple of each inductor can be determined by Equation (25),

$$\Delta i_{L_1} = \frac{V_g D T_{sw}}{2L_1}, \qquad \Delta i_{L_2} = \frac{V_g D T_{sw}}{2L_2}. \tag{25}$$

In addition, the energy stored over the two inductors, defined as $W_{L,HSU}$, can be obtained by Equation (26),

$$\begin{aligned} W_{L1} &= \frac{1}{2} L_1 i_{L_1}^2 = \frac{1}{2} L_1 \{ \frac{I_o}{1-D} + \Delta i_{L_1} \}^2, \\ W_{L2} &= \frac{1}{2} L_2 i_{L_2}^2 = \frac{1}{2} L_2 \{ \frac{I_o}{1-D} + \Delta i_{L_2} \}^2, \\ W_{L,HSU} &= W_{L1} + W_{L2}. \end{aligned} \tag{26}$$

In relation to the proposed DDSB converter depicted in Figure 3, it can be determined that the input current ripple over the inductors L_1, L_2, and L_3 is expressed by Equation (27),

$$\begin{aligned} \Delta i_{L_1} &= \frac{V_g D T_{sw}}{2L_1}, \\ \Delta i_{L_2} &= \frac{V_g D T_{sw}}{2L_2}, \\ \Delta i_{L_3} &= \frac{(V_g + v_{C_1} + v_{C_2} - V_o) D T_{sw}}{2L_3}. \end{aligned} \tag{27}$$

Furthermore, the stored energy over the three inductors, defined as $W_{L,DDSB}$, can be determined by Equation (28), as follows:

$$\begin{aligned} W_{L1} &= \frac{1}{2} L_1 \{ \frac{I_o D}{1-D} + \Delta i_{L_1} \}^2, \\ W_{L2} &= \frac{1}{2} L_2 \{ \frac{I_o D}{1-D} + \Delta i_{L_2} \}^2, \\ W_{L3} &= \frac{1}{2} L_3 \{ I_o + \Delta i_{L_3} \}^2, \\ W_{L,DDSB} &= W_{L1} + W_{L2} + W_{L3}. \end{aligned} \tag{28}$$

3. Comparative Evaluation

In this section, a comparative performance evaluation of the conventional boost, HSU, and the proposed DDSB is presented. Five main power converter characteristics are investigated and validated: (i) steady-state time, (ii) output voltage (iii) gain ratio, (iv) stored energy over inductors, and (v) efficiency.

3.1. Considerations

Consider that all three power converters are fed with an input voltage of V_g = 20 V. The converters will be supplying power to a resistive load of 100 Ω, which will demand an output power of 100 W ($I_o = 1$ A) and a switching frequency $F_{sw} = 50$ kHz. The maximum input current ripple is set to 2.1 A, which represents 42% of the input DC. The maximum output voltage ripple is set to 0.8 V, which represents 0.8% of the output voltage.

For internal capacitors, where the output voltage ripple is not affected by these capacitors, the maximum voltage ripple is required to be 0.3% of their DC voltage. In this study, the capacitors and inductors are represented by non-commercial components in the solution of the ripple equations; nevertheless, this is a good approximation of their commercial components.

3.2. Design Parameters

In order to develop a comparative performance evaluation of the conventional boost and HSU versus the proposed DDSB power converter, common design parameters (shown in Table 1) are listed.

Table 1. Nominal design parameters of all three power converters.

Input voltage	V_g	20	V
Output voltage	V_o	100	V
Input current ripple	Δi_L	4.2	A
Output voltage ripple	ΔV_o	0.8	V
Transistors TP65H070L (GaN)	R_{on}	85	mΩ
Switching frequency	f_{sw}	50	kHz

At the same time, and based on the design considerations listed in Table 1, the conventional boost converter requires, for instance, an inductor $L = 74.82$ µH to provide an input current ripple $\Delta i_L = 4.2$ A. The complete reactive elements of the conventional boost converter are presented in Table 2.

Table 2. Conventional boost converter design.

Inductor	L	74.82	µH
	ESR	25	mΩ
Capacitor	C	20	µF
	ESR	5	mΩ

Correspondingly, the HSU converter requires an inductor $L = 250$ µH to provide an input current ripple $\Delta i_L = 4.2$ A. The complete reactive elements of the HSU converter are shown in Table 3.

Table 3. HSU converter design.

Inductor	L_1, L_2	250	µH
	ESR	25	mΩ
Capacitor	C	10	µF
	ESR	5	mΩ

In the same manner, the DDSB converter requires a capacitor C_3 of 10 µF to comply with the output voltage ripple of 0.8V. The complete list of design considerations for the DDSB converter is listed in Table 4.

Simulations were performed using the software platforms Matlab-Simulink [19] and PLEXIM Plecs [20]. The specific simulation results are presented. The design parameters listed in Tables 1–4 were taken into account.

Table 4. DDSB converter design.

Inductors	L_1, L_2, L_3	250	µH
	ESR	27	mΩ
Capacitors	C_1, C_2, C_3	10	µF
	ESR	5	mΩ

3.3. Steady-State Time Comparison

In the present case, the steady-state time of the conventional boost, the HSU, and the DDSB power converters is assessed. To this end, the following assumption is made: any power converter will reach steady-state when a variation of ±1% oof the output voltage V_o is measured. Under this assumption, measurements of the output voltage V_o are depicted in Figure 7. Additionally, the collected information is summarized in Table 5.

Table 5. Steady-state time summary.

Converter	Overshoot Value (V)	Settling Time (ms)
DDSB	149.012	5.66
Conventional Boost	157.025	5.15
HSU	165.009	7.25

From the information presented in Table 5, the lower overshoot voltage is measured in the DDSB converter. However, the conventional boost reaches a steady state faster than both the DDSB and the HSU power converters.

3.4. Output Voltage Comparison

In this case, the output voltage simulation results are depicted in Figure 6. In addition, in order to verify the correctness of the output voltage ripple, a zoom-in of these measurements is shown.

As observed in Figure 6, the output voltage of the conventional boost and the HSU converters is slightly different from the designed output voltage $V_o = 100$ V. Additionally, the output voltage ripple of the conventional boost and the HSU converters appears slightly below that of the DDSB. Hence, a small correction of the duty cycle should be made. This small change will generate simulation results presented in Figure 7, where all three traces feature a reasonable match. It should be noted that in order to obtain an output voltage of V_o = 100 V, the duty cycle values for the conventional boost, the HSU, and the DDSB are $d = 0.807$, $d = 0.675$, and $d = 0.665$, respectively. As depicted in Figure 7, now all three traces of the output voltage ripple are essentially on top of each other and comply with the design specification of the output voltage ripple. In summary, the DDSB outperforms both the conventional boost and the HSU converters in terms of output voltage gain. As shown, a reduction in the duty ratio of 14.2% and 1% is obtained, respectively, while synthesizing the same output voltage.

3.5. Gain Ratio

This subsection evaluates the gain ratio over an operation range of the conventional boost, the HSU, and the DDSB power converters. As shown in Figure 8, a duty cycle range from [0.5 to 0.85] is taken into account. It can be observed that the proposed DDSB significantly outperforms the conventional boost and even surpasses the HSU by 1% in terms of its voltage gain. Note that the added red-colored marks indicate the necessary duty cycle that outputs 100V in both power converters.

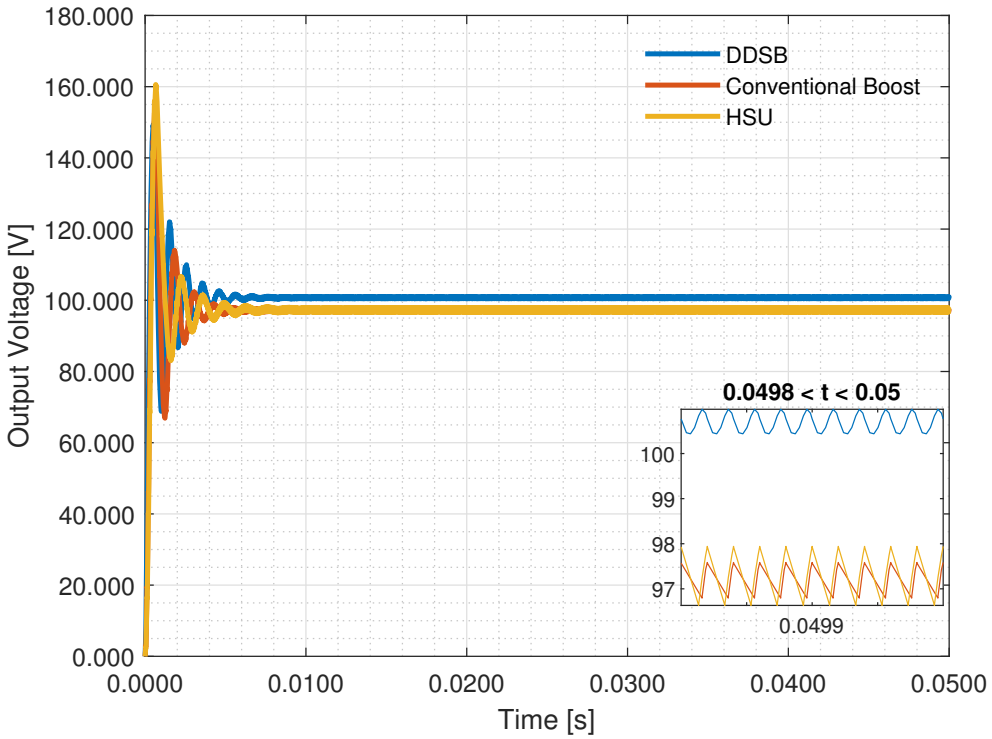

Figure 6. Comparison of the output voltage of the conventional boost and HSU power converters vs. the DDSB converter.

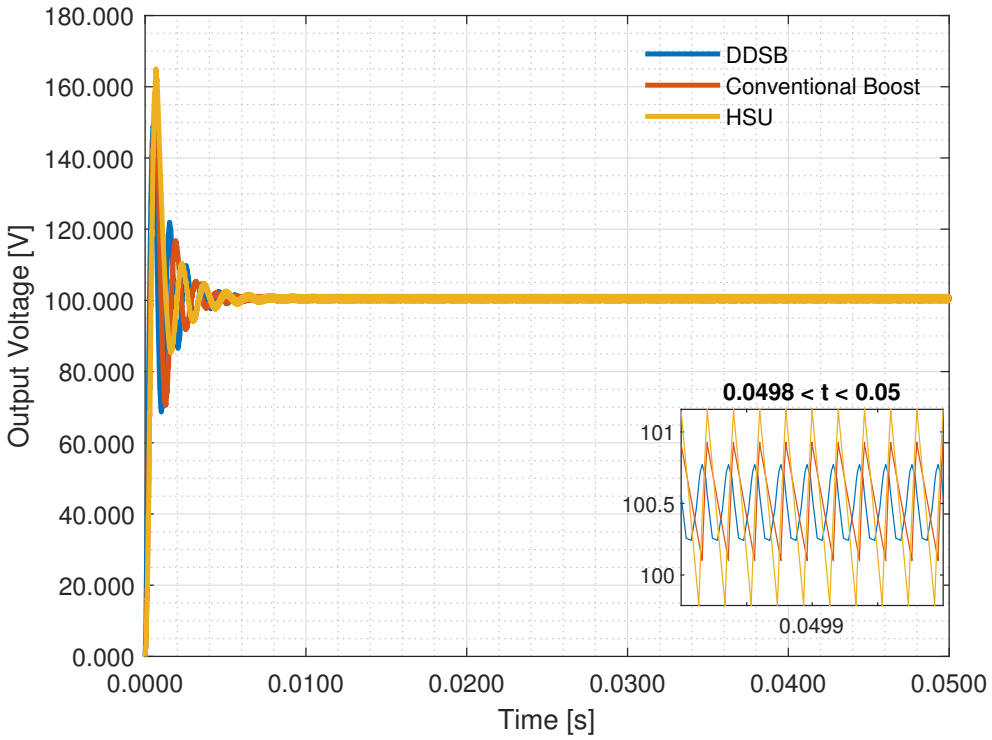

Figure 7. Comparison of the output voltage of the conventional boost ($d = 0.807$), HSU ($d = 0.675$), and DDSB ($d = 0.665$) power converters.

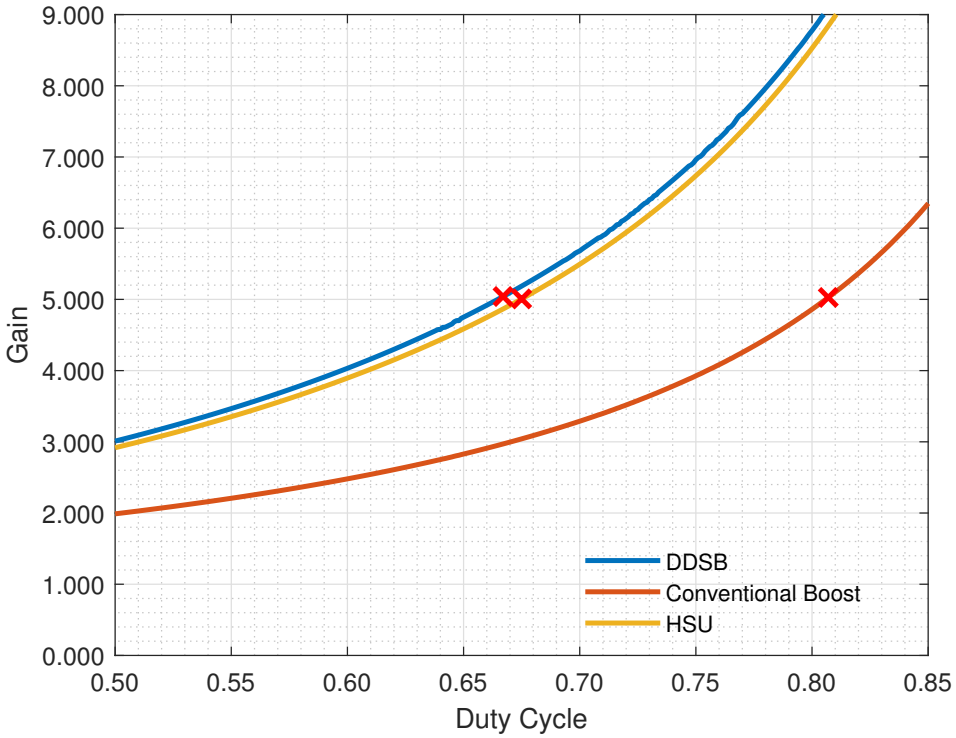

Figure 8. Comparison of the gain ratio of the conventional boost and HSU vs. DDSB power converters.

3.6. Stored Energy Over Inductors

On the one hand, the inductors of any power converter, in order to operate, have to store some amount of energy. Moreover, it must be compliant with a specific design. This energy value is directly related to the inductor size and its operational conditions. On the other hand, a reduction in the size of inductors will have a favorable impact on reducing the power converter cost. In this article, the stored energy over the inductors of the conventional boost, HSU, and DDSB power converters is assessed.

First, using Equation (24), the stored energy over the inductor of the conventional boost is determined. Second, using Equation (26), the stored energy over the inductors of the HSU is computed. Lastly, Equation (28) is used to calculate the stored energy in the inductors of the DDSB. Simulation results of the stored energy over the inductors of all three power converters with respect to their duty cycle are depicted in Figure 9. Similarly, simulation results of the stored energy with respect to their gain ratio are illustrated in Figure 10. Notice that the added red marks depict the necessary stored energy to provide an output voltage of 100V in all three power converters. When the conventional boost is compared to the DDSB, a reduction of 81.25% of stored energy over the inductors is obtained. Similarly, by comparing the HSU to the DDSB, a reduction of 62.50% of stored energy over the inductors is calculated. As shown, in Figures 9 and 10, the DDSB outperforms the conventional boost and the HSU power converters, featuring significantly less stored energy over its inductors.

3.7. Efficiency

Efficiency is one of the main factors in the development and investigation of DC–DC power converters. It is defined as $\eta = \frac{P_i - \Delta P}{P_i} \times 100$, where P_i is the input power, and ΔP accounts for power losses due to switching and conduction. In this article, ΔP is accounted for using standard procedures presented in [4]. Simulation results of the efficiency of all three power converters are shown in Figure 11. According to the traces shown in Figure 11, the DDSB outperforms both the conventional boost and the HSU in terms of efficiency. The red marks indicate the efficiency values when all three power converters output 100 V. At this operating point, the DDSB demonstrates an improvement of 1% and 0.75% in efficiency

compared to the conventional boost and the HSU, respectively. As shown, the DDSB outperforms the conventional boost and HSU converters in terms of efficiency.

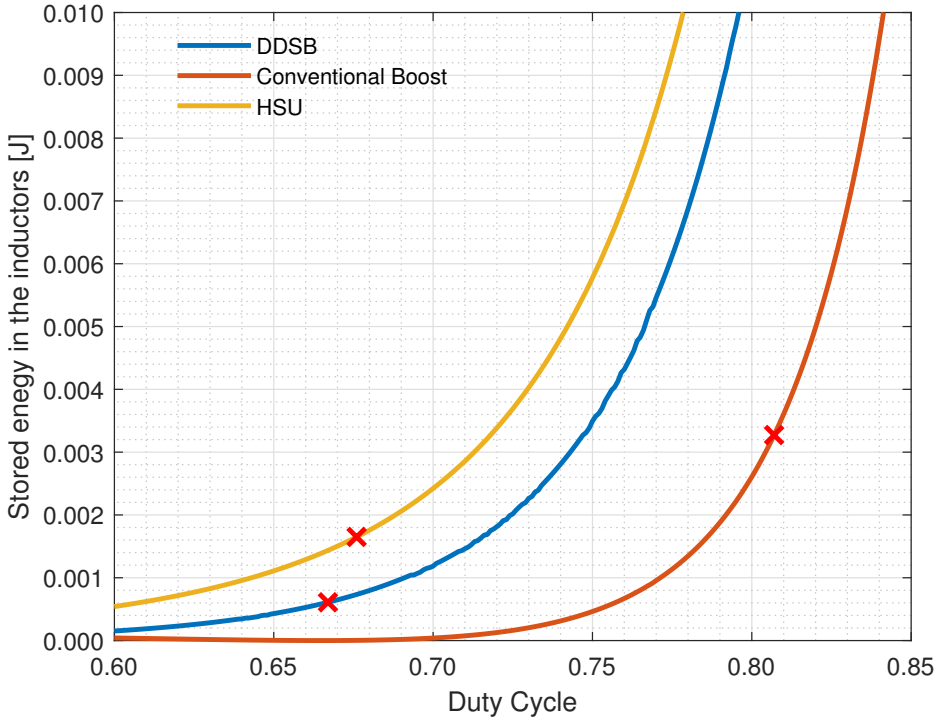

Figure 9. Stored energy in the inductors of the conventional boost, HSU, and DDSB power converters with respect to the duty cycle d.

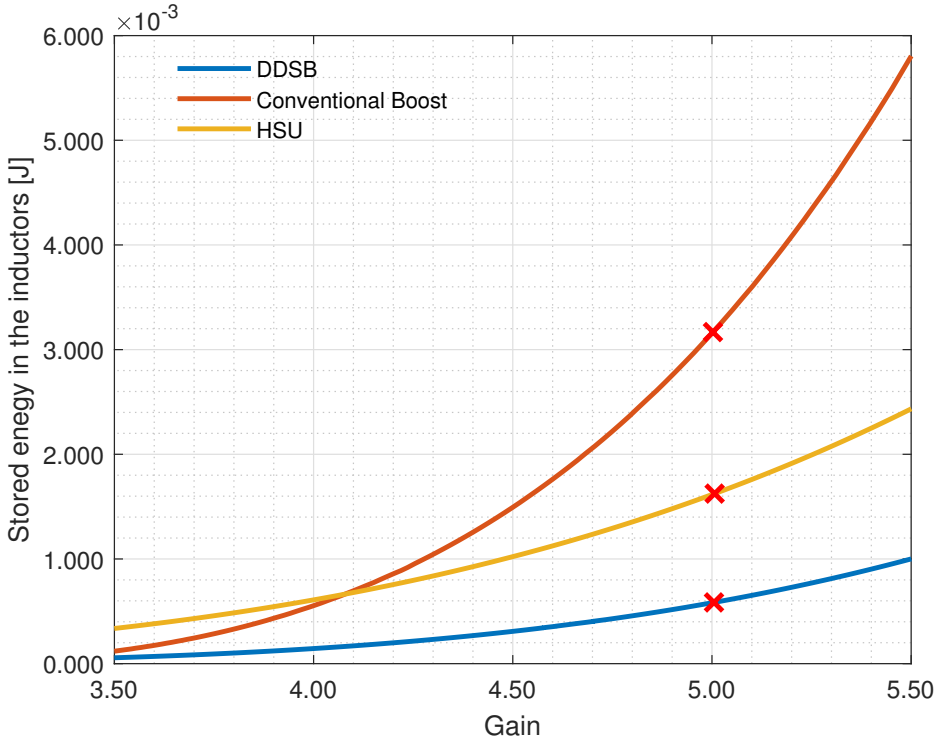

Figure 10. Stored energy in the inductors of the conventional boost and HSU vs. DDSB power converters with respect to the gain ratio.

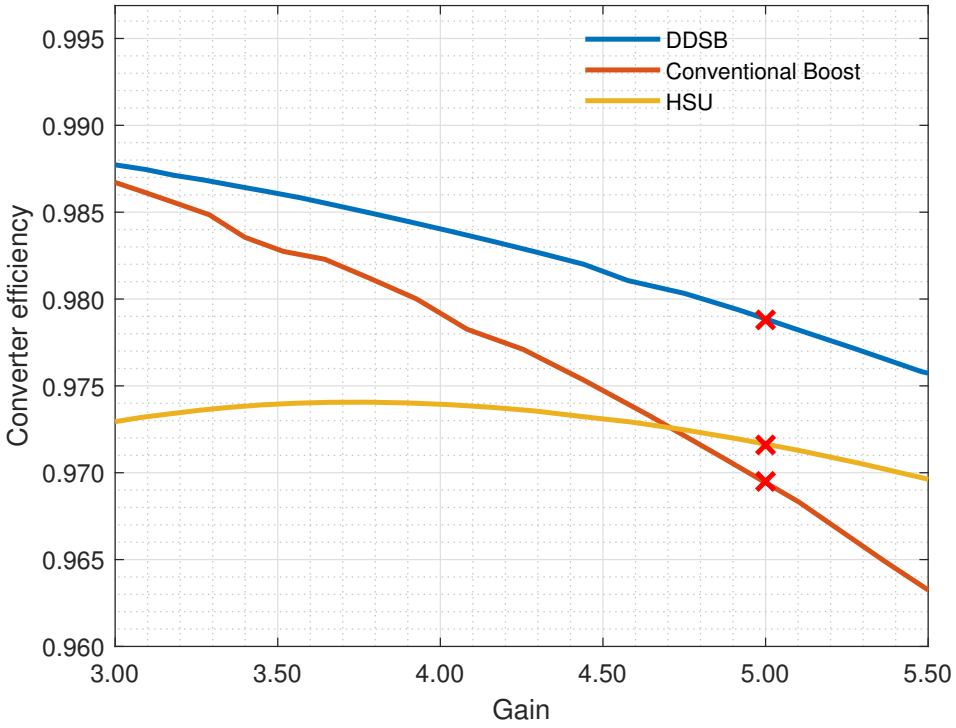

Figure 11. Efficiency of the conventional boost and HSU vs. DDSB power converters, taking into account a fixed load.

4. Experimental Results

To validate the operation of the proposed DDSB power converter, an experimental prototype was built. Its design parameters are indicated in Tables 1 and 4. The converter prototype is depicted in Figure 12. In this section, three main characteristics are validated: (i) validation of the input variables, such as the input current I_g, input voltage V_g, and terminal voltage of transistor $\bar{s}_1$, (ii) validation of the output variables, output current I_o, output voltage V_o, and terminal voltage of transistor $\bar{s}_1$, and (iii) validation of the inductor currents i_{L1} and i_{L2}.

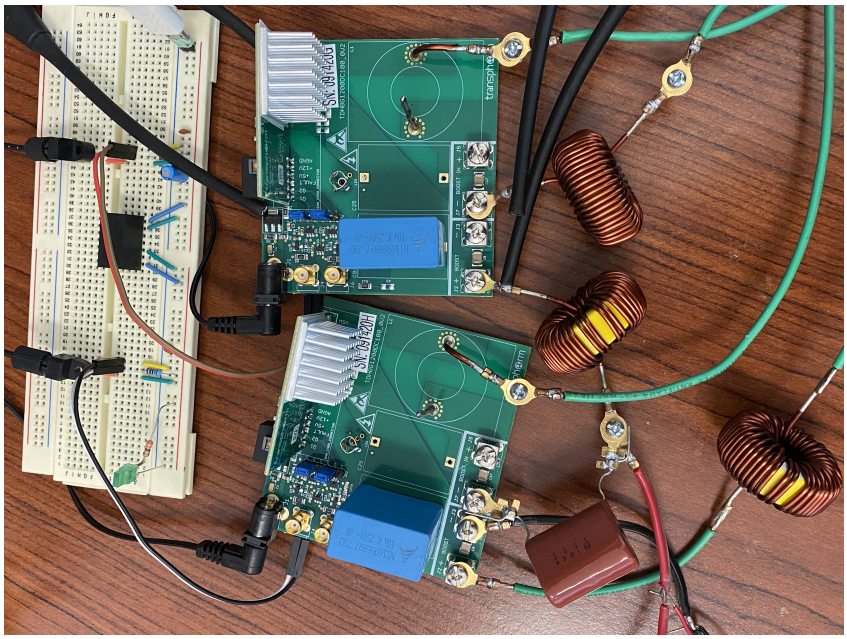

Figure 12. Prototype picture.

4.1. Validation of Input Variables

First, the input voltage V_g, input current I_g, and a single switching signal $\bar{s}_1$ are presented in Figure 13 based on simulation results. Note that while the y-axis for input current is on the left side of Figure 13, the y-axis for input voltage V_g and switching signal $\bar{s}_1$ is on the right side. Similar traces obtained from measurements of the experimental prototype are shown in Figure 14. Traces shown in Figures 13 and 14 feature a reasonable match.

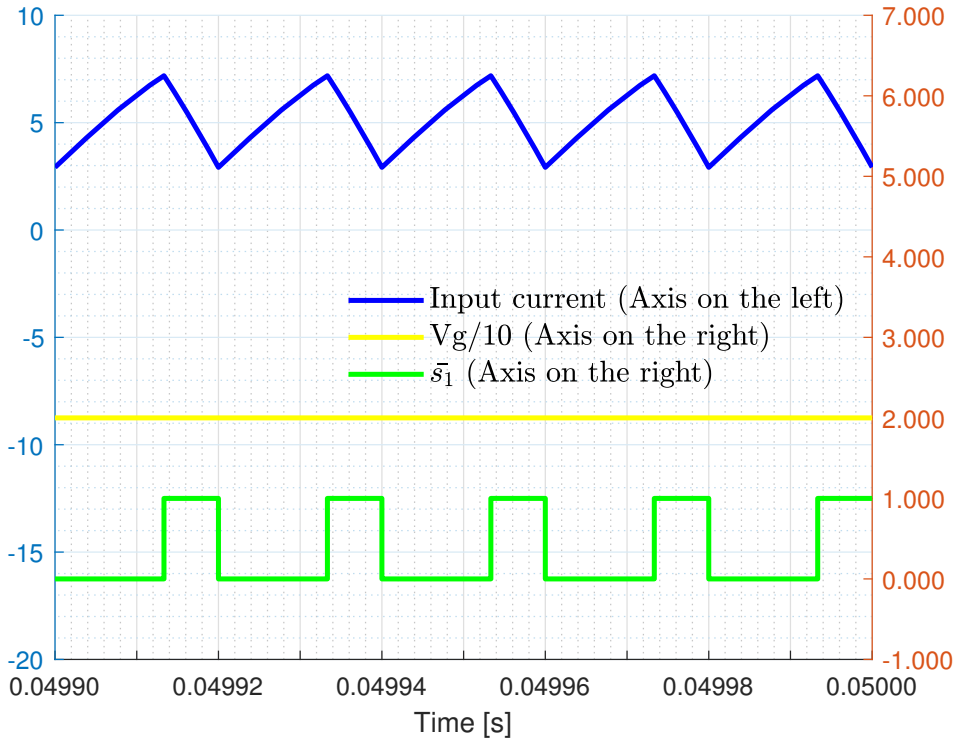

Figure 13. From the top to the bottom: input current I_g (blue trace), input voltage V_g (yellow trace), and switching signal $\bar{s}_1$ (green trace) of DDSB.

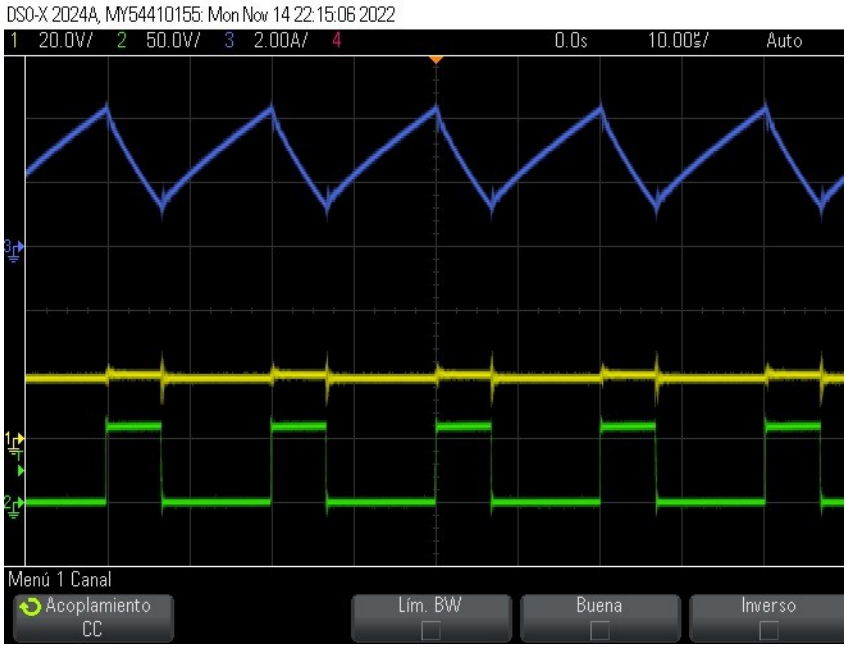

Figure 14. From the top to the bottom: input current I_g (blue trace), input voltage V_g (yellow trace), and terminal voltage of transistor $\bar{s}_1$ = 60 V (green trace) of the DDSB power converter.

4.2. Validation of Output Variables

Measurements of the output voltage V_o, output current I_o, and switching signal s_1 obtained from the simulations results are portrayed in Figure 15. Regarding Figure 15, the input current y-axis is placed on the left side, and the y-axis for the output voltage V_o and switching signal $\bar{s}_1$ are located on the right-side. The output current I_o features a DC offset of 4A.

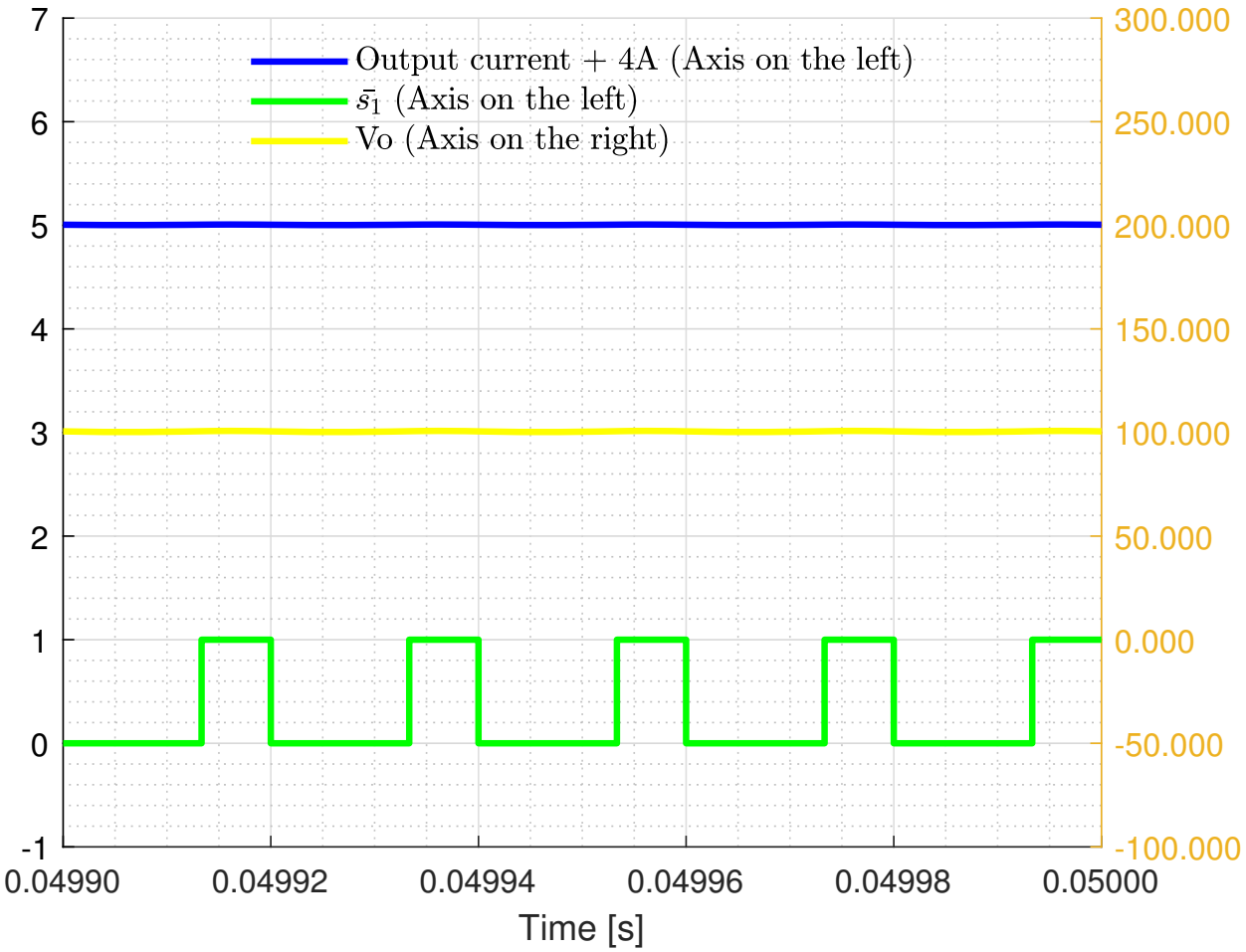

Figure 15. From the top to the bottom: output current I_o (blue trace), output voltage V_o (yellow trace), and switching signal $\bar{s}_1$ (green trace) of DDSB.

In the same fashion, measurements of the output voltage V_o, output current I_o, and terminal voltage of transistor $\bar{s}_1 = 60$ V obtained from the experimental prototype are depicted in Figure 16. By comparing Figures 15 and 16, a good match between the simulation and experimental results is observed.

4.3. Validation of Inductor Currents i_{L1} and i_{L2}

Simulation results of measurements for inductor currents i_{L1} and i_{L2} are shown in Figure 17. An offset of 3A was set to inductor current i_{L1}, while an offset of 2A was set to inductor current i_{L2}. These currents are depicted along with the switching signal $\bar{s}_1$ utilized in former figures. In this case, all y-axes are on the left side of Figure 17.

Similarly, experimental measurements of inductor currents i_{L1} and i_{L2}, as well as the terminal voltage of transistor $\bar{s}_1 = 60$ V, are presented in Figure 18. As shown, a good match is obtained in terms of the average value, current ripple Δi_L, and slopes.

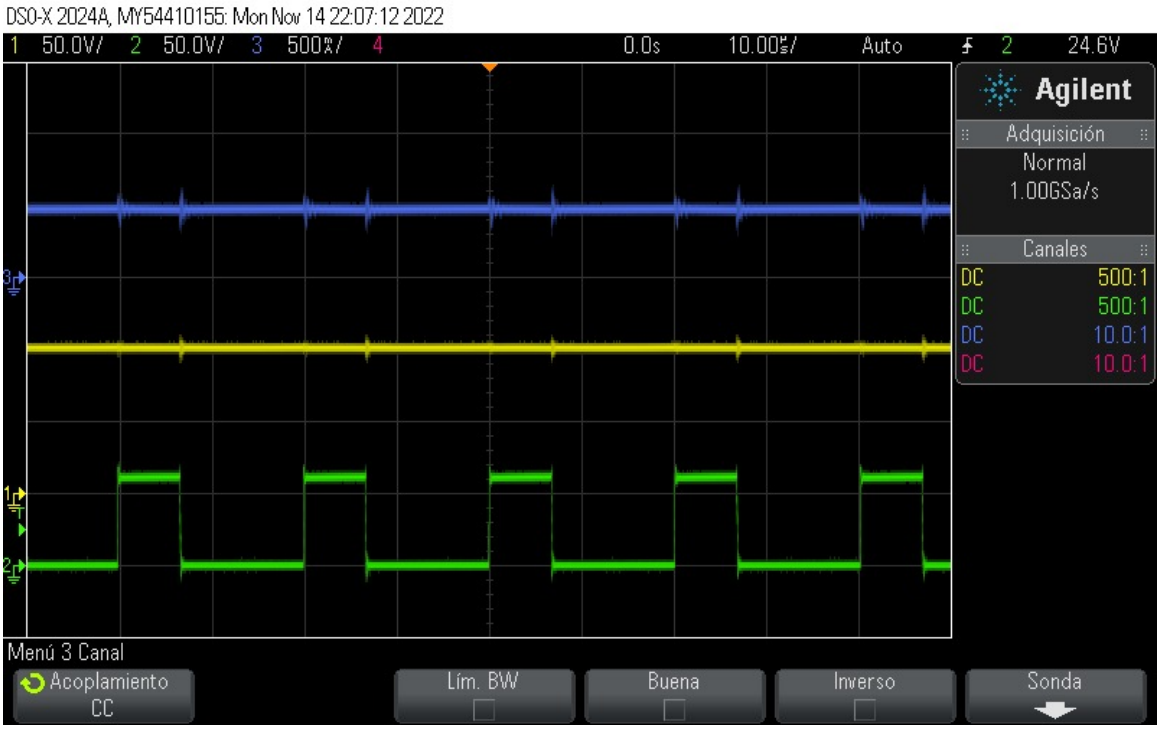

Figure 16. From the top to the bottom: output current I_o (blue trace), output voltage V_o (yellow trace), and terminal voltage of transistor $\bar{s}_1 = 60$ V (green trace) of DDSB.

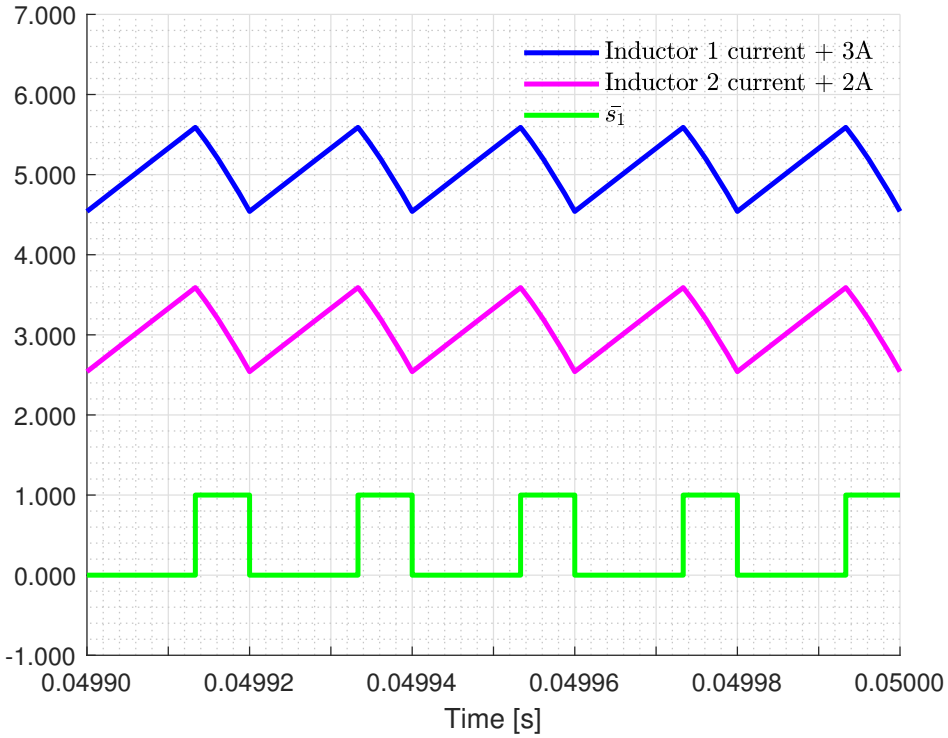

Figure 17. From the top to the bottom: inductor current i_{L1} (blue trace), inductor current i_{L2} (pink trace), and switching signal $\bar{s}_1$ (green trace) of DDSB.

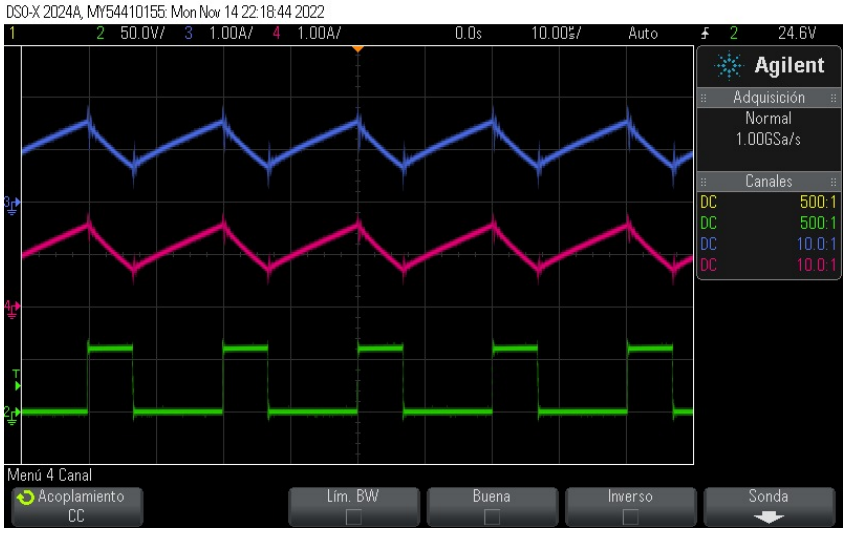

Figure 18. From the top to the bottom: inductor current i_{L1} (blue trace), inductor current i_{L2} (pink trace), and terminal voltage of transistor $\bar{s}_1 = 60$ V (green trace) of DDSB.

5. Conclusions

This paper introduced a dual-switch high step-up DC-DC power converter, called the "DDSB". The particular features of the proposed DDSB are a high step-up voltage gain, relatively low cumulative stored energy over its inductors, low voltage stress on the active switches, and high efficiency even at a relatively high duty ratio. A comparative assessment showed that the DDSB power converter outperforms the conventional boost and the HSU power converters under the same operational conditions, as follows: (i) the DDSB featured a reduction of 14.2% and 1% in the duty ratio to achieve the same output voltage; (ii) the DDSB showed a reduction of 81.25% and 62.50% of stored energy in the inductors with respect to the conventional boost and the HSU, respectively. As a consequence, the physical size of the DDSB was reduced; and (iii) when the conventional boost and the HSU were compared against the DDSB, improvements of 1% and 0.75% in terms of efficiency were obtained, respectively. Furthermore, the principle of operation and the mathematical model of the DDSB were also presented. Finally, experimental results were provided to validate the performance of the proposed converter.

6. Future Work

It would be feasible to conduct further investigations if the constraint of keeping all inductances and capacitances at the same value were released. By doing so, it would be possible to explore alternatives to optimize the power converter's input current and to develop an approach to optimize the energy stored in the converter. Moreover, it could be possible to investigate advanced control techniques applied to this converter and to conduct a sensitivity study in-depth regarding the steady-state time of the DDSB power converter in terms of its inductors, capacitors, and switching frequency. Nevertheless, at this stage, these possible improvements are beyond the scope of this research.

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Abbreviations

The following abbreviations are used in this article:

HSU	high step-up
DDSB	double dual super boost
CCM	continuous conduction mode

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