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Experimental Investigation on SiC MOSFET Turn-Off Power Loss Reduction Using the Current Sink Capacitor Technique

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Abstract: This paper investigates the current sink capacitor technique as a method to minimize the turn-off power losses of SiC MOSFETs operated with zero-voltage switching (ZVS). The method is simple and is based on adding auxiliary capacitors in parallel to the transistors, allowing the sink capacitor to take over part of the channel current, thus limiting the power loss while also advantageously lowering the dv_{ds}/dt ratio. The technique is validated and experimentally studied based on a single-pulse test setup with 1200 V-rated SiC MOSFETs, with several capacitances and gate resistance values, at various switched currents up to roughly 60 A. It is shown that by employing even very small capacitances, in the range of nanofarads, the turn-off power loss can be reduced by over tenfold, with a negligible impact on the volume and complexity of the system. Thus, the presented method can be effectively employed to improve soft-switched power converters.

Keywords: power electronics; power MOSFETs; silicon carbide; switching losses; zero-voltage switching

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1. Introduction

Considering the superior switching performance of SiC MOSFETs compared to their Si counterparts, namely, lower power loss and faster switching speeds, SiC transistors have already been successfully introduced as the power switch of choice in modern power electronics aiming for high efficiency or power density [1–3]. When low-volume solutions are regarded, notable operating frequencies, even in the range of hundreds of kHz, need to be employed [4,5]. Thus, even though the switching losses in SiC devices are already relatively low, they are still a limiting factor for constructing highly compact converters. Hence, soft switching concepts are considered, e.g., in the form of zero-voltage switching (ZVS) [6,7]. Nevertheless, these approaches usually limit the turn-on switching loss only, while the turn-off process, even though it exhibits lower losses in general, is still a substantial hindrance for constructing high-power-density power converters [8–10], as it may lead to enlarged cooling requirements or lower energy efficiencies.

Achieving soft turn-off in SiC MOSFETs to maximize the switching frequency has been a research target for several years now, and a number of publications have presented analytical models for the turn-off process, which also include the impact of stray inductances on switching behavior [9,11–13]. Principally, soft turn-off can be realized via the gate driver [14] or through auxiliary snubber-like circuits in parallel to the switch [15]. The first considered approach is based on the idea that if a specific high current is delivered to the gate during turn-off, the process is largely shortened, and in practice, soft turn-off with minimal power losses is reached [11]. However, as near-short-circuit gate driver currents are required for high-switched MOSFET currents, designing such drivers is a challenging task. Furthermore, this driver behavior leads to extremely fast switching of

the SiC device, leading to colossal dv/dt and di/dt ratios. These, combined with circuit parasitics, even if vastly minimized through the careful design of the power circuit, result in significant issues with EMI generation, as well as increased power losses. However, there are solutions that rely on passive components to improve the switch-off performance, either with conventional RC snubbers [15], more advanced active circuits [16], or streamlined circuits with an auxiliary capacitor as the sole addition [17,18].

Taking into account the simplest solution, with the lowest impact on the volume of the system, a current sink capacitor technique employing an auxiliary capacitor in parallel to the SiC device is considered in this paper. Essentially, the extra capacitor sinks the channel current during the turn-off process and leads to notably reduced turn-off power losses, shorter transition times, and reduced transient overvoltages and oscillations [18]; while the concept has already been presented and analyzed in prior studies, it was either considered for a specific application [18], aimed at more complex circuit structures [16], or focused on modeling while lacking experimental validation with regard to the turn-off loss reduction [17]. To this end, in this paper, a thorough experimental study, taking into account several auxiliary capacitance values, is exhibited, validating the current sink capacitor technique as a general method to minimize the turn-off switching losses of zero-voltage-switched (ZVS) transistors. Therefore, the efficiency of the converters can be maximized, and the cooling requirements for the systems may be lowered.

The article is constructed as follows: After a concise introduction, a theoretical investigation of the turn-off process of SiC MOSFETs with the associated power losses is given in Section 2, focusing on the impact of the suggested current sink capacitor technique. Furthermore, a laboratory test setup is exhibited, along with the experimental study validating the suggested concept. Finally, the paper is concluded in Section 4, establishing the proposed method as a simple technique to limit power losses in ZVS-operated power converters.

2. SiC MOSFET Zero Turn-Off Loss Process Phenomena

The turn-off process of SiC MOSFETs differs from the waveforms described in the literature for traditional Si MOSFETs [19]. This is due to the superior parameters of SiC devices in comparison to Si, in particular, lower junction capacitances [2,20]. To analyze the turn-off of a SiC MOSFET, an equivalent model with a driving circuit included in the transient in-pulse test setup is introduced in Figure 1. Apart from parasitic junction capacitances (C_{gs}, C_{gd}, and C_{ds}), the presented model consists of a MOSFET channel that can be represented as a resistance, $r_{ds(on)}$, voltage-dependent current source described with a transconductance parameter g_{fs} or an open circuit, depending on the stage of the turn-off process. The driving circuit involves gate resistance R_G, which is the sum of the transistor internal and external resistances, and voltage source $V_{(GG)}$, which could take positive and negative values. Additionally, the circuit includes a DC voltage source V_{DC}, freewheeling diode (FWD), and inductor L, as in a standard pulse test arrangement. It is assumed that over the entire examined period, the inductor current I_L takes a constant value.

In the case of a SiC MOSFET, the turn-off waveforms depend on the switching conditions. Three general instances of the turn-off process can be distinguished. The first is a conventional one. In this case, the transistor's voltage v_{ds} rises to the V_{DC} value before the channel current i_{ch} collapses to zero. The second option is a border case in which the voltage v_{ds} reaches V_{DC} and the current i_{ch} reaches zero at the same time. In the last one, the i_{ch} current reaches zero before the v_{ds} voltage rises to the V_{DC} value. The last two of the mentioned cases could be achieved for low R_g and/or a low transistor turn-off current I_L. Moreover, for the second and third instances, the turn-off loss is reduced [11,16,21]. The described cases are depicted in Figure 2a–c.

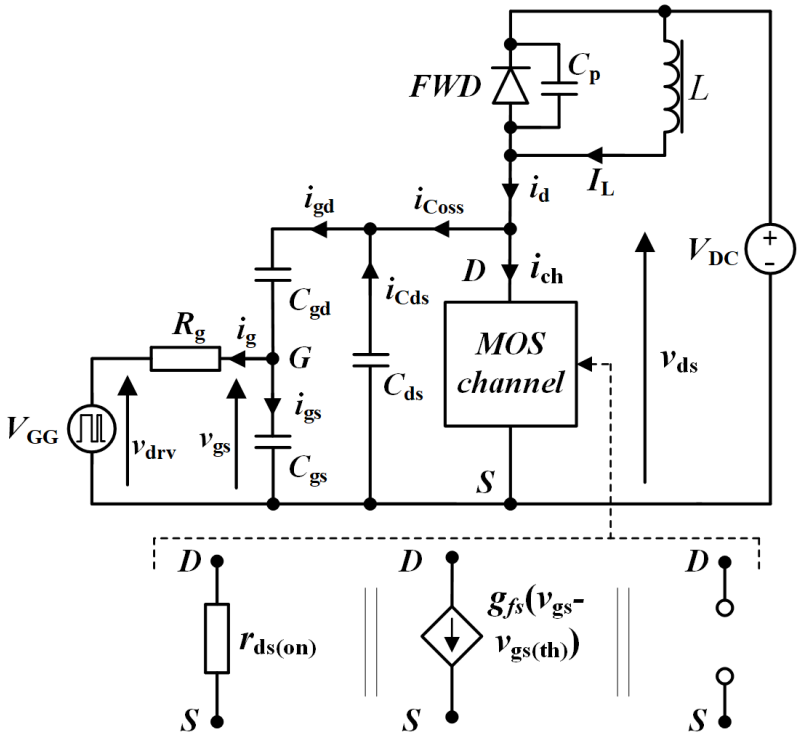

Figure 1. The SiC MOSFET model during turn-off.

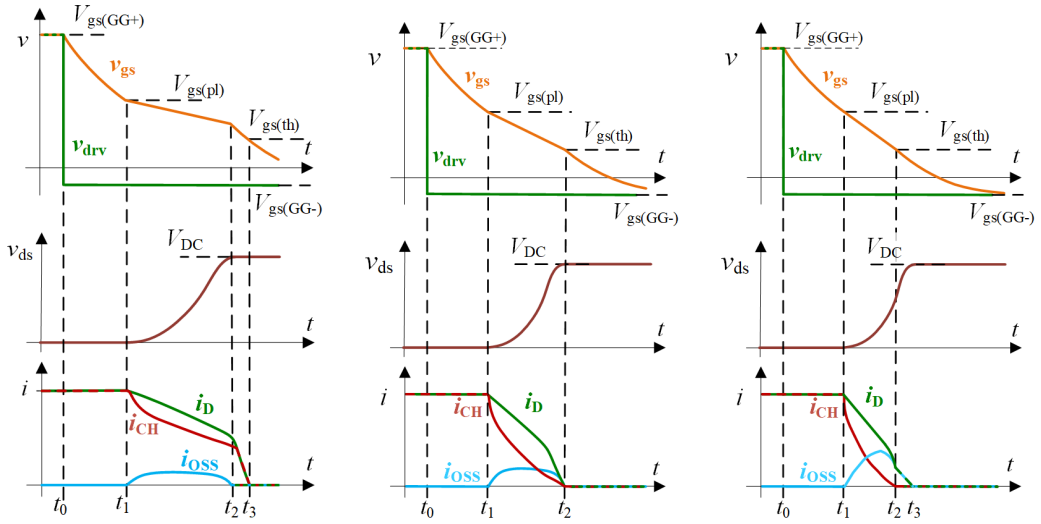

Figure 2. The SiC MOSFET turn-off switching waveforms under different conditions: (**a**) standard turn-off, (**b**) under low current/gate resistance, and (**c**) with additional C_{ds} capacitance.

The turn-off process of an SiC MOSFET begins at the time when the off signal from the master controller is changed, at t_0. The driving voltage source takes a value equal to $V_{gs(GG-)}$ (negative). In all three cases, the gate current i_G charges the input capacitance C_{iss} (the sum of C_{gs} and C_{gd}, where C_{gs} is discharging, and C_{gd} is charging). This interval ends when the gate–source voltage v_{gs} reaches a plateau value $V_{gs(pl)}$ at t_1, which is described as:

$$V_{gs(pl)} = V_{gs(th)} + \frac{I_L}{g_{fs}}, \quad (1)$$

where $V_{gs(th)}$ is the threshold voltage of the MOSFET. After t_1 in each case, the v_{ds} voltage starts to rise with a slew rate, according to the following formula:

$$\frac{dv_{ds}}{dt} = \frac{I_L + g_{fs}(V_{gs(th)} - V_{gs(GG-)})}{C_{oss} + g_{fs}R_G C_{gd}}, \tag{2}$$

where C_{oss} is the output capacitance of the MOSFET (the sum of C_{gd} and C_{ds}). During the voltage rising time (between t_1 and t_2), some parts of the I_L current charge the parasitic capacitance (C_p) of FWD. Therefore, the drain current of the MOSFET i_d decreases (see Figure 2). Simultaneously, the gate current i_g continues charging C_{iss}, as shown below:

$$i_g(t - t_1) = \frac{V_{gs}(t - t_1) - V_{gs(GG-)}}{R_G}. \tag{3}$$

However, unlike in Si MOSFETs, where, in the plateau region, v_{gs} is assumed to be approximately constant, in SiC MOSFETs, because of the lower values of C_{gs}, the voltage v_{gs} decreases during this period. The channel current i_{ch} is controlled via voltage v_{gs}:

$$i_{ch}(t - t_1) = g_{fs}v_{gs}(t - t_1), \tag{4}$$

which also lowers. Nevertheless, in a standard turn-off event, at the end of the voltage rising time, the voltage v_{gs} is above the $V_{gs(th)}$ level. Therefore, after the v_{ds} voltage reaches the value of V_{DC}, i_{ch} is greater than 0. The waveforms presented in Figure 2b,c show a situation with lowered R_g and/or with a low turn-off current I_L. The decreased value of R_g increases the gate current i_g (see Equation (3)), which accelerates the closing of the MOSFET channel. In the case of reduced I_L, a large part of the i_d current flows through the C_{oss} capacitance, which reduces the i_{ch} current and causes it to reach a zero value faster. Therefore, in the cases presented in Figure 2b,c, the v_{gs} voltage reaches the $V_{gs(th)}$ level during the voltage rising time. Consequently, i_{ch} reaches 0 at t_2, which corresponds to the v_{ds} voltage reaching the V_{DC} level (see Figure 2b) or even before the end of the v_{ds} increase (see Figure 2c). In the last stage of the turn-off process (after t_2), the remaining part of i_d falls until it reaches 0. Nonetheless, in the standard case, the i_d current flows through the channel of the transistor (equal i_{ch}) at v_{ds}, even with V_{DC} voltage; as in the case presented in Figure 2b, the i_d current falls to 0 at t_2 (t_3 is equivalent to t_2), and in the case presented in Figure 2c, between t_2 and t_3, i_d is a capacity current equal to i_{oss} under a v_{ds} voltage lower than V_{DC}.

The SiC MOSFET turn-off losses are equal to the integral of the i_{ch} current and v_{ds} voltage during the t_1–t_3 periods, as depicted in the simplified waveforms in Figure 2 and according to Equation (5). Simultaneously, the turn-off losses, following those in Figure 2, may be reduced by shortening the turn-off time using a lower gate resistance. However, shortening the turn-off time increases the $\mathrm{d}v_{ds}/\mathrm{d}t$ and $\mathrm{d}i_{ch}/\mathrm{d}t$ ratios, which leads to enlarged electromagnetic interference (EMI) and transistor voltage overshoots due to parasitic inductances. Moreover, using a low gate resistance also requires a gate driver with high-current capability.

$$E_{off} = \int_{t_1}^{t_3} v_{ds}(t - t_1) \times i_{ch}(t - t_1)\, dt. \tag{5}$$

Finally, the MOSFET turn-off time could be reduced without inducing additional turn-off losses by adding an auxiliary capacitor C_{aux} in parallel to the transistor, as studied further in this paper. In such a circuit, the behaviors of the transistor, parasitic capacitance currents, and transistor voltages are similar to those in normal operation, as shown in Figure 2, albeit with replacing the C_{ds} capacitance as the sum of capacitances C_{ds} and C_{aux}. The auxiliary capacitor C_{aux} takes over part of the transistor current and reduces the $\mathrm{d}v_{ds}/\mathrm{d}t$ ratio, which further leads to lowered turn-off losses, according to Equation (5). Based on the concept that the auxiliary capacitor absorbs part of the transistor current, the technique is named the sink capacitor technique (SCT).

3. Laboratory Model and Experimental Results

To verify the theoretical considerations on reducing turn-off losses by using an additional capacitor connected in parallel to power a MOSFET SiC transistor, a one-pulse laboratory model was built. A simplified schematic of the test setup is shown in Figure 3a, while a photo of the prototype is shown in Figure 3b. To build the laboratory model, 1200 V 40 mΩ SiC MOSFET transistors (MSC040SMA120B4) encapsulated in TO-247-4 were used as the device under testing (DUT) and the freewheeling diode, as they are characterized by low capacitances (C_{iss} = 1990 pF, C_{oss} = 17 pF, and C_{oss} = 156 pF), which is beneficial for the SCT technique, especially considering the output capacitance C_{oss}. Furthermore, the setup consisted of a 62 µH inductor and a gate driver (UCC21750). For testing, a Tektronix oscilloscope (MSO46) with voltage probes (THDP0100; accuracy ± 2%) and a CWT Mini50HF rogowski coil were used for the measurement of the current (a typical accuracy of ±2.0%). Experiments were carried out for the different values of the transistor turn-off currents, gate resistors, and sink capacitors. Specific data on the built one-pulse laboratory test setup are listed in Table 1.

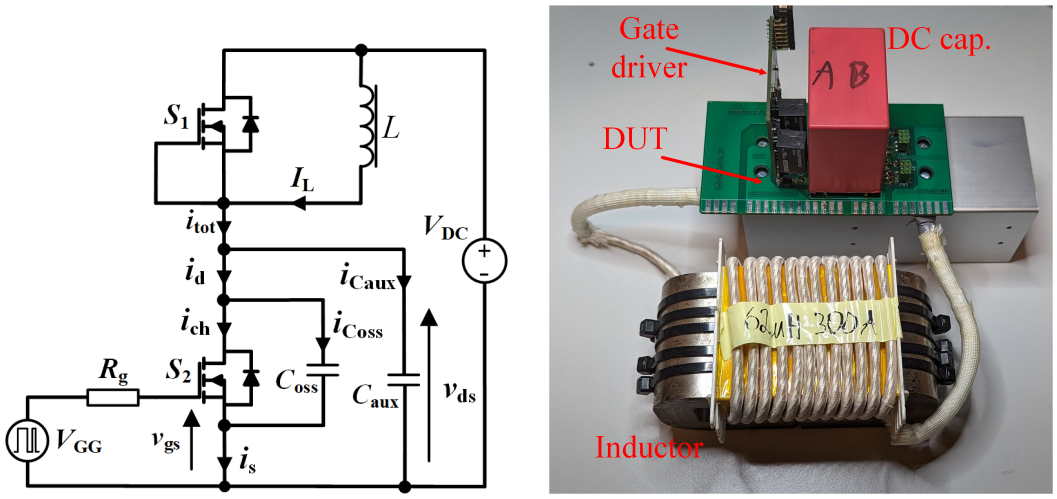

Figure 3. One-pulse test circuits: (**a**) simplified schematic, (**b**) laboratory model.

Table 1. Parameters of the OPT.

Parameter	Value
Transistors S_1 and S_2	MSC040SMA120B4, $V_{ds(bd)}$ = 1200 V
Transistor output capacitance	C_{oss} =156pF at V_{ds} = 1000 V
Transistor internal gate resistance	$R_{g(int)}$ = 1.2 Ω
Inductor	62 µH
Gate driver	UCC21750
External gate resistance R_g	(4.7–47) Ω
Sink capacitance C_{aux}	(0–3) nF
Supply voltage V_{DC}	800 V
Control	DSP STM32H723ZG
Digital oscilloscope	Tektronix MSO46, 350 MHz, 12 bits
Voltage probe	Tektronix THDP0100/100 MHz
Rogowski coil	CWT MiniHF/50 MHz

The testing procedure was as follows: During experiments, transistor S_1 (FWD) was turned off, while transistor S_2 (DUT) was switched via one-pulse signal. When the switch is turned on, the transistor current flows through the voltage source V_{DC}, inductor L, and transistor S_2. The transistor turn-off current is determined using its turn-on time, as the current is proportional to the transistor turning on time, in accordance with Equation (6).

After the transistor turns off, the current flows mainly through inductor L, and the forward-biased body diode of transistor S_1 (until the inductor current reduces to zero). Apart from this, the current flows through the auxiliary C_{aux} and parasitic capacitances of the laboratory model components.

$$I_{S1(off)} = \frac{V_{DC} t_{on}}{L}, \tag{6}$$

where t_{on} is transistor turn-on time.

During testing, the following values were measured and recorded: transistor drain current i_d, transistor drain–source voltage v_{ds}, and transistor gate–source voltage v_{gs}. The experiments were carried out with two different values of sink capacitances C_{aux} = 1 nF and 3 nF, as well as without a sink capacitor. Furthermore, three different external gate resistances $R_g = 4.7\ \Omega, 15\ \Omega, 47\ \Omega$ were considered, as well as a supply voltage of V_{DC} = 800 V, with various transistor turn-off currents, with a maximum current of roughly i_d = 60 A. Four waveforms for two different gate resistance values and two different auxiliary capacitances are shown in Figure 4.

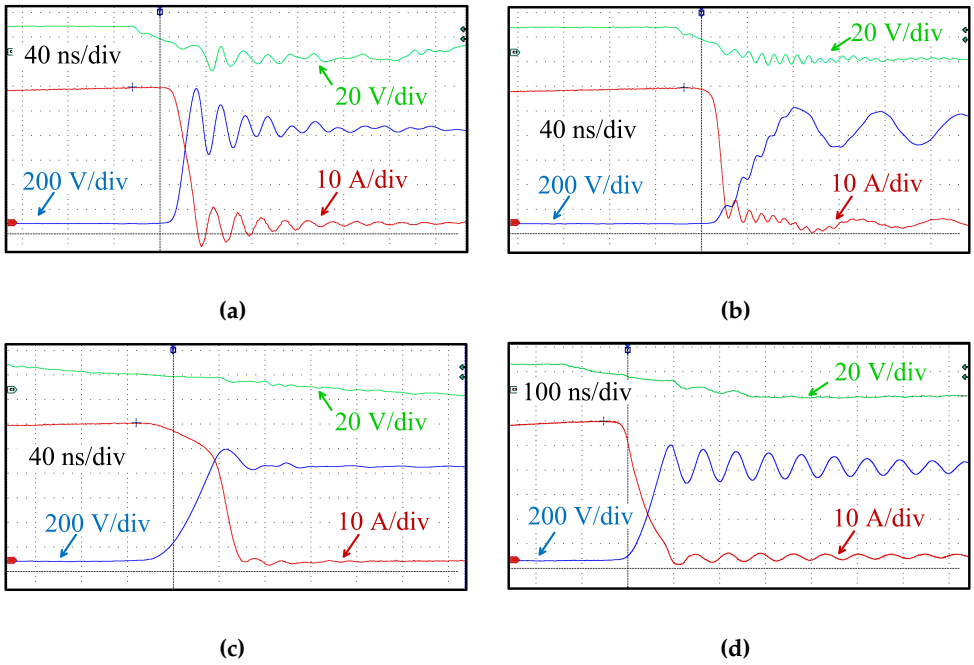

Figure 4. Waveforms of transistor turn-off process for the different values in gate resistance and sink capacitor: (**a**) $R_g = 4.7\ \Omega, C_{aux} = 0$, (**b**) $R_g = 4.7\ \Omega, C_{aux} = 3$ nF, (**c**) $R_g = 47\ \Omega, C_{aux} = 0$, (**d**) $R_g = 47\ \Omega, C_{aux} = 3$ nF.

In accordance with the theoretical analysis, the value of gate resistance exerts a large effect on the v_{ds} voltage rising time (defined as the time required to increase the v_{ds} voltage from 10% to 90% of its steady-state value during the turning off of the transistor). These intervals are approximately 12 ns for $R_g = 4.7\ \Omega$ and roughly 37 ns for $R_g = 47\ \Omega$ in the case without auxiliary capacitance (Figure 4). As can be seen, the voltage rising time depends greatly on the sink capacitor value. For $R_g = 4.7\ \Omega$, due to the use of C_{aux} capacitance, an increase in v_{ds} rising time from 12 ns to 35 ns was observed. Similarly, for $R_g = 47\ \Omega$, the time increases from 37 ns to 48 ns. However, the enlarged v_{ds} voltage rising time using an additional C_{aux} capacitor did not have a negative effect on transistor turn-off losses. On the contrary, these were lowered—the transistor current slope $\mathrm{d}i_{ch}/\mathrm{d}t$ depends not only on the transistor gate circuit but also differs based on whether the sink capacitor is employed or not. When it is used, the transistor current drops to zero faster. Simultaneously, as previously mentioned, using an additional auxiliary capacitance increases the v_ds voltage rising time. These two reasons resulted in lower turn-off losses for the transistor when using the sink capacitor technique,

which is accordance with Equation (5). To prove this, an analysis of transistor turn-off losses, circuit currents, and v_{ds} voltages is presented in the following sections.

Figures 5 and 6 show waveforms obtained via one-pulse laboratory tests and processed using MATLAB 2023b software. Here, the drain current i_d was measured during experiments, while the currents i_{Coss} and i_{Caux} were estimated on the basis of the C_{oss} and C_{aux} capacitances and the measured v_{ds} voltage, according to Equations (7) and (8). The output capacitance i_{Coss} was estimated using the datasheet-based $C_{oss} = f(v_{ds})$ characteristic, taking into account the C_{oss} capacitance dependence on the v_{ds} voltage. Figures 5 and 6 show the results for the gate resistance $R_g = 47\ \Omega$, the two different transistor turn-off currents $i_{d(off)} = (30, 60)$ A, and a circuit with and without sink capacitances ($C_{aux} = (1, 3)$ nF). The turn-off power p_{off} is calculated following Equation (11).

$$i_{Coss} = C_{oss}\frac{\mathrm{d}v_{ds}}{\mathrm{d}t}, \tag{7}$$

$$i_{Caux} = C_{aux}\frac{\mathrm{d}v_{ds}}{\mathrm{d}t}. \tag{8}$$

The channel current i_{ch} is calculated as the difference between the measured i_d current and the estimated i_{Coss} current, as in Equation (9):

$$i_{ch} = i_d - i_{Coss} = i_d - C_{oss}\frac{\mathrm{d}v_{ds}}{\mathrm{d}t}. \tag{9}$$

The sum of the total calculated current is given by:

$$i_{tot} = i_d + i_{Caux} = i_{ch} + i_{Coss} + i_{Caux} = i_{ch} + (C_{oss} + C_{aux})\frac{\mathrm{d}v_{ds}}{\mathrm{d}t}. \tag{10}$$

Turn-off power p_{off} is calculated in accordance with Equation (11):

$$p_{off} = i_{ch}v_{ds}. \tag{11}$$

As depicted in Figure 5, transistor S_2 turn-off losses decrease with an increasing value in the C_{aux} capacitance and decrease with transistor turn-off currents. Moreover, a higher value of C_{aux} leads to reduced $\mathrm{d}v_{ds}/\mathrm{d}t$ and $\mathrm{d}i_{ch}/\mathrm{d}t$ ratios. The change in the current shape mainly occurs during the increase in the v_{ds} voltage. For example, for a case without a sink capacitor C_{aux} and a transistor turn-off current equal to 60 A, the current during the process of increasing voltage v_{ds} increases from 0 to 800 V and the transistor channel current i_{ch} reduces from 56 A to 45 A. However, for sink capacitances C_{aux} equal to 1 nF and 3 nF, the established current variances were from 59 A to 24 A and 57 A to 3 A, respectively. That difference in transistor i_{ch} current reduction causes a substantial effect on turn-off losses.

Figure 5 shows the transistor v_{ds} voltage and measured and estimated currents. For the analyzed cases, it can be stated that there is a minor influence of the employed sink capacitance on the shape of the current i_{tot}. However, the value of the capacitance is crucial considering the value of the capacitance current i_{Caux}. Thus, during commutation, the channel current i_{ch} changes significantly, according to Equation (10). Simply, the sink capacitance takes over part of the transistor current during turning off, lowering the channel current, and as the channel current is the crucial source of power losses [22], these are also advantageously limited. However, a notable drawback of the described technique for achieving soft switching behavior is the excessive ringing of the v_{ds} voltage after the turn-off process has resolved. This is caused by a resonance between the capacitances of the power semiconductor devices and the sink capacitance and the parasitic inductances inevitably apparent in the circuit, e.g., because of the connections. The resonant currents, as shown in Figure 5, are of notable values. For example, considering a case with $C_{aux} = 3$ nF, the current overshoots exceeded 50% of the switched currents. Nevertheless, these currents can be eliminated through conventional snubber circuits [15,19].

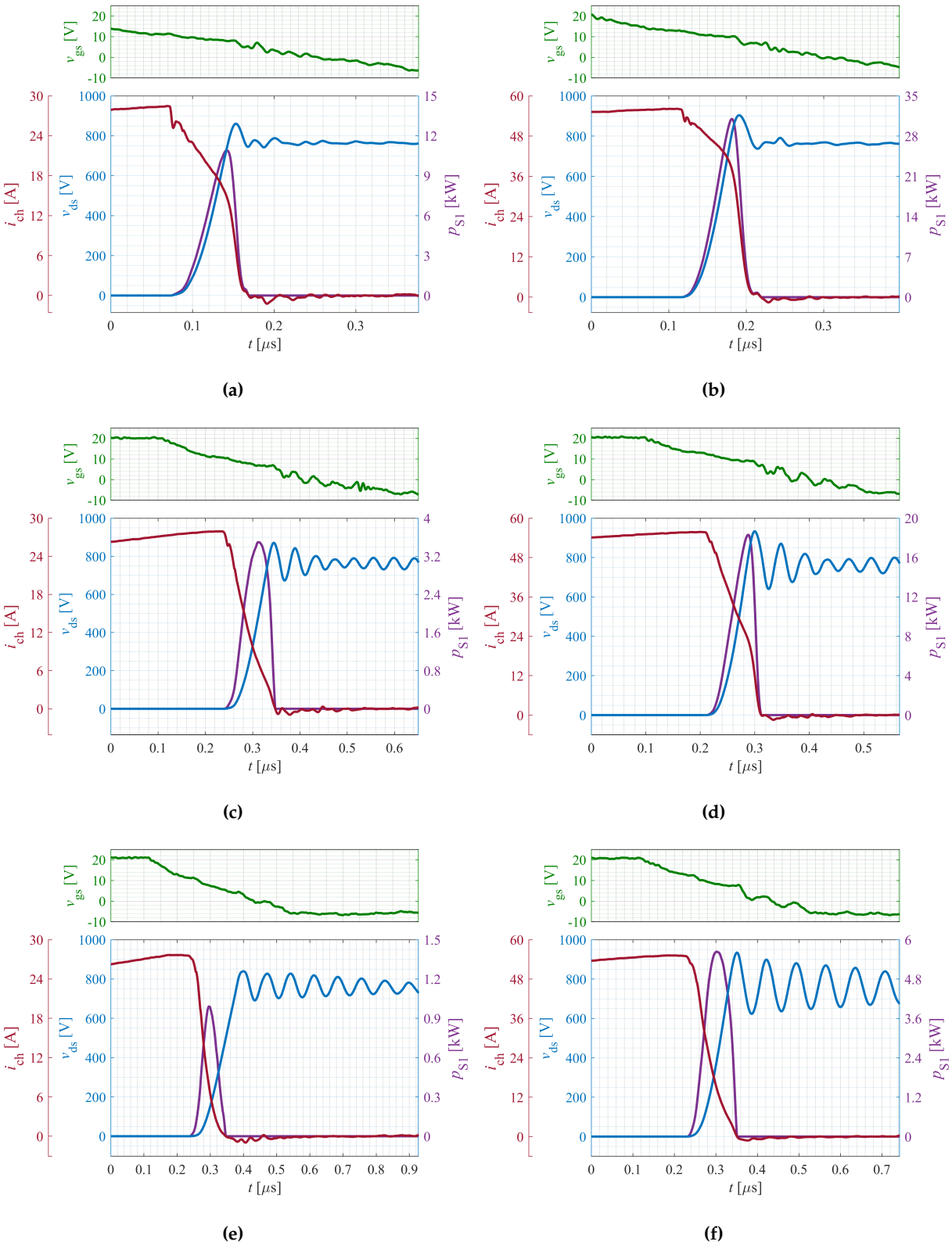

Figure 5. Transistor v_{gs} (green) and v_{ds}(blue) voltages, i_{ch} (red) current and p_{S1} power (violet) during turn-off process for $R_g = 47\ \Omega$; different values of current and sink capacitor: (**a**) $i_d = 30$ A, $C_{aux} = 0$, (**b**) $i_d = 60$ A, $C_{aux} = 0$, (**c**) $i_d = 30$ A, $C_{aux} = 1$ nF, (**d**) $i_d = 60$ A, $C_{aux} = 1$ nF, (**e**) $i_d = 30$ A, $C_{aux} = 3$ nF, (**f**) $i_d = 60$ A, $C_{aux} = 3$ nF.

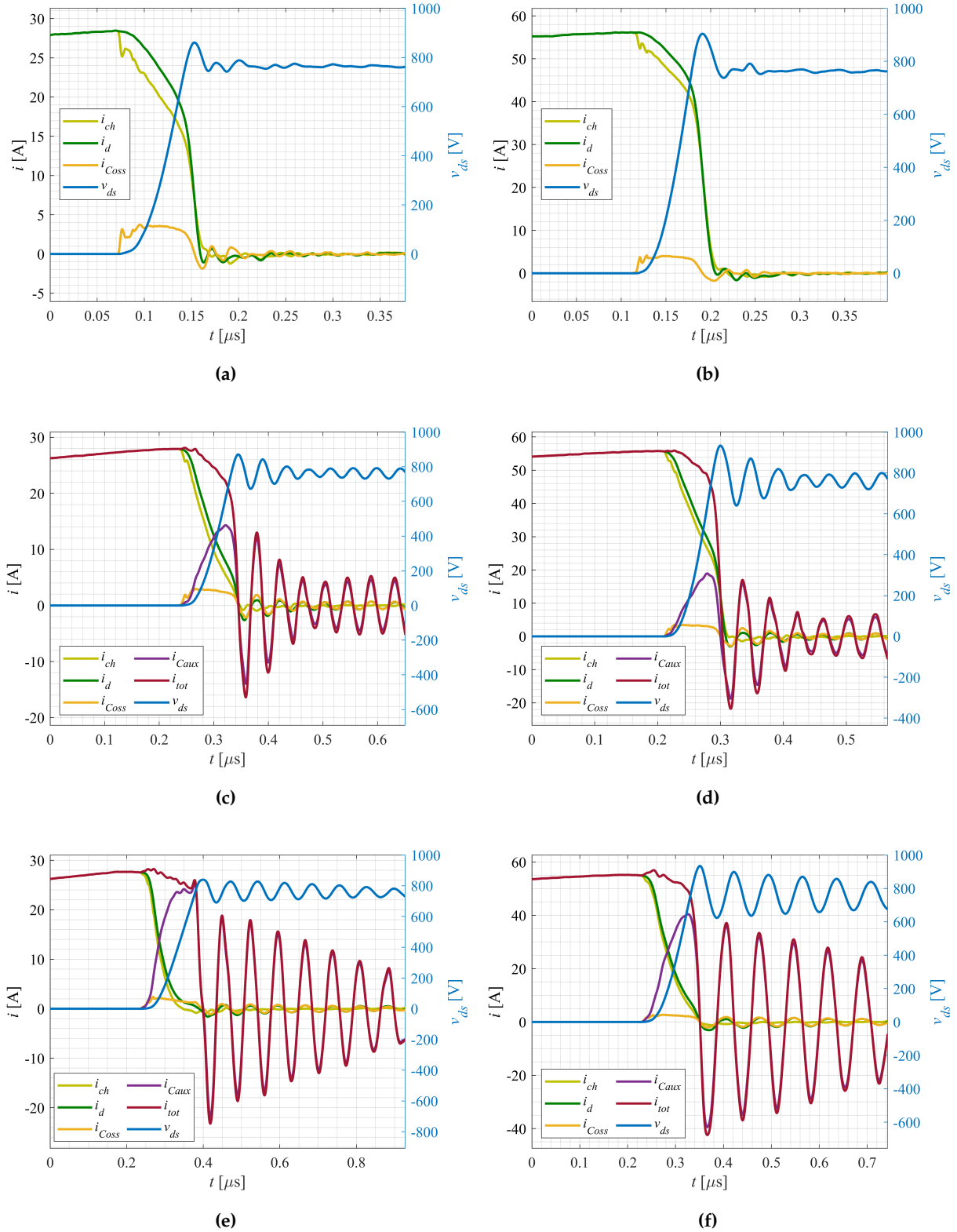

Figure 6. One-pulse test circuit currents and v_{ds} voltage during transistor turn-off process for $R_g = 47\ \Omega$; different current and auxiliary capacitor values: (**a**) $i_d = 30$ A, $C_{aux} = 0$, (**b**) $i_d = 60$ A, $C_{aux} = 0$, (**c**) $i_d = 30$ A, $C_{aux} = 1$ nF, (**d**) $i_d = 60$ A, $C_{aux} = 1$ nF, (**e**) $i_d = 30$ A, $C_{aux} = 3$ nF, (**f**) $i_d = 60$ A, $C_{aux} = 3$ nF.

A power loss comparison is depicted in Figure 7. Here, the turn-off losses are shown for three values of gate resistance R_g, with and without two different sink capacitances C_{aux}, as well as for three different switched currents. For a case with a 60 A turn-off switched current and the highest considered gate resistance $Rg = 47\ \Omega$, the turn-off losses are $E_{off} = 1173$ µJ with the sink capacitor C_{aux}, and 826 µJ and 430 µJ for auxiliary capacitance C_{aux} at 1 nF and 3 nF, respectively. For the smallest tested gate resistance $Rg = 4.7\ \Omega$, the losses for different capacitance values are 136 µJ, 32 µJ, and 13 µJ. When a sink capacitor $C_{aux} = 3$ nF was employed for the experiment with a gate resistance of $Rg = 47\ \Omega$, a turn-off power loss reduction by slightly over threefold was achieved. For the identical sink capacitance used for the test with $Rg = 4.7\ \Omega$, the loss reduction was higher than tenfold. The proportions between the turn-off losses for different configurations are similar for the three studied switched currents and two tested gate resistances $Rg = 4.7\ \Omega$ and $Rg = 15\ \Omega$. This was not the case for $Rg = 47\ \Omega$, as for such a high gate resistance, the transistor's channel current is still higher than zero, even though the voltage V_{ds} has already reached its nominal value (case depicted in Figure 2a). All in all, as shown based on the experiments, the current sink capacitor technique can be effectively employed to diminish the turn-off power losses to a great extent.

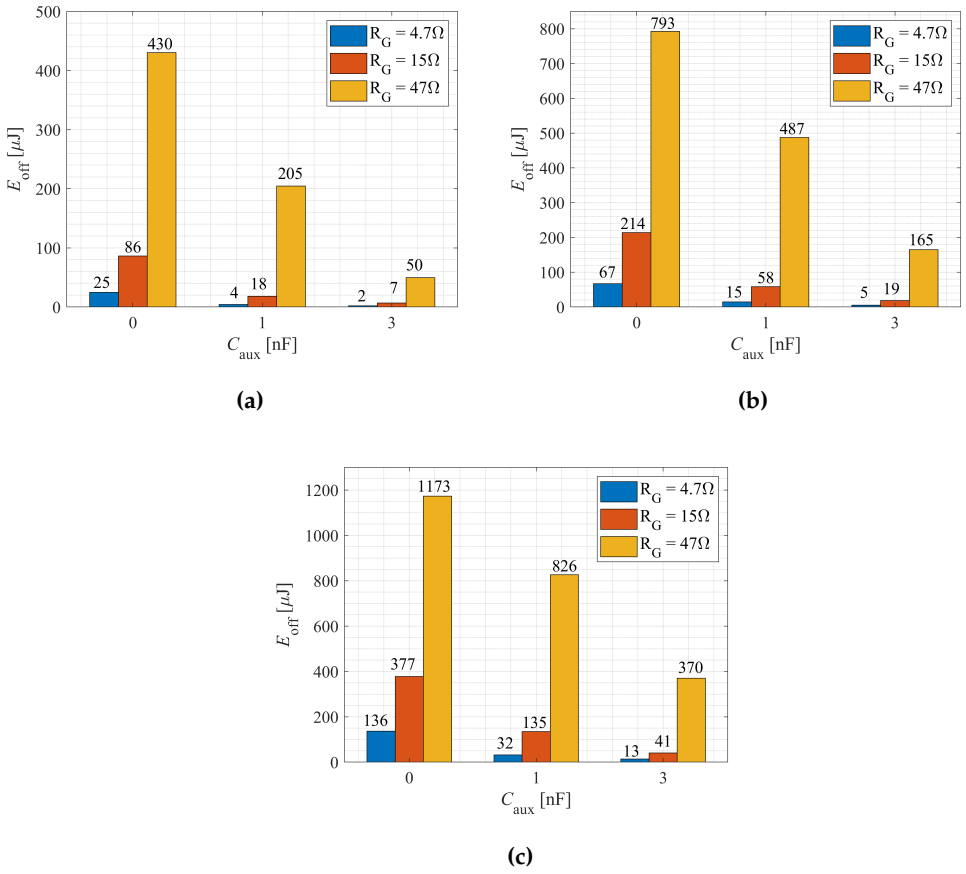

Figure 7. Transistor turn-off loss comparison for different turn-off currents: (**a**) $i_d = 30$ A, (**b**) $i_d = 45$ A, (**c**) $i_d = 60$ A.

4. Discussion

In [17], the authors state that the soft turn-off limit of the transistor is reached when, during the turn-off process, the channel current reaches zero and the voltage v_{ds} equals the supply voltage value (800 V in the conducted studies) at the same moment. This scenario is illustrated in Figure 5c. However, as demonstrated based on the experimental study, additional increases in capacitance or decreases in the gate resistor value beyond the suggested soft turn-off limit in [17] allowed for a further reduction in turn-off losses. In

Figure 7a, for the considered critical case, the turn-off losses were 205 µJ; reducing the gate resistor from $Rg = 47\ \Omega$ to $Rg = 15\ \Omega$ and $Rg = 4.7\ \Omega$ enabled a significant reduction in turn-off losses to 18 µJ and 4 µJ, respectively. Similarly, increasing the sink capacitor from $C_{aux} = 1$ nF to $C_{aux} = 3$ nF resulted in a decrease in losses from 205 µJ to 50 µJ. Thus, the choice of optimal current sink capacitance is not trivial.

Fully appropriate and accurate models of the turn-off process of SiC MOSFETs have still not been presented in the literature, as taking into account all parasitic elements present in the circuit and the various phenomena still hindering SiC MOSFETs, such as charge traps [23] or drain-induced barrier lowering (DIBL) [24], is a very challenging task [20,21]. Therefore, we recommend an experimental approach to choosing the proper capacitance value. Considering that the single-pulse test setup is very simple to arrange and experiment with and that many engineers perform such tests prior to designing full converters to estimate the power losses anyway, conducting transistor turn-off tests for various sink capacitors in real-world circuits would help to establish the optimal capacitance for each specific application.

5. Conclusions

In this paper, an experimental study on turn-off power loss reduction employing a small auxiliary capacitor connected in parallel to the transistor is conducted. The described current sink capacitor technique is aimed at circuits operating with ZVS switching, e.g., converters controlled with triangular current mode (TCM) or a quasi-square wave (QSW). Based on experiments with 1200 V SiC MOSFETs, it is shown that applying the current sink capacitor technique, a turn-off power loss reduction of over tenfold can be attained. The scale of the improvement is highly dependent on the gate resistance, as well as the value of the sink capacitor. Furthermore, to maximize the power loss reduction potential, the technique should be used with advanced gate drivers with high-current capability.

In summary, the technique can be effectively used to minimize the turn-off power losses by a substantial value. The method is especially attractive as it is very simple and requires only very small capacitors, with values in the range of single nanofarads, e.g., C0G SMD capacitors could be employed. Thus, considering whole power converters, the volume increase is essentially negligible, thereby limiting the impact of the converter's power density. Therefore, using the current sink capacitor technique may be deemed beneficial for constructing high-performing, high-power-density soft-switched converters.

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