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Enhanced Four-Level Active Nested Neutral Point-Clamped Inverter

Charles Ikechukwu Odeh [1,*], Arkadiusz Lewicki [1], Marcin Morawiec [1] and Andrzej Jąderko [2]

[1] Department of Electric Drives and Energy Conversion, Faculty of Electrical and Control Engineering, Gdansk University of Technology, ul. Narutowicza 11/12, 80-233 Gdansk, Poland; arkadiusz.lewicki@pg.edu.pl (A.L.); marcin.morawiec@pg.edu.pl (M.M.)

[2] Faculty of Electrical Engineering, Czestochowa University of Technology, 42-201 Czestochowa, Poland; aj@el.pcz.czest.pl

* Correspondence: charles.odeh@pg.edu.pl; Tel.: +48-88-319-8735

Abstract: The classical four-level nested neutral point-clamped (4L NNPC) inverter-leg is a hybrid of the flying-capacitor and diode-clamped 4L-inverter-leg configurations. Though uniform reduced voltage stress (1/3 of input voltage) on constituting switches is evident in the 4L NNPC inverter-leg, trails of the drawbacks of the diode-clamping concept still exist. With the significantly rated off-the-shelf IGBT switch modules (6.5 kV, 1200 A), chances of deployment of the newly evolved Four-Level Nested T-Type inverter (4L NTTI) in certain applications is high. Compared with the classical 4L NNPC inverter, 4L NTTI involves a smaller number of power switches and low conduction losses. However, in 4L NTTI, two of the six active switches have a blocking voltage rating of 2/3 of the input voltage. Considering this limiting topological feature in 4L NTTI, a six-switch inverter-leg for the four-level active neutral point-clamped (4L ANNPC) inverter is presented in this paper. In the proposed 4L ANNPC inverter-leg, only one switch has a voltage stress of 2/3 of the input voltage. This ameliorated voltage stress translates to low-cost and -loss inverter implementation. The operational characteristics and competitiveness of the 4L ANNPC inverter are analyzed in detail and demonstrated with a prototype.

Keywords: blocking voltage; multilevel inverter; sinusoidal pulse-width modulation; total harmonic distortion

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1. Introduction

The proliferation of power electronics power and control circuit configurations is evidence of the much-sought global quest for 'greener' energy harvest and judicious utilization. In this context, single-source multilevel inverter (SSMLI) configurations are among the most deployed power-conditioning circuit configurations. This is because of their innate provision of a range of qualitative output waveform parameters and the convenience in the provision of the lone input DC voltage source [1]. This source is popularly obtained from front-end rectifiers [2–4] and collated renewable energy sources in a battery bank [5,6]. Classical SSMLI topologies are diode-clamped and flying-capacitor, FC, and MLIs. Topological features, controls, and applications of these conventional MLIs have been well documented in the literature [1,7]. The first series of these MLIs are the popular 3-level, neutral point-clamped (3L NPC) versions of the respective MLI [6–9]. The popular variant of the 3-level diode-clamped inverter is the 3-level T-type inverter [10,11], wherein the two clamping diodes have been actively replaced by a bidirectional switch. These 3-level inverter configurations have been widely used in industries for the past years and can be picked off the shelf.

Even though conventional SSMLIs with output voltage levels beyond three still maintain uniform reduced voltage stress on the constituting power devices, such configurations have the inherent pronounced drawback of an excessive number of power circuit component counts. The need for higher output voltage levels is justified in view of the overall

power-conditioning system's operating voltage magnitude and inverters' output voltage quality. A higher number of output voltage levels translates to a qualitative output voltage waveform with less total harmonic distortion, THD, and value. In response to this need, four-level MLI power circuit configurations that depict certain improved topological features have been reported in the literature [12–14]. These improvements stem from a mix of the topological features of the classical SSMLIs. In some of these, the active-clamping concept has been entrenched.

In [12], the single-input voltage source was split by three series-connected capacitor banks with two mid-points. In each phase, two bidirectional switches were used to actively clamp these mid-points to the corresponding output phase node, depicting a compact π-shaped four-level inverter power circuit with six switches. However, this inverter has undue varying voltage stresses on the constituting power switches. The three pairs of switches have blocking voltage ratings of full, two-third, and one-third of the input DC voltage value. Modification of conventional 4-level FC MLI is seen in [13], wherein the 4-level hybrid-clamped inverter (4L-HC) configuration was presented. The supposed high-voltage capacitor near the DC-link in classical FC MLI is replaced by two clamping switches. Reduced uniform voltage stress on the power switches and the existence of many redundant switching states [15] (for ease of balancing the DC-link and flying-capacitor voltages) are the good features of the 4L-HC. But these features go with an extra two power switches in each phase of 4L-HC (eight switches) when compared with the conventional SSMLIs (six switches). Enhancement of 4L-HC was performed in [14]. Therein, a 4-Level active neutral point-clamped (4L ANPC) inverter was presented, which removed the flying-capacitor in each inverter-leg in view of deployment in high-power, medium-voltage applications. The trade-off for this removal is the increased blocking voltage rating of some of the constituting power switches. In 4L ANPC, four out of the eight power switches have to be rated at $2V_{dc}/3$; V_{dc} is the input voltage.

With the distinct hybridization concept, the work in [16] presented a four-level nested neutral point-clamped (4L NNPC) inverter.

A lower number of flying-capacitors and clamping diodes were nested in each inverter-leg alongside the supposed six active power switches, as shown in Figure 1a. These switches have the same voltage rating, as in the classical SSMLIs, $V_{dc}/3$. Thus, the 4L NNPC's power circuit features are very attractive for high-power and medium-voltage applications. Space vector modulation (SVM) [17], sinusoidal pulse-width modulation (SPWM) [18,19], and model predictive [20,21] control schemes have been developed for 4L NNPC. An elaborate 4L NNPC was presented in [22] with targeted application in the marine propulsion system. Such dedicated application comes with an increased component count.

The four-level nested T-type inverter (4L NTTI) in [23] yielded a more compact configuration for the 4L NNPC. Therein, the two inner-most active switches in Figure 1a formed a joint bidirectional switch that clamps the mid-point of the flying-capacitors to the inverter-leg output node, as shown in Figure 1b. This led to the removal of the passive clamping diodes in Figure 1a. However, the $V_{dc}/3$ voltage stress rating of the two power switches in Figure 1a is increased to a voltage stress of $2V_{dc}/3$ in Figure 1b.

It is glaring in Figure 1b that two switches have voltage stress ratings of $2V_{dc}/3$. But, in the proposed four-level active nested neutral point-clamped, 4L ANNPC, the power circuit in Figure 1c, this number is reduced. In this inverter-leg topology, just one switch has a $2V_{dc}/3$ voltage stress rating; the rest of the switches have ratings of $V_{dc}/3$. This feature of the 4L ANNPC inverter paves the way for a significant reduction in the inverter loss and cost when viewed alongside the power circuits in Figure 1a,b.

This paper is organized and sectioned as follows. The inverter configuration, principle of operation, and control/modulation scheme are presented in Section 2. In Section 3, the 4-level inverter variants (4L NNPC, 4L NTTI, and 4L ANNPC) are compared with respect to two operational features: cost and loss performances. The penultimate section presents the validating simulation and experimental results.

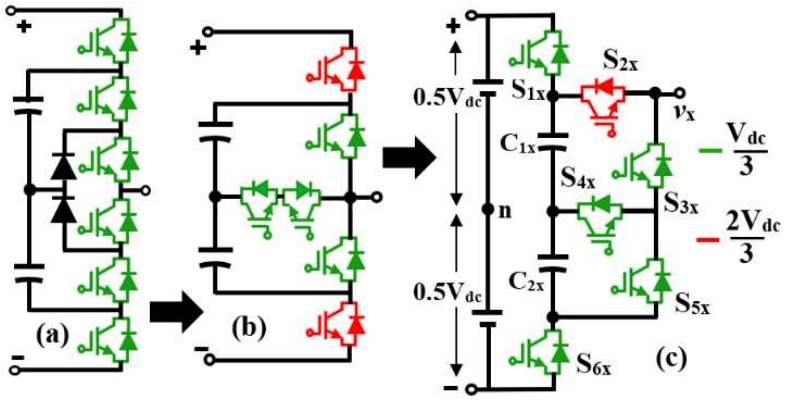

Figure 1. Inverter-legs of the 4L nested neutral point-clamped inverters in (**a**) [16], (**b**) [23], (**c**) Proposed.

2. Proposed 4L, 3-Phase Active Nested Neutral Point-Clamped (4L ANNPC) Inverter

Based on the configuration feature of the proposed inverter-leg, a sequence of the available inverter switching states is tabulated, and an SPWM scheme is used in the switching signals syntheses. The modulation approach developed for the 4L NNPC inverter is well suited for the proposed 4L ANNPC inverter. Thus, the simplified SPWM control scheme in [18] is used to properly regulate and balance the flying-capacitors' voltages in Figure 1c.

A. *Power Circuit of the 3-phase, 4L ANNPC Inverter*

Shown in Figure 1c is the 4L ANNPC inverter-leg. As in Figure 1a,b, the voltage across each of the two series flying-capacitors (C_{1x} and C_{2x}; x is the phase notations: a, b, c) is $V_{dc}/3$; where V_{dc} is the input DC-link. Topologically, the proposed inverter-leg is equivalent to the power circuits in Figure 1a,b, and hence, it can generate four output voltages: $V_{dc}/2$, $V_{dc}/6$, $-V_{dc}/6$, and $-V_{dc}/2$ with reference to the mid-point, n, of the input DC-link. The power switches have 3-switch combinations that synthesize these inverter-leg output voltages; these switching combinations and corresponding leg voltages are shown in Table 1. Three pairs of switches are complementary: $S_{6x} = \overline{S_{1x}}$, $S_{3x} = \overline{S_{2x}}$, and $S_{5x} = \overline{S_{4x}}$.

Table 1. The 3-switch combinations and generated inverter-leg voltages of the 4L ANNPC.

s/n	Switching State Combinations						v_{xn}	Output Level L_x	State RS_x
	S_{1x}	S_{2x}	S_{3x}	S_{4x}	S_{5x}	S_{6x}			
1	1	1	0	1	0	0	$0.5V_{dc}$	3	3
2	1	0	1	1	0	0	$\frac{V_{dc}}{6}$	2	2B
3	0	1	0	1	0	1			2A
4	1	0	1	0	1	0	$-\frac{V_{dc}}{6}$	1	1B
5	0	0	1	1	0	1			1A
6	0	0	1	0	1	1	$-0.5V_{dc}$	0	0

In this table, values of v_{xn} ($-V_{dc}/2$, $-V_{dc}/6$, $V_{dc}/6$, and $V_{dc}/2$) are arbitrarily tagged with corresponding positive integers (0, 1, 2, and 3) to depict the generated inverter-leg output voltage level, L_x. The synthesis of $-V_{dc}/6$ or $V_{dc}/6$ involves a pair of redundant switching combinations, whereas only one switching combination exists for the generation of either $-V_{dc}/2$ or $V_{dc}/2$. This existence and non-existence of redundant switching states, RS_x, in the inverter-leg output voltage level, L_x, is reflected in the last column of Table 1, where the letters A and B are used to denote the two redundant switching states in output voltage levels 1 and 2. Observing from Table 1 and Figure 1c, it is clear that it is just S_{2x} that has a peak voltage stress rating of $2V_{dc}/3$; the rest of the switches have a peak blocking

voltage of $V_{dc}/3$ each. The three-phase power circuit of the 4L ANNPC inverter is shown in Figure 2.

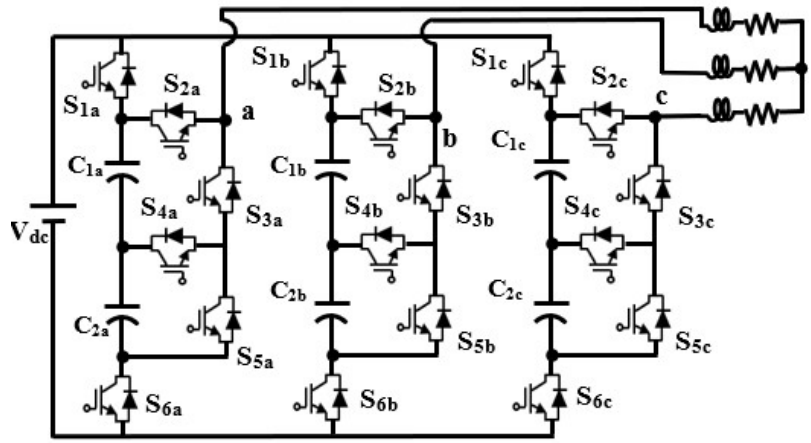

Figure 2. The 3-phase, 4-level active nested neutral point-clamped inverter 4L ANNPC.

B. *Effects of the switching states on capacitor voltages*

In Table 1, the possible ON/OFF switching state combinations in each of the 4L ANNPC inverter-legs are shown. Each of the 6-row switch combinations has a varying effect on the voltage status of the two nested capacitor voltages (v_{C1x}, v_{C2x}), depending on the direction of the corresponding phase current, i_x. Current flow out of the inverter-leg output node is considered positive and negative otherwise. The actual inverter-leg power circuit status for each of these switching state combinations is shown in Figure 3, where each switch comprises active IGBT (T) and passive anti-parallel diode (D). OFF switches are represented by the corresponding anti-parallel diode. From Table 1, rows 1 and 6 switching states are typified in Figure 3a,b, corresponding to states (RS_x) 3 and 0. For both positive and negative flows of i_x, the IGBTs and diodes in the respective current path are indicated. Capacitors C_{1x} and C_{2x} are not involved in either of these current paths, and hence, their voltages (v_{C1x} and v_{C2x}) are not affected.

The synthesis of voltage level $-V_{dc}/6$ involves two redundant switching states: RS_x equals 1A and 1B, corresponding to rows 5 and 4 in Table 1. The operational power circuit status of states 1A and 1B are shown in Figures 3c and 3d, respectively. In Figure 3c, the indicated semiconductor devices in the paths of i_x show that for the positive direction of i_x, C_{2x} is discharged (v_{C2x} decreases); for negative current direction, C_{2x} is charged (v_{C2x} increases); for both current directions, C_{1x} is not involved (v_{C1x} cannot be increased or decreased by state 1A).

For Figure 3d, it can be deduced that in state 1B, positive and negative directions of i_x have equal effects of charging (increasing v_{C1x}, v_{C2x}) and discharging (decreasing v_{C1x}, v_{C2x}) the two series capacitors. Also, the use of the two redundant switching states 2A and 2B in rows 3 and 2 of Table 1 have varying effects on v_{C1x} and v_{C2x} during the synthesis of the $V_{dc}/6$ output voltage level. The two switching conditions are visualized in Figure 3e,f. Just as in state 1B, positive and negative current directions have equal charging (increasing v_{C1x}, v_{C2x}) and discharging (decreasing v_{C1x}, v_{C2x}) effects, C_{1x} and C_{2x}, in state 2A. Considering state 2B, the positive direction of i_x charges C_{1x} (v_{C1x} increases), while the negative current direction discharges C_{1x} (v_{C1x} decreases). For both current directions, C_{2x} is not involved (v_{C2x} cannot be increased or decreased by state 2B). Table 2 summarizes these effects.

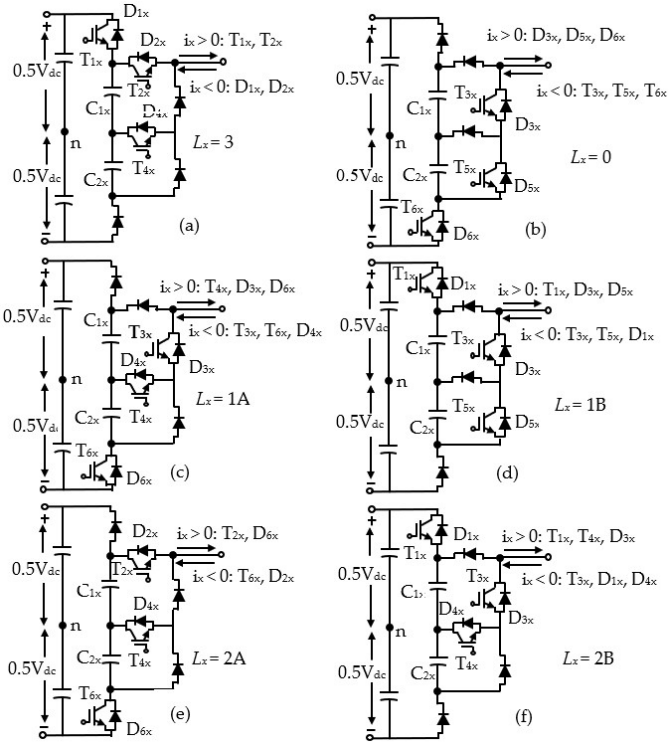

Figure 3. Effects of switching states combinations and inverter-leg current on v_{Cx1} and v_{Cx2}. (**a**) State 3, (**b**) State 0, (**c**) State 1A, (**d**) State 1B, (**e**) State 2A, (**f**) State 2B.

Table 2. Effects of switching states and inverter-leg current directions on the flying-capacitors' voltages.

v_{xn}	L_x	State RS_x	Effects on the Flying-Capacitor Voltages	
			v_{C1x}	v_{C2x}
$0.5V_{dc}$	3	3	No effect	No effect
$\frac{V_{dc}}{6}$	2	2B	Charge ($i_x > 0$)	No effect
			Discharge ($i_x < 0$)	No effect
		2A	Discharge ($i_x > 0$)	Discharge ($i_x > 0$)
			Charge ($i_x < 0$)	Charge ($i_x < 0$)
$-\frac{V_{dc}}{6}$	1	1B	Charge ($i_x > 0$)	Charge ($i_x > 0$)
			Discharge ($i_x < 0$)	Discharge ($i_x < 0$)
		1A	No effect	Discharge ($i_x > 0$)
			No effect	Charge ($i_x < 0$)
$-0.5V_{dc}$	0	0	No effect	No effect

C. *SPWM strategy for the proposed 4L ANNPC inverter*

For proper synthesis of the inverter-leg 4L staircase waveform, the reference voltage for the flying-capacitors' voltages should be $V_{dc}/3$. In real operation, the actual capacitors' voltages have the propensity of deviating significantly from this desired reference voltage value. The respective differences between the actual capacitors' voltages $(v_{Cxi}; i = 1, 2)$ and the reference voltage, $V_{dc}/3$, determine the capacitor voltage deviations, Δv_{Cxi}, in each of the inverter-legs; that is,

$$\Delta v_{Cxi} = v_{Cxi} - V_{dc}/3 \tag{1}$$

In relation to the 'charge' and 'discharge' entries in Table 2,

$$\text{'charge'} = -\Delta v_{Cxi} \tag{2}$$

$$\text{'discharge'} = \Delta v_{Cxi} \tag{3}$$

Referring to Table 2, it can be seen that proper generation of the $V_{dc}/6$ voltage level demands guided choice in choosing the states 2A and 2B. The same goes for the choice of 1A and 1B in generating the $-V_{dc}/6$ voltage level. Such choices are made based on the concept that for either $V_{dc}/6$ or $-V_{dc}/6$ voltage level generation, a switching state should be selected that discharges the capacitor if Δv_{Cxi} is positive. Else, if a capacitor voltage deviation is negative, a switching state should be selected that charges the capacitor. However, owing to the innate series connection of the capacitors, this concept does not hold absolutely. This is because some states, RS_x, entail simultaneous charging or discharging of the capacitors in each inverter-leg, whereas some have no effect on one capacitor but at the same time charge or discharge the other capacitor. Therefore, there is then the need to consider the series capacitors as two groups of capacitors alongside the redundant states, RS_x. This grouping is facilitated by the inherent trend in Table 2. Irrespective of the direction of the inverter-leg current (i_x) in Table 2, states 2A and 2B always have a reverse effect on v_{Cx1}, whereas states 1A and 1B always have a reverse effect on v_{Cx2}. Thus, v_{Cx1} with states 2A and 2B is considered as a group; the other group is v_{Cx2} with states 1A and 1B. Substituting (from (2) and (3)) Δv_{Cx1} and $-\Delta v_{Cx1}$ for 'discharge' and 'charge' in Table 2 and considering separately the effects on groups v_{Cx1} and v_{Cx2}, it can be deduced that:

i. Whenever the product of $\pm\Delta v_{Cx1}$ and $\pm i_x$ turns out to be negative, state 2B should be selected to balance v_{Cx1}; that is $-\Delta v_{Cx1} * i_x$ or $\Delta v_{Cx1} * -i_x$
ii. If the product of $\pm\Delta v_{Cx1}$ and $\pm i_x$ is positive, state 2A should be selected to balance v_{Cx1}; that is $\Delta v_{Cx1} * i_x$ or $-\Delta v_{Cx1} * -i_x$
iii. If the product of $\pm\Delta v_{Cx2}$ and $\pm i_x$ turns out to be negative, state 1B should be selected to balance v_{Cx2}; that is $-\Delta v_{Cx2} * i_x$ or $\Delta v_{Cx2} * -i_x$
iv. If the product of $\pm\Delta v_{Cx2}$ and $\pm i_x$ is positive, state 1A should be selected to balance v_{Cx2}; that is $\Delta v_{Cx2} * i_x$ or $-\Delta v_{Cx2} * -i_x$

These selection criteria are summarized in Table 3. With these switching conditions, v_{Cx1} and v_{Cx2} are controllable irrespective of the direction of the inverter-leg current, i_x.

Table 3. (**A**) Selection criteria for balancing v_{Cx1}; (**B**) Selection criteria for balancing v_{Cx2}.

(**A**)		
L_x	$\Delta v_{Cx1} * i_x$	RS_x that balances v_{Cx1}
2	<0	2B
	>0	2A
(**B**)		
L_x	$\Delta v_{Cx2} * i_x$	RS_x that balances v_{Cx2}
1	<0	1B
	>0	1A

A commensurate single-carrier *SPWM* scheme, shown in Figure 4, is developed for the synthesis of the switches' gating signals in each inverter-leg.

The base reference sine waveforms are given as:

$$v_a = msin(\omega t) \tag{4a}$$

$$v_b = msin(\omega t - 2\pi/3) \tag{4b}$$

$$v_c = msin(\omega t + 2\pi/3) \tag{4c}$$

where m is the modulation index ($0 < m < 1.1547$).

The inclusion of the zero-sequence component, v_0, (following the min–max function concept) to v_a, v_b, and v_c enhances the modulation index range; that is

$$v_0 = -0.5\{\max(v_a, v_b, v_c) + \min(v_a, v_b, v_c)\} \tag{5}$$

$$v_{a0} = v_a + v_0 \tag{6a}$$

$$v_{b0} = v_b + v_0 \tag{6b}$$

$$v_{c0} = v_c + v_0 \tag{6c}$$

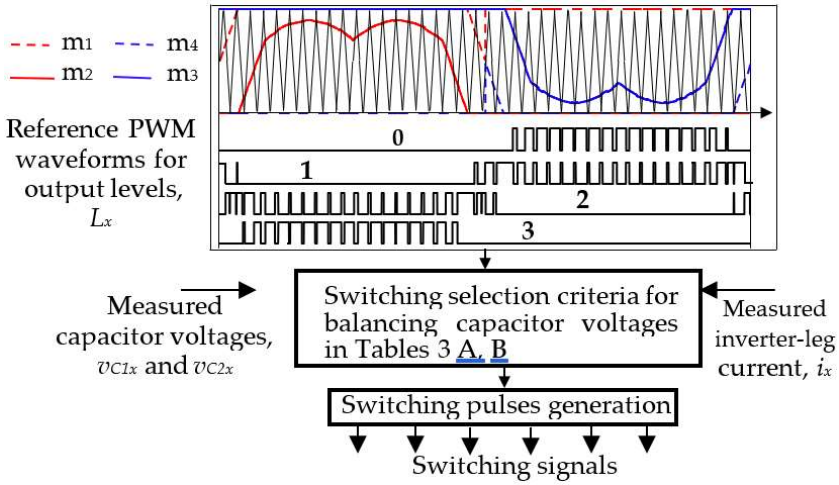

Figure 4. Control steps in each phase of the 4L ANNPC inverter.

In each inverter-leg, the four control signals m_1, m_2, m_3, and m_4 in Figure 4 are synthesized from the respective reference phase waveform. In Figure 5, such synthesis is typified for phase 'a'.

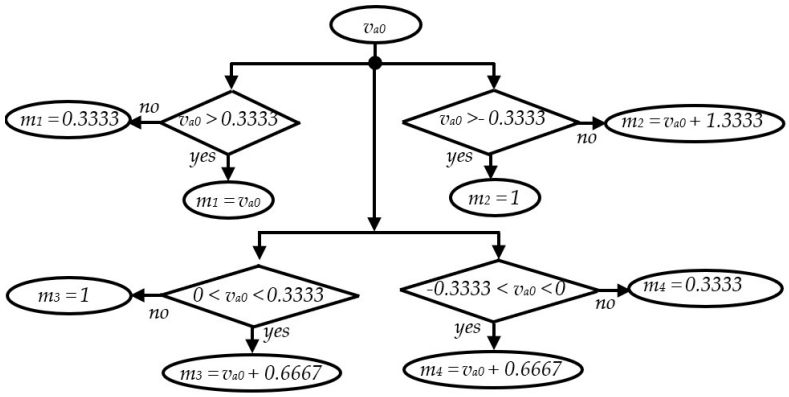

Figure 5. Generation of the four control signals m_1, m_2, m_3, and m_4 in phase 'a'.

The reference PWM waveforms, L_x, for output voltage levels 0, 1, 2, and 3 (these voltage levels are depicted in Tables 1 and 2) are generated by appropriate comparisons of control signals m_1, m_2, m_3, and m_4 with the single triangular carrier, T. With real-time values of the phase current i_x and capacitor banks' voltages, these trains of reference PWM waveforms (L_x) dictate the trend of generating the power switches' gating pulses, after due consideration of the switching selection conditions for balancing the capacitor voltages in Table 3A,B. The overall control steps in each phase of the inverter are depicted in Figure 4.

3. Comparison of Cost Evaluations and Loss Performances

In order to provide clues into the pros and cons of the 4L inverter power circuits in Figure 1, there is a need to probe into their respective cost involvements and operational loss incurrences. Thus, the inverter-leg configurations are compared based on these two performance indices. Medium-voltage power switch modules and their gate drivers are considered. The same *SPWM* scheme and capacitor voltage balancing approach were used in controlling each inverter topology. Similarly, the considered inverter power circuits have equal system parameters.

A. *Four-level inverter-legs cost evaluations and comparison*

Regarding high-power, medium-voltage applications, cost estimations and comparisons of inverter-legs in Figure 1 with the parameters shown in Table 4 are carried out. The costs of switch modules, diodes, and gate drivers are considered in these evaluations. Arbitrarily, Infineon-made power switch modules are considered in these estimations. The results are shown in Table 5.

Table 4. System parameters for the considered 4-level inverter configurations.

Parameter	Value
Inverter rating	4 MVA
DC-link voltage, V_{dc}	4.5 kV
Switching frequency, f	3.3 kHz
Blocking voltage of switches	1.5 kV and 3 kV
RL load	3.56 Ω, 2 mH
Modulation index	0.6 to 1

Table 5. Cost comparison of 4-level inverter-leg variants with semiconductor devices made by Infineon.

Devices	4L NNPC in [16]		T-Type Variant in [23]		Proposed 4L ANNPC	
	No.	Price ($)	No.	Price ($)	No.	Price ($)
FZ1200R17HE4 1700 V, 1200 A IGBT	6	3958	4	2639	5	3299
FZ1200R33HE3 3300 V, 1200 A IGBT	0	0	2	3346	1	1673
DD1200S17H4_B2 1700 V, 1200 A diode	2	1885	0	0	0	0
2ED300C17-S Gate driver	3	764	3	764	3	764
Cost summation		6607		6749		5736

The cost estimation (excluding tax) of the devices in Table 5 is based on the price list from one of the worldwide top-ranked semiconductor vendors (Digi-key corporation). Inverter-leg cost evaluations in this table reveal that the 4L ANNPC inverter in [23] has the highest cost involvement, whereas the proposed enhanced 4L ANNPC inverter has the least cost among the trio. The cost of a leg of the proposed inverter topology is reduced to about 15% and 13.18% in comparison to the 4L-inverter-legs in [16,23], respectively. The bidirectional switch in Figure 1b functions as switches S_{3x} and S_{4x} in Figure 1c (4L ANNPC); the common node (emitters) has been split. S_{3x} and S_{4x} have a voltage stress rating of $V_{dc}/3$. Also, switch S_{5x} in Figure 1b,c has equal voltage stress to $V_{dc}/3$. Hence, the obvious difference in these power circuits is the swapping of the voltage stresses of switches S_{1x}, S_{2x}, and S_{6x}. In Figure 1b, S_{1x}, S_{2x}, and S_{6x} have blocking voltages of $2V_{dc}/3$, $V_{dc}/3$, and $2V_{dc}/3$, respectively. Correspondingly, in Figure 1c, these voltage stresses are now $V_{dc}/3$, $2V_{dc}/3$, and $V_{dc}/3$ for switches S_{1x}, S_{2x}, and S_{6x}. Consequently, only one switch has a blocking voltage of $2V_{dc}/3$ in Figure 1c as compared to two in Figure 1b. Hence, for the 4.5 kV input DC voltage, the convincing approach of the cost estimations has been demonstrated with switch modules of 1700 V and 3300 V voltage ratings and of an equal 1200 A current rating. The difference in the cost estimations of inverter-legs in Figure 1b,c is because in Figure 1c, there is a reduction in the voltage stress rating of one power switch module. Modules' voltage stress ratings vary directly with their cost. On the other hand, the additional cost of two clamping diodes significantly outweighs the effect of the reduced costs of low-voltage-rated switches in Figure 1a.

B. *Four-level inverter-legs loss computations and comparison*

The PSIM simulation package was used in the computations of power losses in the semiconductor devices. PSIM thermal modules were deployed; the parameters of modules were obtained from the datasheets provided by Infineon for DD1200S17H4_B2, FZ1200R17HE4, and FZ1200R33HE3 switch modules (Germany, Munich, Theresienhöhe 11A, Infineon). Entries in Table 4 were used in the PSIM simulation models of the 4-level inverters. The conduction losses in the IGBT and anti-parallel diode are summed up to determine the conduction loss for each switch module.

Similar computation and module loss assignment is performed for the turn-on and turn-off switching losses. The explained control scheme in Section 2(c) has been used equally on the three 4L-inverter-legs in view of obtaining a fair, balanced loss comparison.

Displayed in Figure 6 are the plots of variations of conduction and switching losses for the switch modules in the 4L-inverter-leg configurations with respect to the system modulation index, m, defined as

$$m = \sqrt{3} v_{ref} / V_{dc} \tag{7}$$

where v_{ref} is the magnitude of the inverter-leg voltage reference, and V_{dc} is the DC-link voltage; m values of 0.6 to 1 were considered in the loss computations.

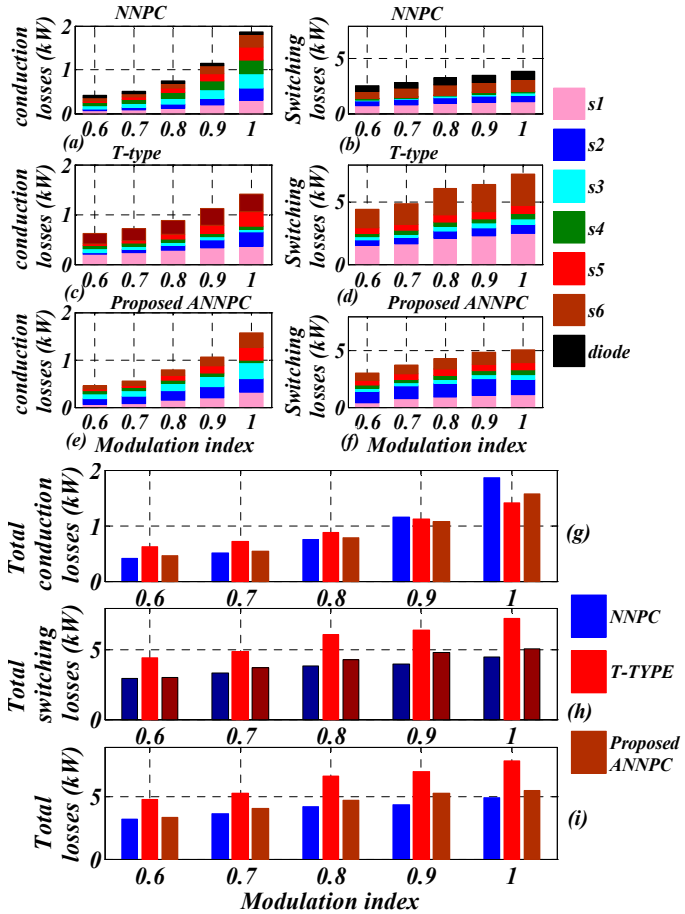

Figure 6. Conduction, switching, and total losses of the 4L-inverter-legs. (**a**,**b**) NNPC in [16]; (**c**,**d**) T-type in [23]; (**e**,**f**) Proposed ANNPC; (**g**) Total conduction losses; (**h**) Total switching losses; (**i**) Total losses.

Figure 6a,c,e shows that the inverter-leg power circuit presented in [16] leads in the computed conduction loss values. These losses were mainly dissipated in the six IGBT modules; the two clamping diodes incur only about 3% of these losses at an m value of 1. The T-type 4L-inverter-leg in [23] has the lowest conduction loss value. For the considered modulation index range, the trend of the total conduction losses in the three 4L-inverter-legs is shown in Figure 6g.

Computations of the switch modules' switching losses hinge on their turn-on and turn-off switching losses and the turn-on energy loss equations provided in (8).

$$P_{sw-on} = (E_{on} * f) * \frac{V_{dc}}{V_{cc\_datasheet}} \tag{8a}$$

$$P_{sw-off} = (E_{off} * f) * \frac{V_{dc}}{V_{cc\_datasheet}} \tag{8b}$$

$$E_{on},\ E_{off} = \int V_{CE}(t) * i_C(t)dt \tag{8c}$$

where E_{on}/E_{off} is the switch turn-on/turn-off energy loss; $V_{cc\_datasheet}$ is the DC bus voltage in the E_{on}/E_{off} characteristics of the datasheet, defined as 'DC bus voltage' in the test conditions; V_{CE} is the collector-Emitter voltage; and i_C is the collector current. From Table 4 and extracted datasheet characteristics of the two switch modules used, f, V_{dc} and $V_{cc\_datasheet}$ are common constant parameters to both modules. Hence, the clear difference in the computed switching losses in these switches is their E_{on}/E_{off} values, as can be deduced from Equation (8c). V_{CE} voltage values of these two switch modules are responsible for the differences in the computed switching loss values in the considered inverter-leg variants. As evidenced in Figure 6b,d,f, the T-type 4L-inverter-leg has the highest switching loss values among the trio. In this inverter-leg, the two outer switches (S_{1x} and S_{6x}) with voltage stress of $2V_{dc}/3$ dissipate over 78% of the inverter-leg's switching losses for the specified range of m. The proposed 4L ANNPC inverter-leg ranks second, dissipating about 69.5% of the maximum dissipated T-type 4L-inverter-leg switching losses; Figure 6f. The only $2V_{dc}/3$-rated switch (S_{2x}) dissipates about 27% of the switching losses in this inverter-leg at the unity modulation index. The 4L-inverter-leg in [16] brought the rear, with about 62.3% of the maximum dissipated T-type 4L-inverter-leg switching losses; Figure 6b. In this figure, variations in dissipated losses among the six equal-voltage-stressed modules are dependent on their turn-on durations. These on-times are dictated by the applied control/modulation scheme.

The trends of the 4L-inverter-leg configurations' losses are displayed in Figure 6g–i. Summation of conduction and switching losses results in the total losses for each of the inverter-leg configurations. From this group plot, the T-type 4L-inverter-leg power circuit has the maximum loss dissipations. The proposed 4L ANNPC inverter-leg ranks second with about 70% of the highest dissipated total T-type 4L-inverter-leg losses. The 4L-inverter-leg in [16] has the minimum total losses with about 62.2% of the highest dissipated total T-type 4L-inverter-leg losses.

4. Simulation and Experimental Performances

In this section, simulation and experimental studies on the proposed 3-phase, 4-level active nested neutral point-clamped inverter power circuit in Figure 2 are carried out. In both studies, the selection criteria for balancing the flying-capacitor voltages (in Table 3) and the presented control steps in Figure 4 were deployed in the inverter control. Scaled-down system parameters were used in both the simulation and laboratory investigations. The obtained simulation results of the proposed 4L ANNPC inverter are experimentally validated with a laboratory prototype.

A. *Simulation Results*

The 3-phase power circuit of the 4L ANNPC inverter, Figure 2, was modeled in PLECS (version 4.4) and SIMULINK/MATLAB (MATLAB 9.11) simulation environments. Corresponding logic circuit models were also created using the outlined control scheme in Section 2 (C). The DC-link voltage (V_{dc}) value is 200 V, and the flying-capacitor banks' capacitance is 470 µF each. An RL load (R and L are 20 Ω and 20 mH, respectively) is connected in each phase of the inverter, whose modulation index is 0.95 at a carrier frequency of 3.3 kHz. Simulated inverter input and output waveforms were obtained.

With reference to the mid-point of the input voltage in Figure 2, the 4L-inverter-leg voltages are shown in Figure 7. Correspondingly, the simulated inverter line voltage and current waveforms are displayed in Figure 8; therein, the line voltages have seven voltage steps. Profiles of the voltage stresses across the power switches in phase 'a' are shown in Figure 9. Among the six switches, only switch S_{2a} has a voltage stress of 133.33 V ($2V_{dc}/3$); others have a voltage stress of 66.67 V ($V_{dc}/3$) each. For the indicated input voltage value, profiles of the capacitor banks' voltage waveforms in phase 'a', along with the inverter-leg voltage, are displayed in Figure 10a, where the deployed control scheme provided good balancing of the capacitor voltages in all the phases. In Figure 10b, the FFT spectrum of the line voltage waveform is displayed with a total harmonic distortion, THD, value of 17.74%; sideband harmonics did appear around the inverter switching frequency of 3.3 kHz. In a simulation run, at 0.32 s, the capacitor voltages' balancing scheme in Table 2 was deactivated and activated again at 0.4 s. Resulting profiles of the flying-capacitor voltages are shown in Figure 11, wherein the decaying and rising times of the capacitor voltages are the same (0.02 ms).

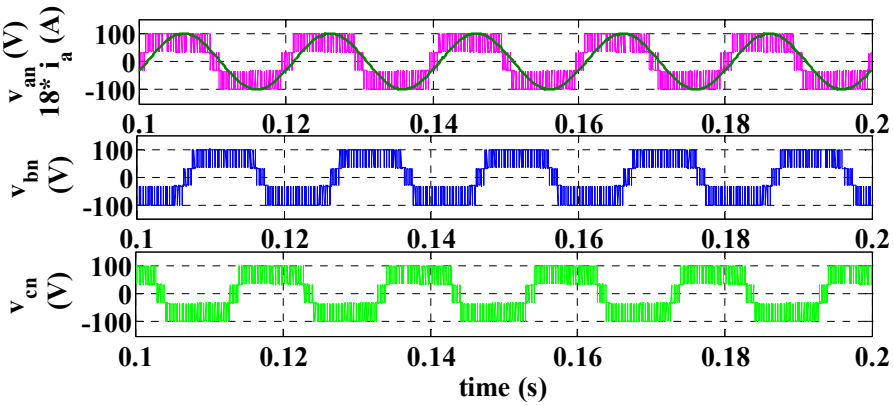

Figure 7. Simulated 4L-inverter-leg voltages and phase 'a' current.

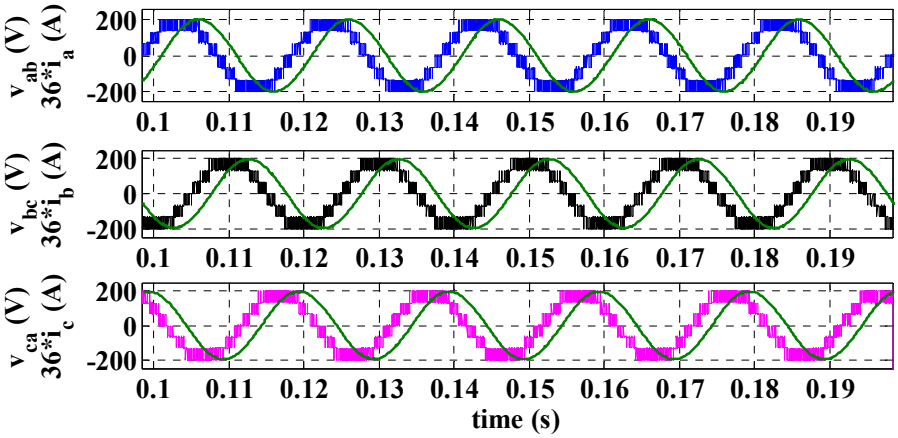

Figure 8. Simulated line voltage and current waveforms of the 4L ANNPC inverter.

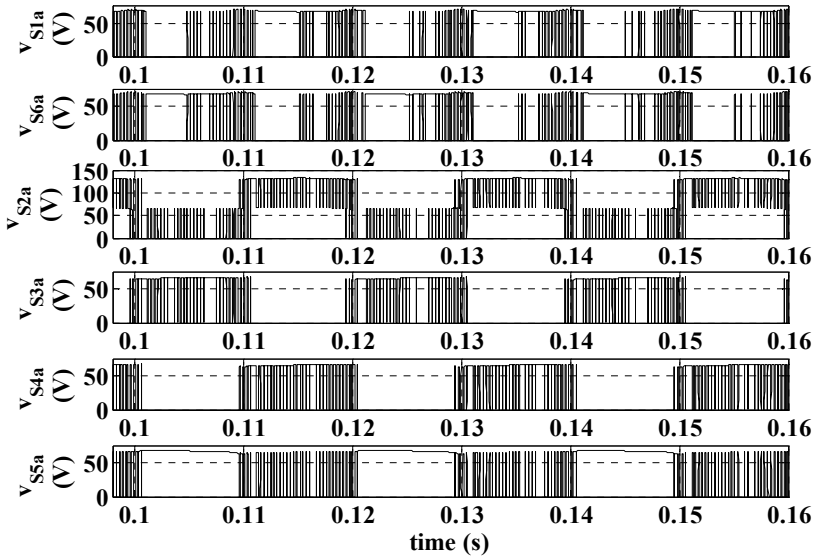

Figure 9. Switches' blocking voltages in phase 'a'.

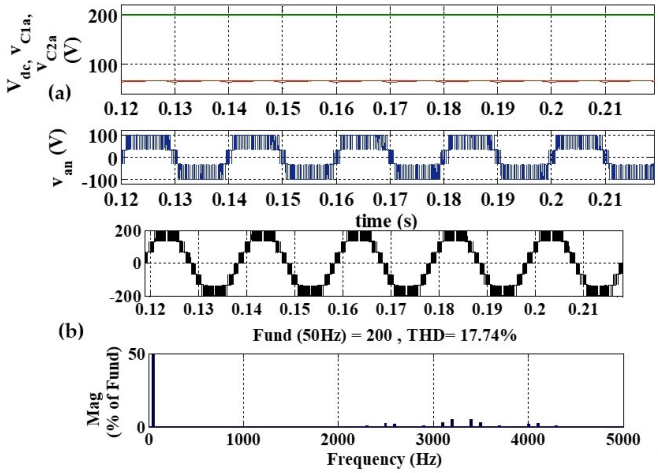

Figure 10. (**a**) Profiles of the flying-capacitor voltage waveforms in phase 'a', (**b**) FFT spectrum of the inverter line voltage waveform.

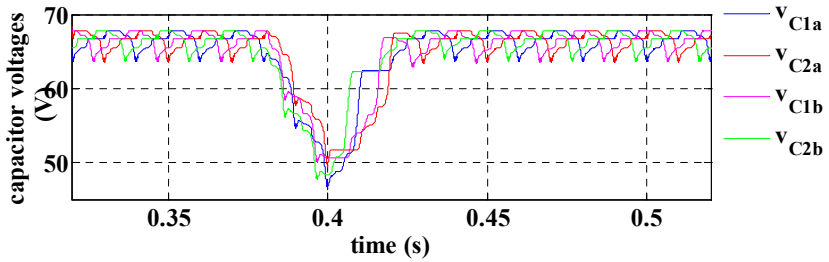

Figure 11. Deactivation and activation of the capacitor voltages' balancing scheme.

B. *Experimental Results*

Shown in Figure 12 is the experimental stand of a scaled-down prototype of the 4L ANNPC inverter. An on-board ADSP21363L DSP processor and Altera Cyclone II FPGA (Analog Devices, Inc., Otl-Aicher-Strasse, Munich, Germany) were used to implement the SPWM control scheme presented in Figure 4. In the FPGA platform, the needed deadtime (1.5 μs) was appropriately added to the synthesized gating signals. Infineon discrete IGBT switches were used in the power circuit. The prototype parameters and specifications are shown in Table 6. The modulation index value was set to 0.95.

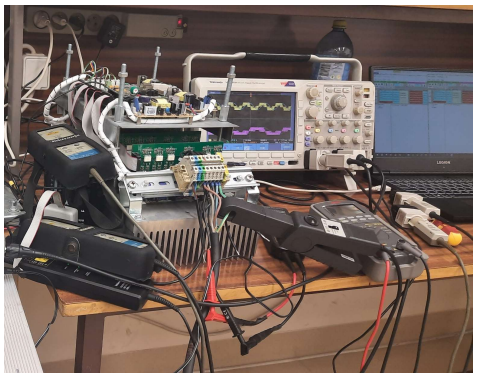

Figure 12. Experimental laboratory stand.

Table 6. Prototype specification.

Component	Specification
Power switches	AIKW50N60CT
Fundamental frequency	50 Hz
Carrier frequency	5 kHz
Flying-capacitors	470 µF, 600 V
switching frequency Carrier frequency	3.3 kHz
RL load	20 Ω, 20 mH
DC-link voltage	200 V

The experimental waveforms of inverter-leg voltages, line voltages, and currents from the 4L ANNPC inverter prototype are displayed in Figure 13. Comparatively, these waveforms are in agreement with their simulated counterparts in Figures 7 and 8.

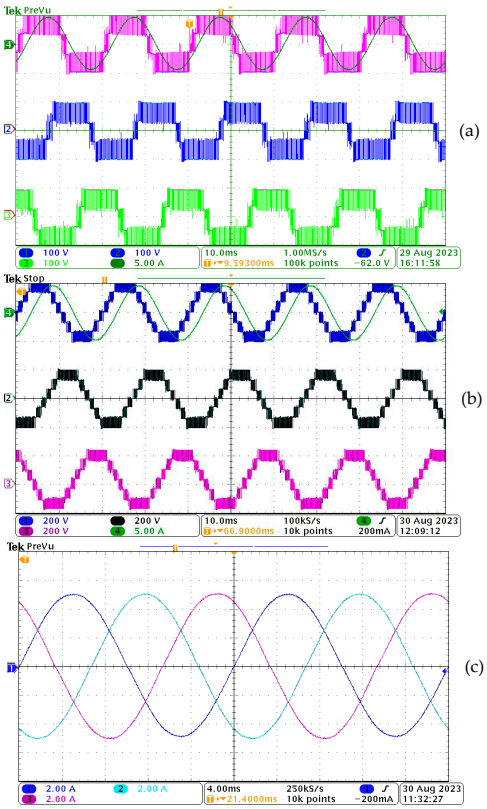

Figure 13. Laboratory results from the proposed 4L ANNPC inverter. (**a**) Inverter-leg voltages, (**b**) Line voltage waveforms, (**c**) Line current waveforms.

In Figure 14a, the displayed experimental voltage stress waveforms of switches in phase 'a' agree with the 4L ANNPC inverter-leg concept in Figure 1c. The flying-capacitor experimental voltage waveforms, together with the input and inverter-leg voltages, are shown in Figure 14b for phase 'a'. Evidently, these voltage waveforms further validate the effectiveness of the deployed modulation scheme in Figure 4, as earlier used for simulated results in Figure 10a. The experimental line voltage frequency spectrum in Figure 14c also contains sideband harmonics around the inverter switching frequency of 3.3 kHz, just as its simulated Figure 10b counterpart.

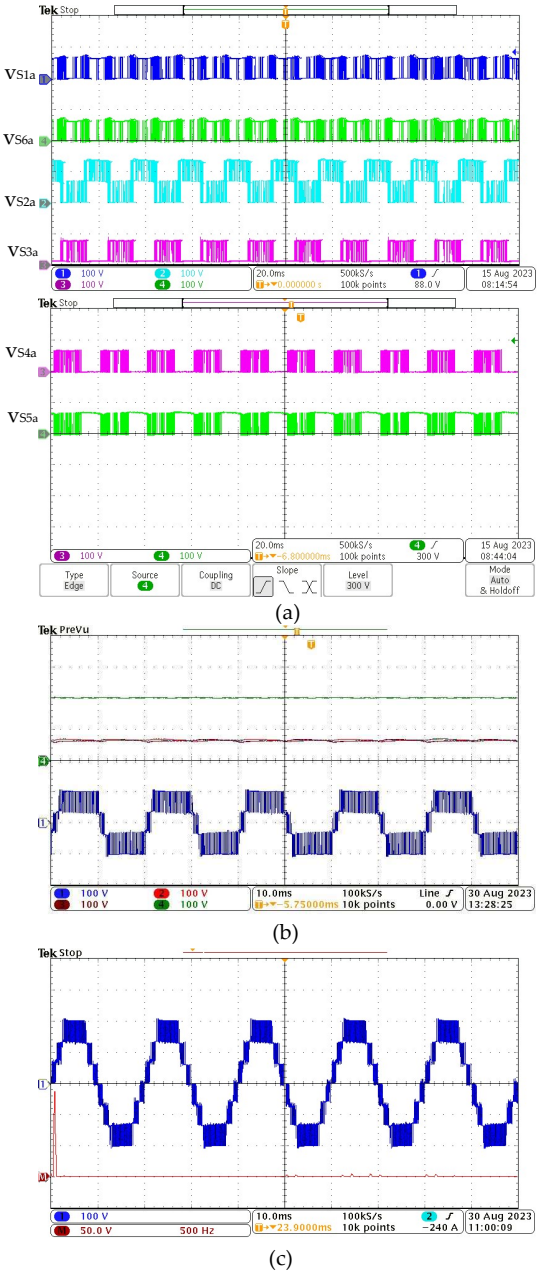

Figure 14. Experimental voltage waveforms in phase 'a'. (**a**) Blocking voltages of all 6 power switches; (**b**) Profiles of the flying-capacitor voltages; (**c**) FFT spectrum of line voltage v_{ab} waveform.

Deactivation and activation of the capacitors' balancing scheme was experimentally typified in Figure 15; capacitor voltage profiles concur with the simulated results in Figure 11 for v_{C1a}, v_{C2a}, v_{C1b}, and v_{C2b}.

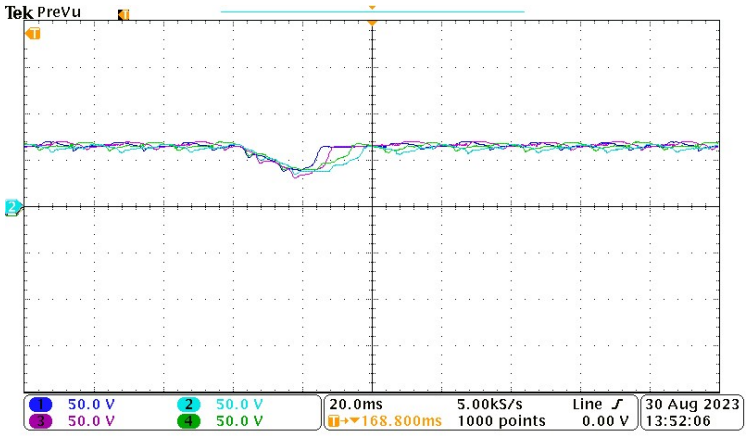

Figure 15. Experimental deactivation and activation of the capacitor voltages' balancing scheme.

Dynamic behavior of the inverter operation is examined by changing the modulation index value from 0.95 to 0.7 and back to 0.95 again. In Figure 16, the number of levels in the output line voltage waveform changes from 7 to 5 and back again to 7. The corresponding load current shows a decrease and increase in its amplitude values but maintained its sinusoidal waveform, as shown. Moreover, the flying-capacitors' voltages were effectively balanced during these dynamic operations, as shown therein.

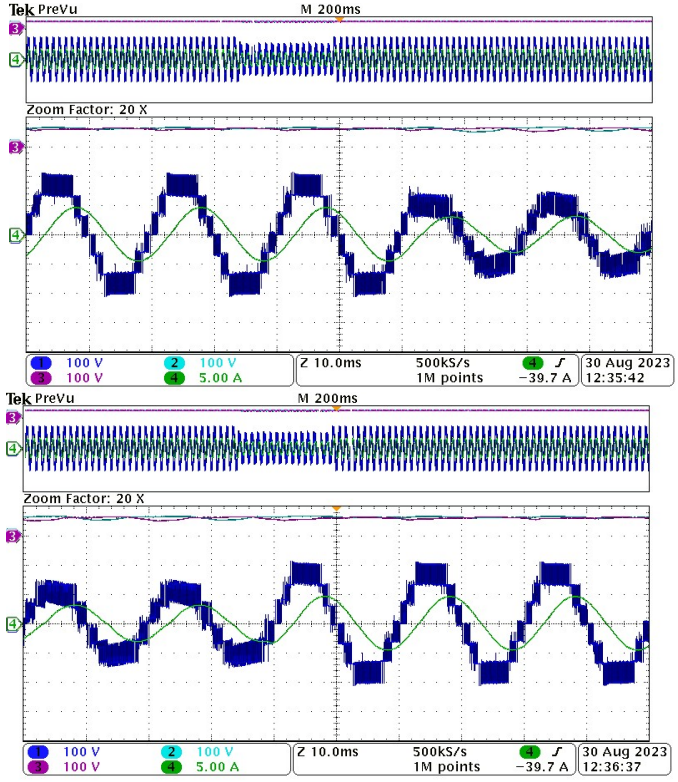

Figure 16. Measured experimental dynamic operational flying-capacitor, line voltage, and current waveforms for step changes in the modulation index: 0.95 to 0.7 and back to 0.95.

5. Conclusions

Presented in this paper is a four-level active nested neutral point-clamped, 4L NNPC, inverter. Details of its topological features, operational principle, and control scheme have been provided. The innate ameliorated blocking voltage on the power switches of this inverter results in low cost and loss. With a 2 MVA, 4.5 kV input DC voltage system, it has been demonstrated through cost estimations that the 4L NNPC inverter-leg has

the minimum cost involvement when compared to the four-level inverter-legs proposed in [16,20]. Moreover, the same topological feature gives the 4L NNPC inverter-leg superior lost performance over its T-type counterpart in [20]. The performance of the proposed 4L NNPC inverter has been presented through simulations and scaled-down experiments on a prototype unit; results have been adequately presented.

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