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# Performance Analysis of Interconnection and Differential Power Processing Techniques under Partial Shading Conditions

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**Abstract:** Partial shading conditions can cause low output power, hotspots, and a reduced lifespan in photovoltaic arrays. Interconnection (IC) and differential power processing (DPP) can be used to mitigate these effects. When individually applied to an array, these techniques can significantly increase the generated power. A few authors studied the combined use of these schemes under specific conditions such as large-scale arrays or a complex combination of several techniques, making it difficult to identify the individual contribution of each technique. Here, we aimed to determine whether the combined use of a switching-inductor DPP circuit and a total-cross-tied interconnection scheme presents better performance than each standalone technique, using a small-scale photovoltaic array. An array was tested using IC, DPP, and a combination of both techniques, and the array was subjected to 13 shading patterns and two irradiance levels. The performance in each case was assessed using maximum output power, performance ratio, mismatch power loss, and power enhancement indicators. The results showed that a standalone differential power processing circuit presents better performance than when it is combined with an interconnection. The DPP showed performance ratio values of up to 97%, mismatch power losses lower than 36.9%, and a power enhancement of up to 95.9%. The standalone interconnection shows the worst performance among the three techniques.

**Keywords:** interconnection; differential power processing; total-cross-tied scheme; switching-inductor converter; partial shading conditions



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## 1. Introduction

A photovoltaic panel (PV) can convert solar energy into electricity. Several panels can be connected into an array to increase the output voltage and/or current. The power generation of a solar array can be affected by various factors, including partial shading conditions (PSC) [1]. These conditions occur due to a mismatch between the irradiance values on each PV of an array and can be caused by nearby buildings, trees, leaves, bird droppings, dust deposition, or debris. Partial shading can lead to negative effects such as low conversion efficiency [2,3], overheating [1,4,5], reduced lifespan [6,7], and fires [8,9].

Several methods were proposed to reduce mismatch due to partial shading conditions, including bypass diodes [10], array reconfiguration [11–13], interconnections [14–17], full-power processors [18–20], parallel power processors [21–23], and differential power processors [24–26]. The most traditional method is the use of bypass diodes, but they can create multiple local maxima on the power-versus-voltage output curve of the array [27], making it harder to find the best operating point.

Interconnection (IC) is a technique in which the electrical connections between PVs are statically arranged to better distribute the power production of an array under partial shading conditions. The most common type is the series-parallel (SP), but there are also series, parallel, bridge-link (BL), honey-comb (HC), total-cross-tied (TCT), and hybrid methods [28,29]. The interconnection schemes are illustrated in Figure 1.

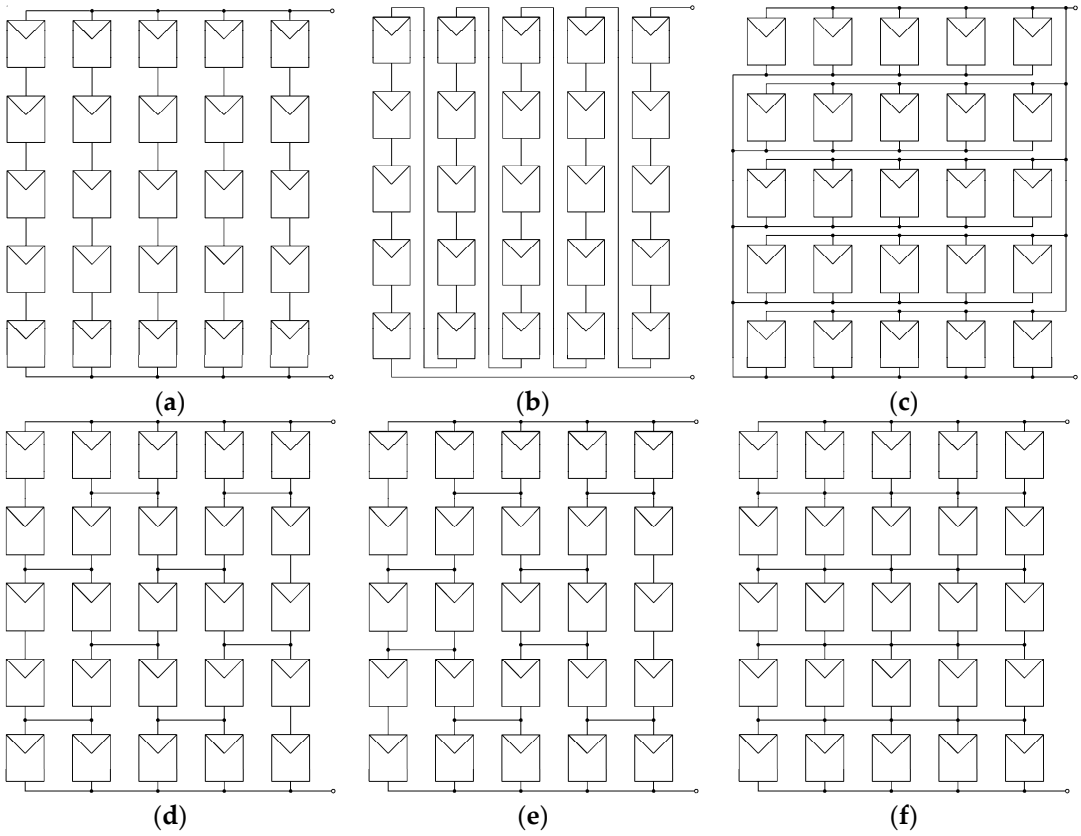



**Figure 1.** Interconnection schemes: (**a**) series-parallel; (**b**) series; (**c**) parallel; (**d**) bridge-link; (**e**) honey-comb; (**f**) total-cross-tied.

Several researchers showed that the total-cross-tied method presents the best performance between interconnections. The authors in Ref. [30] analyzed the effect of uniform and nonuniform partial shadings on photovoltaic arrays with different IC schemes. They used a 5 × 4 array subjected to 14 shading patterns and irradiance varying from 300 W/m$^2$ to 1000 W/m$^2$. They configured the array using series-parallel, bridge-link, honey-comb, and total-cross-tied interconnections. The authors found that the fault tolerance of TCT is superior among the ICs, with a higher power production and lower losses. In addition, TCT presents the best performance under random partial shadings. The researchers in Ref. [31] developed general mathematical models for different ICs and array sizes (symmetric and asymmetric). They applied four shading patterns on series-parallel, total-cross-tied, bridge-link, ladder, and honey-comb ICs. Their results showed that TCT exhibits the best performance due to the number of internal interconnections in an array: the higher the number of interconnections, the lower the power losses. Low power losses were also reported in Ref. [17]. Those authors pointed out that a 3 × 3 array with TCT can show a maximum power value 10.6% higher and a power enhancement value 17.5% higher than those of the traditional series-parallel interconnection. The authors used heavy shading levels for simulations and experimental tests: 800 W/m$^2$ for unshaded and 100 W/m$^2$ for shaded solar panels. ICs can be applied at the cell level in a photovoltaic panel, as demonstrated in Ref. [32]. They tested series-parallel, bridge-link, TCT, and series ICs with a 50 Wp, 36-cell PV, submitted to 15 shading patterns and four irradiance levels per shading pattern. These researchers found that the total-cross-tied method exhibits the lowest mismatch losses (32.1% maximum) and higher power enhancement (up to 62.4%) among the tested ICs.

Other IC techniques were investigated to minimize the effects of partial shading conditions, such as the use of bypass diodes, hybrid ICs, and array reconfiguration. The authors of Ref. [33] affirmed that despite the fact that bypass diodes can reduce the negative

effects of partial shadings, they cannot avoid the formation of hot spots; this could lead to damage to one or more solar panels. They also concluded that other electronic techniques show some advantages, but they use several electronic components, which can make the circuits costly, and involve complex software and hardware for control. On the other hand, the increase in cabling costs is irrelevant when compared to the increase in power generation achieved with interconnections. Hybrid ICs were studied in Ref. [16]. These authors considered simple ICs (SP, BL, HC, and TCT) and hybrid examples (SP-TCT, BL-TCT, HC-TCT, and HC-BL). Their tests included the effect of external parameters (variations of irradiance due to partial shading conditions) and internal parameters (variations in the ideality factor, series, and shunt resistance between photovoltaic cells). The researchers in Ref. [16] concluded that TCT shows the best performance, with variations of both internal and external parameters, followed by the HC-BL and HC-TCT hybrid interconnections. In Ref. [14], the authors analyzed the performance of hybrid ICs in large-scale arrays ($9 \times 9$). They studied HC-TCT and BL-TCT, concluding that those hybrid ICs can yield up to 6% more power than simple TCT, but are harder to implement on smaller arrays due to the limited connection points available between PVs. Static array reconfiguration applied to SP, BL, HC, and TCT was investigated in Ref. [34]. These researchers found that TCT still presents the best results, reducing mismatch losses by up to 32.88% and power losses by up to 66.66%. The effect of dynamic partial shading conditions, like passing clouds, can be reduced with array reconfiguration, according to Ref. [28]. These authors showed that parallel IC provides the highest output power, with the least mismatch, but the low output voltage and high levels of output current can hinder its practical use; TCT is deemed the best option among the tested interconnections. To further increase power generation, electrical and physical reconfiguration techniques can be used, although they can be more complex to implement [35].

Differential power processing (DPP) is another technique for reducing mismatch effects. DPP circuits attempt to transfer a fraction of the generated power from unshaded to shaded PVs, either equalizing the voltage between series-connected solar panels or making them work at their respective maximum-power points. The result is an increase in overall output power. DPP converters can be categorized into several architectures [36], as shown in Figure 2. The PV-to-PV architecture (Figure 2a) relies on non-isolated switching converters to compensate for mismatches between solar panels. PV-to-bus, in Figure 2b, uses multiple isolated switching converters with their outputs connected to the main series string. They can also have their outputs connected, forming an isolated bus used to transfer power between converters, as shown in Figure 2c. Finally, a single-input multi-output converter or several bidirectional converters can be used in PV-to-string architecture (Figure 2d) to directly transfer power from the string to the PVs.

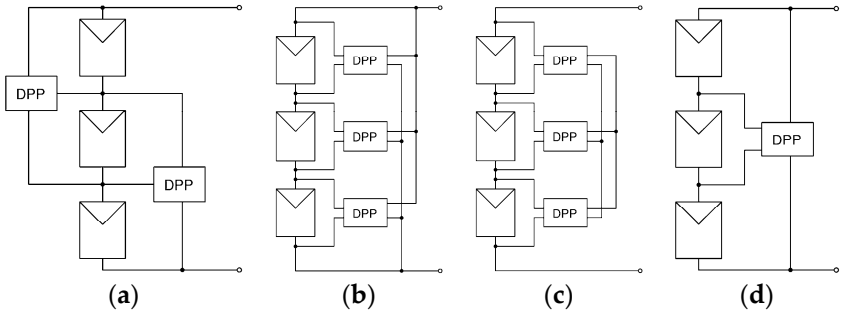



**Figure 2.** Differential power processing architectures: (**a**) PV-to-PV; (**b**) PV-to-bus; (**c**) PV-to-isolated-bus; (**d**) PV-to-string.

Several topologies can be used in DPP circuits, such as buck-boost [37], flyback [24], boost [38], switched capacitors [39], switched inductor-capacitors [40,41], LC circuits [42], and LLC-resonant circuits [43]. Among them, the buck-boost, also known as a switching inductor, is a non-isolated circuit with few components, and it is a simple and cost-effective

solution for mismatch [44] that has been studied by several authors. In Ref. [45], the authors developed a multi-stacked buck-boost DPP with a single switch and without current sensors. They eliminated the sensors by using a voltage equalization control method, which simplifies the system. Despite being simple, the buck-boost DPP achieved a 92% efficiency in power extraction. These authors also stated that this control strategy could be applied to other DPP architectures, like a multi-winding flyback or an LLC-resonant DPP converter. Multiple buck-boost circuits can also be used without affecting overall efficiency. The authors in Ref. [37] applied a multidimensional perturb and observe maximum-power-point tracking (MPPT) algorithm to a multiple-buck-boost DPP, to achieve a distributed MPPT. This approach reduced the number of switches in the circuit and improved the system response to quick irradiance changes. This converter presented up to a 92.3% efficiency.

Researchers in Ref. [46] developed a mathematical analysis for a buck-boost in a PV-to-PV architecture to improve modeling and simulation. They validated their results using simulations with a voltage equalization method and a fixed duty cycle of 50%. They concluded that the longer the series string of PVs in an array, the higher the differential current levels passing through the converters, which can lead to higher losses and low efficiency. To overcome this issue, Ref. [47] proposed a system with modular DPP converters, in which the control circuits of the buck-boost converters are independent. This approach allows strings to be of any length, without impairing performance. It also dispenses the use of a central MPPT converter on the array output, since this task can be performed in a distributed way by the DPP control circuits. These authors achieved up to 98% efficiency with a buck-boost DPP.

Although there are several studies regarding array interconnection and differential power processing, only a few authors have studied how a differential power processor and an interconnection scheme behave when combined in a photovoltaic array. In Ref. [42], the authors analyzed the performance of four interconnections schemes (SP, TCT, BL, and central-cross-tied) when a switching-inductor DPP is applied to a $4 \times 4$ photovoltaic array under different shading patterns and irradiance levels. They used five different shading patterns and varied the irradiance from 200 to 800 $W/m^2$ over the shaded panels. PSIM simulation software was used to validate the results, but no electronic component values were given. Nevertheless, these authors stated that they used a switching frequency of 50 kHz to obtain an adequate voltage stress over the inductors. Their results indicate that the use of DPP on SP and central-cross-tied ICs improves the output power of the array, but it declines to zero on TCT and BL. This occurs because the architecture of a differential power processing circuit requires at least two series-connected PVs to work. Photovoltaic panels in TCT and BL are not always directly connected in series with each other; therefore, DPP circuits cannot work properly if they are applied to an interconnected array in the traditional manner.

A combined scheme with three different techniques was proposed by Ref. [48] to overcome this problem. The authors used electrical reconfiguration, series-DPP, and parallel-DPP in the same array. The magic-square enhanced reconfiguration technique was first applied to sub-units of a $6 \times 6$ array to equalize the received irradiance under various shading patterns. Then, bidirectional Cùk DPP converters in a PV-to-PV configuration were applied between sub-units of the series-connected array to equalize the generated current between them, since each sub-unit can present a different average received irradiance. Finally, inverted-buck parallel-DPP converters were used between PV strings to equalize their voltages. Additionally, DPP circuits work with a maximum-power-point tracking algorithm instead of simple voltage equalization to enhance performance. Their MPPT uses a proportional and integral controller to set the duty cycles of each DPP circuit. These authors validated their system by simulation, in which they applied five shading patterns to the system. Their results show that the combination of three techniques increases the maximum output power and efficiency in comparison to those of each technique used alone. Although a TCT-only array shows mismatch power losses of up to 33%, which is a good performance, the combined techniques present mismatch losses of only 2.27%. In

general, the proposed system yields from 11% to 21% more power than an array of the same size using TCT and bypass diodes. An important drawback of this system is its complexity: according to these authors, a 6 × 6 array requires 64 switches (transistors), several current sensors across the array, a large number of components, and sophisticated control algorithms. Therefore, it is intended for large-scale solar plants, like solar farms, and it is not suitable for small-scale PV systems, like residential applications, composed of smaller photovoltaic arrays.

The authors of Ref. [49] applied a combined DPP, composed of a switched-inductor and a resonant switched-capacitor, to a TCT interconnected, small-scale photovoltaic array. This is a modified version of a traditional switching inductor circuit, where the switching sequence of the transistors is modified to support the resonant capacitor. The switched inductor compensates for mismatches between two adjacent rows of the array, while the resonant switched-capacitor compensates for mismatches between adjacent groups of rows. These authors simulated the circuit under six shading patterns, each one with random irradiance levels ranging from 600 to 100 $W/m^2$, operating in voltage equalization mode (fixed 50% duty cycle), and compared the results with those of simple SP and TCT arrays. The proposed system showed an efficiency between 95% and 99% in comparison to the expected output power under the standard test conditions, a power enhancement of up to 30% above SP and 19% above TCT output power, a higher fill factor, and lower absolute mismatch losses. Since the number of required switches is half the number of rows in the array, and the control strategy is simple, this may be a good alternative for small-scale PV systems. However, these authors use a boost circuit with MPPT connected to the output of the array, so there is no way to clearly distinguish the contribution of the combined IC and DPP from the boost circuit in regards to overall performance enhancement. Moreover, to add a resonant switched capacitor to the system, the array must have an even number of rows and at least four rows to work properly.

In essence, partial shading conditions can be detrimental to photovoltaic arrays, decreasing the output power and possibly leading to negative effects such as hotspots and reduced lifespan. Several techniques can be used to mitigate their effects, like interconnection and differential power processing. These techniques can significantly increase the generated power when individually applied to an array, as shown by many researchers in the literature. However, if these techniques are combined into the same array, they could present a better performance. A few authors studied the combined use of IC and DPP in an array in specific conditions, i.e., in large-scale arrays. No information regarding how they perform in a small-scale array is provided; thus, the proposed solutions may not be suitable for residential use. IC and DPP are also studied using a complex combination of several techniques, including a maximum-power-point tracking (MPPT) circuit after the array, which makes it hard to identify the individual contribution of the interconnection and the differential power processing circuit to the overall performance of the system.

In this work, we aimed to determine whether the combined use of a switching-inductor differential power processing circuit and a total-cross-tied interconnection scheme presents better performance than each individual technique in a small-scale photovoltaic array. The main contributions of this work are: (a) the proposition of an alternative method to adapt a switching-inductor differential-power-processing circuit in a total-cross-tied interconnected photovoltaic array; (b) the proposal of a system suitable for small-scale photovoltaic arrays with any number of rows and columns; (c) simple implementation, since there is no need for current sensors, a large number of switches, or complex control algorithms; (d) a test including no other partial-shading compensation techniques or MPPT circuits, ensuring that the performance of IC and DPP can be clearly accessed.

This paper is organized as follows: Section 2 describes the procedures adopted to perform the simulations and extract and analyze the data. Section 3 compares the performance of total-cross-tied interconnection, differential power processing, and both techniques used simultaneously on the photovoltaic array and discusses the performance indicators. Finally, Section 4 summarizes the main findings of this work.

## 2. Materials and Methods

### *2.1. General Proceedings*

The datasheet specifications of the photovoltaic panel used in this work are listed in Table 1.

**Table 1.** Specifications of the photovoltaic panel used in this work.

| Characteristic | Value |
|---|---|
| Manufacturer | Yingli Solar |
| Model | YL245-29b |
| Cell type | Multicrystalline |
| Number of cells | 60 |
| Maximum power ($P_{MP}$) | 245 Wp |
| Open-circuit voltage ($V_{OC}$) | 37.8 V |
| Short-circuit current ($I_{SC}$) | 8.63 A |
| Voltage at $P_{MP}$ ($V_{MP}$) | 30.2 V |
| Current at $P_{MP}$ ($I_{MP}$) | 8.11 A |
| Temperature coefficient of $V_{OC}$ | −0.33%/°C |
| Temperature coefficient of $I_{SC}$ | 0.06%/°C |

Twelve solar panels were used in a three-row, four-column photovoltaic array to perform simulation tests. Three shading compensation techniques were applied to the array: total-cross-tied interconnection; switched-inductor differential power processing; and the combination of the two previous techniques, that is, DPP circuits applied to an IC array (IC + DPP).

Then, 13 shading patterns, divided into five families, were applied to the array using each shading compensation technique. Each shading pattern was tested with two irradiance levels—high (700 W/m$^2$) and low (400 W/m$^2$)—for the shaded photovoltaic panels. The testing workflow is illustrated in Figure 3.

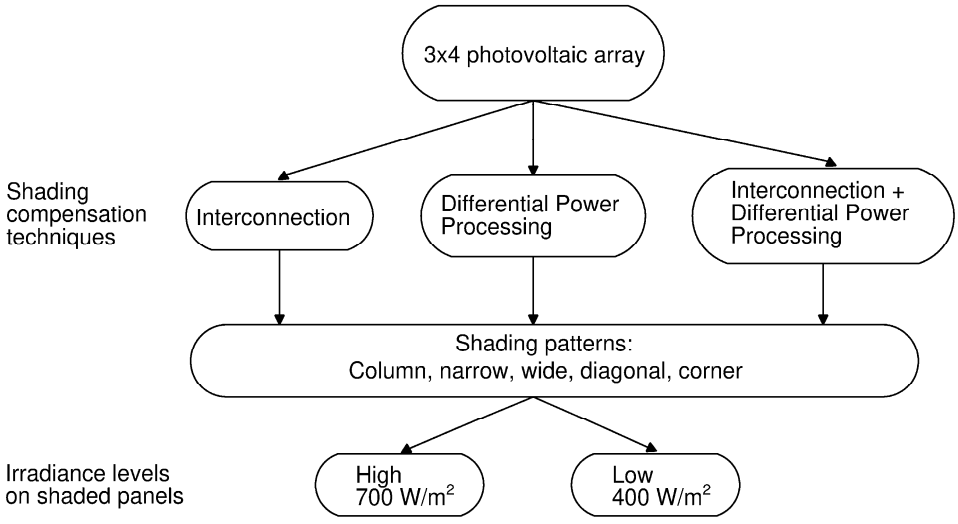



**Figure 3.** Testing workflow.

For each one of the 78 test conditions, the power-versus-voltage (P-V) curve and the maximum power point (MPP) were extracted. The results were analyzed by comparing the maximum-power-point values and three other indicators (performance ratio, mismatch power loss, and power enhancement) for each shading pattern.

### *2.2. Specific Proceedings*

The circuits and shading conditions were simulated on LTspice at 25 °C.

A one-diode model for the photovoltaic panels [50] was used, as illustrated in Figure 4, where $I_{PV}$ is the photovoltaic current, $D$ is the internal diode, $R_{SH}$ is the shunt resistance, $R_S$ is the series resistance, $V_{OUT}$ is the output voltage, and $I_{OUT}$ is the output current.

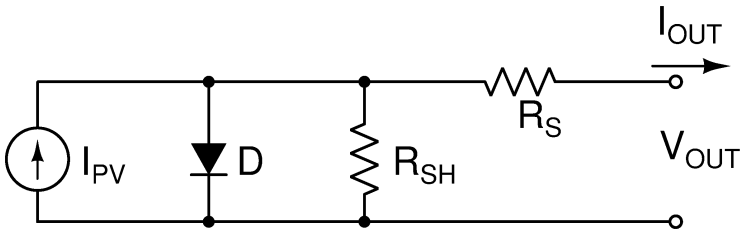



**Figure 4.** One-diode model of a photovoltaic panel.

The photovoltaic array was subjected to three partial-shading compensation techniques, shown in Figure 5. The total-cross-tied interconnection technique (Figure 5a) connects all solar panels in the same row in parallel and then all rows in series. In the switched-inductor differential power processing technique (Figure 5b), the array presents a traditional series-parallel connection; DPP circuits are applied to each column of series-connected PVs. Differential power processing circuits require series-connected solar panels to work properly [42]; therefore, Figure 5c depicts the combined interconnection and DPP technique (IC + DPP), in which an interconnected array is assigned a set of DPP circuits between its rows.

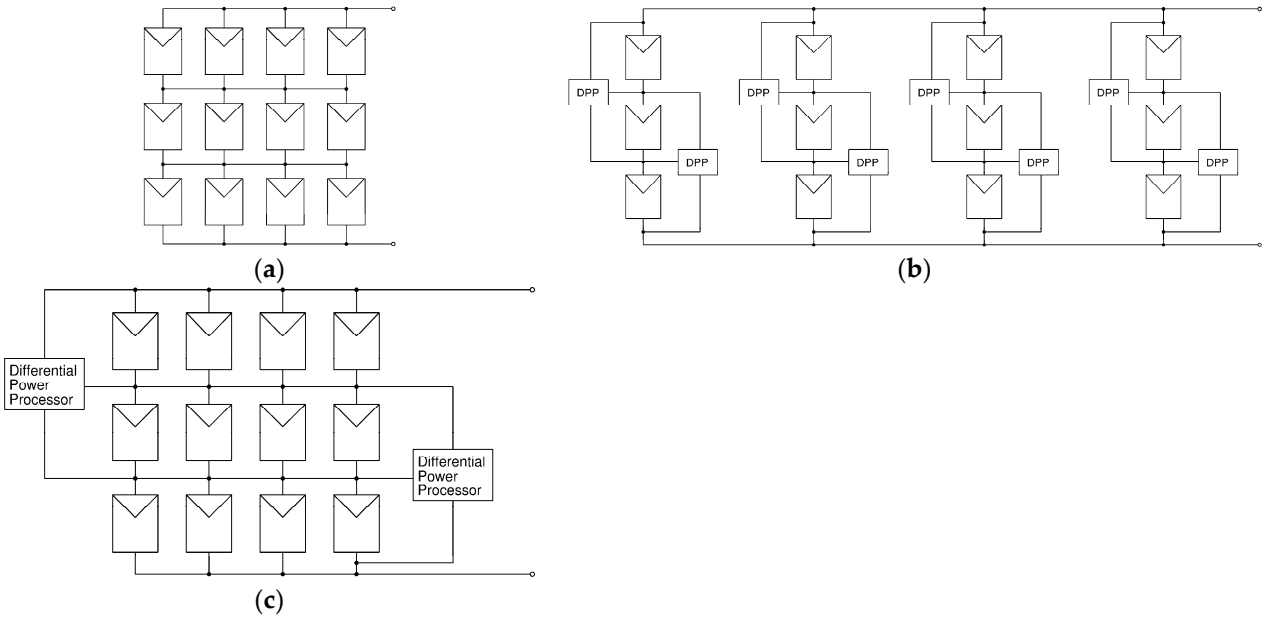



**Figure 5.** Schematic of partial-shading compensation techniques: (**a**) interconnection; (**b**) differential power processing; (**c**) combined interconnection and differential power processing.

A switched-inductor DPP circuit based on the work of Ref. [49], shown in Figure 6a, uses an inductor $L$ to store and transfer energy from one photovoltaic panel to another to balance their overall power production. Two MOSFET transistors, $T_1$ and $T_2$, work in complementary periods to charge and discharge the inductor. The circuit also has two fast-recovery diodes, $D_1$ and $D_2$, for MOSFET protection, and two capacitors, $C_1$ and $C_2$, to reduce the voltage ripple between PVs.

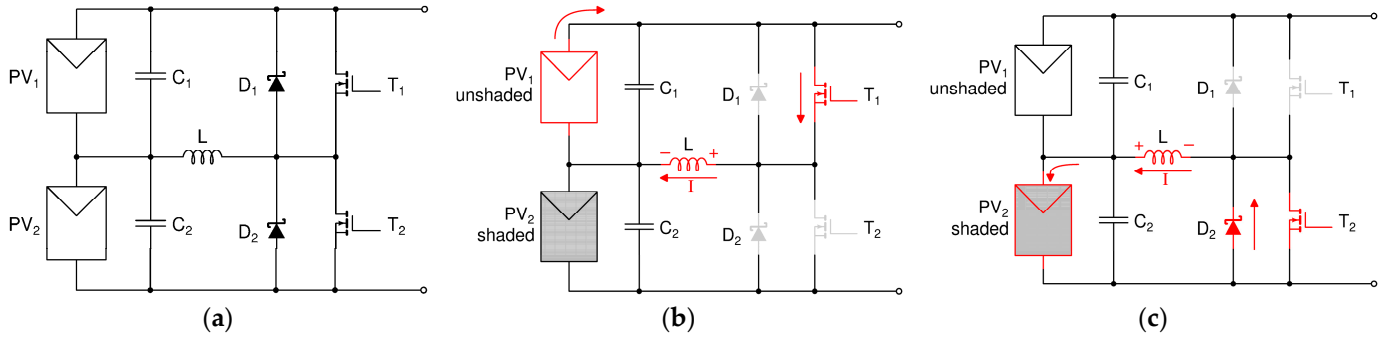



**Figure 6.** Switched-inductor differential power processor: (**a**) circuit; (**b**) stage 1 of operation; (**c**) stage 2 of operation.

In the voltage equalization strategy, the DPP works in two stages, as depicted in Figure 6b,c. If the $PV_2$ is shaded, the DPP needs to transfer energy from $PV_1$ (unshaded) to $PV_2$. In stage 1 (Figure 6b), $T_1$ is on, and $T_2$, $D_1$, and $D_2$ are off; part of the energy generated on $PV_1$ is stored in the inductor $L$ via $T_1$. The voltage on $L$ is equal to the voltage across $PV_1$. In stage 2 (Figure 6c), $T_1$ and $D_1$ are off, and $T_2$ and $D_2$ are on. The inductor $L$ now transfers its stored energy to $PV_2$ by discharging it via diode $D_2$, thus keeping the voltage across $PV_2$ approximately the same as on $PV_1$, which is thus a positive value. This way, $PV_2$ cannot present a negative voltage and act as a load, which is the typical behavior in series-connected photovoltaic modules where one of them is partially shaded. With a positive voltage, $PV_2$ maintains the yielding energy, and the total generated power of the array increases. The capacitors $C_1$ and $C_2$ stabilize the voltages on $PV_1$ and $PV_2$ to maintain the voltage equalization strategy. In this scenario, $C_1$ is charged by $PV_1$ at stage 1, and $C_2$ is charged by the inductor $L$ at stage 2.

The inductance $L$ is given by Equation (1) [49], where $\delta$ is the duty cycle, $V_{OC}$ is the open-circuit voltage of the photovoltaic module, $f$ is the switching frequency, and $\Delta I$ is the current ripple on the inductor.

$$L = \frac{\delta \cdot V_{OC}}{2 \cdot f \cdot \Delta I} \tag{1}$$

The capacitance of $C_1$ and $C_2$ is given by Equation (2) [49], where $\Delta V$ is the voltage ripple on the capacitor.

$$C = \frac{\delta}{8 \cdot f^2 \cdot L \cdot \Delta V} \tag{2}$$

The models used in the differential power processing circuit are STB120NF10, for the MOSFET, and MBR20100CT, for the fast-recovery diode. The inductor is 300 µH, and the capacitors are 100 µF. The circuit works at a switching frequency of 50 kHz and a 50% duty cycle. The current ripple on the inductor is approximately 0.6 A, and the voltage ripple on the capacitors is around 1 mV.

Thirteen shading patterns were used to assess the array's P-V curves under each partial-shading compensation technique. These patterns are classified into five families: column, narrow, wide, diagonal, and corner. Each family is divided into subcategories, depending on the shadow extension. Figure 7 shows the shading patterns used in this work.

Each shading pattern was applied to the array using two irradiance levels on the shaded solar panels: 700 W/m$^2$ (high irradiance), representing light shadow; and 400 W/m$^2$ (low irradiance), representing heavy shadow. Unshaded PVs received 1000 W/m$^2$.

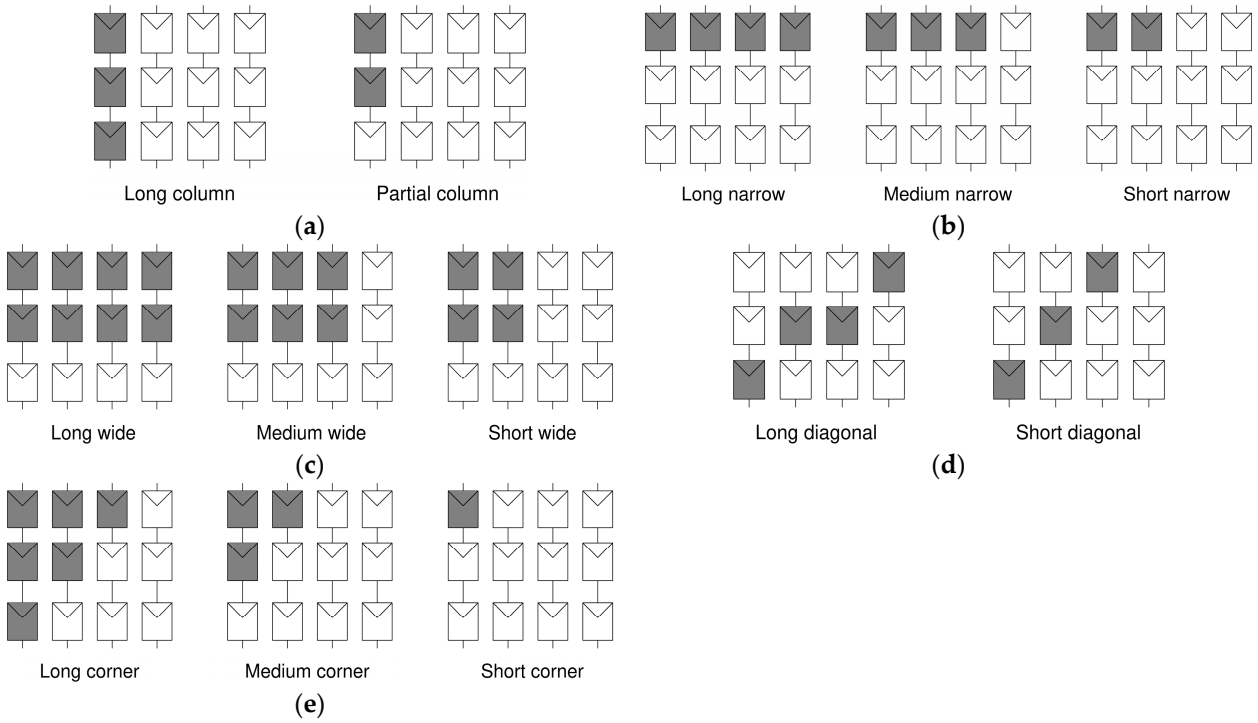



**Figure 7.** Shading patterns used in the tests: (**a**) column; (**b**) narrow; (**c**) wide; (**d**) diagonal; (**e**) corner. Each pattern is divided into two or three subcategories, according to shadow extension.

After extracting the P-V curves from the simulations, the relationship between each test condition's maximum power point values was examined. In addition, three performance indicators were calculated: performance ratio, mismatch power loss, and power enhancement. The performance ratio (PR) shows the relationship between the maximum real output power of the array ($P_{MP}$) and the output power at the standard test conditions ($P_{STC}$). Equation (3) shows the formula for the performance ratio.

$$PR = \frac{P_{MP}}{P_{STC}} \cdot 100\ (\%) \tag{3}$$

Mismatch power loss (MPL) is defined as the power loss due to the shadings over the array, with the standard test conditions as a reference, as described in Equation (4).

$$MPL = \frac{P_{STC} - P_{MP}}{P_{STC}} \cdot 100\ (\%) \tag{4}$$

Power enhancement (PE), as stated in Equation (5), compares the increase in yielded power with the partial-shading compensation technique to the output power of the same array using a simple series-parallel interconnection. This indicator uses the real output power of the array, $P_{MP}$, and the series-parallel output power, $P_{SP}$.

$$PE = \frac{P_{MP} - P_{SP}}{P_{SP}} \cdot 100\ (\%) \tag{5}$$

## 3. Results and Discussion

### *3.1. P-V Curves*

There are a total of 78 test conditions in this work: three shading compensation techniques subjected to 13 shading patterns and 2 irradiance levels. Each condition produces its own P-V curve, as presented in the Supplementary Materials.

All curves presented the expected behavior, with just one maximum power point. The only exception occurs for the wide long shading pattern at 700 W/m$^2$, where there is a small local maximum between 25 V and 30 V. This local maximum presents an amplitude of 850 W. Compared to the expected power value in that range of the P-V curve for this case (around 800 W), it represents an increase of about 6%, which can be neglected without prejudicing further analyzes.

A positive aspect of all three techniques is the absence of local maxima in power-versus-voltage curves for each shading pattern tested, as all curves present only one maximum power point. This can simplify the application of maximum-power-point tracking algorithms on a photovoltaic array, since they only have one maximum power point to track, so even simple algorithms and circuits can perform this task. If the curves showed more than one maximum, more complex MPPT algorithms should be used to differentiate the global maximum from any local maxima.

### *3.2. Shading Patterns*

The presence of just one global maximum power point per curve allows for the analysis of only the relation between the MPP values of all partial-shading compensation techniques. This analysis is first performed for the maximum power extraction capability of the photovoltaic array under several shading patterns, considering high and low irradiance levels.

#### 3.2.1. High-Irradiance Shading (700 W/m$^2$)

Figure 8 depicts the maximum output power for each technique (IC, DPP, and IC + DPP) and shading pattern at 700 W/m$^2$ of irradiance.

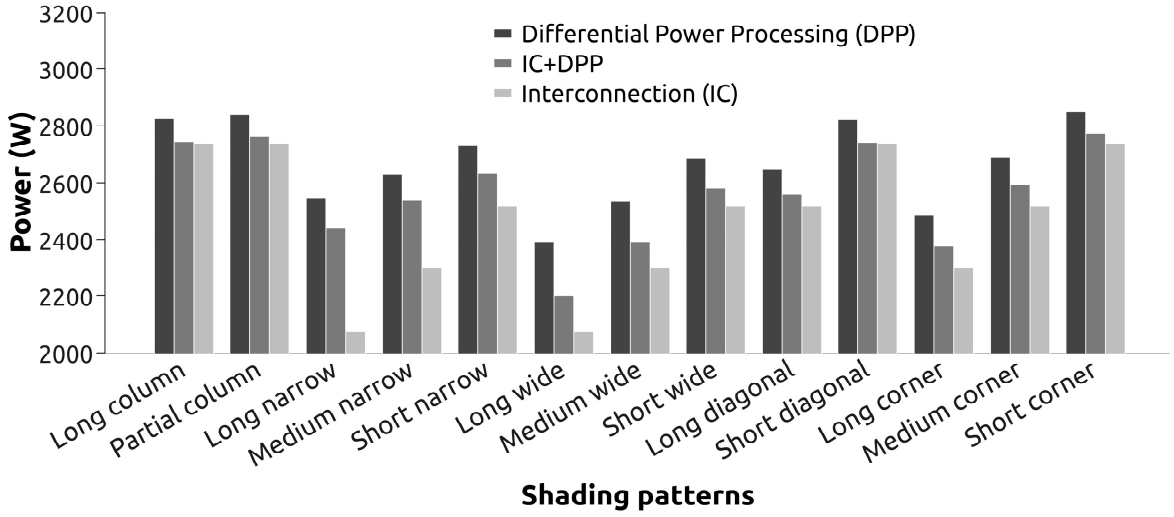



**Figure 8.** Maximum output power at 700 W/m$^2$ according to the shading pattern.

The performance of each partial-shading compensation technique varies according to the shading pattern, with IC showing the lowest values. The shading patterns that present the highest output power during interconnection are the long and partial column, the short diagonal, and the short corner patterns. In general, the more photovoltaic panels shaded in the same row, the lower the output power. Thus, the cited shading patterns present the highest output power because they have one photovoltaic module shaded per row. Short narrow, short wide, long diagonal, and medium corner patterns present intermediate values. Heavily-shaded patterns, like long corner, long narrow, medium wide, and long wide patterns, show the lowest generated power, as they present at least one row with several (or all) shaded modules.

The differential power processing technique shows the same behavior between shading patterns as IC, but with a better performance. In DPP, having two or more photovoltaic panels shaded in series has a similar effect to that of having shaded panels in parallel in an interconnected array. This way, when the array presents one or more shaded rows, the DPP circuits redistribute the generated power between unshaded and shaded rows, increasing the output power. This is the case in long narrow, medium narrow, long wide, and medium wide patterns, where there is a significant difference between the MPP of differential power processing and interconnection. The behavior of the combined IC and DPP techniques at high irradiance is the same as that of the DPP technique, so the analysis for the differential power processing circuits is valid for this case.

In general, the DPP technique always yields the highest power at 700 W/m$^2$, in any shading pattern studied in this work. The IC + DPP technique yields intermediate power values between DPP and IC. Since DPP works with differential currents, smaller current differences make the circuits more efficient. This explains the larger output power differences seen between DPP and the other techniques at high irradiance levels.

#### 3.2.2. Low-Irradiance Shading (400 W/m$^2$)

Figure 9 shows the maximum output power for each technique and shading pattern at 400 W/m$^2$ of irradiance.

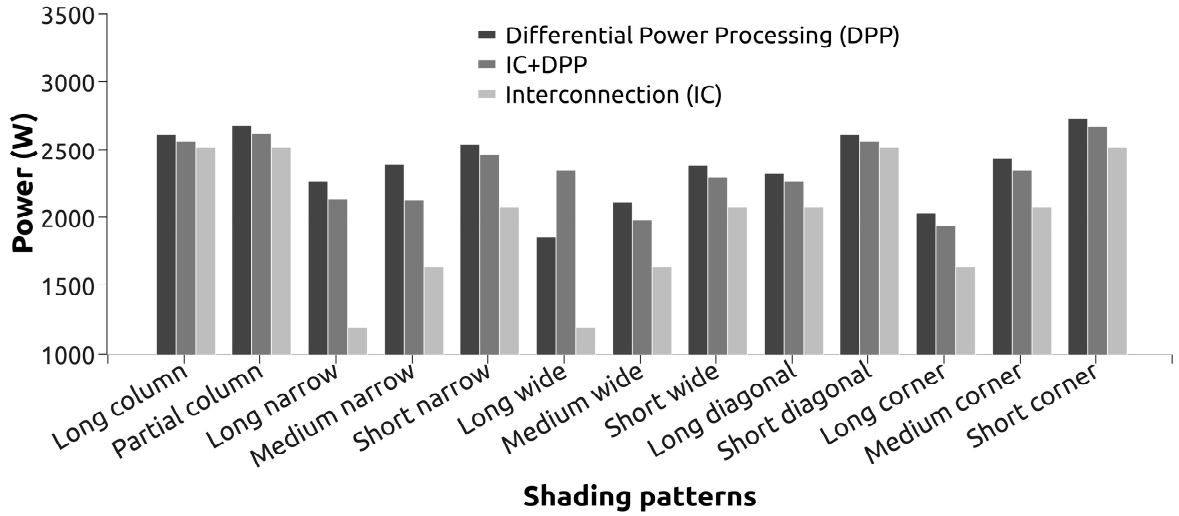



**Figure 9.** Maximum output power at 400 W/m$^2$, according to the shading pattern.

Figure 9 shows that the relationship between the maximum output power and the shading pattern for the interconnection and differential power processing techniques presents the same behavior as that of a high irradiance level; hence, the analyses in Section 3.2.1 are valid here. However, some differences occur in the combined IC and DPP technique. The power difference between DPP and IC + DPP is smaller in most shading patterns, especially in the short-shading patterns. This performance increase can be explained by the action of the DPP circuits in the IC + DPP technique, which improves the power distribution over the parallel-connected photovoltaic panels in each row of the TCT interconnection.

The overall output power at 400 W/m$^2$ is lower than at 700 W/m$^2$, since at low irradiance, the power difference between the shaded and unshaded photovoltaic panels is higher. In this situation, the DPP circuits yield more power in almost all shading patterns, which is the same result shown in Section 3.2.1, except for the long wide shadow pattern. In this pattern, IC + DPP yields more power than the DPP technique due to the uniform shading distribution over the upper part of the array and the action of the DPP circuits, as previously stated. In addition, the output power difference between the three techniques is smaller at low irradiance level.

The combined IC and DPP technique usually presents lower efficiency than does the DPP technique alone because in IC + DPP, there is a reduced number of differential power processing circuits. On one hand, the reduced number of circuits could be a positive characteristic, decreasing the system complexity. On the other hand, however, using fewer DPP circuits on several parallel-connected photovoltaic panels forces each circuit to deal with higher differential currents. In the DPP technique, each DPP circuit has to deal with the differential current of just two series-connected solar panels. For example, considering two series-connected PVs with the maximum difference in irradiance level between them (1000 W/m$^2$ and 400 W/m$^2$), there is 5.27 A of differential current flowing through the inductor and the transistors of the circuit. Considering two groups of four parallel-connected solar panels (from the TCT interconnection), the maximum differential current is 20.21 A, which is 3.83 times greater than that in the previous case. This higher differential current leads to greater losses, thus reducing the overall system efficiency and decreasing the output power.

It is more beneficial to use just the interconnection in places where the most common shading patterns on the array could be predicted, and the shading levels are less intense, which is an advantage of this technique. This happens because the maximum power values of the three techniques exhibit less significant differences at high irradiance levels, and IC is simpler to implement than DPP, although this could lead to lower power extraction from the photovoltaic array. On the other hand, in places where there is a higher probability of low-irradiance and unpredictable shading patterns, it is more efficient to use the standalone differential power processing technique.

### *3.3. Performance Indicators*

#### 3.3.1. Performance Ratio

Performance Ratios for each shading pattern are shown in Figure 10a, for high irradiance level, and Figure 10b, for low irradiance level.

The performance ratio of the DPP technique at high irradiance levels (Figure 10a) shows the smallest variation range among the three techniques studied in this work and achieves up to 97% performance under the short corner shading pattern, which is the pattern with the least shaded modules. It is also always superior to the IC + DPP and IC techniques. The combined interconnection and DPP technique presents an intermediate PR value between that for DPP and IC; in some shading patterns, it shows the same value of IC, i.e., in long column, partial column, and short diagonal patterns. The interconnection technique presents the worst performance ratios at high irradiance levels, as low as 70.6% for the long narrow and long wide patterns. In these patterns, the effect of partial shading cannot be compensated by the interconnection because one or more rows of the array are completely shaded. Narrow and wide shading families exhibit the worst performance in IC, indicated by their low PR values.

The behavior of the performance ratio at low irradiance levels (Figure 10b) is similar to that in the 700 W/m$^2$ case shown in Figure 10a, with some exceptions. The performance of DPP and IC + DPP is superior to that of the IC in all shading patterns. In addition, these techniques show similar PR values at low irradiances, although DPP still presents PR values greater than those of IC + DPP. However, there is an exception in regards to the long wide shading pattern, where IC + DPP performs better than all other techniques. This particular case shows that IC + DPP exhibits good performance when a photovoltaic array is under heavy shading conditions, achieving a performance ratio of 79.7% when 2/3 of the solar array is heavily shaded. The interconnection technique shows lower PR values when compared to those of the high irradiance levels, achieving values as low as 40.5%.

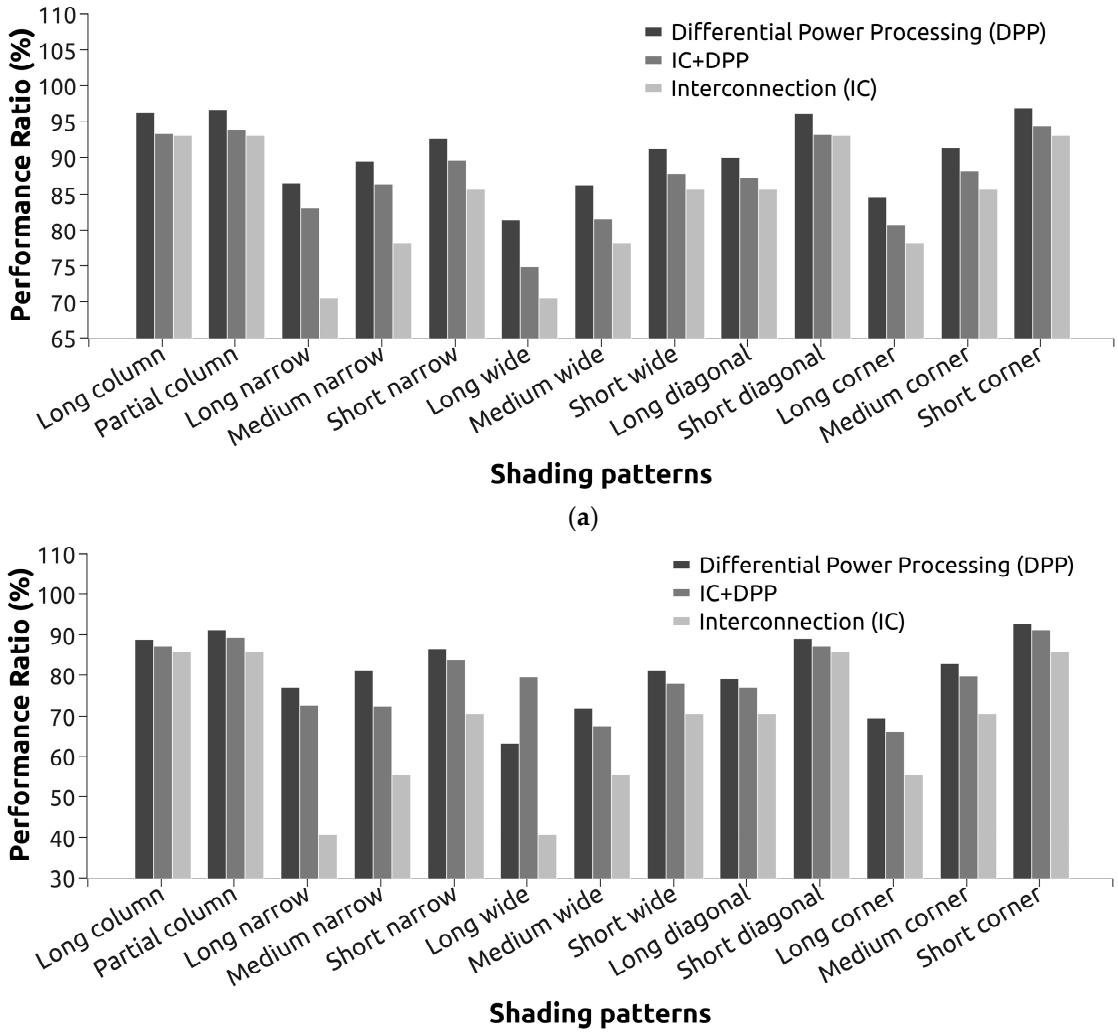


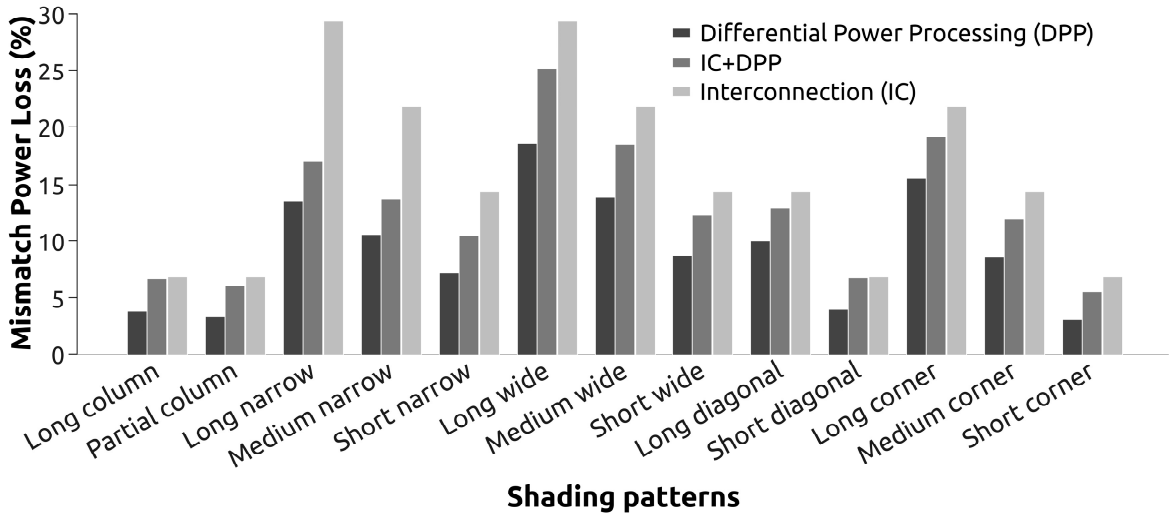

**Figure 10.** Performance ratio indicator for: (**a**) high irradiance level (700 W/m$^2$); (**b**) low irradiance level (400 W/m$^2$).

#### 3.3.2. Mismatch Power Loss

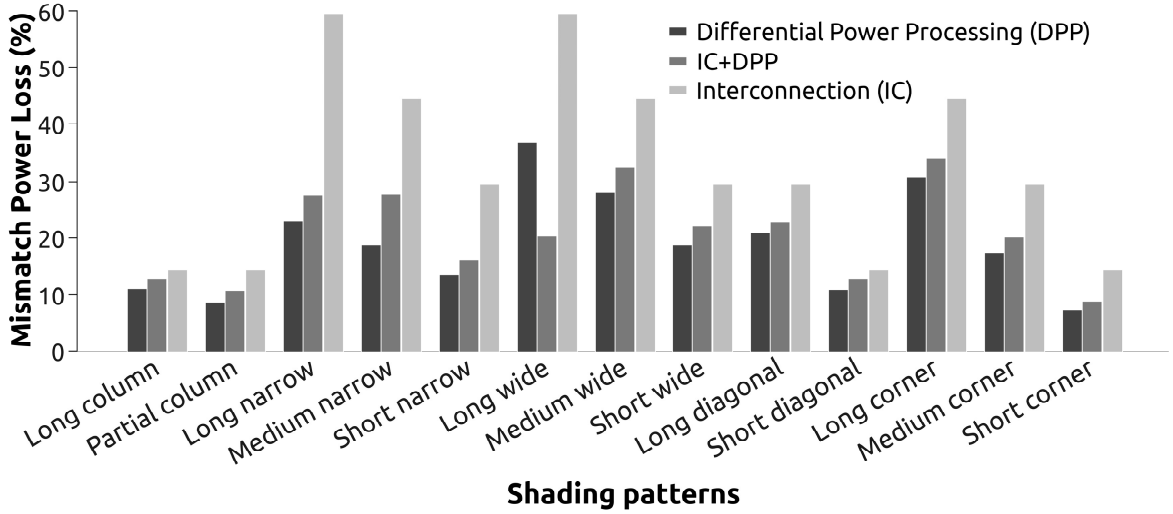
Mismatch power losses for high and low irradiance values are shown in Figures 11a and 11b, respectively.

The lower the mismatch power loss, the better. Thus, the differential power processing technique shows the best results at high irradiance levels (Figure 11a). IC + DPP always presents mismatch power losses greater than DPP, but they are less or equal to the interconnection values. The IC technique shows the worst results, losing more power due to mismatch than the other techniques.

Some shading patterns present higher mismatch power loss values than others due to the way the shadows are distributed on the photovoltaic array. Shading patterns with more shaded PVs show greater MPL values. Examples are the wide shading patterns and the long corner shading pattern. The opposite is also valid, as seen in the short corner pattern. Among the patterns with the same number of shaded panels, the mismatch power loss of DPP and IC + DPP show similar behaviors. However, the IC behavior is different: the greater the number of shaded solar panels in the same row (parallel-connected), the greater the MPL. This can be seen in the long narrow, medium narrow, long wide, medium wide, and long corner shading patterns.




(**a**)




(**b**)

**Figure 11.** Mismatch power loss indicator for: (**a**) high irradiance level (700 W/m$^2$); (**b**) low irradiance level (400 W/m$^2$).

At low irradiance level (Figure 11b), the relationship between partial-shading compensation techniques and shading patterns is the same as that shown at a high irradiance level. In general, MPL values are higher at 400 W/m$^2$ than at 700 W/m$^2$, since the difference between the shaded and unshaded photovoltaic panels is higher. The exception for the long wide pattern explained in Section 3.3.1 also occurs in this case, where IC + DPP shows a lower mismatch power loss than does DPP. The maximum mismatch power loss for DPP is 36.9%, under the long wide shading pattern.

Overall, the MPL results are in agreement with the performance ratio.

#### 3.3.3. Power Enhancement

Figure 12a,b shows the power enhancement values for high and low irradiance, respectively.

The differential power processing technique presents the best results at 700 W/m$^2$ (Figure 12a) when compared to the other shading compensation techniques, exhibiting values up to 27.9%. IC + DPP shows a significant power enhancement, but it is always lower than the DPP values. IC exhibits very low power enhancement values (nearly zero in most cases), and is the worst technique at high irradiance levels.

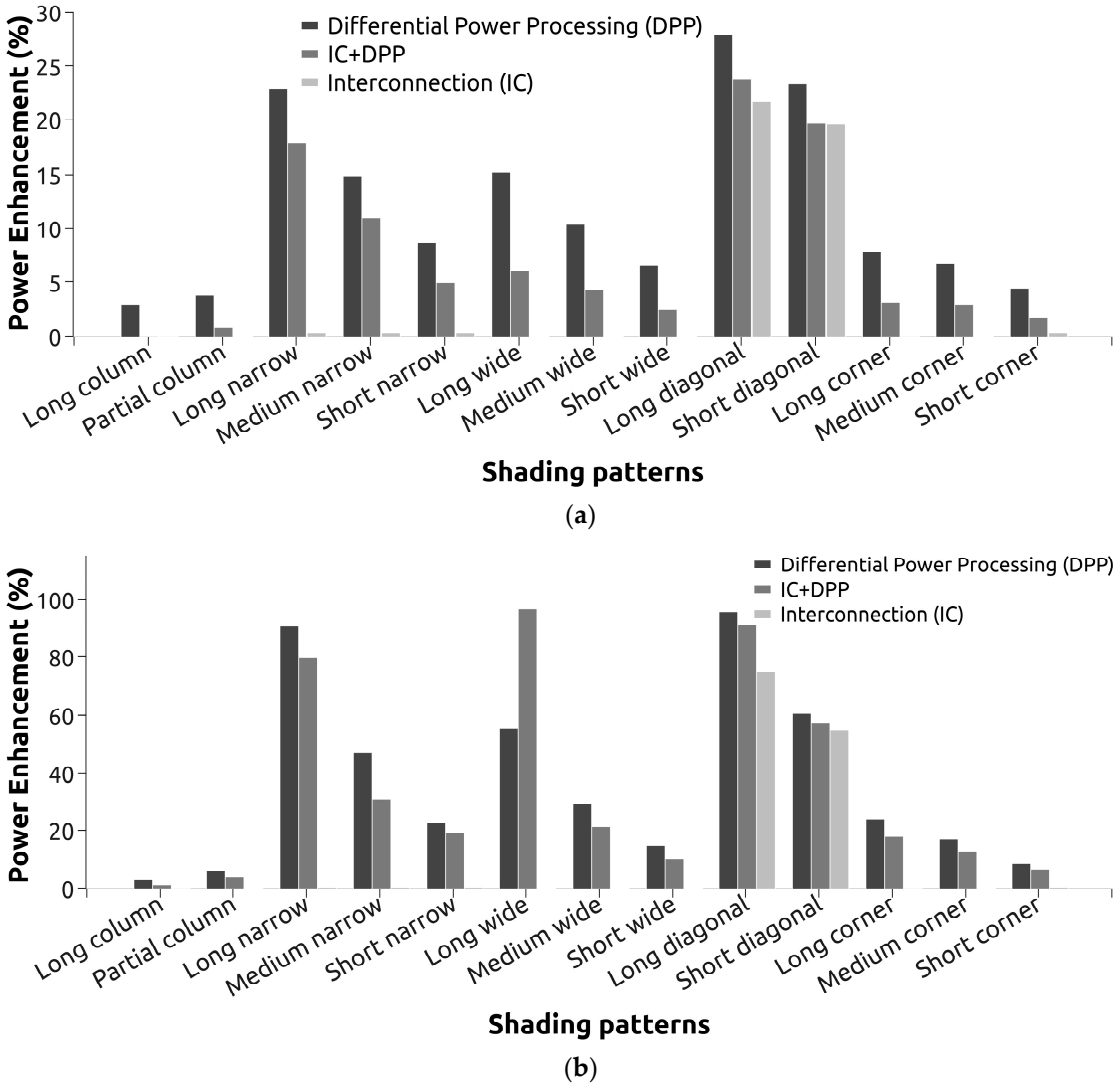



**Figure 12.** Power enhancement indicator for: (**a**) high irradiance level (700 W/m$^2$); (**b**) low irradiance level (400 W/m$^2$).

An exception occurs for diagonal shading patterns, which present significant PE values. In this shading family, power enhancement is high due to the way in which the shaded PVs are distributed in the array: all columns have just one shaded solar panel. The power enhancement indicator compares the output power of the shading compensation techniques with the output power of a common SP array. In this way, short diagonal and long diagonal patterns should yield the same power as medium narrow and long narrow patterns, respectively, in a series-parallel array. But with shaded panels concentrated in the same interconnected row, narrow patterns do not present the shading compensation advantage expected in an interconnected array, leading to low power enhancement. When diagonal shading patterns are applied to an IC array, the fact that the shadows are distributed uniformly between rows and columns leads to an advantage, as each interconnected row shows the same equivalent behavior. This results in a uniform power production over the array and high PE values for diagonal shading patterns, as shown in Figure 12a. This advantage does not occur in the long corner pattern. Despite the shadows being uniformly distributed, they cover 50% of the array, hence considerably decreasing the output power. Even so, DPP and IC + DPP present better power enhancement under these shading patterns.

When the PE values for DPP and IC + DPP are examined, it can be noted that they are similar. Narrow, wide, and diagonal patterns present the highest power enhancement values. These patterns exhibit a high number of shaded PVs; the way in which the shadows are distributed also affects the results, as explained above. In contrast, in an SP array, more shaded panels lead to lower power generation and performance, while DPP circuits (standalone or combined with IC) offer better shading compensation and higher amounts of produced power.

At low irradiance (Figure 12b), differential power processing is the best technique for all shading patterns, with PE values of up to 95.9% under the long diagonal shading pattern. There is just one exception, i.e., the condition under the long wide shading pattern. IC + DPP, as discussed earlier for high irradiance, presents high power enhancement values, but they are lower than the DPP values. The IC technique shows no power enhancement for almost all shading patterns at low irradiance. In general, the graphics in Figure 12 present the same behavior; for low irradiance, the PE values are significantly higher. This increase in power enhancement is due to the poor performance of the series-parallel interconnection when low-irradiance shadows are present on the photovoltaic array. These shadows significantly decrease the output power in traditional arrays. DPP circuits in the DPP and IC + DPP techniques can balance the power production of solar panels in a partially shaded array, thus increasing the produced power and leading to high power enhancement values at 400 $W/m^2$, which is a significant advantage for DPP and IC + DPP circuits in heavily shaded photovoltaic arrays.

## 4. Conclusions

In this work, we aimed to determine whether the combined use of a switching-inductor differential power processing circuit and a total-cross-tied interconnection scheme presents better performance than each technique alone in a small-scale photovoltaic array. A 3 $\times$ 4 array was tested using interconnection, differential power processing, and a combination of both techniques, subjected to 13 shading patterns and two irradiance levels. The performance in each case was assessed using maximum output power, performance ratio, mismatch power loss, and power enhancement indicators.

We found that the combination of an interconnection scheme and a differential power processing circuit does not present better performance than each standalone technique applied to a photovoltaic array. A standalone differential power processing technique shows better performance in a photovoltaic array than when combined with an interconnection scheme. The standalone interconnection presents the worst results under most of the test conditions and indicators evaluated in this work.

In general, the higher the irradiance received by the photovoltaic array, the higher its maximum power point, although some exceptions were found. At a high irradiance level (700 $W/m^2$), the differential power processing circuit exhibited better performance in all shading patterns tested, while the MPP of the interconnected array was the lowest in all cases. At a low irradiance level (400 $W/m^2$), the differential power processing circuit was the most efficient, except for under the wide long shading pattern. Also, the maximum power values of the combined interconnection and differential power processing technique are very close to the values of the DPP technique applied to the photovoltaic array.

The DPP presented better results for all performance indicators evaluated in this work. We found performance ratio values of up to 97% for the DPP, mismatch power losses of less than 36.9% in low-irradiance conditions, and power enhancement of up to 95.9%.

Although the IC + DPP technique uses fewer differential power processing circuits than does the standalone DPP technique, it shows lower performance compared to the DPP technique due to higher losses. These losses are caused by higher differential currents applied to the components of the DPP circuit, reducing the overall efficiency of the IC + DPP technique.

**Supplementary Materials:** The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/en17133252/s1, Figures S1–S13: P-V curves for each shading pattern and irradiance level.

**Author Contributions:** Conceptualization, E.C.G.; methodology, E.C.G.; formal analysis, E.C.G.; investigation, E.C.G.; writing—original draft preparation, E.C.G.; writing—review and editing, T.S.C. and T.M.d.S.; visualization, T.S.C. and T.M.d.S. All authors have read and agreed to the published version of the manuscript.

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