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Hierarchical Structure-Based Wireless Active Balancing System for Power Batteries

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Abstract: This paper conducts an in-depth study of a wireless, hierarchical structure-based active balancing system for power batteries, aimed at addressing the rapid advancements in battery technology within the electric vehicle industry. The system is designed to enhance energy density and the reliability of the battery system, developing a balancing system capable of managing cells with significant disparities in characteristics, which is crucial for extending the lifespan of lithium-ion battery packs. The proposed system integrates wireless self-networking technology into the battery management system and adopts a more efficient active balancing approach, replacing traditional passive energy-consuming methods. In its design, inter-group balancing at the upper layer is achieved through a soft-switching LLC resonant converter, while intra-group balancing among individual cells at the lower layer is managed by an active balancing control IC and a bidirectional buck–boost converter. This configuration not only ensures precise control but also significantly enhances the speed and efficiency of balancing, effectively addressing the heat issues caused by energy dissipation. Key technologies involved include lithium-ion batteries, battery management systems, battery balancing systems, LLC resonant converters, and wireless self-networking technology. Tests have shown that this system not only reduces energy consumption but also significantly improves energy transfer efficiency and the overall balance of the battery pack, thereby extending battery life and optimizing vehicle performance, ensuring a safer and more reliable operation of electric vehicle battery systems.

Keywords: lithium-ion battery; battery management system; battery balancing system; LLC resonant converter; wireless self-organizing network technology

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1. Introduction

With the rapid development of the electric vehicle industry, the demand for efficient, safe, and reliable battery management systems (BMSs) has significantly increased [1,2]. As the primary energy source for electric vehicles, lithium-ion batteries directly impact a vehicle's range and safety [3]. Therefore, the effectiveness of battery management systems not only determines the efficiency of vehicle operation but also has a profound impact on the sustainable development of the entire electric vehicle industry [4]. However, traditional battery balancing methods, which typically rely on passive energy dissipation methods such as resistive discharge balancing, although relatively simple in structure, are inefficient and often result in significant energy waste. These methods fail to meet the modern electric vehicle's demand for efficient energy management. As a result, developing new, efficient active balancing systems has become a critical research direction in the field of battery management [5–7].

Currently, in the research of battery management systems, both academia and industry are focused on developing more efficient energy management methods. Some studies

have introduced advanced technologies such as soft-switching techniques and resonant converters to enhance energy transfer efficiency and reduce energy losses during the battery balancing process [8,9]. These technologies have shown promising results in laboratory settings, effectively improving energy conversion efficiency and reducing internal resistance losses. However, in practical applications, these methods still face challenges such as complex wiring designs, high manufacturing costs, and insufficient system reliability, which limit their widespread adoption in large-scale battery management systems [10].

In the industrial sector, the development of battery management technologies is also advancing continuously. Leading companies such as Panasonic (Osaka Prefecture, Kadoma City, Japan), and Samsung (Seoul, Republic of Korea) SDI are actively seeking innovative solutions for battery management systems. Panasonic and Samsung SDI have also made significant progress in enhancing battery balancing efficiency and system reliability, but technical bottlenecks remain, especially in large-scale applications, where balancing stability and efficiency in complex scenarios is still challenging [11].

Compared to traditional passive balancing methods, active balancing technology has demonstrated significant advantages in battery management systems [12,13], particularly in handling large voltage discrepancies between battery cells. When substantial voltage differences occur within a battery module, active balancing technology can quickly adjust the voltage of individual cells, ensuring consistency and stability across the entire module. This approach is more efficient than traditional passive balancing as it reduces energy waste and significantly enhances the overall reliability and safety of the battery management system. As a result, active balancing technology has become a crucial component in modern battery management system design [14].

In the context of the widespread application of lithium-ion batteries (LIBs) in electric vehicles (EVs) and grid-connected energy storage systems, the limitations of traditional wired battery management systems (BMSs) have become increasingly evident. As an emerging solution, wireless battery management systems (WBMSs) have garnered significant interest within the research community. Recent studies [15–17] have not only laid an important theoretical foundation for the further development of WBMSs but have also revealed broad application prospects in areas such as electric vehicle battery health monitoring.

This paper proposes an innovative wireless hierarchical structure-based active balancing system for batteries, aimed at addressing the current challenges of low efficiency, high energy consumption, and thermal management in battery management systems by integrating wireless self-networking technology with advanced power electronics conversion techniques. This system simplifies the overall structure, reduces wiring complexity, and significantly lowers costs and weight, further enhancing the system's flexibility and reliability.

The main innovations of this study are as follows:

1. Application of wireless self-networking technology: For the first time, wireless self-networking technology is applied to battery management systems, greatly simplifying the traditionally complex wiring designs. This technology not only reduces the system's cost and weight but also enhances its scalability and adaptability, making it more flexible and reliable in various application scenarios.
2. Innovative hierarchical balancing method: A hierarchical balancing strategy is proposed, using a soft-switching LLC resonant converter for inter-group balancing and an active balancing control IC with a bidirectional buck–boost converter for intra-group balancing. This hierarchical design significantly improves the efficiency and speed of the balancing process while effectively addressing thermal management issues caused by energy dissipation, further enhancing the system's overall stability and reliability.

In summary, the wireless hierarchical structure-based active balancing system proposed in this paper demonstrates significant technological advancements in the field of battery management, particularly in improving energy management efficiency, reducing thermal management burdens, and enhancing system flexibility and reliability. This innovative design provides a new technological solution for battery management systems in electric vehicles and other applications, with broad application prospects.

2. System Scheme Analysis and Demonstration

2.1. Inter-Group Balancing Scheme Analysis and Argumentation

The objects of inter-group equilibrium are bottom-level unit groups composed of several monomers. Equilibrium topology requires energy exchange between bottom-level groups and the entire battery pack. Traditional inter-group active balancing schemes can generally be divided into two categories: one is balanced topology, derived from basic converter topology improvements; and the other is energy transfer circuits, based on passive energy storage devices combined with power switches

The switching mode of the LLC converter employed in the design belongs to soft switching. Soft switching refers to the inclusion of both zero-voltage switching (ZVS) of the primary-side MOSFET and zero-current switching (ZCS) of the secondary-side rectifier diode [18,19]. The waveforms of ZVS and ZCS are illustrated in Figure 1.

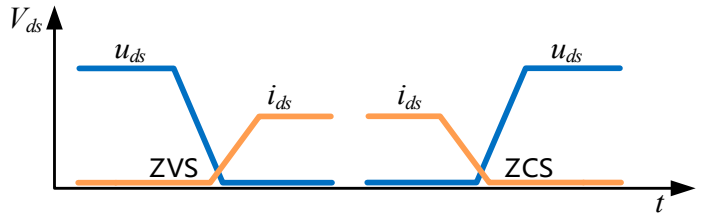


Figure 1. Switching waveforms of ZVS and ZCS in resonant converters.

For battery pack applications, the efficiency of the converter stage is one of the key factors. There are mainly two types of LLC converters: half-bridge LLC converters and full-bridge LLC converters. The primary-side switching structures of the two types are illustrated in Figure 2.

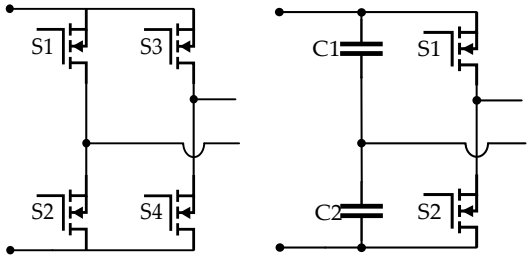


Figure 2. Full-bridge structure (**a**) vs. half-bridge structure (**b**).

In the full-bridge structure, diagonal switching transistors conduct simultaneously, while in the half-bridge structure, upper and lower transistors conduct complementarily. The operating current in the half-bridge structure is twice that of the full-bridge structure, and the root mean square (RMS) current in the half-bridge structure is four times that of the full-bridge structure. Additionally, the number of switches in the half-bridge structure is half that of the full-bridge structure, resulting in the total MOSFET conduction loss of the half-bridge structure being twice that of the full-bridge structure.

Although the half-bridge structure requires only half the primary turns for the same voltage gain and magnetic flux swing, its primary winding resistance is half that of the full-bridge structure. However, the copper loss in the primary coil of the half-bridge structure is still twice that of the full-bridge structure, and the RMS current in the half-bridge structure is four times that of the full-bridge structure [20]. A comparison between the key parameters of the half-bridge and full-bridge structures is shown in Table 1.

Table 1. Ratios of corresponding parameters between half-bridge and full-bridge structures.

I_{rms}	${I_{rms}}^2$	Number of Switching Transistors	N_p	R_{pri}	Copper Loss in the Primary Coil of Transformer
2	4	1/2	2	1/2	2

In battery balancing scenarios, there are high requirements for both switch conduction losses and copper losses. By comparing the data in the table above, to enhance the efficiency of energy transfer in high-primary-current battery balancing applications, where conduction losses dominate, the full-bridge switching circuit should be employed.

Another crucial part of the LLC converter is the selection of the secondary-side rectification structure. Based on the type of rectifier, it can be divided into synchronous and non-synchronous types. Synchronous rectification replaces the secondary-side rectifier diode with an MOSFET. Although it improves energy transfer efficiency to some extent, it introduces complexity in structure and control methods [21]. Considering the higher reliability requirements for balancers in battery balancing applications, we only present a discussion on non-synchronous rectification structures.

The commonly used non-synchronous LLC secondary-side rectification structures mainly include two types: full-bridge rectification and full-wave rectification. Their structures are illustrated in Figure 3.

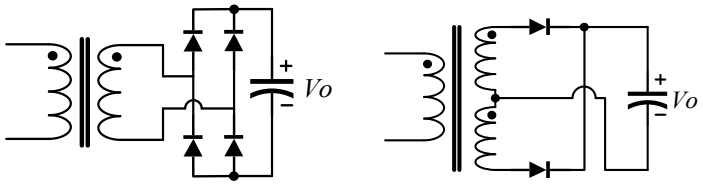


Figure 3. Full-bridge rectification (**a**) vs. full-wave rectification structure (**b**).

The rated voltage of the diodes used in full-wave rectifiers is twice that of the full-bridge rectifiers. However, since only two diodes are used in the full-wave rectifier compared to the four diodes required in the full-bridge rectifier, and because each diode in both rectifier circuits carries the same average current, the total conduction loss of diodes in the full-wave rectifier is only half that of the full-bridge rectifier.

The full-wave rectifier has two secondary windings, so the resistance for the same winding area doubles. The RMS current of each winding in the full-wave rectifier is $\sqrt{1/2}$ that of the full-bridge circuit, resulting in the total secondary winding copper loss of the full-wave rectifier being twice that of the full-bridge rectifier.

In addition, from the perspective of circuit structure, in applications requiring high output voltage, the use of a full-bridge rectifier is more suitable. This is because, compared to a full-wave rectifier, it can utilize diodes with a theoretical rated voltage half that of the full-wave rectifier. On the other hand, in applications with low output voltage and high current, employing a full-wave rectification structure is more appropriate. This is because its total conduction loss is lower, and it requires fewer components, leading to lower costs.

2.2. Intra-Module Balancing Scheme Analysis and Demonstration

The intra-module balancer is a transformer used for active balancing between individual cells within a single module. Compared to inter-module balancers, the number of intra-module transformers is higher. In order to truly replace traditional passive balancing methods, the structure of the intra-module balancer must first be sufficiently simple [22]. Additionally, its circuit structure must ensure inter-module decoupling, meaning that there should be no voltage reference relationship between the balancing circuits of different modules. Otherwise, in the case of ultra-large-scale series-connected lithium-ion battery

balancing, circuit damage may occur due to the existence of reference points with the same voltage between different modules [23].

A bidirectional buck–boost converter with integrated active balancing IC control is used for intra-cell balancing between individual cells [24,25]. By controlling the PWM duty cycle of the switching transistors, it can regulate the voltage on the target output side and control the output current, thereby achieving effective balancing. This approach is particularly suitable for applications involving large-scale individual cell grouping.

2.3. Inter-Module Wireless Communication Scheme

In the context of data communication in balancing systems, ZigBee, Wi-Fi, Bluetooth, and LoRa are common wireless communication methods. Table 2 compares these common wireless communication technologies based on key characteristics:

Table 2. Comparison of key characteristics: ZigBee, Wi-Fi, Bluetooth, and LoRa in wireless communication technologies [26].

Characteristic	ZigBee	Wi-Fi	Bluetooth	LoRa
Power Consumption	Low	High	Very low	Ultra low
Transmission Range	Medium (10–100 m)	Long (100–300 m)	Short (within 10 m)	Very long (several kilometers)
Data Transfer Rate	Medium (250 kbps)	High (hundreds of Mbps)	Medium–low (1–3 Mbps)	Low (<50 kbps)
Network Coverage	Wide (supports multi-node mesh)	Wide (covers large areas, but limited nodes)	Small (point-to-point or small networks)	Wide (covers very large areas)
Self-Organizing Capability	Strong (supports auto-configuration and adjustment)	Medium (requires manual configuration)	Weak (point-to-point connection)	Medium (supports mesh, but complex setup)
Suitable Scenarios	Ideal for large-scale, low-power wireless sensor networks	Suitable for high-data-rate, large-data-transmission scenarios	Suitable for short-range, low-power device connections	Suitable for ultra-long-range, low-data-rate IoT applications
Interference Resistance	Strong (suitable for complex electromagnetic environments)	Medium (may be susceptible to interference)	Weak (easily affected by other wireless devices)	Strong (excellent interference resistance)
Deployment Cost	Low	Medium–high	Low	Medium

The table above clearly illustrates the advantages of ZigBee in terms of power consumption, network coverage, self-organizing capability, and interference resistance, especially in large-scale battery management systems. Compared to other wireless communication technologies, ZigBee ensures system reliability and stability while effectively reducing system complexity and costs, making it the preferred choice for wireless communication in this study.

In recent years, technologies such as ZigBee have made significant progress in low power consumption and wide coverage, showing strong competitiveness in the application of battery management systems. For example, Cao et al. (2024) indicated that battery management systems using ZigBee technology have significant advantages in low power consumption and high reliability [16].

3. Hardware Design

The chosen solution employs a full-bridge full-wave rectifier LLC converter as the balancing topology. A schematic diagram of this structure is shown in Figure 4.

LLC converters offer several ideal characteristics compared to traditional hard-switching and other types of resonant converters. They feature high operating efficiency, low electromagnetic interference (EMI) emissions, and high power density, all of which are desirable traits for applications like onboard battery packs. As shown in Figure 4, the yellow box highlights the main circuit of the LLC converter, with the primary excitation energy pro-

vided by the entire battery pack [27]. The blue and black lines represent the double-switch structure used for battery gating. A high-speed switching bridge structure, consisting of power switches S1–S4, generates a square wave to excite the secondary resonant tank. The common control method for LLC converters is frequency modulation control. The resonant tank itself is designed with a resonant frequency, and under the excitation of square waves at different frequencies, the resonant tank outputs sinusoidal resonant currents that are in phase with the switching signals but with varying energy levels. The gain of the resonant tank, defined as the relationship between input and output voltage and current, measures this resonance. The output sinusoidal resonant current can be transferred through a transformer to the rectification structure, and eventually, after passing through output capacitors for smoothing and filtering, it achieves stable DC output. While the hardware structure of LLC converters is relatively simple, their parameter design involves some complexity. In the following sections, we delve into detailed discussions on the design of the resonant tank parameters and other components.

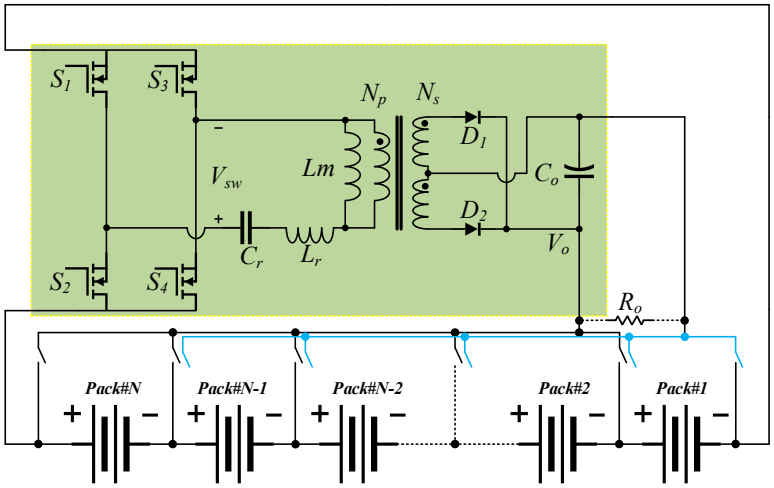


Figure 4. Top-level LLC equalization structure diagram.

(1) LLC Operating States and Key Modes

The LLC resonant converter's resonant network has two resonance frequencies. The LLC operating states are defined based on the relationship between these two resonance frequencies and the excitation frequency of the switching bridge. In the project, a full-bridge LLC converter is utilized, and its individual structure is depicted in Figure 5.

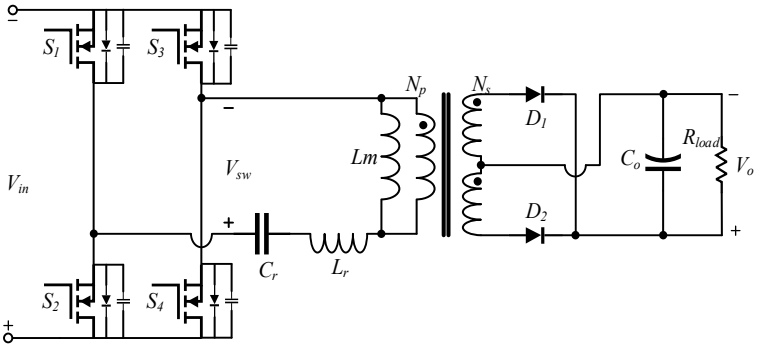


Figure 5. Full-bridge LLC converter.

As shown in Figure 5, the resonance frequency of the resonant network's resonant capacitor Cr and resonant inductor L_r is generally denoted by f_{r1}. Initially, when Cr and L_r resonate, energy is transferred from the primary side of the transformer to the secondary side. At this point, the primary-side coil is clamped due to the coupling effect of the

transformer, so the primary-side magnetizing inductance L_m does not initially participate in resonance. Therefore, only series resonance occurs at this time. The expression for the resonance frequency f_{r1} is as follows:

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

The resonant tank current over time is depicted in Figure 6.

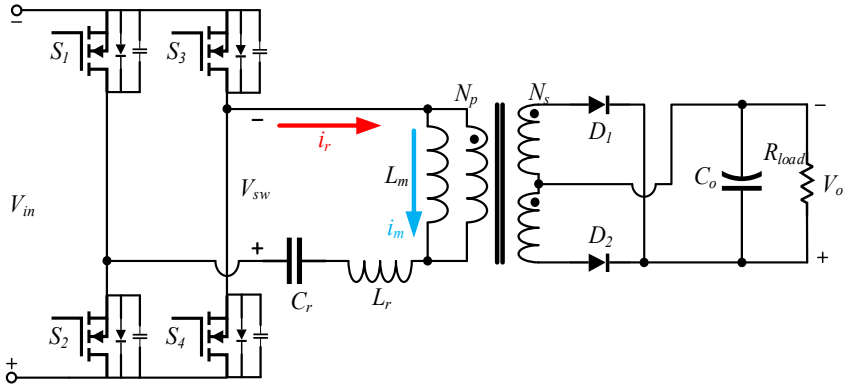
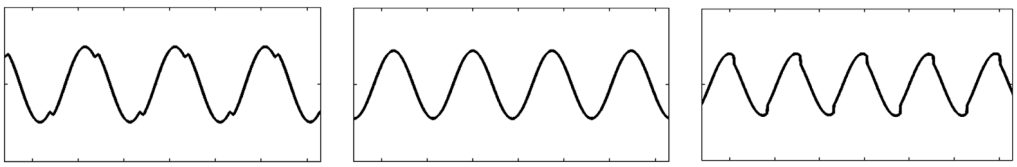


Figure 6. Initial resonant current in the resonant tank.

After the initial stage, the converter reaches a point where the resonant current i_r equals the magnetizing current i_m, as shown in Figure 6. At this point, the magnetizing inductance L_m participates in resonance, resulting in series–parallel resonance. During this stage, energy is not transferred from the primary side to the secondary side. The expression for the resonance frequency f_{r2} under these conditions is as follows:

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{2}$$

By comparing the forms of Equations (1) and (2), it is evident that f_{r2} must be smaller than f_{r1}. With the determination of these two key resonance frequencies, we can now discuss the relative relationship between the switching frequency f_s and the resonance frequencies f_{r1} and f_{r2}, leading to three operating states of the LLC converter: under-resonance ($f_{r2} < f_s < f_{r1}$), quasi-resonance ($f_s = f_{r1}$), and over-resonance ($f_s > f_{r1}$). The corresponding resonant current waveforms for these three states are illustrated in Figure 7a–c, respectively.



(**a**) $f_{r2} < f_s < f_{r1}$ (**b**) $f_s = f_{r1}$ (**c**) $f_s > f_{r1}$

Figure 7. Three operating states of the converters.

Among the three operating states mentioned above, the under-resonance state encompasses all resonance states and exhibits soft-switching characteristics. This state is the main focus of our analysis, focusing on several operating modes.

The timing waveforms are depicted in Figure 8.

The current state of mode 1 ($t_0 \sim t_1$) is illustrated in Figure 9. It is assumed that all resonance involving the output capacitors of the switching transistors is ignored, and all device characteristics are ideal.

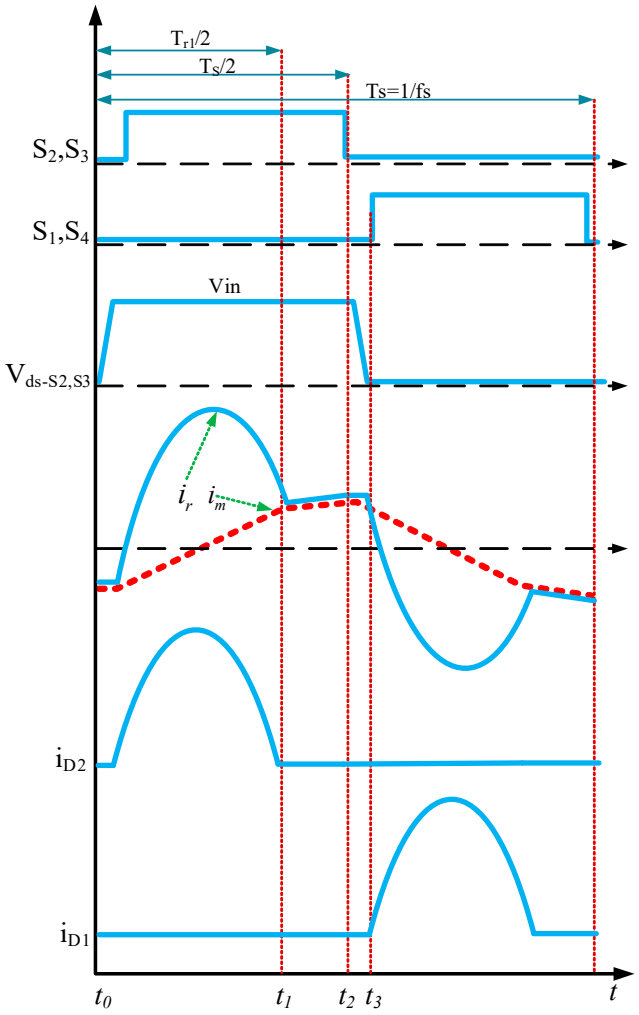


Figure 8. Timing diagram for key mode analysis.

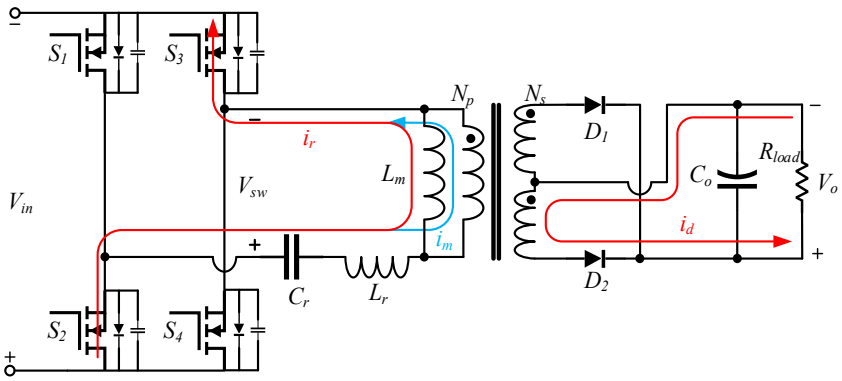


Figure 9. Schematic diagram of mode 1 current transformer.

At time t_0, the switching transistors S_2 and S_3, and the secondary-side diode D_2 are conducting. At this point, only series resonance occurs in the network. The resonant current i_r is a sinusoidal resonant current, while the magnetizing current i_m linearly increases. At time t_1, the two currents are equal, at which point the current through the secondary-side diode drops to zero, and then, reverse voltage is applied to achieve zero-current switching (ZCS). Subsequently, mode 2 is entered.

The current distribution during mode 2 ($t_1 \sim t_2$) is depicted in Figure 10.

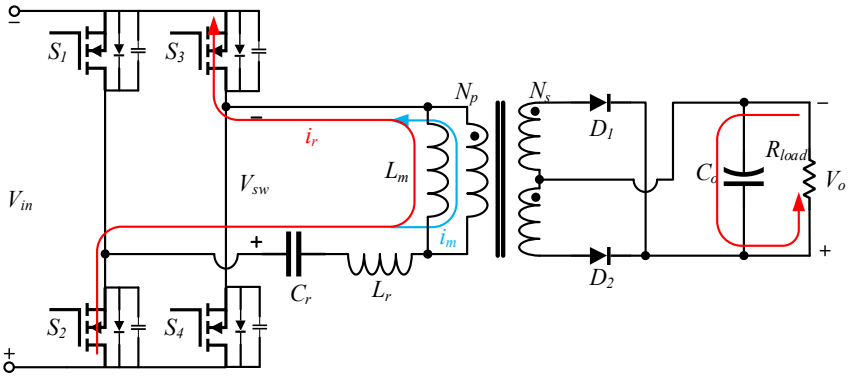


Figure 10. Schematic diagram of mode 2 current transformer.

At time t_1, the resonant current i_r equals the magnetizing current i_m. At this moment, no energy is transferred from the primary side to the secondary side, so the two arms of the rectifier bridge are in reverse-bias cutoff state. At this time, the primary-side coil participates in resonance, which is equivalent to three components undergoing series–parallel resonance. The resonance frequency at this time is f_{r2}, as mentioned earlier. Since the inductance of L_m is greater than that of L_r, the corresponding series–parallel resonance frequency is lower. This is manifested in the waveform as a decrease in slope. At time t_2, S_2 and S_2 are turned off, entering mode 3.

The current distribution during mode 3 ($t_2 \sim t_3$) is depicted in Figure 11.

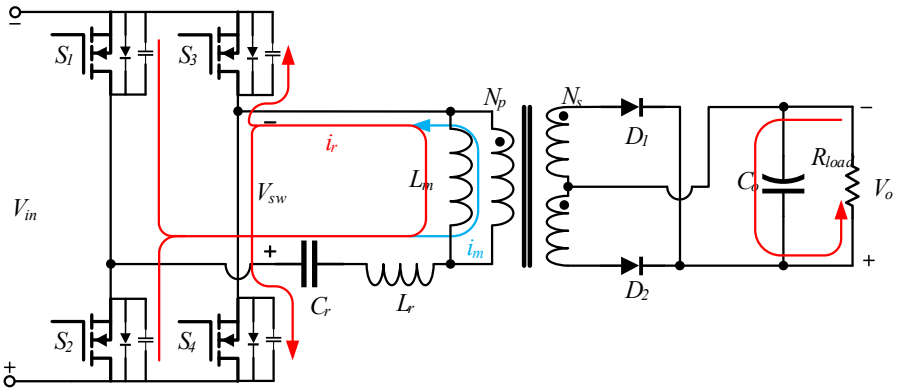


Figure 11. Schematic diagram of mode 3 current transformer.

This is one of the most critical modes involving soft switching. At time t_2, all switches enter the off state. At this moment, the resonant current does not experience any sudden changes. It charges the output capacitors of S_1 and S_4 according to the path shown in the figure, while discharging the output capacitors S_2 and S_3. The dead time should be greater than the time it takes for the output capacitors to discharge to zero. Discharging to zero provides the basic condition for zero-voltage switching (ZVS) during the next switch-on. ZVS is the second soft-switching state that LLC converters possess, following ZCS. This period of time is of significant engineering reference value for embedded chips. By applying Kirchhoff's current law (KCL) and solving differential equations, we can derive an approximate expression for the minimum time required for the output capacitors to discharge to zero, as shown in Equation (3).

$$\Delta t = \frac{2C_{ds}V_{in}}{i_r(t_2)} \tag{3}$$

In the equation, C_{ds} represents the output capacitance of the switch. The dead time generally lasts for a short duration. Therefore, the current remains approximately constant during this period. Thus, the current at time t_2 is taken as the value of the current during the

entire dead time for calculation purposes. Subsequently, at time t_3, the converter enters the zero-voltage switching (ZVS) stage and transitions to the subsequent mode. The analysis in this stage is similar to the above and will not be reiterated here.

(2) LLC Parameter Calculation

LLC parameter calculation relies on the derived expressions mentioned earlier. The main design process flowchart is depicted in Figure 12. The design process starts with the selection of Q and m values, which are used to determine the specifications of the resonant circuit. Subsequently, iterative calculations are performed to ensure that the maximum DC gain meets the required specifications. At each step, various loss factors in the actual design are also considered, and parameters are adjusted to optimize performance. Finally, all key parameters are verified to ensure the effectiveness and reliability of the design.

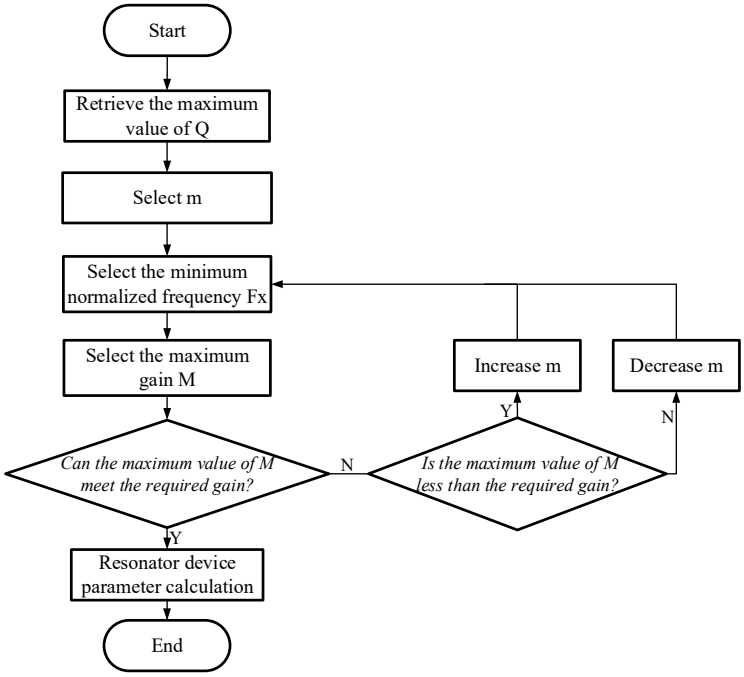


Figure 12. Flowchart of LLC parameter design process.

The basic parameters of the battery pack are shown in Table 3.

Table 3. Basic parameters of the battery pack.

Monomer type	Ternary Lithium Battery
Monomer encapsulation type	18,650
Monomer nominal voltage	3.7 V
Monomer nominal capacity	2600 mAh
Bottom-level grouping number	5
Number of battery cells in series	20

The input voltage of the LLC converter is equal to the total voltage of the battery pack. Its nominal value is 74 V, with the maximum value calculated using the fully charged voltage of 4.2 V, resulting in 84 V. The minimum value is calculated using the undervoltage of individual cells at 3.4 V, resulting in 68 V. Each group consists of four 18,650 lithium-ion cells. Based on calculation with the individual cell voltages mentioned earlier, the maximum value is 16.8 V and the minimum value is 13.6 V. The maximum charging current of the battery pack is taken as 2 C, which is 5.2 A.

The input voltage range of the LLC converter is taken as 70–94 V, and the output voltage range is 14–16.5 V. The output voltage ripple requirement is not high and is set at a maximum

of 1 V. The maximum output current is 5 A, resulting in a maximum output power of approximately 83 W. The series resonant frequency of the converter is set at 100 kHz.

Firstly, we need to determine the turns ratio N of the transformer. The turns ratio of the transformer must satisfy the condition that the minimum output voltage can be obtained at the maximum input voltage. Calculating according to Equation (4), we obtain N to be approximately 6.7. Considering the voltage drop caused by the rectifier bridge diodes, the voltage drop in the switching transistor, and other parasitic parameters, we take N as 6 in the actual design to compensate for these losses.

$$N = \frac{V_{in\max}}{V_{o\min}} \tag{4}$$

Then, the DC gain range needs to be determined, that is, to solve for $M_{\min}$ and $M_{\max}$, which are calculated according to the formulas shown in (5).

$$\begin{aligned} M_{\min} &= \frac{V_{o\min} N}{V_{in\max}} \\ M_{\max} &= \frac{V_{o\max} N}{V_{in\min}} \end{aligned} \tag{5}$$

Substituting into Equation (5), we finally obtain $M_{\min} \approx 0.894$ and $M_{\max} \approx 1.414$.

Next, the equivalent load impedance R_{ac} is calculated using the transformed expression derived earlier, as shown in Equation (6).

$$R_{ac} = \frac{8N^2}{\pi^2} R = \frac{8N^2 V_o^2}{\pi^2 P_o} \tag{6}$$

When V_o is at its minimum value, the minimum equivalent secondary-side resistance is calculated to be $R_{ac\min} = 68.9\ \Omega$. When V_o is at its maximum value, the maximum equivalent secondary-side resistance is calculated to be $R_{ac\max} = 95.72\ \Omega$.

Taking $Q_{\max} = 0.6$ and $m = 6.3$, the values are not directly calculated here. Instead, a set of Q and m values is first chosen according to the method shown in Figure 12. Then, after calculating all the parameters, the maximum DC gain corresponding to $Q_{\max}$ is verified to determine whether the selected values should be used.

Next, we first solve for the minimum normalized resonant frequency value $F_{X\min}$. According to the curves corresponding to different Q values shown in Figure 12, when Q and m are fixed, there is a unique curve corresponding to them. When the curve is at its gain peak, the corresponding normalized resonant frequency is $F_{X\min}$. Therefore, $F_{X\min}$ can be calculated according to the following equation:

$$\frac{d}{dF_X} M(F_{X\min}, m, Q_{\max}) \Big|_{Q_{\max}=0.6, m=6.3} = 0 \tag{7}$$

$F_{X\min}$ is approximately 0.667. At this point, we can also calculate the boundary switching frequency $f_{s\min}$ of the converter's capacitive–inductive working region, $f_{s\min} = F_{X\min} \times f_r = 66.7$ kHz.

Next, we verify whether the selected Q and m values can meet the gain requirements of the converter. Directly substituting $Q_{\max}$, m, and the obtained $F_{X\min}$ into the DC gain expression, we find that the DC gain at this point is approximately 2.34, which is greater than $M_{\max} \approx 1.414$. Therefore, the selected Q and m values meet the design requirements without the need for further iteration.

Next, we calculate the values of the resonant components by solving the system of equations below:

$$\begin{cases} Q_{\max} = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac\min}} \\ f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \\ m = \frac{L_r + L_m}{L_r} \end{cases} \tag{8}$$

We obtain $C_r = 0.32$ μF, $L_r = 7.94$ μF, and $L_m = 50$ μH.

The LLC power supply input side is structured as a full bridge. The maximum withstand voltage at the primary side is around 90 V. Considering the dynamic situation of the full bridge where two closed bridge arms simultaneously withstand the voltage of the battery pack, the voltage tolerance of each switch needs to be greater than 90 V. Additionally, we need to calculate the effective value of the current flowing through the switch devices. Assuming a converter efficiency of 95%, the calculation expression is as follows:

$$I_{rms} = \frac{P_o}{\eta V_{in}} \tag{9}$$

The calculated effective current is approximately 1.2 A. Based on the above calculation results, the UMW15N10 N-channel MOSFET from UMW company (New Taipei City, Taiwan, China) is selected. Its single-device breakdown voltage is 100 V, which is approximately twice the safety threshold when both bridge arms withstand the voltage. Its on-state resistance R_{dson} is approximately 60 mΩ, and its maximum continuous drain current capability is 10 A.

For the resonant inductor, a discrete design is adopted instead of using transformer leakage inductance. The inductance is chosen as an integer value of 8 μF based on the theoretical value calculated earlier. The PQ2020 magnetic core is selected. The peak resonant current obtained earlier is approximately 1.7 A. The total area and number of turns of the coil are calculated according to the following formula. In actual wires, the effective cross-sectional area decreases due to the skin effect when passing high-frequency currents. This reduction is generally measured using the skin depth δ, as expressed in Equation (10).

$$\delta = \sqrt{\frac{\rho}{\pi \mu_0 \mu_r f_{\mathrm{smax}}}} \tag{10}$$

The maximum switching frequency is calculated under the condition of maximum output voltage at no load and maximum input voltage, resulting in approximately 115 kHz. It is appropriately rounded up to 125 kHz for calculation. Here, $\rho = 1.75 \times 10^{-8} (\Omega \cdot \mathrm{m})$ represents the electrical conductivity of copper, $\mu_r = 1$ represents the relative permeability, and $\mu_0 = 4\pi \times 10^{-7} (\mathrm{H/m})$ represents the vacuum permeability. The calculated skin depth is approximately 0.443 mm. The wire diameter should be less than half of the skin depth, so a wire diameter of 0.2 mm is selected.

The formula for the number of turns is expressed as Equation (11).

$$N_L = \frac{I}{\pi (\frac{d}{2})^2 J} \tag{11}$$

The number of turns of the inductor coil wire is approximately 120, calculated using the formula, where d is the wire diameter (0.2 mm); J is the current density coefficient, typically taken as the empirical value of 450 A/cm^2; and I is the peak current (1.7 A).

Transformer design generally employs the AP method, which considers factors such as operating frequency, magnetic flux density, and core losses. Since an external discrete resonant inductor is used, minimizing magnetic leakage and flux leakage in the transformer core is important. The PQ-type magnetic core is selected. The AP factor is defined as the product of the core cross-sectional area A_e and the window area A_w, calculated using the formula shown in Equation (12), with units in cm^4.

$$AP = \sqrt[3]{\left(\frac{P_{\mathrm{o}}}{k \Delta B f_s}\right)^4} \tag{12}$$

In Equation (12), k represents the window utilization factor, typically ranging from 0.15 to 0.4. Here, we take k = 0.3 for calculation purposes. ΔB denotes the rate of change of magnetic flux density, which depends on the magnetic core material and structural

dimensions. A value of 300 mT is commonly chosen based on engineering experience. The calculated AP value is approximately 19.4 cm^4. Selecting the PQ3230 magnetic core meets the requirements.

After selecting the magnetic core, the number of turns for the secondary coil is calculated according to Faraday's law of electromagnetic induction, as shown in Equation (13).

$$N_s = \frac{V_o}{2\Delta B A_e f_{s\min}} \tag{13}$$

The magnetic core has an A_e value of 80 mm^2. Assuming the lowest switching frequency, the calculated number of turns for the secondary coil is approximately 5. Using the turns ratio, the number of turns for the primary coil is determined to be 30 turns. The skin depth can be calculated based on the results of the resonant inductor calculated earlier. Using a wire diameter of 0.2 mm, the number of strands is calculated according to Equation (11), resulting in approximately 120 strands for the primary side and about 500 strands for the secondary side.

4. Software Design

4.1. Implementation of LLC Balancing Digital Controller Code

The LLC digital controller board employs a state machine as the scheduling core, with the state transition diagram shown in Figure 13.

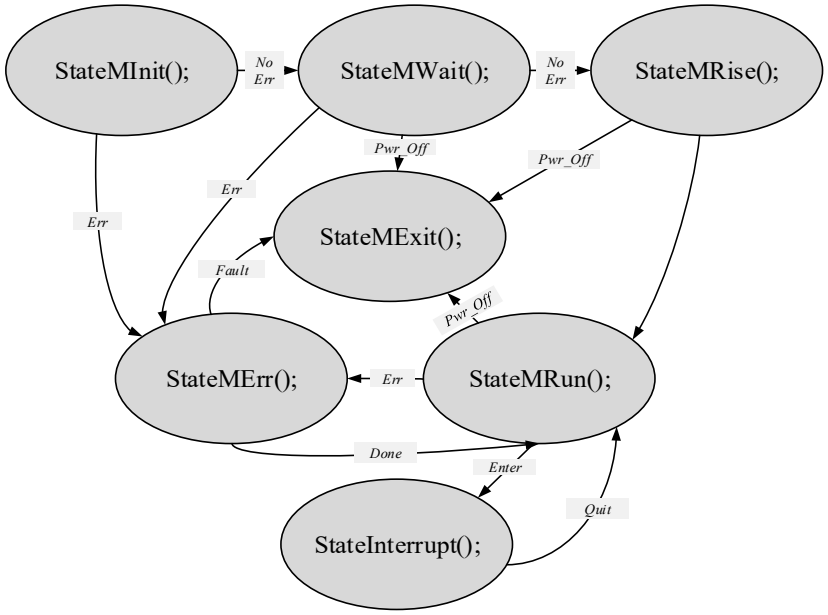


Figure 13. State transition diagram of the LLC equalizer.

The meanings of the states involved in Figure 13 are explained in Table 4.

Table 4. State interpretation table.

Status	Meaning
StateMInit();	Power supply initialization state
StateMWait();	Power supply waiting for self-check state
StateMRise();	Soft start state
StateMRun();	Power supply operational state
StateMErr();	Power supply error state
StateInterrupt();	Interrupted state
StateMExit();	Standby state

The interpretations of the state transition conditions are shown in Table 5.

Table 5. State transition condition interpretation table.

State Transition Condition	Meaning
No Err	No error
Err	Error
Fault	Non-recoverable fault
Done	Fault clearance
Pwr_Off	Power-off state
Enter	Interrupt trigger
Quit	Interrupt exit

After LLC power-up, it initially enters the initialization state. This program segment is mainly responsible for configuring the initial-state parameters of the LLC power supply, including the configuration of various protection thresholds. The waiting state comes after the initialization configuration is completed, where all register configurations are ready. It waits for a period of time to ensure that the digital power supply is stable and free of faults. Additionally, it waits for the balance status indication code from the wireless module. If balancing is required, it decides whether a power soft start is necessary. Once in the soft start state, the microcontroller outputs a variable-frequency PFM wave to control the power supply for a slow start. After starting, control is handed over to the PI loop, and it enters the running state. In the running state, it is responsible for updating some displayed power status information and waiting for periodic interrupt signals. When an interrupt occurs, it enters the interrupt function to obtain power parameters.

The interrupt state consists of two different rate interrupts: one with a period of 20 µs (fast interrupt) and the other with a period of 5 ms (slow interrupt). The fast interrupt is mainly responsible for obtaining the voltage and current results measured by ADC, while also protecting against various abnormal conditions. The workflow for both interrupts is illustrated in Figure 14.

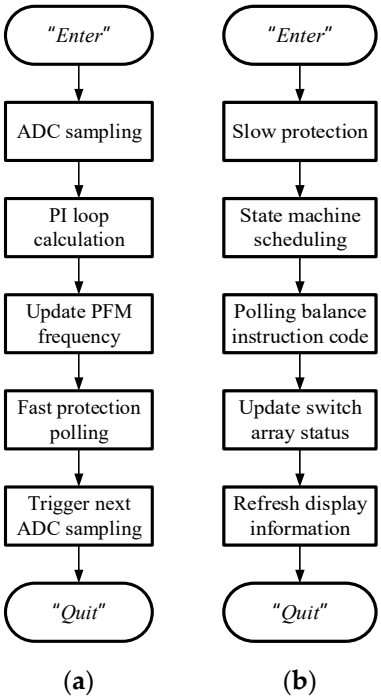


Figure 14. Interrupt execution flow. (**a**) 20 µs interrupt execution flow. (**b**) 5 ms interrupt execution flow.

The exit state is engaged when the system experiences power loss to perform certain tasks, such as saving critical balancer data. Alternatively, it transitions to the power exit

state when a general error state becomes unrecoverable. Once critical information is saved, no further actions are taken.

4.2. Balancing Strategy Formulation

4.2.1. Criterion Selection

In addition to having a rational hardware scheme, a battery balancing system also requires a complementary scheduling strategy to achieve efficient system operation.

Firstly, it is necessary to select the balancing criteria for lithium-ion batteries. This project proposes adopting a hierarchical system. At the bottom level, individual active balancing circuits controlled by active balancing IC are planned to achieve energy transfer. Active balancing IC can accurately execute active balancing based on individual voltage errors, so at the bottom level, individual voltage is used as the balancing criterion.

For top-level inter-group balancing, there can be multiple choices for balancing criteria, including individual open-circuit voltage (OCV), individual capacity, and state of charge (SOC). Since the most direct indicator of remaining battery capacity is SOC, SOC is the ideal balancing criterion. However, SOC cannot be directly obtained [28]. SOC can be estimated by measuring the open-circuit voltage (OCV) in a static state. Furthermore, the ampere-hour integration method can also be used for online SOC estimation. It does not concern the internal electrochemical characteristics of the battery but only focuses on the external characteristics of battery charging and discharging [29]. It is calculated by measuring the current flowing into and out of the battery per unit time and integrating according to the definition of SOC, as shown in Equation (14).

$$SOC(t) = SOC(0) - \frac{1}{Q_n}\int_0^t \eta I(\tau)d\tau \tag{14}$$

Formula (14) represents the state of charge (SOC) of a single cell in terms of its initial residual charge $SOC(0)$, rated charge capacity Q_n, and the current flow I into or out of the battery. In this equation, I is negative during charging, representing the current flowing into the battery, and positive during discharging, representing the output or discharge current. η is the Coulomb transfer efficiency coefficient, which signifies the degree of internal energy loss of the battery during the charge–discharge process.

4.2.2. Balancing Scheduling Strategy

The scheduling strategy plays a crucial role in achieving a balance between balancing speed and efficiency.

In this project, a hierarchical structure is proposed as the composition of the entire battery pack, complemented by two sets of active balancing systems. The bottom-level active balancing system is designed to use single-cell voltage as the criterion for active balancing circuits, while the top-level adopts a digital LLC converter as the active balancing energy transfer link.

Here, we primarily discuss the balancing criterion for the top-level LLC balancing section. Following the earlier discussion, SOC is chosen as the criterion for top-level balancing. Even if other criteria are selected, the balancing scheduling logic remains consistent, aiming to align the criteria towards consistency. Additionally, all criteria are positively correlated, ensuring a uniform balancing approach. Here, we focus our discussion solely on SOC as the subject of analysis.

In Equation (15), the variance s^2, the range of individual cell criteria δ_1 during equalization, and the deviation $\delta_{2,i}$ of the individual criterion from the criterion mean are typically used. $\delta_{2,i}$ represents the deviation of the criterion of the i-th equalization battery cell from the criterion of the remaining equalization battery cells. In practical use, δ_1 and $\delta_{2,i}$ are generally combined to make scheduling decisions for the equalization system's resources.

$$\begin{cases} \overline{SOC} = \sum_{i=1}^{n} SOC_i \\ \delta_1 = SOC_{\max} - SOC_{\min} \\ \delta_{2,i} = SOC_i - \overline{SOC} \\ s^2 = \sum_{i=1}^{n} \delta_{2,i}^2 / n \end{cases} \tag{15}$$

SOC_i represents the SOC of the i-th balancing battery cell; $\overline{SOC}$ is the average SOC of all balancing units; SOC_{max} and SOC_{min} are the maximum and minimum values of the criterion in the balancing units, respectively. The initiation and termination of balancing can be determined by the range δ_1 and a specified range threshold ΔSOC_1. Balancing is initiated when $\delta_1 > \Delta SOC_1$; otherwise, balancing is terminated.

Additionally, in balancing topologies where energy can flow bidirectionally, determining which cells to charge and which to discharge can utilize $\delta_{2,i}$ as a criterion. By specifying a threshold ΔSOC_2, and taking the average of the balancing cell criteria as the median of the variation, when $\delta_{2,i}$ falls within the interval $[\overline{SOC} - \Delta SOC_2, \overline{SOC} + \Delta SOC_2]$, the i-th cell neither charges nor discharges. It remains completely disconnected from the balancing loop. If $\delta_{2,i}$ is on the right side of this interval, the i-th cell performs discharge operations; if it is on the left side, passive charging operations are executed.

Considering the complexity of actual batteries during vehicle operation, the timing of balancing is crucial. Balancing timing can generally be divided into two categories: charging balancing and vehicle start-up discharge balancing. Given the complexity of vehicle operating conditions and the instability of current during operation, several ineffective balancing operations may occur. To maintain battery consistency while reducing unnecessary energy transfers, balancing timing typically selects the battery charging phase and the vehicle deceleration and stop phase. Balancing during deceleration and stop is recommended because the current gradually decreases, and the current value is relatively stable. Balancing performed promptly during these stages effectively addresses any inconsistencies in battery conditions that arise during operation.

4.2.3. Equalization Scheduling Process

The equalization process is primarily divided into two parts: charging state equalization and equalization during vehicle stop and idle periods. When the battery pack enters the charging equalization waiting state, if any equalization battery cell is fully charged, the charging equalization is immediately initiated. The entire pack charges the cells with lower SOC at this time, sequentially, until the conditions for initiating equalization are no longer met, and the charging equalization is exited. When the vehicle stops and the battery pack enters the idle state, the parking equalization is immediately initiated. The parking equalization continues until the conditions for stopping equalization are no longer met. When the vehicle is in the startup state, the bottom-layer active equalization between individual cells should be turned off to avoid multiple ineffective equalizations, which would reduce the battery's charge and discharge lifespan and increase unnecessary energy loss. The complete equalization execution process is illustrated in Figure 15.

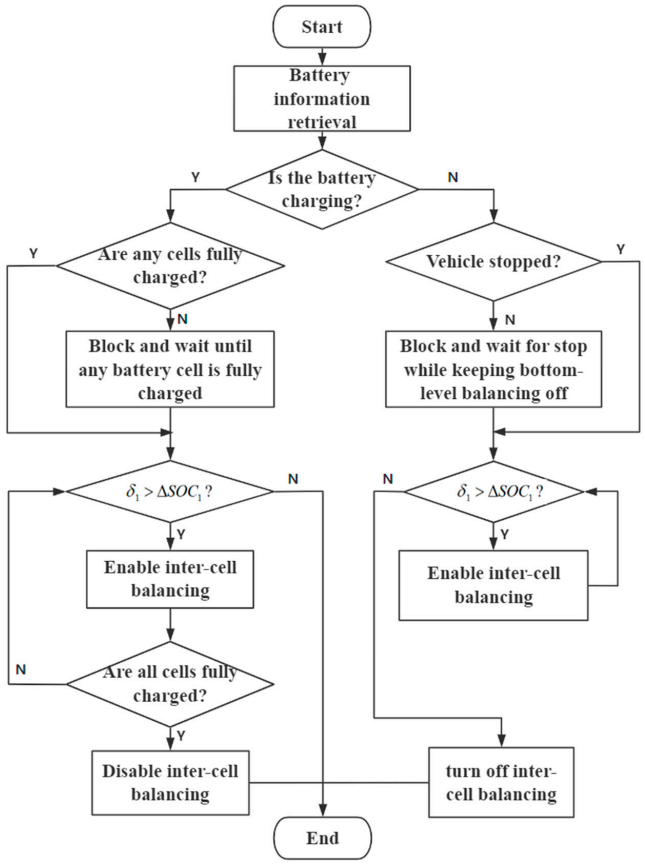


Figure 15. Hierarchical equalization system scheduling flowchart.

4.3. Wireless Communication Software Design

4.3.1. Comparison of Wireless Networking Topologies

The wireless networking involved in the design encompasses terminal devices, each representing a bottom-level battery pack. Depending on the scale of the battery pack, it can consist of varying numbers of bottom-level groups. ZigBee 3.0 supports multiple network topologies, each corresponding to different scales of devices. Here, we primarily discuss two networking topologies.

(1) Star Network

The star network is the most basic and commonly used topology, as depicted in Figure 16.

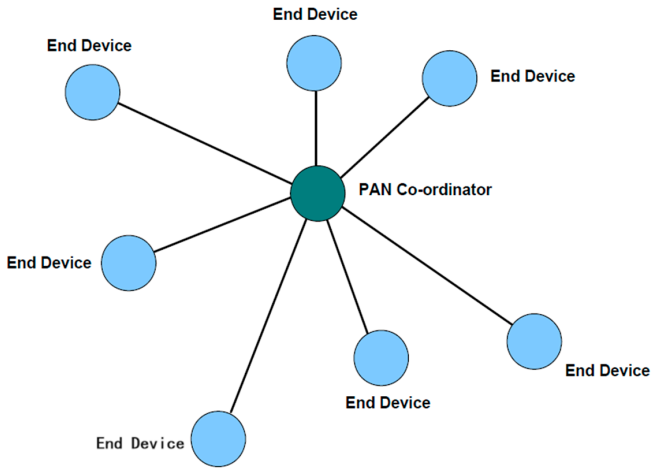


Figure 16. Star network topology.

This topology offers the highest efficiency in protocol stack communication execution. It is relatively easy to locate and diagnose faulty nodes, and nodes can be easily added or removed. As it does not involve routing devices, the network scale is limited. In NXP's ZigBee module, the star network topology supports up to 256 nodes, making it suitable for small-scale applications.

(2) Mesh Networking

To address scenarios with a larger number of devices, the ZigBee 3.0 protocol stack provides comprehensive software support for mesh networking. This mode supports self-organizing networks with a very large number of devices, theoretically accommodating up to 65,536 groups of devices, which is the maximum allocatable PANID. However, the actual number of devices that can be connected is influenced by factors such as communication efficiency and wake-up speed, typically being less than this value. The topology of this network is as follows. The topology of this network is as shown in Figure 17.

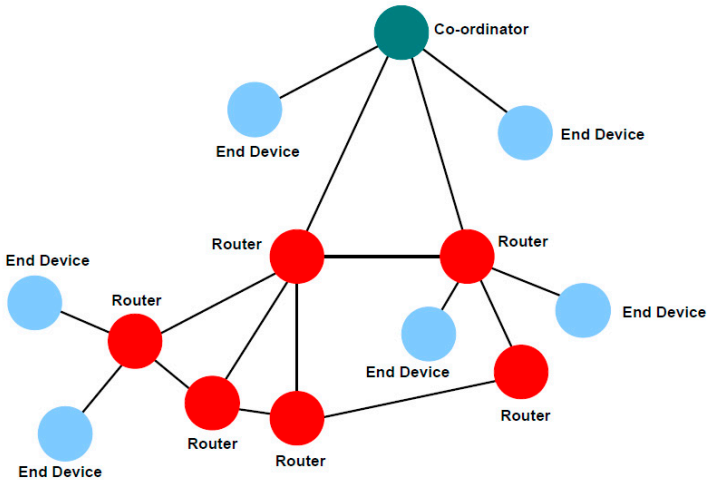


Figure 17. Mesh network topology.

In summary, the star topology suffices to meet the networking requirements of automotive power battery packs, enabling efficient sensor networking with minimal power consumption. If there is a need for larger-scale networking, mesh networking can be easily implemented through software upgrades.

4.3.2. Inter-Module Wireless Node Software Design

The top-level wireless module is primarily responsible for acquiring relevant data from the lower-level node groups through a designated broadcast protocol and processing the data from the lower-level groups. It then determines whether balancing is required. If balancing is necessary, it sends trigger information to the LLC digital control board via a serial port. The LLC control board retrieves the balancing instruction code during its 5 ms polling interval, and then, proceeds with a series of preparations to initiate balancing among the lower-level groups.

The top-level wireless communication protocol is a key focus of the design. Unlike the traditional wired CAN bus device polling mode for information retrieval, it can achieve device communication time alignment through ZigBee's broadcast mode. Sub-devices can actively upload their battery pack data after receiving a unified broadcast beacon, following a specified delay. This eliminates the occurrence of a system bus deadlock that can happen with polling-based data retrieval, where if a sub-device fails to respond due to a fault, the system bus becomes stuck. The workflow diagram for delayed communication is shown in Figure 18. The central wireless module needs to coordinate with the lower-level wireless modules. The wireless node numbered 1 in the lower-level group responds to the broadcast beacon, delays for 5 ms, and then, continues to receive until completion after receiving the broadcast beacon.

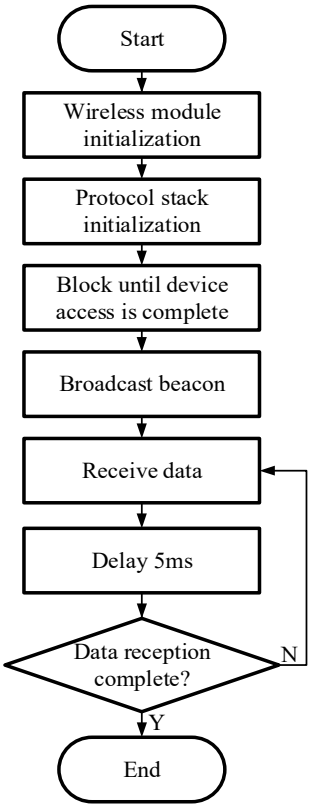


Figure 18. Top-level central wireless node operational flowchart.

The lower-level groups transmit data to the top-level central node through wireless modules according to a predefined protocol. Each node in the lower-level group can receive broadcast messages, and then, initiate different delays based on their device number, with the reception beacon as the time reference point. The delay intervals between adjacent numbered devices are set to 8 ms, coordinated with the 5 ms interval above. Each round of broadcast beacon issuance recalibrates the reference point, so the offset effects of different device clocks can be ignored.

In addition to responding to the central node's broadcast messages, lower-level nodes also need to read individual cell voltage information and bottom-level group current information through the I^2C bus, estimate the SOC within the group, and package the data into protocol frames for upload.

Simultaneously, they need to respond to special scheduling situations from the central node, controlling the initiation and shutdown of active balancing within the group. These are all the functionalities of the lower-level wireless nodes. The design of the entire wireless architecture adopts a distributed computing approach, where decision-making processes are deployed hierarchically across each node for computation. After completion, the results are aggregated to the central node, which also helps alleviate the computational burden on the LLC digital controller. The central node is responsible for making balancing decisions, transmitting concise balancing codes to the top-level balancer, which then executes corresponding balancing operations based on validated instruction codes.

5. System Testing

5.1. LLC Digital Power Board Testing

To validate the theoretical analysis and calculations presented earlier, a PCB was designed, manufactured, and debugged. The physical circuit board of the digital power supply is shown in Figure 19. Additionally, the wireless module plugged into the digital power control board also possesses computational capabilities, serving as the central node in the entire battery group network.

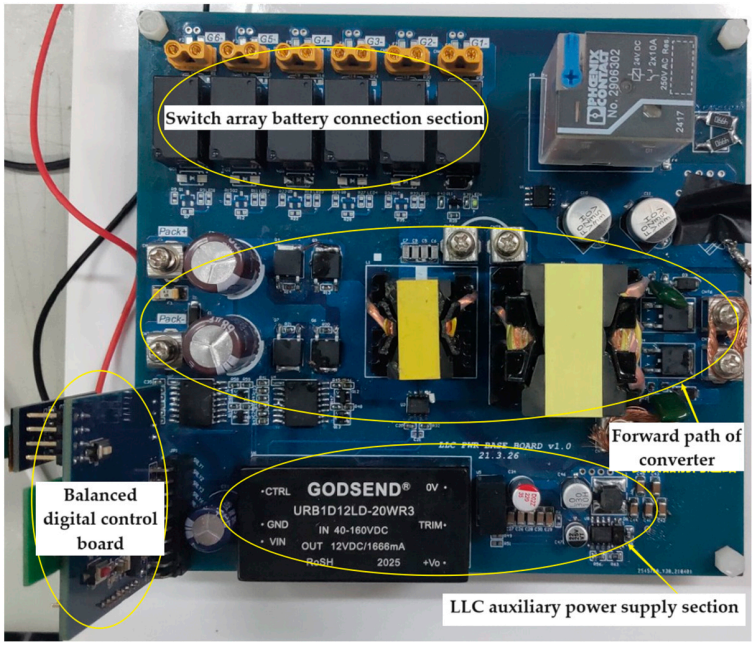


Figure 19. Physical circuit image of LLC equalization converter.

A high-voltage programmable power supply was used as the input terminal for the LLC balancing board to simulate the battery pack (see Figure 20). An electronic load was employed to simulate the bottom-level battery group. Key waveform tests were conducted under different load conditions. The input voltage of the high-voltage power supply was set to 90 V. Firstly, tests were conducted on the fabricated resonant power supply to verify the specific operating frequency under quasi-resonant working conditions. Figure 21 shows the actual resonant frequency in a quasi-resonant state at 110.4 kHz. This frequency demonstrates the efficiency and performance of the system under different load conditions, validating the designed operating frequency.

Next, the power supply is tested under certain input voltages with loads. The designed input voltage range for the converter is from 70 V to 94 V, and the input voltage for testing is set at 85 V. The following waveform graphs depict key waveforms under load conditions. In the waveform graphs, V_{sw} represents the voltage at the midpoint of the two bridge arms, V_d represents the voltage waveform of the output rectifier diode, and V_{c_r} represents the voltage waveform at the terminals of the resonant capacitor.

The key waveforms of the LLC balancing converter with a 10% load are shown in Figure 22.

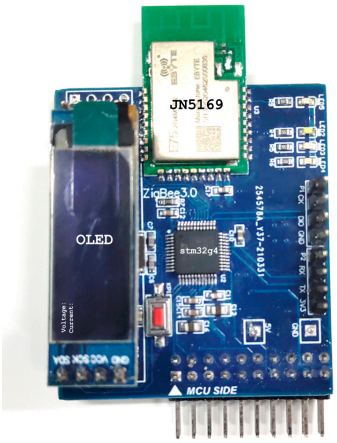


Figure 20. LLC equalization digital control board.

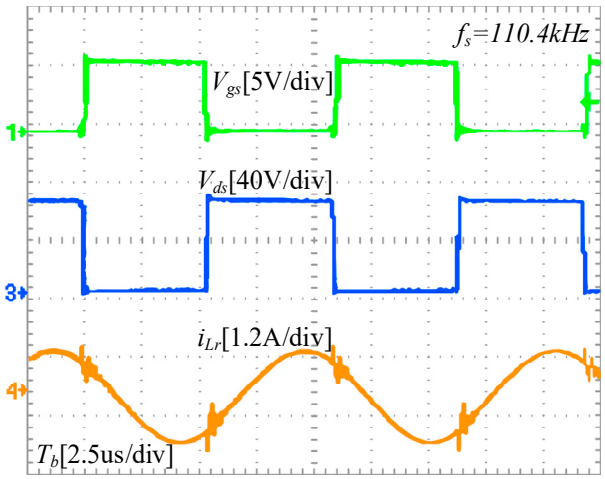


Figure 21. Actual resonant frequency in quasi-resonant state testing.

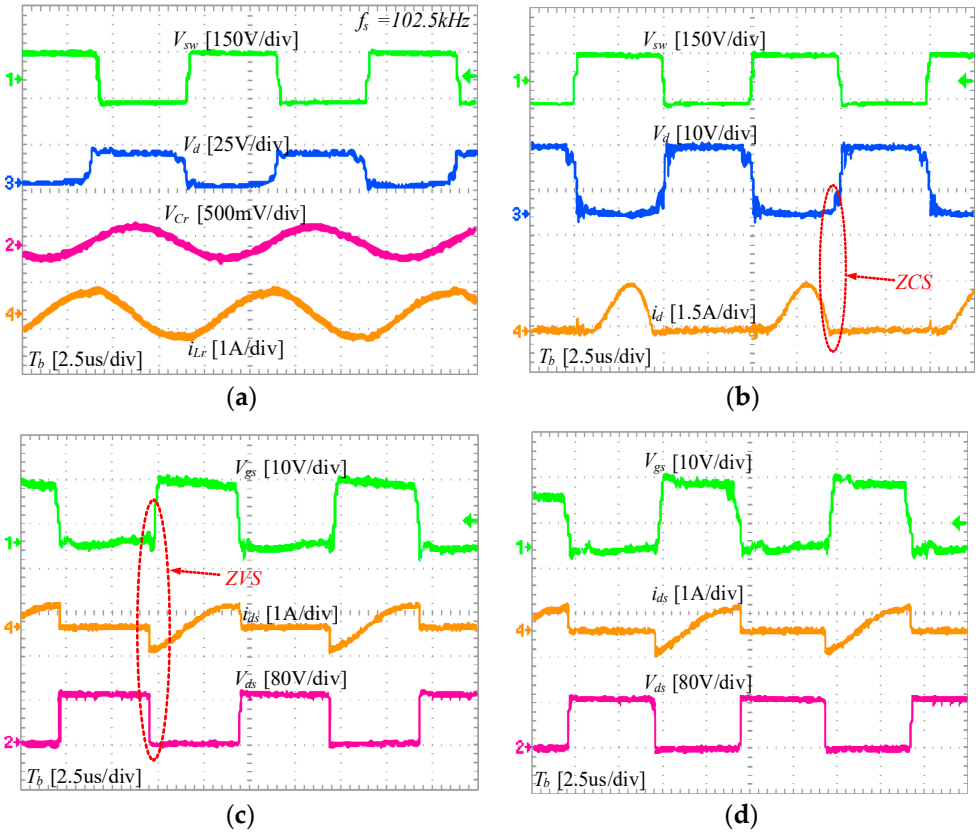


Figure 22. Key waveforms at 10% load. (**a**) Resonant tank waveform. (**b**) Secondary-side diode waveforms. (**c**) Gate drive and drain–source waveforms of switch S_2. (**d**) Gate drive and drain–source waveforms of switch S_4.

Figure 22a shows the key waveform of the resonant tank, while Figure 22b depicts the voltage and current waveforms of the secondary-side diode. It can be observed that the current through the rectifier diode drops to zero before the reverse-bias cutoff, achieving ZCS. Figure 22c,d display the gate drive waveforms of the two lower switches S_2 and S_4 in the full-bridge configuration, along with the voltage and current waveforms of their respective drain–source terminals. It is evident that the voltage across the drain–source terminals of the switches has dropped to zero before turn-on, achieving ZVS.

The key waveforms of the LLC balancing converter with 50% load are depicted in Figure 23.

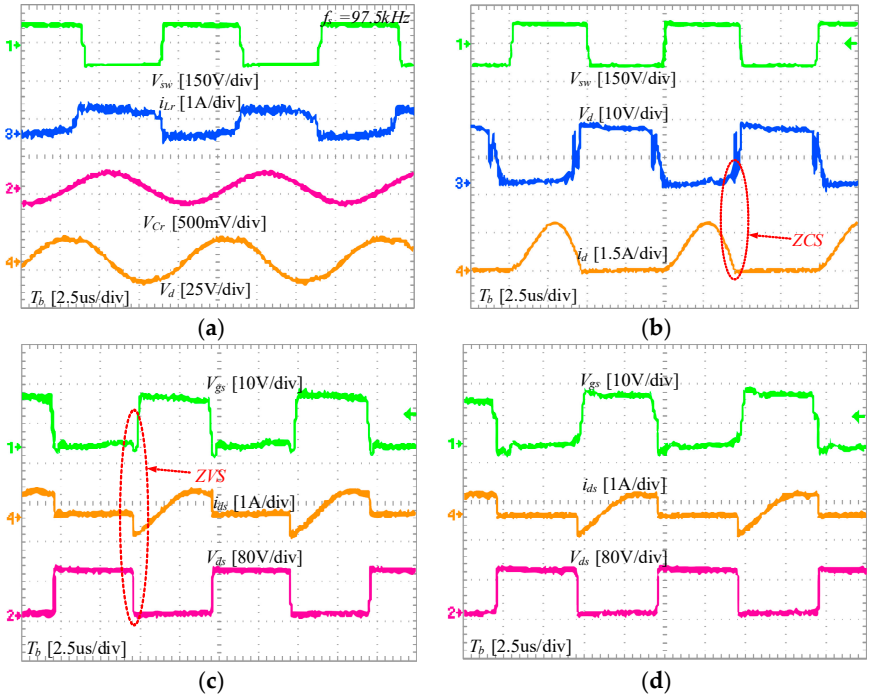


Figure 23. Key waveforms at 50% load. (**a**) Resonant tank waveform. (**b**) Diode waveforms. (**c**) Gate drive and drain–source waveforms of switch S_2. (**d**) Gate drive and drain–source waveforms of switch S_4.

Figure 23 presents the key waveforms at a 50% load condition. Figure 23a,b show the waveforms of the resonant tank and diode, similar to the 10% load condition. Figure 23c,d show the gate drive waveforms and drain–source voltage and current waveforms of the switches under higher-load conditions, demonstrating that ZVS and ZCS remain effective.

The key waveforms of the LLC balancing converter under 100% load are shown in Figure 24.

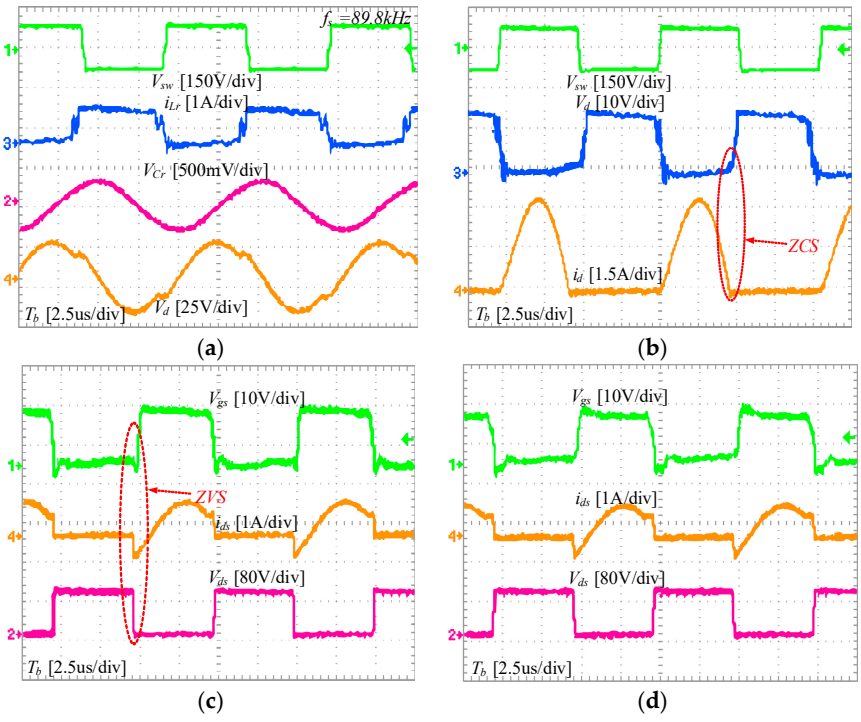


Figure 24. Key waveforms at 100% load. (**a**) Resonant tank waveform. (**b**) Diode waveforms. (**c**) Gate drive and drain–source waveforms of switch S_2. (**d**) Gate drive and drain–source waveforms of switch S_4.

The waveforms depicted in Figure 24 illustrate the performance of the LLC balancing converter under full-load conditions. Both the primary-side switching devices and the secondary-side rectifying diodes continue to achieve ZVS and ZCS, respectively. The resonant tank of the converter operates consistently in the capacitive region, demonstrating that the performance of the fabricated LLC balancing converter meets the requirements for balancing.

Finally, Figure 25 shows the efficiency curve of the converter under different input voltages and load conditions. The results indicate that, through the use of burst control methods, the efficiency can be maintained at 0.87 or above under light-load conditions, and higher under heavier-load conditions.

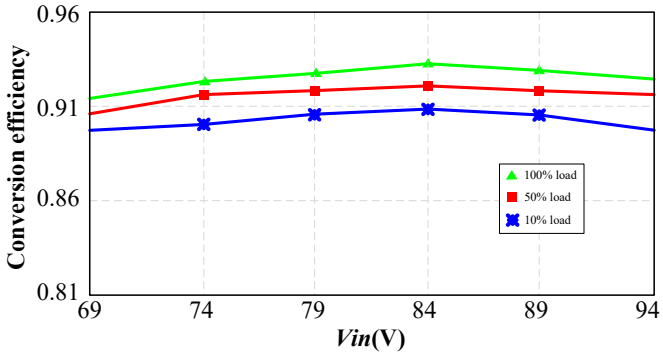


Figure 25. Efficiency curve of the converter.

Under light-load conditions, the switching frequency is typically higher, which theoretically results in lower efficiency. However, by employing burst control methods, the efficiency under light-load conditions can be maintained at 0.87 or above. The system typically operates under load conditions heavier than light load, where the efficiency is generally higher compared to light-load conditions.

5.2. Top-Level Inter-Group Balancing Effect Testing

The top-level inter-group balancing and intra-group active balancing can operate independently. When necessary, the bottom-level balancing can be centrally scheduled by the top-level balancing. Systematic testing has been conducted for intra-group balancing. Next, the performance of inter-group balancing converters is verified, divided into static balancing and charging balancing. Unlike intra-group balancing, inter-group balancing uses the SOC of the bottom-level group as the balancing criterion.

The entire battery pack system consists of five groups of bottom-level battery modules, each comprising four cells of the 18650 type. The cell model and characteristic parameters are consistent with those of the inter-group balancing mentioned earlier. The nominal voltage of each group is 14.8 V, and the fully charged nominal voltage is 16.5 V, with a capacity of 2.6 Ah.

First, static balancing testing is conducted. The SOC (state of charge) status of the bottom-level groups obtained through lookup is shown in Table 6.

Table 6. Initial state of charge (SOC) for single-set static equalization.

Group Number	Initial SOC
Pack#1	93.98%
Pack#2	76.21%
Pack#3	47.79%
Pack#4	40.68%
Pack#5	22.18%

The SOC variation process during static balancing is illustrated in Figure 26. The entire balancing process lasts approximately 160 min. After balancing, the SOC conditions

are presented in Table 7. The initial SOC difference is 71.8%, while the difference at the end of balancing is approximately 1.43%. Before balancing, the SOC standard deviation is 25.67%, whereas after balancing, it is less than 0.6%.

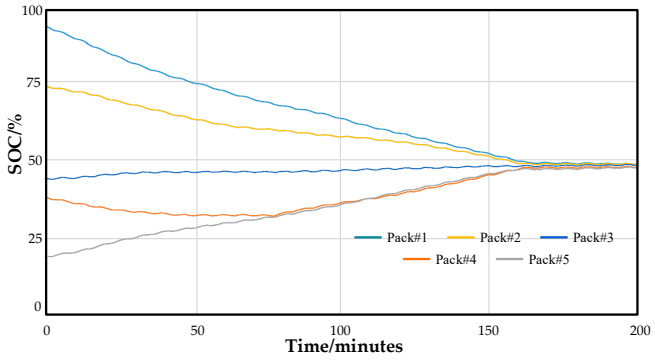


Figure 26. State of charge (SOC) variation in static equalization.

Table 7. Final state of charge (SOC) for single-set static equalization.

Group Number	Initial SOC
Pack#1	51.12%
Pack#2	50.98%
Pack#3	49.69%
Pack#4	50.76%
Pack#5	50.18%

The next step is to conduct the charging balancing test. The SOC conditions of the bottom-layer groups obtained through table lookup are presented in Table 8.

Table 8. Initial state of charge (SOC) for single-set charging equalization.

Group Number	Initial SOC
Pack#1	60.76%
Pack#2	47.97%
Pack#3	36.24%
Pack#4	22.38%
Pack#5	9.82%

The entire balancing process lasted approximately 101.7 min and concluded with the charging balancing. The variation in balancing is illustrated in Figure 27. The charging balancing duration is notably shorter than the idle balancing. The distribution of SOC at termination is presented in Table 9. The initial SOC standard deviation was 18.03%, which reduced to less than 0.6% after balancing.

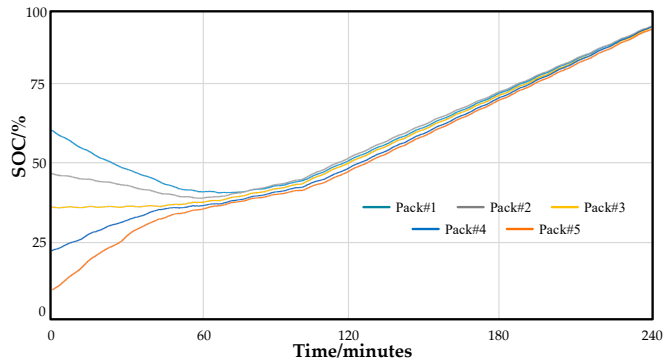


Figure 27. State of charge (SOC) variation process in charging equalization.

Table 9. Final state of charge (SOC) for single-set charging equalization.

Group Number	Initial SOC
Pack#1	93.79%
Pack#2	92.95%
Pack#3	93.25%
Pack#4	92.37%
Pack#5	93.76%

5.3. Bottom-Level Intra-Group Active Balancing Testing

The bottom-level balancing board mainly accomplishes ZigBee wireless communication and internal battery balancing within the group. ZigBee wireless communication can be achieved once the protocol stack networking is configured. The focus of testing lies in the balancing part, where one group is selected as the balancing target, comprising four individual cells within a bottom-level group.

The testing is divided into two parts: charging balancing and idle balancing (parking). First, the idle balancing is tested at a temperature of 25 °C, using Samsung's INR18650-29E lithium-ion battery cells. Figure 28 shows the front view of the intra-module ETA3000 equalization interposer. This interposer is used to achieve effective battery balancing within the module. Figure 29 shows a schematic diagram of the equalization interposer insertion into the battery pack, demonstrating how the interposer is installed for balancing operations.

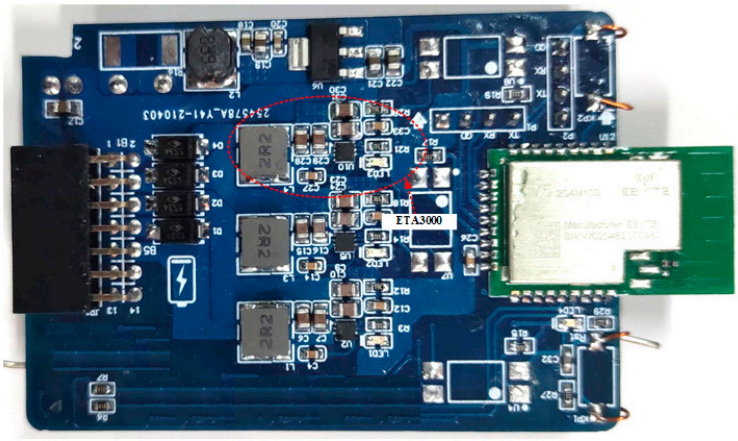


Figure 28. Physical image of intra-module ETA3000 equalization interposer.

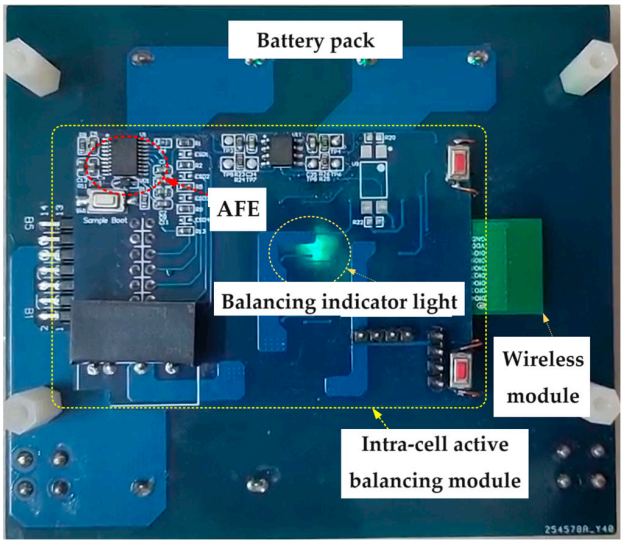


Figure 29. Schematic diagram of equalization interposer insertion.

The internal balancing process is based on the open-circuit voltage (OCV). The OCV of each individual cell before idle balancing is presented in Table 10, while Figure 30 illustrates the voltage variation curve during intra-module static equalization at 25 °C. The balancing process lasts approximately 67.5 min, reducing the voltage difference between cells from an initial 1388 mV to 38 mV. Prior to measuring the OCV, the batteries are allowed to rest for at least 2 h to ensure full stabilization of the electrochemical reactions. This resting period is crucial for obtaining accurate and stable OCV readings [30].

Table 10. Open-circuit voltage of cells before static equalization.

Battery Serial Number	Open-Circuit Voltage
Cell#1	4.584 V
Cell#2	3.196 V
Cell#3	3.421 V
Cell#4	4.308 V

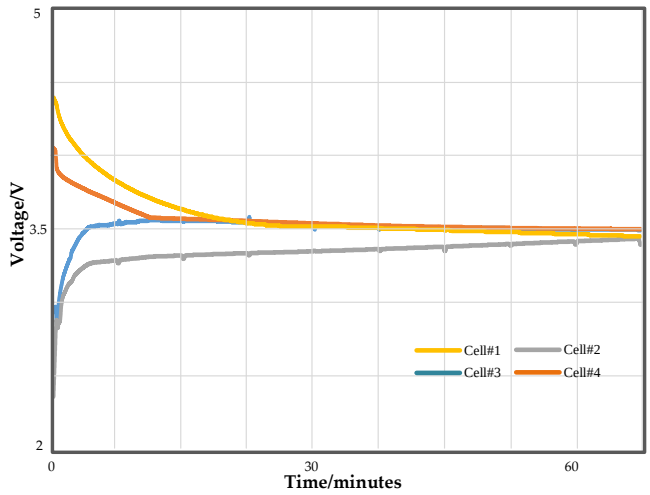


Figure 30. Curve of intra-module static equalization at lower level.

The entire balancing process lasted approximately 67.5 min. The initial voltage spread across the battery pack before balancing was 1388 mV. The individual cell voltages after balancing are shown in Table 11.

Table 11. Open-circuit voltage of cells after static equalization.

Battery Serial Number	Open-Circuit Voltage
Cell#1	3.790 V
Cell#2	3.784 V
Cell#3	3.786 V
Cell#4	3.808 V

The voltage spread between individual cells after balancing is 38 mV. The data in the curve are recorded immediately after the balancing process ends. If we consider the voltage rebound after static balancing, the voltage spread between individual cells will further decrease.

The balancing efficiency, η_e, refers to the remaining percentage of the overall energy of the battery pack after the balancing process is completed. It is estimated using the principle of energy conservation for capacitors, approximating the battery as a capacitor. Its definition is shown in Equation (16).

$$\eta_e = \frac{(1/2)CV^2_{\text{before balancing}}}{(1/2)CV^2_{\text{after balancing}}} = \frac{V^2_{\text{before balancing}}}{V^2_{\text{after balancing}}} \quad (16)$$

With $V_{\text{before balancing}} = 15.509$ V and $V_{\text{after balancing}} = 15.168$ V, substituting into Equation (16) yields a balancing efficiency of 95.6%. Considering the approximation of the battery as a capacitor, the actual balancing efficiency value will be slightly lower than the calculated value.

Next, we test the balancing changes under charging conditions. The initial conditions of the experiment are consistent with those before, and the initial voltage of each cell is as shown in Table 12.

Table 12. Open-circuit voltage of cells before charging equalization.

Battery Serial Number	Open-Circuit Voltage
Cell#1	3.581 V
Cell#2	3.687 V
Cell#3	2.503 V
Cell#4	2.723 V

From the table, the inter-cell voltage difference before balancing is calculated to be 1078 mV. Figure 31 shows the voltage variation curve during intra-module charging equalization. The balancing process lasts approximately 43 min, reducing the voltage difference between cells from an initial 1078 mV to 33 mV.

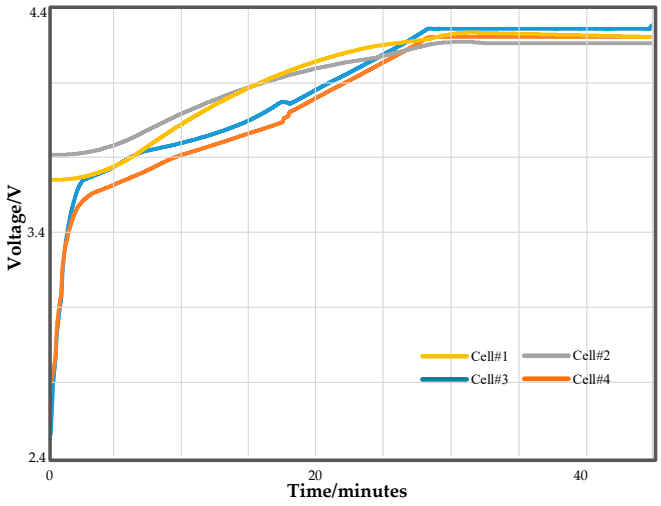


Figure 31. Curve of intra-module charging equalization at lower level.

As shown in Figure 31, the balancing process lasts approximately 43 min. Since this is charging balancing, its speed is relatively faster compared to static balancing. The distribution of inter-cell voltages after balancing is shown in Table 13.

Table 13. Open-circuit voltage of cells after charging equalization.

Battery Serial Number	Open-Circuit Voltage
Cell#1	4.185 V
Cell#2	4.159 V
Cell#3	4.218 V
Cell#4	4.186 V

Table 12 shows the open-circuit voltage (OCV) of the cells after charge equalization. The voltage deviation between the cells is 33 mV, which is less than 50 mV, indicating a good balancing effect among the individual cells. Additionally, Table 12 also indicates that the maximum OCV difference between cell #3 and cell #2 is 59 mV. This voltage difference is relatively small in battery management systems and does not significantly

impact the overall performance and lifespan of the battery module. A small OCV deviation suggests good consistency between the cells, and the active balancing mechanism further ensures consistent performance and efficient operation of the battery pack during charge and discharge cycles. Figure 32 shows the charging current and equalization current curves measured during the charging equalization process. These curves illustrate the energy transfer between cells during the charging equalization process.

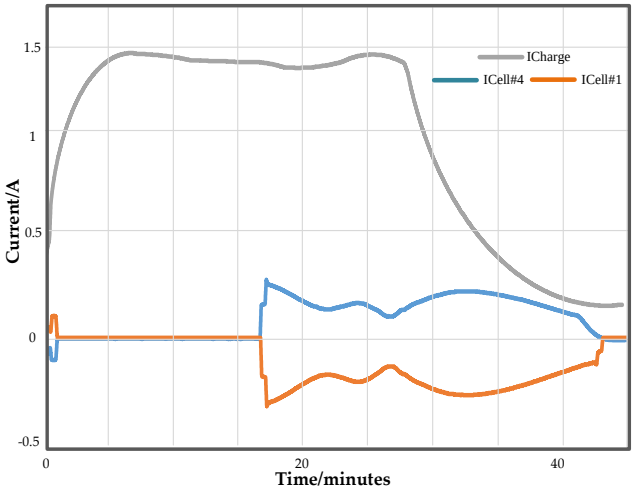


Figure 32. Charging equalization current curve.

5.4. Performance Comparison of Battery Balancing Methods

To validate the performance of the proposed wireless hierarchical active battery balancing system, we conducted systematic experimental tests and compared the results with existing active balancing systems. The main findings from our experiments are presented in the following subsections.

5.4.1. Comparison of Balancing Efficiency

In our experiments, we measured the efficiency of traditional passive balancing systems to be approximately 70%, and hybrid balancing systems to be around 85%. The proposed system, utilizing LLC resonant converters and bidirectional buck–boost converters, achieved a balancing efficiency of 95%, as shown in Figure 33.

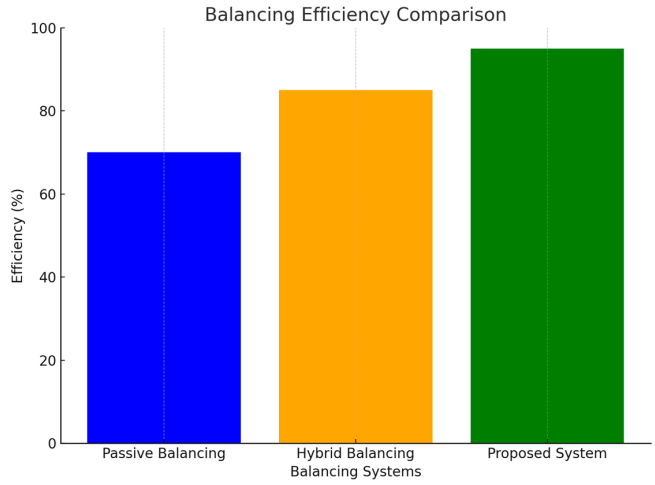


Figure 33. Balancing efficiency comparison.

5.4.2. Comparison of Energy Consumption

Regarding energy consumption, we found that traditional passive balancing systems consume about 30% of energy per balancing cycle, while hybrid balancing systems consume

15%. The proposed system significantly reduced energy consumption to only 5%, as shown in Figure 34.

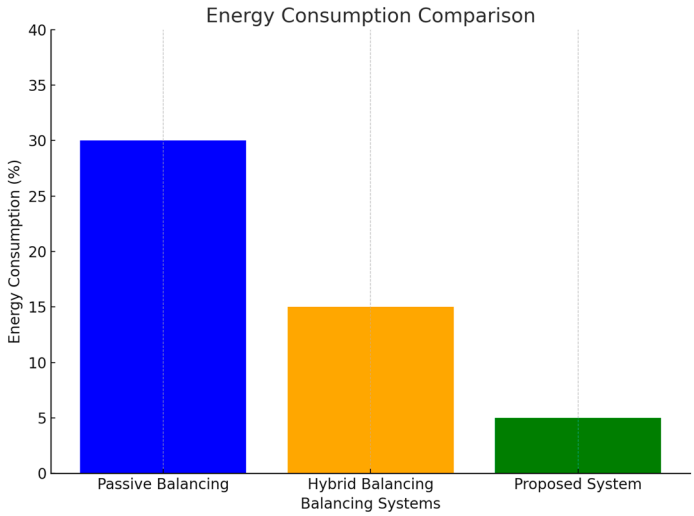


Figure 34. Energy consumption comparison.

5.4.3. Comparison of Thermal Management

Traditional balancing systems generate a substantial amount of heat during the balancing process, requiring additional cooling systems. In our experiments, traditional systems required an extra cooling power of 20 W per balancing cycle, hybrid systems required 10 W, while the proposed system required only 2 W, demonstrating significant advantages in thermal management, as shown in Figure 35.

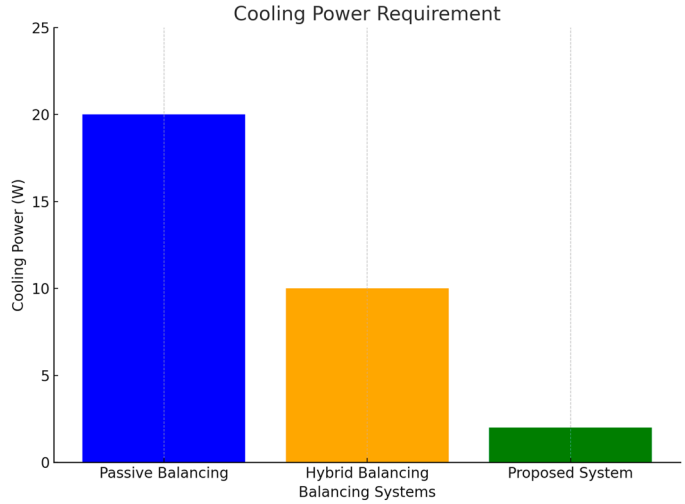


Figure 35. Cooling power requirement.

5.4.4. Comparison of System Reliability

We analyzed the failure rates of different systems and found that traditional wired communication systems have a high failure rate of about 5% per year due to complex wiring. With the application of wireless self-organizing network technology, the failure rate decreased to 1%, highlighting the significant improvements in system reliability brought by wireless technology, as shown in Figure 36.

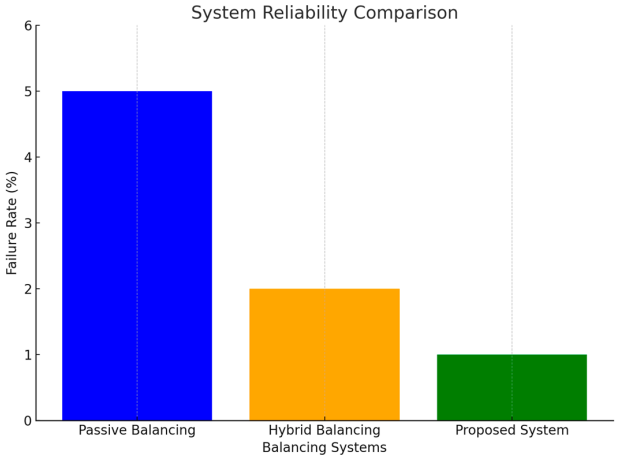


Figure 36. System reliability comparison.

6. Conclusions

This paper proposes and validates a wireless hierarchical active battery balancing management system for automotive power battery packs, aimed at meeting the demands for reliability and efficient balancing. The circuit structure and operation of the system were thoroughly described and verified, with the introduction of LLC resonant converters to enhance the performance of the active battery balancing system. Compared to traditional passive balancing methods, the proposed approach significantly improves balancing efficiency, with an increase of approximately 36%.

At the lower design level, a highly integrated active balancing IC control scheme was employed, combined with low-power wireless self-organizing network technology to achieve the theoretical hierarchical balancing structure. On the software side, a non-polling Beacon-style wireless sensor data transmission protocol was developed, effectively reducing communication anomalies caused by device failures in traditional polling methods and simplifying the complexity of protocol software development. Additionally, a complete set of control procedures for the balancing system was established.

Finally, a comprehensive set of test hardware was produced, and extensive testing was conducted to validate the feasibility of the proposed solution. The test results demonstrate that the system excels in reducing energy consumption and improving energy transfer efficiency, with an efficiency increase of approximately 10%, significantly enhancing the overall balance of the battery pack. These improvements not only extend battery life but also optimize vehicle performance, ensuring the safe and reliable operation of electric vehicle battery systems.

Author Contributions: Conceptualization, J.X. and H.L.; Methodology, J.X. and H.L.; Software, J.X. and J.Q.; Validation, J.Q. and L.S.; Formal analysis, L.S. and Z.C.; Investigation, J.Q. and Y.Z.; Resources, H.L. and Z.C.; Data curation, Z.C. and S.C.; Writing—original draft, J.X. and H.L.; Writing—review & editing, S.C.; Project administration, L.S. and Y.Z.; Funding acquisition, H.L. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: Authors Luhong Shi and Zuhong Chen were employed by the company Zhejiang Kangli Automation Technology Co., Ltd. Authors Sheng Chen and Yong Zheng were employed by the company Zhejiang Jingsheng Microelectronics Co., Ltd. The remaining authors

declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

References

1. Ramkumar, M.S.; Reddy, C.S.R.; Ramakrishnan, A.; Raja, K.; Pushpa, S.; Jose, S.; Jayakumar, M. Review on Li-Ion Battery with Battery Management System in Electrical Vehicle. *Adv. Mater. Sci. Eng.* **2022**, *2022*, 3379574. [CrossRef]
2. Mishra, S.; Swain, S.C.; Samantaray, R.K. A Review on Battery Management System and Its Application in Electric Vehicle. In Proceedings of the 2021 International Conference on Advances in Computing and Communications (ICACC), Kakkanad, India, 21–23 October 2021; pp. 1–6.
3. Hannan, M.A.; Lipu, M.S.H.; Hussain, A.; Mohamed, A. A review of lithium-ion battery state of charge estimation and management system in electric vehicle applications: Challenges and recommendations. *Renew. Sustain. Energy Rev.* **2017**, *78*, 834–854. [CrossRef]
4. Thiruvonasundari, D.; Deepa, K. Optimized Passive Cell Balancing for Fast Charging in Electric Vehicle. *IETE J. Res.* **2023**, *69*, 2089–2097. [CrossRef]
5. Waseem, M.; Ahmad, M.; Parveen, A.; Suhaib, M. Battery technologies and functionality of battery management system for EVs: Current status, key challenges, and future prospectives. *J. Power Sources* **2023**, *580*, 233349. [CrossRef]
6. Cao, Z.; Gao, W.; Fu, Y.; Mi, C. Wireless Battery Management Systems: Innovations, Challenges, and Future Perspectives. *Energies* **2024**, *17*, 3277. [CrossRef]
7. Wei, X.; Zhu, B. New Clean Energy Automotive Engineering Center, Tongji University Shanghai, Cao'an road 4800, China. In *The Research of Vehicle Power Li-Ion Battery Pack Balancing Method, Proceedings of the 2009 9th International Conference on Electronic Measurement & Instruments (ICEMI'2009), Beijing, China, 16–19 August 2009*; IEEE: New York, NY, USA, 2009; Volume 2, pp. 511–515.
8. Sayed, K.; Almutairi, A.; Albagami, N.; Alrumayh, O.; Abo-Khalil, A.G.; Saleeb, H. A Review of DC-AC Converters for Electric Vehicle Applications. *Energies* **2022**, *15*, 1241. [CrossRef]
9. Luo, X.; Kang, L.; Lu, C.; Linghu, J.; Lin, H.; Hu, B. An Enhanced Multicell-to-Multicell Battery Equalizer Based on Bipolar-Resonant LC Converter. *Electronics* **2021**, *10*, 293. [CrossRef]
10. Rahman, A.; Rahman, M.; Rashid, M. Wireless Battery Management System of Electric Transport. In *IOP Conference Series: Materials Science and Engineering*; IOP: Bristol, UK, 2017; Volume 260.
11. Ackshaya, V.; Shankar, S.N.; Balaji, G.S.; Mathankumar, M. LC Based Active Cell Balancing for Efficient Energy Management in Automotive Batteries. *IOP Conf. Ser. Earth Environ. Sci.* **2024**, *1375*, 012017. [CrossRef]
12. Krishnamoorthy, U.; Kumar, G.S.S.; Barua, S.; Fayek, H.H. Investigation of active cell balancing performance for series connected lithium-ion cells in electric vehicle applications. *IET Power Electron.* **2023**, *16*, 2492–2503. [CrossRef]
13. Fan, T.E.; Liu, S.M.; Yang, H.; Li, P.H.; Qu, B. A fast active balancing strategy based on model predictive control for lithium-ion battery packs. *Energy* **2023**, *279*, 128028. [CrossRef]
14. Muhammad, U.; Ghulam, A.; Saleh, H. Characteristics of Battery Management Systems of Electric Vehicles with Consideration of the Active and Passive Cell Balancing Process. *World Electr. Veh. J.* **2021**, *12*, 120. [CrossRef]
15. Marsic, V.; Amietszajew, T.; Igic, P.; Faramehr, S.; Fleming, J. Wireless Communication Test on 868 MHz and 2.4 GHz from inside the 18650 Li-Ion Enclosed Metal Shell. *Sensors* **2022**, *22*, 1966. [CrossRef]
16. Samanta, A.; Williamson, S.S. A Survey of Wireless Battery Management System: Topology, Emerging Trends, and Challenges. *Electronics* **2021**, *10*, 2193. [CrossRef]
17. Lee, M.; Lee, J.; Lee, I.; Lee, J.; Chon, A. Wireless Battery Management System. In Proceedings of the 2013 World Electric Vehicle Symposium and Exhibition (EVS27), Barcelona, Spain, 17–20 November 2013; pp. 1–5.
18. Beiranvand, R.; Rashidian, B.; Zolghadri, M.R.; Alavi, S.M.H. Using LLC Resonant Converter for Designing Wide-Range Voltage Source. *IEEE Trans. Ind. Electron.* **2010**, *58*, 1746–1756. [CrossRef]
19. Abdel-Rahman, S. Resonant LLC Converter. In *Operation and Design*; Infineon Technologies North America (IFNA): Lebanon, NJ, USA, 2012; Volume 19.
20. Lin, B.-R.; Dong, J.-Y. ZVS Resonant Converter With Parallel–Series Transformer Connection. *IEEE Trans. Ind. Electron.* **2010**, *58*, 2972–2979. [CrossRef]
21. Liu, C.-Y.; Liu, Y.-H.; Wang, S.-C.; Yang, Z.-Z.; Ye, S.-P. An Adaptive Synchronous Rectification Driving Strategy for Bidirectional Full-Bridge LLC Resonant Converter. *Energies* **2021**, *14*, 2298. [CrossRef]
22. Zilio, A.; Fogagnolo, D.; Gallo, E.; Biadene, D.; Mattavelli, P. A Multiport Converter for Flexible Active Balancing in Li-Ion Batteries. *IEEE Trans. Ind. Electron.* **2023**, *71*, 7085–7094. [CrossRef]
23. Zhang, Z.; Gui, H.; Gu, D.-J.; Yang, Y.; Ren, X. A Hierarchical Active Balancing Architecture for Lithium-Ion Batteries. *IEEE Trans. Power Electron.* **2016**, *32*, 2757–2768. [CrossRef]
24. Wang, S.; Yang, S.; Yang, W.; Wang, Y. A New Kind of Balancing Circuit with Multiple Equalization Modes for Serially Connected Battery Pack. *IEEE Trans. Ind. Electron.* **2020**, *68*, 2142–2150. [CrossRef]
25. Manjunath, K.; Kalpana, R.; Singh, B.; Kiran, R. A Two-Stage Module Based Cell-to-Cell Active Balancing Circuit for Series Connected Lithium-Ion Battery Packs. *IEEE Trans. Energy Convers.* **2023**, *38*, 2282–2297. [CrossRef]

26. Karunarathne, G.G.K.W.M.S.I.R.; Kulawansa, K.A.D.T.; Firdhous, M.F.M. Wireless Communication Technologies in Internet of Things: A Critical Evaluation. In Proceedings of the 2018 International Conference on Intelligent and Innovative Computing Applications (ICONIC), Mon Tresor, Mauritius, 6–7 December 2018; pp. 1–5. [CrossRef]
27. Park, S.-S.; Eom, M.-H.; Lee, S.-T.; Kim, R.-Y. Accurate Analysis Method and Voltage Gain Curve Derivation Algorithm Based on Time-Domain Analysis for High-Efficiency LLC Resonant Converter Design. *Electronics* **2023**, *12*, 2030. [CrossRef]
28. Tao, S.; Jiang, B.; Wei, X.; Dai, H.A. Systematic and Comparative Study of Distinct Recurrent Neural Networks for Lithium-Ion Battery State-of-Charge Estimation in Electric Vehicles. *Energies* **2023**, *16*, 2008. [CrossRef]
29. Jenkins, B.; Krupadanam, A.; Annaswamy, A.M. Fast Adaptive Observers for Battery Management Systems. *IEEE Trans. Control. Syst. Technol.* **2019**, *28*, 776–789. [CrossRef]
30. Petzl, M.; Danzer, M.A. Advancements in OCV Measurement and Analysis for Lithium-Ion Batteries. *IEEE Trans. Energy Convers.* **2013**, *28*, 675–681. [CrossRef]