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Comprehensive Study of SDC Memristors for Resistive RAM Applications

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Abstract: Memristors have garnered considerable attention within the scientific community as devices for emerging construction of Very Large Scale Integration (VLSI) systems. Owing to their inherent properties, they appear to be promising candidates for pivotal components in computational architectures, offering alternatives to the conventional von Neumann architectures. This work has focused on exploring potential applications of Self-Directed Channel (SDC) memristors as novel RRAM memory cells. The introductory section of the study is dedicated to evaluating the repeatability of the tested memristors. Subsequently, a detailed account of the binary programming testing process for memristors is provided, along with illustrative characteristics depicting the impact of programming pulses on a memory cell constructed from a memristor. A comprehensive data analysis was then conducted, comparing memristors with varying types of doping. The results revealed that SDC memristors exhibit a high level of switching, certainty between the Low Resistance State (LRS) and High Resistance State (HRS), suggesting their capability to facilitate the storage of multiple bits within a single memory cell.

Keywords: SDC memristor; resistive RAM; memristor programming; non-linear circuit

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1. Introduction

Due to the limitations of the von Neumann architecture, in the conventional computing systems the solution of many classical problems such as combinatorial optimization, neural networks, inverse logic, etc., usually require huge computational space, memory and extremely long running times. To solve these problems efficiently, new computer architecture proposals are constantly being researched. Among many of them the architecture involving Memristors brought a great attention of the scientific community as devices for the new generations of Very Large Scale Integration (VLSI) systems. Memristors are non-linear two-terminal components postulated by Leon O. Chua in 1971 [1]. After Professor Chua's postulation regarding memristors, subsequent years were dedicated to the quest for the actual implementations of the memristor. In 2008, the engineering team under the leadership of Stanley Williams at HP Laboratories presented the first physical realization of the proposed element [2,3].

One of the most attractive properties of memristors is that the memristor can adopt a continuous range of different equilibrium states when the power is switched off at any time [4]. It follows that memristors can serve as a non-volatile analogue memory. The existence of nanoscale memristor behavior opens up a wide range of possibilities in the realization of low-power, high-density memory technologies that could replace existing technologies (flash memories and dynamic random-access memories) and have been thoroughly examined in-depth over the past few decades through extensive scientific research [5–12]. When two sufficiently different internal state values are chosen to encode desired states, memristors can be used as non-volatile multi-state memory cells [13–16]. This property seems to find a perfect application in memory devices industry, as the possible memory capacity might increase exponentially. Since memristors can handle analogue

values and, in addition, the memristor is able to simulate synaptic connections between neurons, some future memristor-based devices could be designed to mimic biological functions and be used to build a brain-like computer [17–19]. An intriguing investigation concerning SDC memristors involves their application in modulation/demodulation transceiver links within the context of Binary Phase Shift Keying (BPSK) communication systems [20].

The research delved into the potential applications of SDC (Self-Directed Channel) memristors with various types of doping as prospective new RRAM/CBRAM memory cells. In Figure 1, a comparison between currently employed DRAM memory cells and a potential RRAM memory cell based on a memristor is depicted. Such a cell would possess numerous advantages, including the absence of the need for refreshing with each working cycle, data retention even after power loss, and, leveraging features such as multi-state capability, the ability to perform logical operations directly in the memory without the necessity for prior readout to the CPU register. The construction of SDC-doped memristors has been elucidated in the literature [21–23].

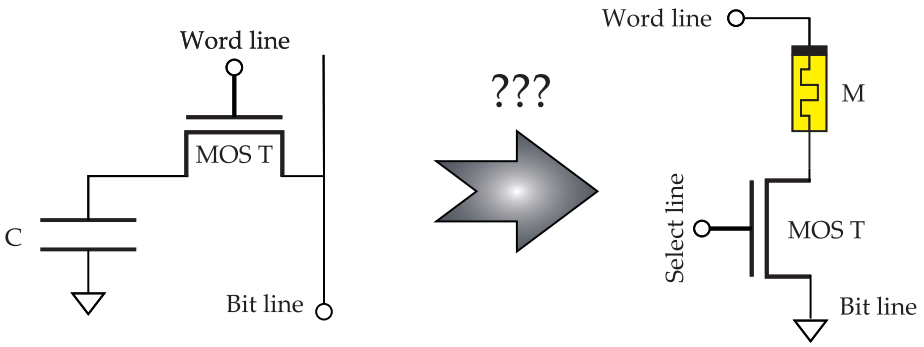


Figure 1. Proposition of the replacement the of a conventional DRAM memory cell with a memristor-based RRAM memory cell.

The initial section of the document involved the verification of memristor quality by calculating indicators describing of its quality and repeatability. Subsequently, the process of testing the binary state programming of memristors was described, and exemplary programming characteristics of memristors were presented. In the following section, an individual analysis for a specific case was detailed, followed by a collective data analysis comparing various doping types of memristors. Conclusions were drawn, and an algorithm for programming multi-state SDC memristors has been proposed.

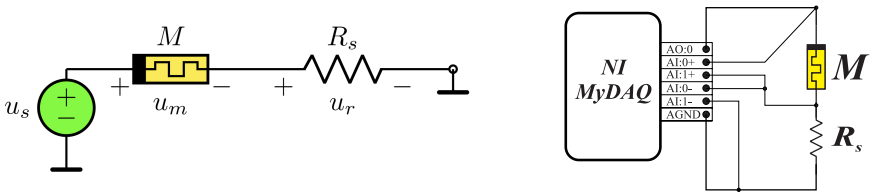
2. Materials and Methods

SDC (Self-Directed Channel) memristors with tungsten, tin, chromium, and carbon doping were tested and compared with each other during the tests. In order to measure the memristor current and to limit it below its nominal value, i.e., 1 mA for W, Sn, and Cr-doped memristors and 50 µA for C doping [21], the memristor was connected in series with a high quality linear resistor R_s. In the case of W, Sn, Cr doping, the resistance R_s was 5.11 kΩ while in the case of C doping, R_s was 47.5 kΩ. The u_r voltage measured at resistor R_s, according to Ohm's law, is directly proportional to the current and its known resistance, which allows the memristor current to be obtained by multiplying the voltage across the resistor by the reciprocal of its resistance. The conceptual diagram of the measurement system is shown in Figure 2a. All tested memristors were prepared using the same forming procedure before the tests began. With the myDAQ University Kit from National Instruments containing a measurement board and function generator, the supply voltage was generated and the u_m and u_r signals were collected [24]. The current of the memristor were calculated using Ohm's law ($i_m = \frac{u_r}{R_s}$). The circuit connection diagram for the measuring device is shown in Figure 2b. For the AC analysis tests conducted in Section 3, the sampling rate of the acquisition signal depended on the frequency of the forcing signal, so that 1000 points were

collected for each signal period. The relation between sampling rate f_r and the forcing signal frequency f_s can be expressed as:

$$f_r = 10^3 f_s \quad (1)$$

The sampling frequency for bi-stable programming tests was constant and set to 10 kHz. The timer of the measurement card was synchronized with the timer of the signal generator.



(**a**) (**b**)

Figure 2. (**a**) The conceptual diagram of the measurement system. (**b**) Connection diagram of the memristor with NI myDAQ University Kit.

For the generation, acquisition, and processing of specific signals, a dedicated algorithm written in the Python (ver.3.10) programming language was employed. This algorithm utilizes the `nidaqmx` library for communication with DAQ (Data Acquisition) devices, along with supporting libraries for numerical computations and data processing, including `pandas`, `numpy`, `scipy`, and `matplotlib`. For specific computations and visualizations, the Matlab R2023a software package was also employed.

Self-Directed Channel Memristors

SDC memristors exhibit variability in resistance by leveraging ion-conductive properties, specifically through the migration of Ag^+ ions within the device structure [21,22,25].

Despite the presence of numerous thin layers, the manufacturing process remains straightforward and dependable. All layers, including the top electrode, are deposited in situ in a single processing step through sputtering. The consistent separation between the Ag-source (comprising $Ge_2Se_3/Ag/Ge_2Se_3$ layers) and the top electrode allows for high-temperature processes, enabling prolonged continuous operation at 150 °C [21]. Additionally, there is no need for a high voltage forming step, as the set voltage during regular device operation can efficiently transition a pristine device into a low-resistance state [26] Moreover, the programming voltages and compliance current values required are significantly lower compared to traditional metal-oxide RRAMs, resulting in reduced power consumption [25,27].

Each package encompasses 16 discrete SDC devices initially in a high-resistance state (MΩ–GΩ range) [21]. The initial operational step produces Sn ions from the SnSe layer, facilitating their incorporation into the active Ge_2Se_3 layer. This incorporation process involves the formation of self-trapped electrons within the Ge_2Se_3 active layer, leading to the distortion of Ge–Ge bonds by reacting with Ag. This distortion creates an 'opening' near the Ge–Ge sites, establishing a natural conductive channel for the movement of Ag+ during device operation. Importantly, this pathway does not manifest as a metallic filament between electrodes but functions as a channel with resistance influenced by varying concentrations of Ag. The tunable resistance can be adjusted in both lower and higher directions by manipulating Ag movement through the application of positive (SET) or negative (RESET) potential, respectively, across the device [26]. The absence of a physical conductive filament results in a less abrupt set transition (yielding a low-resistive state, LRS) compared to metal-oxide technology [27]. In contrast, the reset operation (leading to a high-restive state, HRS) occurs suddenly, disrupting loop symmetry. The low power consumption is attributed to small currents and notably low voltage levels required for set and reset, as there is no necessity for initiating a true soft breakdown in the device [25].

Knowm Inc. produces four versions of dopants introduced into the active layer of memristors:

- Tungsten W;
- Carbon C;
- Tin Sn;
- Chromium Cr.

Each dopant alters the dynamic switching characteristics of resistance [21,23]. In Figure 3, the construction and operating principle of these devices are depicted in a simplified manner.

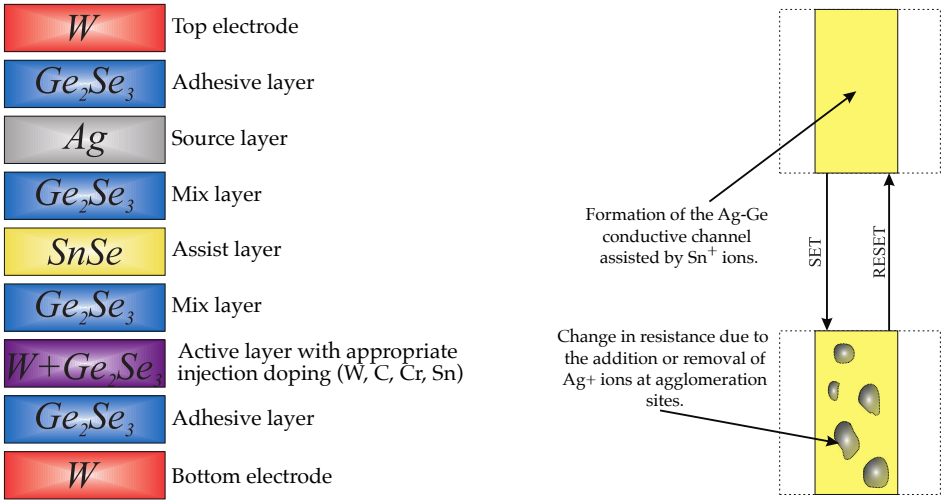


Figure 3. Construction and principle of operation of SDC memristors. (**a**) Sandwich structure of the KNOWM SDC memristor [21,23]. (**b**) Graphical interpretation of memristor resistance change [21,23].

3. Analysis of SDC Memristors Quality

This section presents the study over the quality of the memristor behaviour over the switching process. This aspect is especially important from the point of view of potential applications of SDC memristors in memristive RAM cells.

3.1. Pinched Hysteresis Loop of the SDC Memristors

One of the fingerprints of memristors is their specific response on periodic signals [1]. When the periodic signal with zero mean is applied (current or voltage) all memristors must exhibit a characteristic hysteresis loop pinched at origin of $v - i$ domain. This phenomenon is said to provide necessary and sufficient conditions for identifying experimentally whether a device is a memristor, or not [28,29]. In Figure 4, the characteristic hysteresis loops on $v - i$ domain for each SDC memristors considered in the work are presented. The amplitude and frequency of the generating sine signal was $V_s = 1.5$ [V] and $f_z = 20$ [Hz] accordingly. It can be noticed that SDC memristors are unstable during the switching process both from the OFF state (high resistance) to the ON state (low resistance) and v.v. For clarity of the observation the averaged signal over all 100 periods of the generation signal has been presented, here indicated by the red line. To illustrate the evolution of the memristor's hysteresis loop during the course of the investigation, the measurement points was colorized using a gradient based on the sequential number of signal periods. As observed, the $i_m = f(u_m)$ characteristic of the memristor undergoes changes with successive periods of the driving signal, indicating a correlation with the supplied energy, i.e., the temperature of the memristor. This phenomenon is particularly pronounced in the case of Chromium-doped memristors. The comprehensive study over the variations of the memristors behavior with temperature has been studied in [22]. On Figure 5 the calculated STD (standard deviation) factor from the average has been presented. Looking at STD

values one can assume that the most stable switching might be considered the memristor with carbon dopant where the STD factor does not exceed 6×10^{-4} on the other hand the chromium doped memristor where the STD factor reaches values of 5×10^{-2}. It is worth to notice that deviations from the average are higher during the resetting process. This phenomenon can be seen on Figure 4. The exception is the memristor doped with Tin where some unstable behavior are noticed during the setting process. Significant deviations from the referenced characteristics can also be seen at the final periods, so trivially it is hard to separate two different transition characteristic, based only on electric energy provided to the memristor. On the other hand after set and reset process all memristors reaches stable state condition what is the most important in the field of RRAM application.

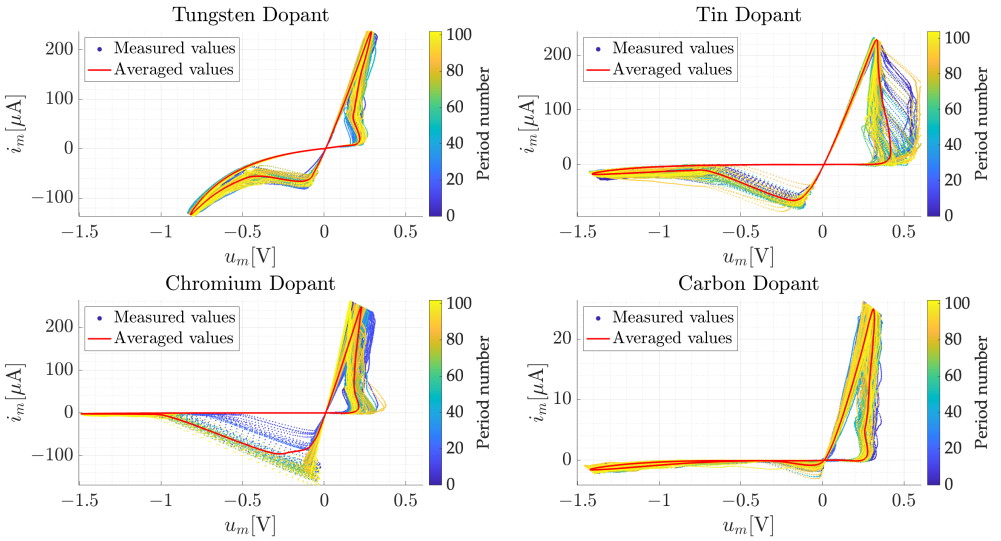


Figure 4. Averaged values of hysteresis loops $u_m - i_m$ along with measured values, for varying memristor doping, for a signal with an amplitude of $V_s = 1.5$ [V] and a frequency of $f_z = 20$ [Hz]. The measurement points are colored with gradient according to the period number.

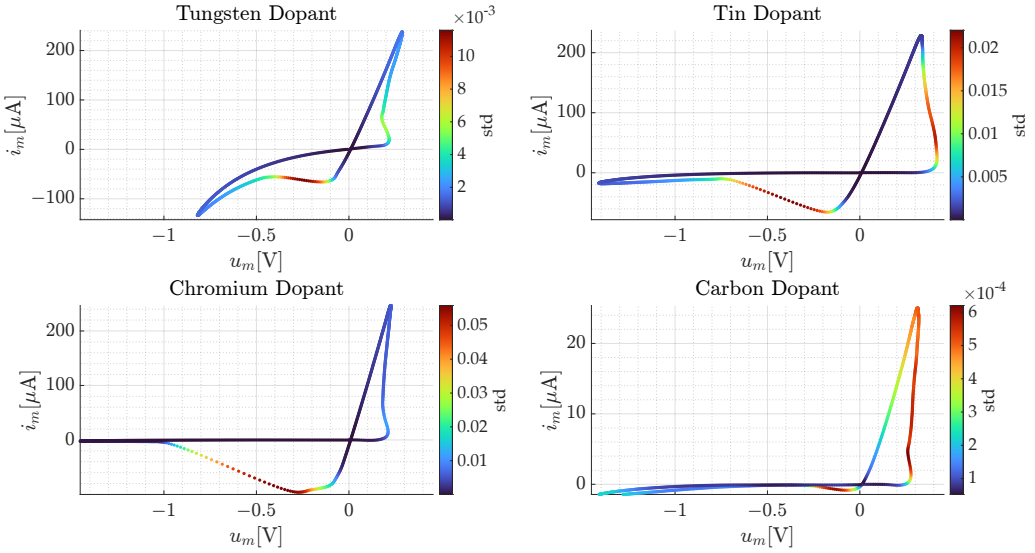


Figure 5. Averaged hysteresis loops $u_m - i_m$ with standard deviation of i_m marked for each point, for a signal with an amplitude of $V_s = 1.5$ [V] and a frequency of $f_z = 20$ [Hz].

To analyze the quality of data and assess the repeatability of a given memristor's behavior, certain statistical coefficients were calculated based on the collected measurement data. In order to compare the measured values for each period j (where $j \in \langle 1, m \rangle$, and m is the number of periods) with the averaged period, the coefficient δ_j was proposed. It is

understood as the normalized standard deviation relative to the coefficient of the mean value and can be described by the following relationship [30]:

$$\delta_j = \sqrt{\frac{\sum_{k=1}^{n}\left(\bar{i_k} - i_{k,j}\right)^2}{\sum_{k=1}^{n}\left(\bar{i_k}\right)^2}} \tag{2}$$

where $n = 1000$ represents the number of points per period, j denotes the index of the successive period, $i_{k,j}$ signifies the current at point k during the j-th period, and $\bar{i_k}$ indicates the current at point k for the averaged period.

To estimate the error across all periods in a given measurement, the coefficient ε was proposed as the root mean square of the coefficients δ_j. The relationship is expressed as follows [30]:

$$\varepsilon = \sqrt{\frac{1}{m}\sum_{j=1}^{m}\delta_j^2} \tag{3}$$

Using the Matlab environment, the aforementioned coefficients were computed for each measurement and aggregated in Table 1.

Table 1. The value of the error ε for collected measurement signals of memristors with various doping levels and different parameters of the driving signal. The smallest error is highlighted in green, while the largest is marked in red.

f[Hz]	Tin			Chromium		
	V_s = 0.5 V	V_s = 1 V	V_s = 1.5 V	V_s = 0.5 V	V_s = 1 V	V_s = 1.5 V
1	7.73×10^{-4}	9.95×10^{-5}	4.90×10^{-5}	3.95×10^{-3}	5.19×10^{-4}	1.76×10^{-4}
5	1.58×10^{-3}	3.52×10^{-5}	2.44×10^{-4}	3.05×10^{-4}	2.43×10^{-4}	6.94×10^{-4}
10	6.12×10^{-4}	7.23×10^{-5}	4.39×10^{-4}	3.04×10^{-4}	9.46×10^{-4}	1.45×10^{-3}
20	3.54×10^{-4}	8.04×10^{-5}	3.26×10^{-4}	2.59×10^{-3}	1.68×10^{-3}	1.12×10^{-3}
50	1.16×10^{-3}	3.98×10^{-4}	1.37×10^{-3}	3.66×10^{-4}	0.80	0.88
100	2.70×10^{-4}	1.69×10^{-5}	0.02	1.77×10^{-3}	1.93×10^{-4}	4.94×10^{-4}
f[Hz]	Tungsten			Carbon		
	V_s = 0.5 V	V_s = 1 V	V_s = 1.5 V	V_s = 0.5 V	V_s = 1 V	V_s = 1.5 V
1	2.26×10^{-4}	1.10×10^{-5}	3.05×10^{-6}	7.43×10^{-4}	8.04×10^{-6}	2.35×10^{-6}
5	6.33×10^{-6}	6.72×10^{-6}	1.51×10^{-5}	1.99×10^{-4}	7.89×10^{-6}	4.74×10^{-6}
10	7.53×10^{-6}	3.25×10^{-5}	2.48×10^{-5}	1.11×10^{-3}	1.79×10^{-5}	1.21×10^{-5}
20	1.19×10^{-5}	8.29×10^{-6}	1.92×10^{-6}	1.50×10^{-5}	3.13×10^{-5}	9.02×10^{-6}
50	4.68×10^{-4}	5.72×10^{-6}	1.10×10^{-4}	0.27	2.46×10^{-5}	1.57×10^{-5}
100	4.72×10^{-5}	3.57×10^{-6}	2.06×10^{-6}	3.83×10^{-6}	3.06×10^{-5}	6.78×10^{-6}

It can be observed that the chromium-doped element is the least stable, while other dopings exhibit a similar level of stability. The smallest error estimate ε is observed for tungsten doping with a supply voltage amplitude $V_s = 1.5$ V and a frequency $f = 20$ Hz, whereas the largest is for chromium doping with $V_s = 1.5$ V and $f = 50$ Hz. The worst-case scenario is intriguing, as the memristor behaved almost like a resistor for the first 15 periods before undergoing a state change. In Table 2, the medians of error estimates med(ε) for each type of doping are presented.

Table 2. The median estimation of errors med(ε) for each type of doping in memristors.

Doping	Carbon	Chromium	Tin	Tungsten
med(ε)	1.54×10^{-5}	8.20×10^{-4}	3.40×10^{-4}	9.63×10^{-6}

3.2. Change in the Memristor's Resistance

The memristor as an non-linear element has its internal variable state which has an direct influence on it's final resistance. The memristor's state changes proportionally to the magnetic flux or electric charge that has passed through the element. On the Figure 6 the resistance variation during the setting and resetting process described in Section 3.1 is presented, notice that resistance axis is in logarithmic scale. For the comparison reason the parameters of the generating signal is the same as for the hysteresis loop presented on the Figures 4 and 5. It can be noticed that applying the input signal the memristor's state, i.e., its resistance, can be changed significantly in the order of some magnitudes. The setting process requires smaller voltage value then resetting. This aspect is studied in the next section.

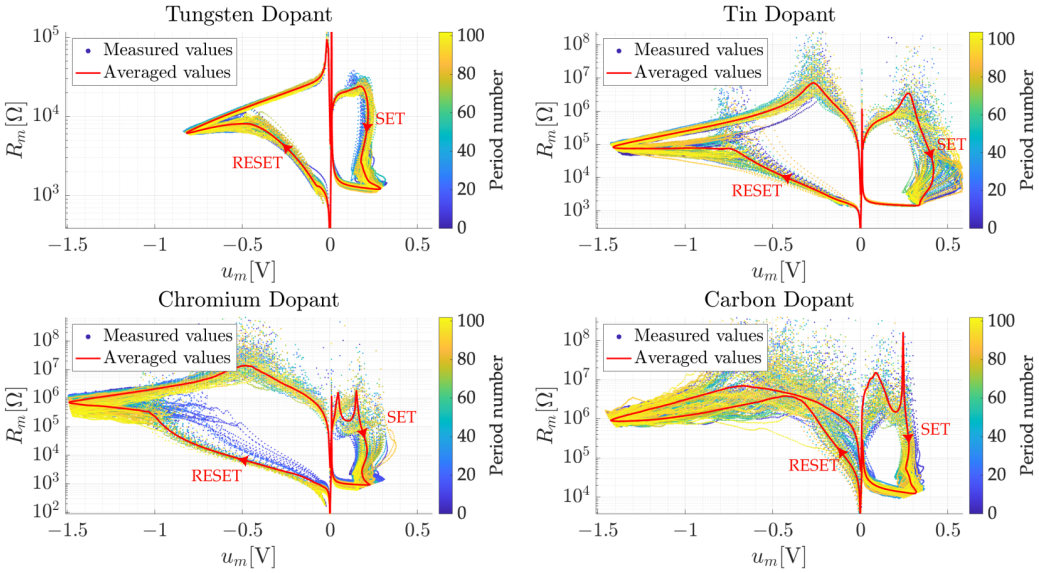


Figure 6. The averaged memristor resistance R_m as a function of its voltage u_m, for a signal with an amplitude of $V_s = 1.5$ [V] and a frequency of $f_z = 20$ [Hz], along with the measured points. The measurement points are colored with gradient according to the period number. The direction of transitions between individual states of the memristor are indicated by arrows.

4. The Testing Process for Memristor Programming

The programming process of the circuit shown in Figure 2b was carried out by supplying the memristor with appropriate pulses: programming pulses (with positive polarization), measuring resistance (at low amplitude, below the threshold voltage of the memristor), and resetting pulses (with negative polarization). The tests pulses for the resistance measurement uses the property of the memristors that below some threshold voltage the memristor state, i.e., its resistance stays unchanged. The conceptual process of setting and resetting the memristor is illustrated in Figure 7.

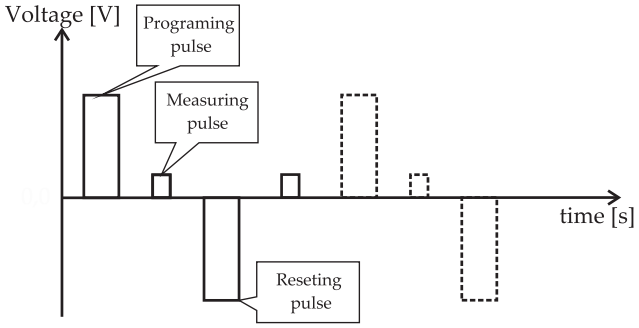


Figure 7. The conceptual flow of the testing process.

During the process of the experiments, current and voltage waveforms of the memristor are recorded for each pulse. Subsequently, for the purpose of smoothing measurements and reducing the impact of disturbances, a Savitzky–Golay smoothing filter is applied, as described in [31]. During the resistance measurement pulse, the instantaneous resistance is calculated from the recorded and filtered current and voltage signals using the equation $r = \frac{u(t)}{i(t)}$. Subsequently, its average value is determined by the following formula:

$$R = \frac{1}{T} \int_0^T r(t)\, dt \tag{4}$$

where: r is the instantaneous resistance, T pulse width and R reference resistance value. During the programming pulse, the following parameters are calculated from the recorded, filtered current and voltage signals:

- Charge flowing through the memristor q;
- Memristor energy E.

Memristor energy is calculated as the integral of the instantaneous power, which is the product of the instantaneous current and the instantaneous voltage:

$$E = \int_0^T i(t)u(t)\, dt \tag{5}$$

The charge flowing through the memristor is calculated as the integral of the instantaneous current according to the following relationship:

$$q = \int_0^T i(t)\, dt \tag{6}$$

5. Algorithm for Memristor Programming

The block diagram of the testing process is presented in Figure 8. The main concept of the algorithm is to generate programming pulses until the R_{ON} state is achieved, i.e., the memristor's resistance is within the specified range. The resistance ranges have been experimentally determined and based on previous studies of the memristor response to various pulses, and they are as follows:

- For memristors doped with tungsten, tin, and chromium: $R_{\mathrm{ON}} \in \langle 0, 5 \rangle$ [kΩ], $R_{\mathrm{OFF}} \in \langle 10, \infty \rangle$ [kΩ]
- For memristors doped with carbon: $R_{\mathrm{ON}} \in \langle 0, 100 \rangle$ [kΩ], $R_{\mathrm{OFF}} \in \langle 200, \infty \rangle$ [kΩ]

Between the R_{ON} and R_{OFF} states, there is an unknown state used for error detection, referred to as *unknown*.

After acquiring the data, which includes the pulse width $\Delta t_{\mathrm{pulse}}$ and pulse amplitude V_{pulse}, the memristor is brought into the R_{OFF} state by applying a reset pulse. Subsequently, a programming pulse with the specified parameters is generated, followed immediately by resistance measurement using a measuring pulse. If the R_{ON} state is achieved, reset pulses are generated until the R_{OFF} state is reached. If the R_{ON} state is not achieved, the generation of programming and resistance-measuring pulses is repeated until the R_{ON} state is reached or the maximum number of pulses, here 10, is reached. The parameters of the programming, resistance-measuring, and resetting pulses are presented below:

- Reset pulse: pulse width $\Delta t_{\mathrm{pulse}} \in \{5, 10, 50, 100\}$[ms],
  pulse amplitude $V_{\mathrm{pulse}} \in \{1, 1.5, 2\}$[V],
- Reset pulse: pulse width $\Delta t_{\mathrm{pulse}} = 100$ [ms],
  pulse amplitude $V_{\mathrm{pulse}} = -2.5$ [V],
- Resistance-measuring pulse: pulse width $\Delta t_{\mathrm{pulse}} = 10$ [ms],
  pulse amplitude $V_{\mathrm{pulse}} = 0.15$ [V].

The parameters of the reset pulse were selected to ensure the memristor's reset to a high-resistance state. To obtain signals during the pulse, values above a certain voltage on

the memristor or resistance were screened using a kind of trigger set above the signal noise level. A test is defined as the time in which a single transition of the memristor occurs from the R_{OFF} state to the R_{ON} state, and experiments involve conducting 100 tests. The studies were carried out for each combination of programming pulse amplitude and width. All measured values were aggregated and saved in a `*.csv` file for in-depth analysis.

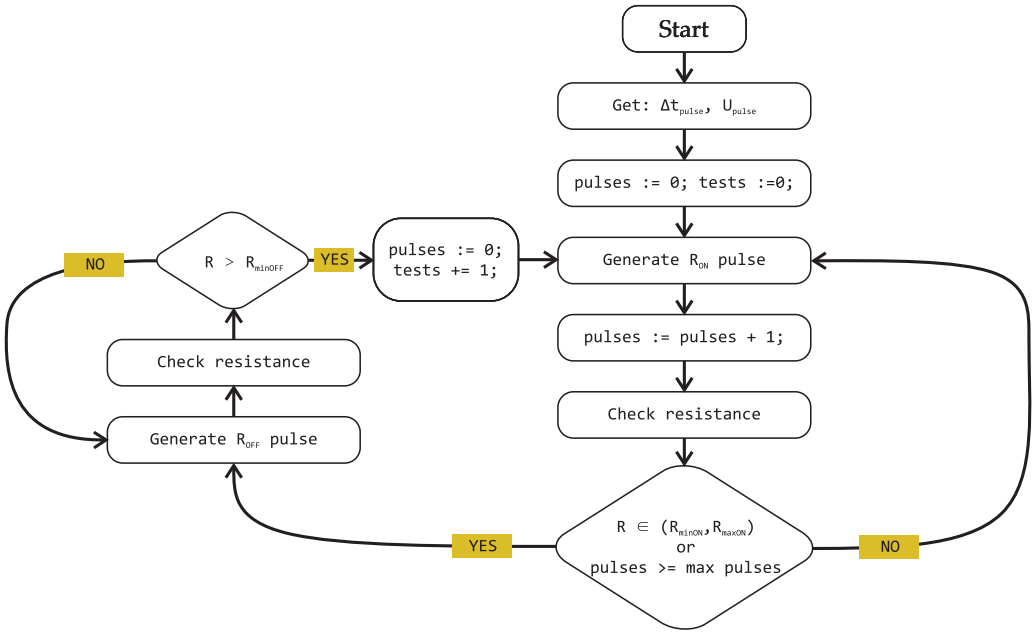


Figure 8. Simplified block diagram of the investigation of a bistable memristor.

6. Results

This section presents the results of tests carried out while programming the memristor to ON and OFF states. Both memristor's behavior during the transient time and the impact of the programming pulses characteristics are discussed. Some preliminary conclusions are provided.

6.1. Sample Memristor Characteristics during Programming

In Figure 9, the current waveform $i_m(t)$ and voltage waveform $u_m(t)$ during the programming pulse with a pulse width of 50 [ms] and an amplitude of 1.5 [V] are presented. As observed, the waveforms can be approximated fairly well with an exponential function, as demonstrated in the figure. It is evident that the programming was successful, as both current and voltage have stabilized in a low-resistance state. The application of the Savitzky–Golay smoothing filter is apparent, leading to the smoothing and noise reduction of the obtained data.

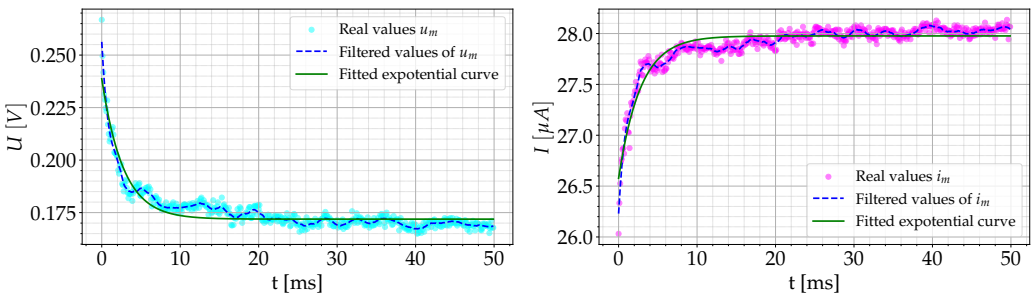


Figure 9. The current waveform $i_m(t)$ and voltage waveform $u_m(t)$ during the programming pulse with a pulse width of 50 ms and an amplitude of 1.5 V.

In Figure 10, the resistance waveform $R(t)$ and the conductance waveform $\mathcal{G}(t)$ of the memristor during the programming pulse are presented, with a pulse width of 50 ms and an amplitude of 1.5 V. These waveforms are also exponential, as demonstrated by fitting the waveforms to an exponential curve.

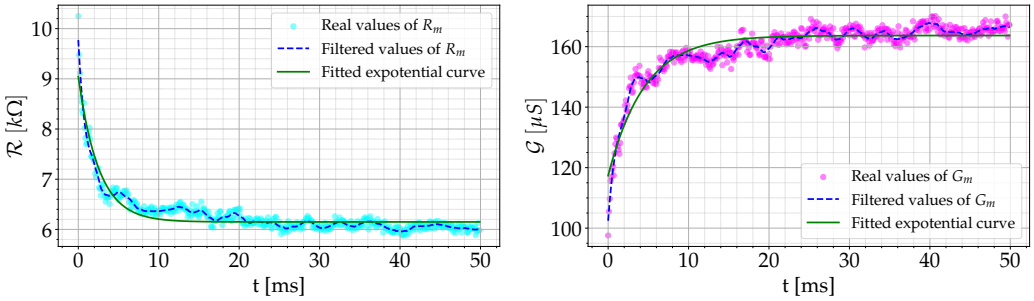


Figure 10. The evolution of resistance $R(t)$ and conductance $\mathcal{G}(t)$ of the memristor during the programming pulse with a pulse width of 50 ms and an amplitude of 1.5 V.

In Figure 11, the evolution of resistance $R(t)$ of the memristor is presented in the domain of supplied energy E and supplied charge q to the memristor during the programming pulse.

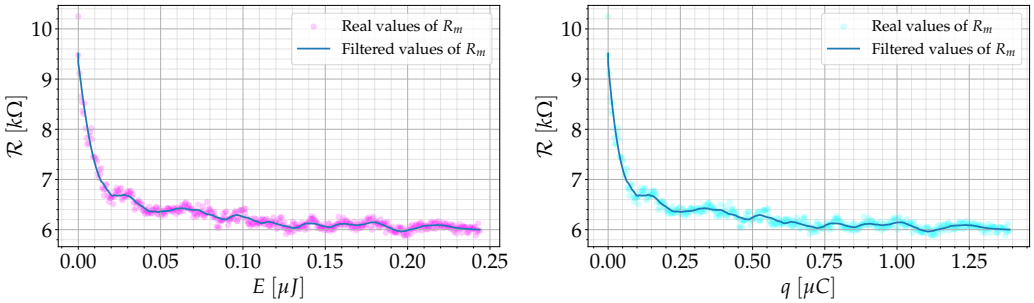


Figure 11. The evolution of resistance $R(t)$ in the domain of energy E and charge q during the programming pulse with a pulse width of 50 ms and an amplitude of 1.5 V.

6.2. Sample Results of the Study for Selected Cases

The collected data from the measurements were aggregated and analyzed. The following section delineates an illustrative individual case, pertaining to a tin-doped memristor that was programmed with pulses of 1.5 V amplitude and a programming pulse width of 5 ms.

In Figure 12a, the number of pulses after which each test was concluded is presented in the form of a bar chart. It can be observed that a portion of the tests was completed after the first pulse, while there are tests that concluded after a number of pulses exceeding one. In Figure 12b, a cumulative charge delivered to the memristor during the test is presented in the form of a bar chart. Figure 12c shows a chart representing the energy dissipated in the memristor during the test. As can be observed, these charts are clearly correlated with the chart in Figure 12a. In Figure 12d, a bar chart is presented, showing the number of tests that concluded after a given pulse. It can be observed that the first pulse, 76% of the tests were successful.

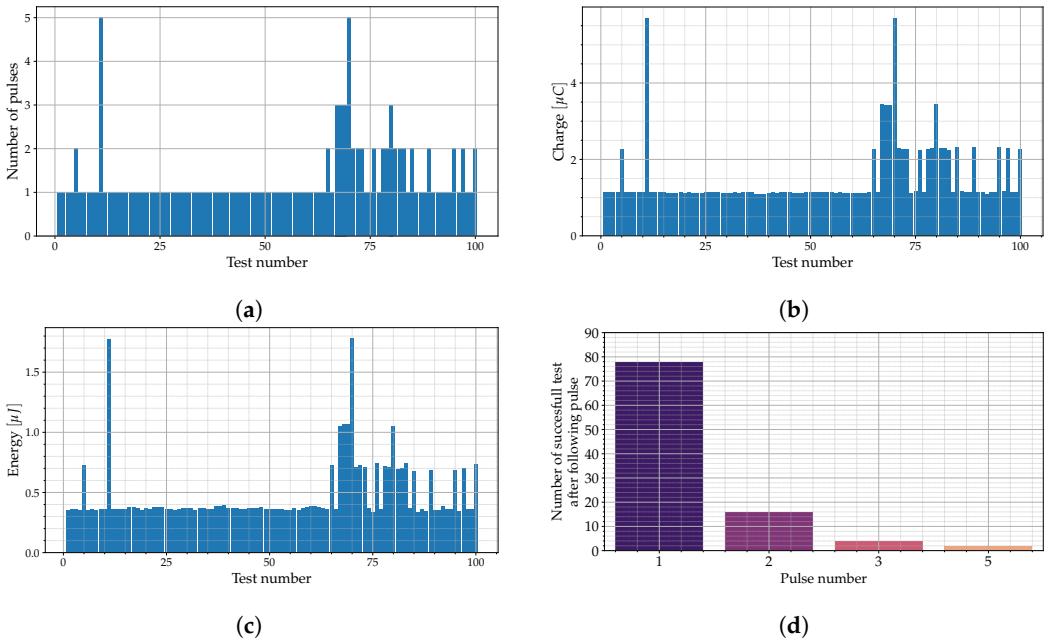


Figure 12. Experimental outcomes for tin-doped memristors subjected to a pulse with a width of 5 ms and an amplitude of 1.5 V. (**a**) The number of pulses after which the test was concluded. (**b**) The charge delivered to the memristor during the test. (**c**) The energy dissipated in the memristor during the test. (**d**) The number of tests concluded after a specific number of pulses.

6.3. Collective Analysis of the Data

To compare the results of bi-stable programming research, several comparative graphs were created. In Figure 13, the averaged energy required to write one bit is presented in the form of a bar chart, depending on the doping of the memristor, pulse width, and pulse amplitude. Additionally, to represent the spread of results, an error bar was applied, calculated based on the confidence interval [32]. The averaged energy was computed based on the cumulative energy supplied to the memristor during a single test. As observed, the average energy needed to program one bit increases with the widening of the pulse and its amplitude. It can also be inferred that for low pulse width values, the averaged energy does not significantly increase with amplitude, and in most types of memristor doping, it even decreases, the reason for this is that there is no need for a large number of programming pulses. The spread of energy values required for writing one bit is not high.

In Figure 14, the averaged charge required to write one bit is presented in the form of a bar chart, depending on the doping of the memristor, pulse width, and pulse amplitude. The charts exhibit a high correlation with the graphs in Figure 13, showing similar dependencies. This is not surprising, as energy is highly dependent on the supplied charge q.

In Figure 15, a bar chart is presented, showing the percentage of tests in which the R_{ON} state was achieved after the first pulse, depending on the doping of the memristor, pulse width, and pulse amplitude. The registered data from Figure 15 have been aggregated and shown in Table 3. It can be observed that the percentage of tests resulting in a state change after the first programming pulse increases with the widening of the pulse and its amplitude. It is noteworthy that a high efficacy (even reaching 100%) of state switching after the first programming pulse is achieved with a small pulse width of 5 ms and a high amplitude of 2 V. It can also be inferred that the chromium-doped memristor exhibits the highest efficiency in switching between states, even for low pulse amplitudes.

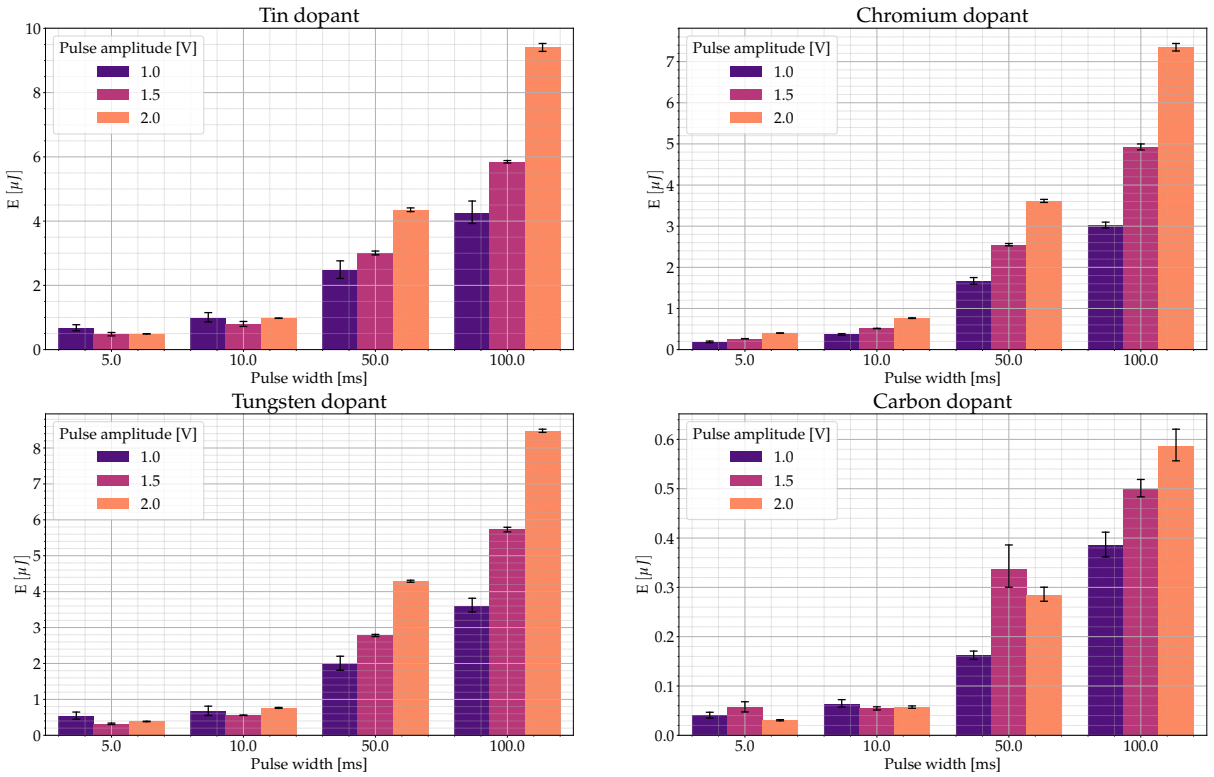


Figure 13. Comparative charts of the averaged energy required for write a single bit, as a function of memristor doping, programming pulse width, and its amplitude.

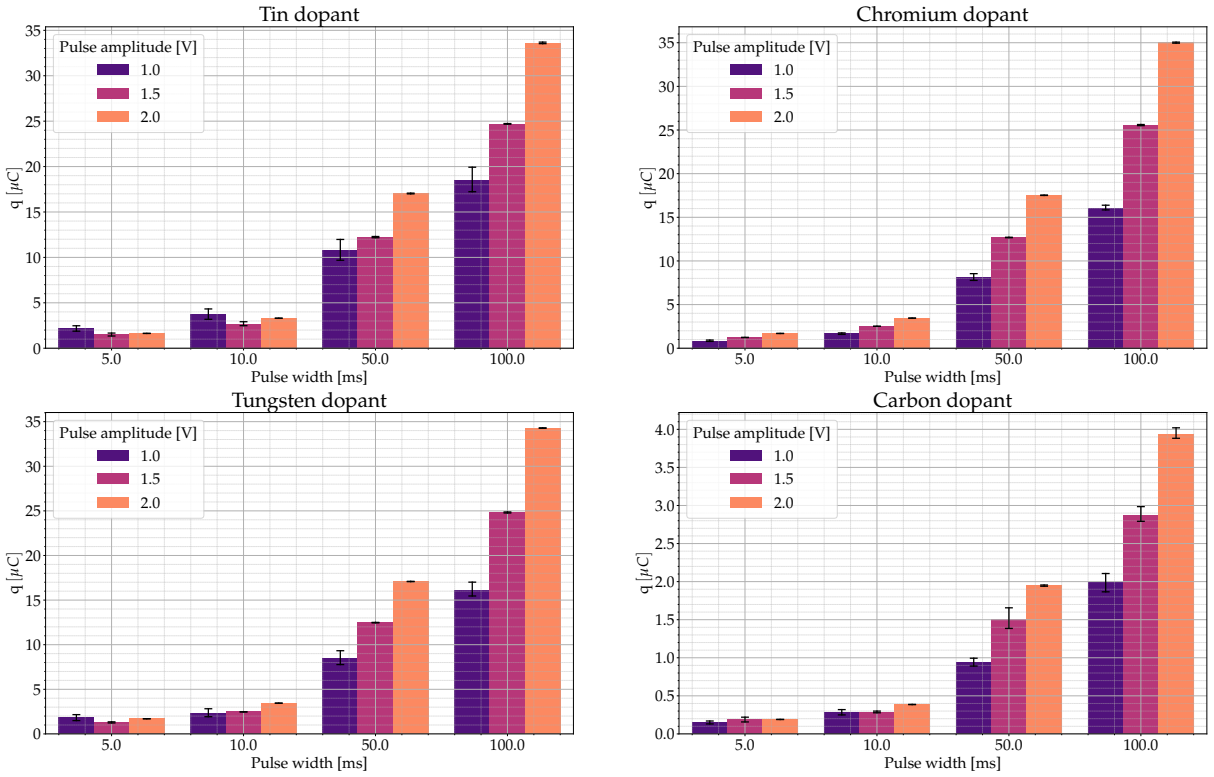


Figure 14. The averaged charge required to write one bit.

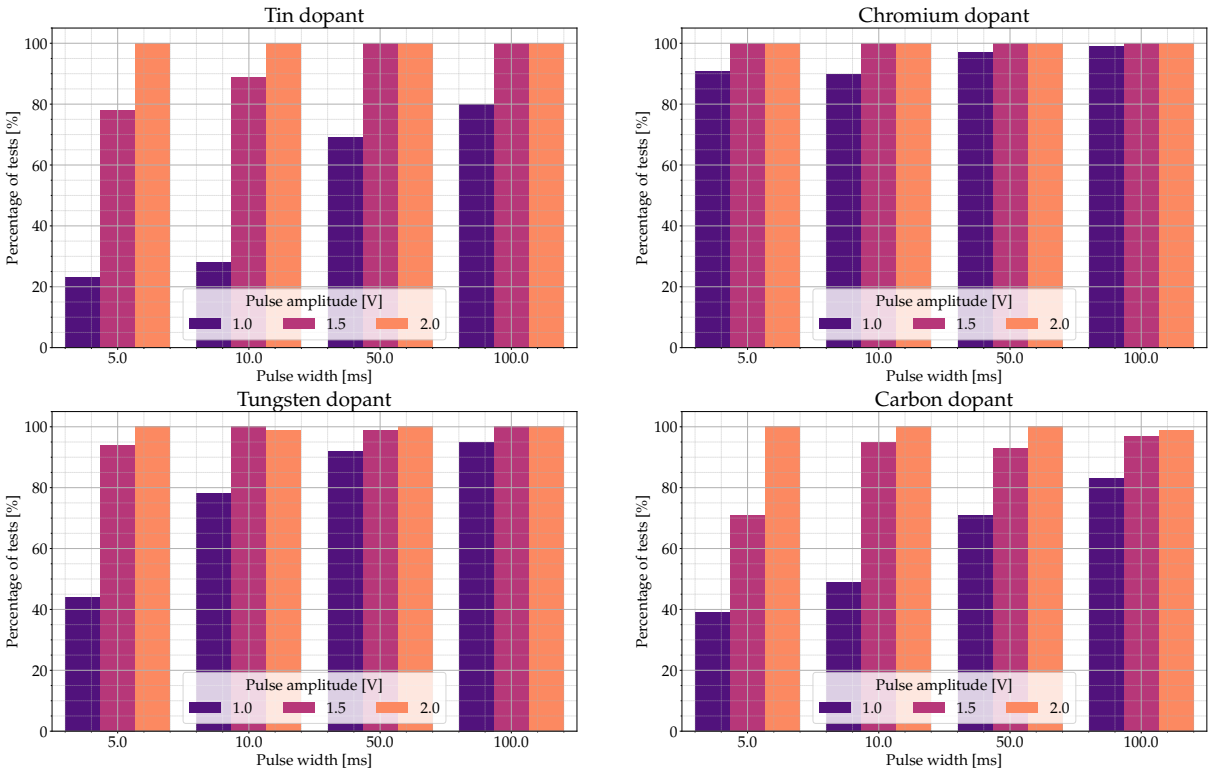


Figure 15. The percentage of tests in which the R_{ON} state was achieved after the first pulse.

Table 3. Percentage of tests in which the R_{ON} state was reached after the first pulse. Depending on pulse width Δt, pulse amplitude V_{pulse}, and memristor doping.

Dopant	**Carbon**			**Chromium**			**Tin**			**Tungsten**		
V_{pulse} [V] / Δt_{pulse}	**1.0**	**1.5**	**2.0**	**1.0**	**1.5**	**2.0**	**1.0**	**1.5**	**2.0**	**1.0**	**1.5**	**2.0**
5 ms	39	71	100	91	100	100	23	78	100	44	94	100
10 ms	49	95	100	90	100	100	28	89	100	78	100	99
50 ms	71	93	100	97	100	100	69	100	100	92	99	100
100 ms	83	97	99	99	100	100	80	100	100	95	100	100

In Figure 16, the averaged value of the resistance R_m after the first programming pulse is presented in the form of a bar chart, depending on the doping of the memristor, pulse width, and pulse amplitude. It can be observed that the average resistance of the memristor decreases with the increase in pulse width and amplitude. Additionally, the memristor resistance is much more sensitive to the amplitude of the programming pulse than its width. An increase in the amplitude of the programming pulse causes a significantly higher change in the resistance value compared to an increase in pulse width.

In Figure 17 the distribution of memristor resistance R_m, after first programming pulse, divided by its doping has been shown. As can be observed, a chromium-doped memristor exhibits the lowest resistance values after the first pulse, with values concentrated most closely around the mean resistance value.

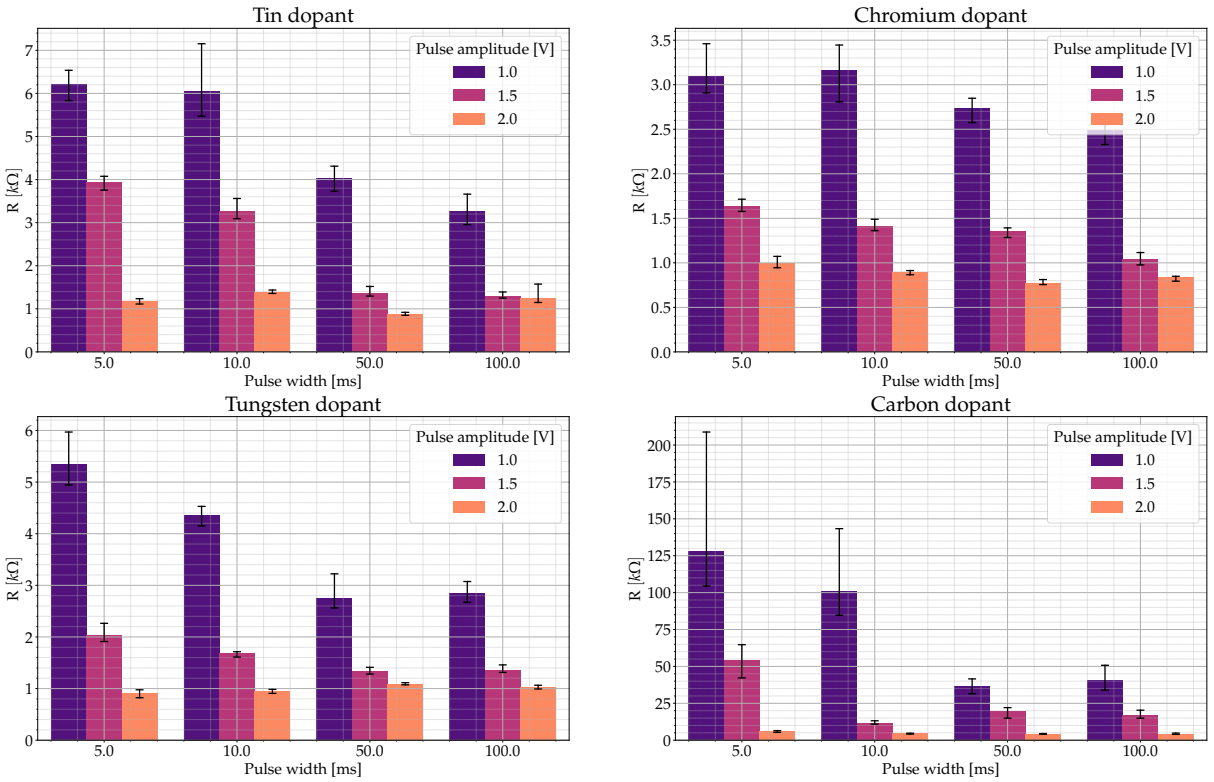


Figure 16. The averaged value of the resistance R after the first programming pulse.

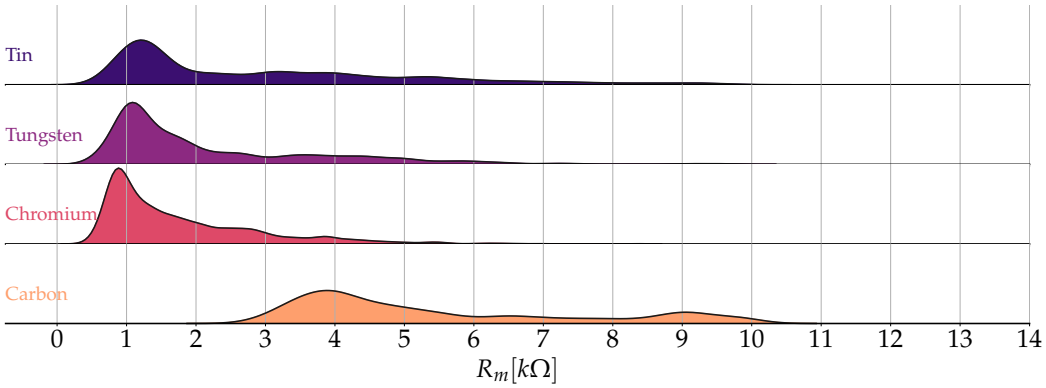


Figure 17. Distribution of the resistance values of the memristor R_m obtained after the first programming pulse with subdivisions based on its doping.

7. Conclusions

As a result of the conducted research on programming memristors, the following conclusions were drawn:

1. SDC Memristors exhibit a high certainty of switching between LRS and HRS states and seem to be appropriate candidate for a 1-bit memory cell. The carbon-doped memristors exhibit the most favorable characteristics due to their minimal average energy consumption during state transitions. However, the low nominal current may introduce measurement errors, especially in the high-resistance state (HRS) where noise and disturbances can impact accuracy.
2. The research indicates that SDC memristors are much more sensitive to the programming pulse voltage than its width. Hence, it is possible to shorten the programming time (with high certainty) by increasing the voltage and reducing the pulse width. Optimal programming is achieved with a pulse of 2 V amplitude and 5 ms width,

providing a high certainty of state switching after the initial pulse, low average energy consumption, and rapid programming.

3. Observations during certain programming tests revealed that the memristor exhibited a phenomenon known as state retention, where it became entrapped within specific resistance ranges. Subsequent pulses did not induce a change in its state, a phenomenon previously documented in the literature [33–35]. Additionally, it was observed that, to successfully program a memristor following several failed programming pulses, employing a reset pulse before the subsequent programming pulse proved more effective than relying solely on programming pulses.
4. Given the variation in resistance values observed during the execution of identical programming pulses for memristors, even those with the same doping type, it becomes imperative to validate the current state, which was also mentioned [13].
5. Due to the limited time retention characteristics of the SDC memristor, employing it as a RAM cell without periodic state refreshing poses a potential risk of inadvertent alteration of the programmed state. Therefore, the application of SDC memristors appears more suitable in neuron models, such as Leaky Integrate-and-Fire Neurons [36].
6. Precise execution of write and read operations, selection and control, as well as reliability verification of multi-state memristors, should continue to be the focus of materials and electrical engineering research.
7. The series connection of the linear resistor and memristor results in a lack of control over the amount of charge flowing through the memristor. This involves some measurement uncertainty. The workaround for this problem may be the proposal to convert the signal generation from a voltage source to a current source. This aspect is the subject of further research.
8. In the context of multi-bit memory cells, it is recommended to employ various pulse voltage values to power the memristor. The most noticeable changes occur when adjusting the amplitude, enhancing adaptability and increasing potential information storage capacity. This approach positions the memristor as a promising candidate for configurations involving multi-bit memory. The memristors' application for multi-bit memory cell is the subject of further study.
9. Future research will delve into the impact of the Joule heating effect on memristors and effect of PVT variations.

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Data Availability Statement: The data acquired during measurements and programming algorithms have been publicly shared on the GitHub platform at the following link: https://github.com/mancorz98/memristor_programming_study (accessed on 11 December 2023).

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