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Single- and Three-Phase Dual-Active-Bridge DC–DC Converter Comparison for Battery Electric Vehicle Powertrain Application

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Abstract: Dual-active-bridge (DAB) DC–DC converters are of great interest for DC–DC conversion in battery electric vehicle (BEV) powertrain applications. There are two versions of DAB DC–DC converters: single-phase (1p) and three-phase (3p) architectures. Many studies have compared these architectures, selecting the 3p topology as the most efficient. However, there is a gap in the literature when comparing both architectures when single-phase-shift (SPS) modulation is not used to drive the converter. The aim of this study was to compare 1p and 3p DAB DC–DC converters driven by optimal modulation techniques appropriate for BEV powertrain applications. Mathematical loss models were derived for both architectures, and their performances were compared. A case study of a 100 kW converter was considered as an example to visualize the overall efficiency of the converter for each layout. The 1p DAB DC–DC converter architecture outperformed the 3p layout in both its Y–Y and D–D transformer configurations. The higher performance efficiency, lower number of components, and reduced design complexity make the 1p DAB DC–DC converter topology a favorable choice for BEV powertrain applications.

Keywords: battery electric vehicles; dual-active-bridge DC–DC converter; electric powertrain; phase-shift modulation

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1. Introduction

Battery electric vehicles (BEVs) have been of great interest over the past decade, and their adoption rate has increased over the last few years. However, they are still less mature than internal combustion engine (ICE) vehicles. The three main components of a BEV powertrain are the traction battery, traction motor, and power converter, which condition the power flow between them [1]. Much research has been conducted to make BEV more competitive with internal combustion engine (ICE) vehicles. While a great portion of these works mainly focused on the traction battery or traction motor, our focus in this study was on the power-conversion stage.

The power conversion stage in a BEV powertrain is divided into DC–DC and DC–AC stages [2]. The dual-active-bridge (DAB) DC–DC converter is a promising power converter architecture for the first stage [3]. It is a well-known converter used in grid applications, battery charging stations, and onboard BEV chargers [4–11]. It has been proposed for these applications owing to its numerous features, such as galvanic isolation, high power density, efficiency, and soft-switching capability. Although there is much research discussing the DAB DC–DC converter's use in these specific applications, little research has been conducted on its use in the DC–DC conversion stage of BEV powertrains. The converter has two main topology variants: single-phase (1p) layout and three-phase (3p) layout. Many studies have compared both converter variants and selected the 3p topology as the most efficient and compact for application among the two [12–15]. However, one study conducted in [11] explored the application of 3p DAB converters within DC microgrids, comparing it with the 1p topology and evaluating various parameters affecting converter performance (efficiency, dynamic response, and soft-switching characteristics), and concluded that both 1p and 3p DAB can be used in their case study.

Although many modulation techniques are used to optimize the 1p and 3p DAB DC–DC converter efficiencies (as mentioned in Section 2), both DAB variants in these studies were only compared using the traditional single-phase-shift (SPS) modulation technique to drive the converter. SPS is known to have limitations concerning soft-switching capability and low efficiency during light-load operations or when the converter's voltage gain is far from unity. This conventional modulation technique also applies a higher current stress to the power switches and components, and its impact is greater in the 1p DAB layout than in the 3p layout.

The work presented in this paper follows a different approach than other studies to select which layout is the most appropriate for the DC–DC conversion stage of the BEV powertrain. First, optimal hybrid modulation techniques are used instead of the traditional SPS to drive the converter variants. This is in accordance with the BEV requirements because the battery and DC bus voltage values are far from each other, and the SPS is not effective in such a scenario. Second, mathematical loss models for the transformer, inductor, and power switches are established in detail to conduct an efficiency comparison. In addition, the dynamic responses of each converter variant are compared. This is fair in the comparison because both variants were compared under the optimum operating conditions. Moreover, the Y–Y and D–D 3p transformer configurations were included in the comparison with the 1p layout. This makes the work presented a more comprehensive, fair, and contextual comparison between the two DAB DC–DC converter variants, as opposed to the previously presented works. It also reduces the lack of literature on the BEV powertrain DC–DC conversion stage and extends the number of papers in the literature discussing DAB DC–DC converter topology comparisons using modulation techniques other than SPS.

This paper is divided into five sections. The first section introduces the study and provides the reader with context. The second section provides a brief but concise literature review of optimal hybrid modulation techniques that drive both 1p and 3p DAB DC–DC converter architectures. Section 3 presents a comprehensive summary of the converter waveforms operating under a suitable hybrid modulation technique for BEV powertrain applications. Section 4 provides the technical specifications of the magnetic components and power switch modules selected for the design of the three distinct converter architectures and derives the mathematical loss model of each selected component. Section 5 visualizes the graph losses of the components and the converter performance. Section 6 derives the total losses and efficiency graphs and discusses the results. Finally, Section 7 concludes the work realized in this paper. This study suggests that the 1p DAB DC–DC converter topology can outperform the 3p architecture, unlike the conclusions drawn in previous studies, especially in the field of BEV powertrain applications.

2. Literature Review of DAB DC–DC Converter Optimal Modulation Techniques

The DAB DC–DC converter layout is symmetrical. Active power switches are used to ensure bidirectional power flow [16–18]. The topologies of the 1p and 3p DAB DC–DC converters are shown in Figures 1 and 2, respectively, assuming ideal power switches and transformers. A conventional and traditional way to control the converter consists of switching semiconductor devices with 50% or 33% duty cycles for 1p and 3p architectures, respectively, delaying the secondary gate signals by a phase shift (PS). The transformer leakage inductance or external inductor serves as an instantaneous energy-storage element. The two bridges can be considered primary or secondary based on the desired power flow direction because the converter is inherently bidirectional. Although DAB DC–DC converters have many intriguing capabilities, as previously discussed, they may be vulnerable to reactive power problems (circulating currents). Taking n as the transformer turn ratio, and V_1 and V_2 as the input and output voltages of the converter, when the voltage gain $d = nV_2/V_1$ is far from unity, the reactive power increases and significantly reduces efficiency. This increases the power switch conduction and switching losses, along with the RMS current of the inductor [19,20]. In fact, if the square voltages produced by the bridges and inductor current are out of phase, the reactive power will always be a problem for the DAB DC–DC converter, and it will need to be reduced or eliminated [20].

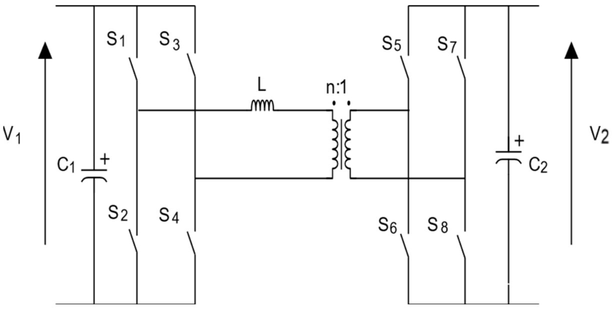
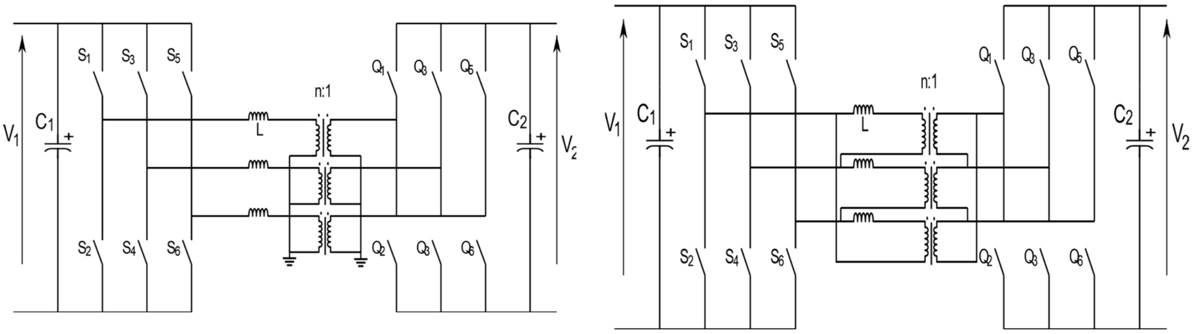


Figure 1. The 1p DAB DC-DC converter layout.



(**a**) (**b**)

Figure 2. The 3p DAB DC-DC converter configurations: (**a**) Y-Y configuration; (**b**) D-D configuration.

The voltage gain may change depending on application requirements. In BEV, the nominal voltage of the battery is approximately 400 V for regular passenger vehicles, whereas the DC bus voltage connected to the DC–AC conversion stage must be approximately 800 V [21,22]. A transformer with a unity turns ratio results in a voltage gain d = 2, which is far from unity. Significant research has been conducted to develop better modulation techniques by adding more degrees of freedom to control transferred power. Globally, these modulation strategies were grouped under triple-phase-shift (TPS) modulation for the 1p layout and duty-cycle control (DCC) for the 3p topology. This more general modulation technique uses additional degrees of freedom consisting of power switch duty cycles along with the PS ratio between the transformer′s primary and secondary. TPS and DCC have several variants. Each variant was primarily developed by solving optimization problems to minimize the inductor current RMS or peak value, minimize the fundamental reactive power, or maximize the fundamental active power. Subsequently, the final optimal duty-ratio expressions were obtained. Papers proposing the TPS and DCC modulation techniques are reviewed in this section.

2.1. The 1p DAB DC-DC Converter

For the 1p DAB DC-DC converter, the authors of [23] integrated zero-voltage switching (ZVS) constraints with the optimization of current stress and applied the Karush-Kuhn-Tucker (KKT) conditions to develop an optimal algorithm. In this algorithm, the objective function is the current stress, and the transmission power model serves as the equality constraint. All the power switches in [23] achieved ZVS throughout the entire operating range while simultaneously minimizing the current stress. However, the authors proposed seven optimal operating modes for different operating power ranges. This creates ambiguity when selecting the optimal modes to hybridize for a specific application. The authors of [24] employed an offline particle swarm optimization (PSO) method to derive a comprehensive set of TPS ratios to minimize the RMS current across the entire operating range. They also provided generalized per-unit analysis and global minimal solutions to the problem. Nevertheless, they offered 12 optimal operating modes for bidirectional power flow with different power ranges, with only a maximum power of two-thirds the converter maximum power. The authors of [25] proposed an optimal asymmetric modulation (OADM) technique to enhance the efficiency of the converter, particularly under light-load conditions. The peak inductor current was chosen as the optimization target, serving as a proxy for the RMS current, thus significantly reducing the complexity of online calculations. In addition, this modulation scheme expanded the ZVS compared to other modulations, reducing current-related losses in the converter. The authors offered four operating modes, each of which was obtained by hybridizing two modulation techniques and providing different duty-ratio expressions. This solved the ambiguity and confusion introduced by [23,24]; however, none of the proposed operation modes provided full-power range converter operation, which is inconvenient for many applications. Another approach to optimize the duty ratio is based on fundamental component approximation (FCA). The authors of [19] used the FCA to maximize the fundamental active power, whereas in [26], it was used to minimize the inductor's current fundamental amplitude. In contrast, the studies presented in [27,28] employed an FCA to minimize the fundamental reactive power. The derivation and implementation of FCA methods are straightforward and can significantly enhance 1p DAB efficiency. However, when using the FCA for square voltages, the inductor current or output power introduces significant errors when the duty ratio approaches zero. Consequently, the resulting duty ratios may not be optimal for minimizing the circulating current [29]. FCA introduces errors in light load operation, and the previously mentioned time-domain analysis (TDA) methods do not offer a full power range operation or clarify the boundaries between the operation modes. Other studies have been conducted to adhere to the TDA methods and propose solutions to the previously mentioned problems. Papers [30–32] proposed a TDA based on Lagrange functions and KKT conditions to offer optimal duty-ratio expressions for the full operating range, soft switching for almost all power switches, and minimal RMS and peak inductor current. These studies proceeded differently to select optimal duty ratios, but the three converged towards a similar hybrid modulation technique suitable for the specific application of a 1p DAB DC-DC converter for a BEV powertrain. It should be mentioned that in [33,34], multiagent (MA) artificial intelligence (AI)-based TPS was introduced to tackle challenges in DC microgrids such as uncertainties, conserving power balance, minimizing current stress, and output voltage regulation. These new approaches improve the converter dynamic response performance and mitigate many challenges of input-series output-parallel (ISOP) DAB converters and solid-state transformers (SSTs). However, the TPS modes used were already discussed in [21], and based on them, the optimal hybrid modulation scheme was derived in that study. In addition, the BEV powertrain does not require several DAB converters to work together and does not suffer from the uncertainty problem as in DC microgrid applications, particularly for regular BEVs. Because dynamic selection of different duty ratios based on various TPS modulation modes is not required in the case of BEVs, this study focused only on using a predefined DAB model based on a preselected modulation technique. Consequently, the hybrid modulation technique proposed in [30–32] is discussed in detail, and the 1p architecture design is based on this in the upcoming sections.

2.2. The 3p DAB DC–DC Converter

Regarding the 3p DAB DC-DC converter, the authors of [35,36] offered a simultaneous pulse-width modulation (PWM) technique in which the duty cycles of both the primary and secondary bridges were forced to be equal, adding an additional degree of freedom compared with SPS and offering a wider ZVS range. Seven switching modes were introduced, each with an overlapping ZVS range. However, these studies only examined the potential ZVS ranges of 3p DAB and did not offer solutions for determining optimal control parameters. An optimized modulation strategy was proposed in [37] to minimize the RMS inductor current. The multifrequency approximation method was developed and used to deduce the analytical expressions for the RMS inductor current and transmission power. Based on this, an optimization algorithm using the interior-point method is employed to address the RMS current minimization problem and determine the control variables for the modulation strategy. However, the authors did not provide any information about the soft-switching range or detailed converter losses and only focused on the minimized RMS current compared to the SPS modulation. The work in [38] introduced an optimized hybrid modulation scheme that minimized the total power losses in the converter under varying load and voltage conditions. The optimization scheme, which considers switching, conduction, and core losses, determines the optimal operating mode for a given operating point by choosing between novel zero-vector modulation and traditional SPS. The proposed modulation technique divides converter operation into 12 distinct modes. The current and power expressions are given for each, and they offer considerable efficiency improvements under light-load conditions. However, the boundaries between the modes are not clear, and the selection of numerous operating modes for real-time operation is complex. A much simpler modulation with fewer operating modes was proposed in [39,40], known as asymmetric duty-cycle control (ADCC). Triangular and trapezoidal current modes were introduced, analyzed, and integrated. Loss analysis demonstrated that the proposed modulation schemes significantly reduced both semiconductor and transformer losses and extended the zero-current switching (ZCS) range, particularly under light-load conditions. The proposed hybrid modulation divides the 3p DAB operation into three modes: a light-load mode, where the phase currents have a triangular shape; a medium-power mode, where the currents have a trapezoidal shape; and a heavy-load mode using SPS. The boundaries between the operation modes are provided along with the duty cycles and power expressions for each mode. The research in [41] proposed a DCC optimal modulation strategy (OMS) for 3p DAB, leveraging a novel piecewise TDA and optimization process to derive the optimal control parameters for minimizing the RMS phase current. Furthermore, it introduced a new closed-form minimum current stress optimization (MCSO) DCC scheme based on the theoretical findings of the TDA optimization. The MCSO scheme effectively reduces the transformer phase currents and extends the soft-switching range under partial-load conditions and wide voltage variations. Compared with the ADCC proposed in [40,41], the OMS and MCSO offer better efficiency over a wide voltage range and fixed power. However, for a fixed voltage gain and varying power, the modulation techniques exhibit almost the same performance. In addition, three of them used the triangular mode for extremely light-load operations. Another modulation strategy proposed in [42] enhances the soft-switching range of 3p DAB, even with significant voltage variations. The loss analysis demonstrated that this strategy significantly improved the efficiency of 3p DAB, particularly under light-load conditions. The authors also used the triangular current mode in a light-load operation. However, they did not explicitly express the different duty cycles and converter powers. For simplicity, and because the 3p DAB application in this study does not require a wide voltage range operation, the work presented in this paper mainly uses the analysis provided by [39,40] for 3p DAB, which is discussed in more detail in the upcoming section.

3. DAB DC-DC Converter Optimal Operation for BEVs Powertrain

In this section, the hybrid modulation techniques based on which the 1p and 3p DAB DC-DC architectures are compared and reviewed. To keep the review short and simple, and due to DAB's symmetrical operation and its specific application discussed in this paper, only the boost forward operation ($d > 1$ and the power is transmitted from the battery to the DC-AC stage) is considered. Duty cycles and power expressions are provided. In the next section, inductor and line current expressions are provided along with their typical waveforms to obtain a better understanding of the component design, selection, and loss calculation.

3.1. The 1p DAB DC-DC Converter

During light-load operation, the triangular phase-shift (TrgPS) modulation technique is recognized as the most suitable method to drive the 1p DAB while optimizing the RMS/circulating currents along the ZVS range [20,30–32,43,44]. Typical voltages and current waveforms are shown in Figure 3, and the inductor current expression is given by Equations (1) and (2). The duty ratios during this operation, D_1 and D_2, which are the primary and secondary inner duty ratios, respectively, and D_3, which is the PS duty ratio between the primary and secondary sides, are given as a function of D_f in (3) (their expressions are given with respect to the half-switching period T_h for waveform symmetry). D_f is the PS duty ratio between the positive end potential V_p of the inductor and the secondary voltage of the transformer brought to the primary V_s fundamentals [19,20,45]. Its expression is given by Equation (4). This is considered the converter control input to reduce the number of control variables from three to one. Furthermore, unlike the remaining duty ratios, this is the only control variable monotonically related to the input power. The TrgPS power expression, along with its minimum and maximum values, is expressed in (5) and (6), respectively.

$$0 < t < D_3T_h \ : \ i_L(t) = \frac{V_1}{L}t \tag{1}$$

$$D_3T_h < t < D_2T_h \ : \ i_L(t) = \frac{(V_1 - nV_2)}{L}(t - D_3T_h) + \frac{V_1}{L}D_3T_h \tag{2}$$

$$\begin{cases} D_1 = \frac{2d}{d\ -1}D_f \\ D_2 = \frac{2}{d\ -1}D_f \\ D_3 = D_2 - D_1 \end{cases} \tag{3}$$

$$D_f = \frac{D_2}{2} - \frac{D_1}{2} + D_3 \tag{4}$$

$$0\ <\ D_f < \frac{d\ -1}{2d}:\ P_{1p_{Trg}} = \frac{dV_1^2D_f^2}{(d\ -1)f_sL} \tag{5}$$

$$\begin{cases} P_{1p\_Trg\_min} = 0 \\ P_{1p\_Trg\_max} = \frac{(d\ -1)V_1^2}{4df_sL} \end{cases} \tag{6}$$

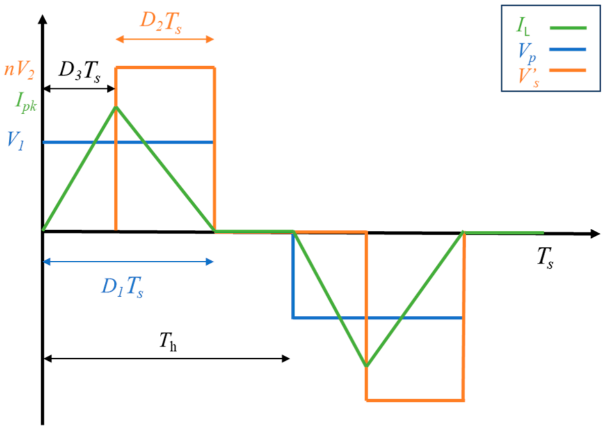


Figure 3. Single-phase triangular phase-shift modulation.

In heavy-load conditions, the authors of [20,30–32,46] showed that the extended phase-shift (EPS) modulation technique is the most appropriate modulation method for driving the DAB DC-DC converter. The typical waveforms for this modulation are shown in Figure 4. The main difference between EPS and conventional SPS modulation techniques is the introduction of an additional degree of freedom along with the bridge PS, which is the inner PS between the two-phase legs of the transformer's secondary side for boost operation. The primary PS ratio D_1 remained unchanged and was forced to be equal to one. The legs of the two primary phases are always phase-shifted by half of the switching period T_h. The inductor current and duty-cycle expressions are given by Equations (7)–(10), and (11), respectively. The converter transferred power expression is given by (12), where the minimum and permissible maximum powers under this operating mode are given by Equation (13).

$$0 < t < t_1 = (D_3 + D_2 - 1)\ T_h : \ i_L(t) = \frac{(V_1 + nV_2)}{L} t + i_L(0) \tag{7}$$

$$t_1 < t < D_3 T_h : \ \ i_L(t) = \frac{V_1}{L}(t - t_1) + \frac{(V_1 + nV_2)}{L} t_1 + i_L(0) \tag{8}$$

$$D_3 T_h < t < T_h : \ i_L(t) = \frac{V_1 - nV_2}{L}(t - D_3 T_h) + \frac{V_1}{L}(1 - D_2 T_h) + \frac{(V_1 + nV_2)}{L} t_1 + i_L(0) \tag{9}$$

$$i_L(0) = -i_L(D_3 T_h) = -\frac{(V_1 + nV_2(D_2 + D_3 - 2))}{4L} T_h \tag{10}$$

$$\begin{cases} D_1 = 1 \\ D_2 = 1 + (d \ - 1)\left(2D_f - 1\right) \\ D_3 = \frac{d\left(2D_f - 1\right) + 1}{2} \end{cases} \tag{11}$$

$$\frac{d \ - 1}{2d} < \ D_f < \frac{1}{2}: \ P_{1p_{EPS}} = \frac{dV_1^2\left(4D_f\left(1 \ - D_f\right)\left(d^2 - 2d + 2\right) - (d \ - 1)^2\right)}{8f_s L} \tag{12}$$

$$\begin{cases} P_{1p\_EPS\_min} = P_{1p\_Trg\_max} \\ P_{1p\_EPS\_max} = \frac{dV_1^2}{8f_s L} \end{cases} \tag{13}$$

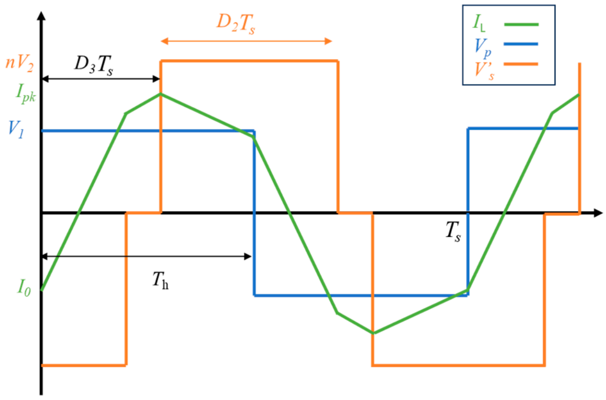


Figure 4. Single-phase extended phase-shift modulation.

3.2. The 3p DAB DC-DC Converter Y-Y Configuration

Compared to 1p DAB, despite the higher number of components, 3p DAB converter operation under the conventional SPS modulation technique provides a number of additional advantages, such as improved magnetic material use, significantly smaller dc-link capacitors, and thus, higher power density from a theoretical point of view [47]. However, under SPS operation, the 3p DAB suffers from the circulating/RMS current problem and a limited ZVS range when the voltage gain d is far from unity. To increase the soft-switching range and decrease the RMS/circulating current effect throughout a large voltage range, the asymmetrical duty-cycle control (ADCC) method was addressed in [40]. Two optimal modulation techniques have been suggested, analyzed, and smoothly combined in hybrid modulation for 3p DAB DC-DC converter operation depending on the operation power level, that is, light or heavy load operation. These modulation techniques greatly enhance converter efficiency based on the asymmetrical duty-cycle technique used in other isolated dc-dc converters [36,37,42,48–51]. D_f is still used as the main control parameter, and because, in the case of 3p DAB, waveform analysis is realized for the entire switching period T_s, its expression is given by an analogy to (4) in (14).

For light-load operations, 3p-TrgPS modulation has been proven to be the optimal modulation technique that extends the soft-switching range and minimizes the RMS current. Its name is derived from the inductor current shape, because the current waveform is triangular [39–42]. Typical waveforms for this modulation for a Y-Y transformer configuration are shown in Figure 5. The inductor current and duty-cycle expressions are given by Equations (14)–(16). For intervals $\mathrm{T_s/3 + D_1T_s < t < D_2T_s{+}T_s/3}$ and $\mathrm{2T_s/3 < t < D_2T_s{+}2T_s/3}$, the inductor current expression can be derived similarly to the first interval simply by dividing by -2. Note that the analysis is performed for the entire switching period T_s; therefore, the expression of D_f becomes that described in (17). The converter transferred power expression is given by (18), where the minimum and permissible maximum powers under this operating mode are given by (19).

$$0 < t < D_3T_s : \ i_L(t) = \frac{2}{3}\frac{V_1}{L}t \tag{14}$$

$$D_3T_s < t < D_1T_s : \ i_L(t) = \frac{2}{3}\frac{(V_1 - nV_2)}{L}(t - D_3T_s) + \frac{2}{3}\frac{V_1}{L}D_3T_s \tag{15}$$

$$\begin{cases} D_1 = \frac{d}{d\ -1}D_f \\ D_2 = \frac{1}{d\ -1}D_f \\ D_3 = D_f \end{cases} \tag{16}$$

$$D_f = D_2 - D_1 + 2D_3 \tag{17}$$

$$0 < D_f < \frac{d-1}{3d} : \ P_{Y-Y_{Trg}} = \frac{dV_1^2D_f^2}{(d-1)f_sL} \tag{18}$$

$$\begin{cases} P_{Y-Y\_Trg\_min} = 0 \\ P_{Y-Y\_Trg\_max} = \frac{(d-1)V_1^2}{9df_sL} \end{cases} \tag{19}$$

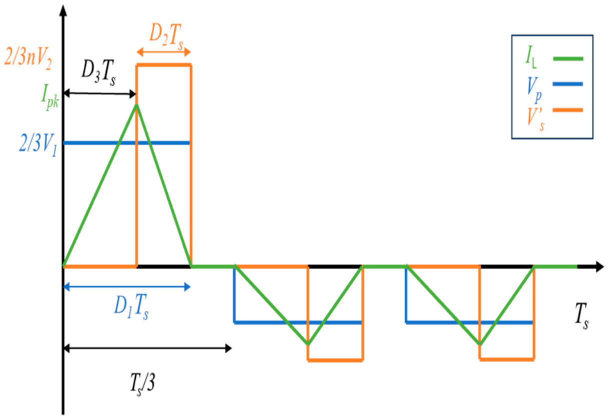


Figure 5. Y-Y three-phase triangular phase-shift modulation.

The load angle D_f can be increased further to provide more power to the converter. Consequently, the inductor current shape became trapezoidal, as shown in Figure 6. Therefore, the modulation technique is known as 3p trapezoidal phase-shift (3p-TrapPS) modulation. This modulation has been proven to be optimal for operations above the 3p-TrgPS boundaries [39,40,52]. The inductor current and duty-cycle expressions are given by (20)–(22) and (23), respectively, for the Y-Y transformer configuration: for intervals $\mathrm{T_s/3 + D_1T_s < t < D_2T_s + T_s/3}$ and $\mathrm{2T_s/3 < t < D_2T_s + 2T_s/3}$, the inductor current expression can be derived similarly to the first interval simply by dividing by −2. The converter transferred power expression is given by (24), where the minimum and permissible maximum powers under this operating mode are given by (25).

$$0 < t < D_3T_s:\ i_L(t) = \frac{2}{3}\frac{V_1}{L}t \tag{20}$$

$$D_3T_s < t < D_1T_s:\ i_L(t) = \frac{2}{3}\frac{(V_1 - nV_2)}{L}(t - D_3T_s) + \frac{2}{3}\frac{V_1}{L}D_3T_s \tag{21}$$

$$D_1T_s < t < T_s/3:\ i_L(t) = -\frac{2}{3}\frac{nV_2}{L}(t - D_1T_s) + \frac{2}{3}\frac{(V_1 - nV_2)}{L}(D_1T_s - D_3T_s) + \frac{2}{3}\frac{V_1}{L}D_3T_s \tag{22}$$

$$\begin{cases} D_1 = \frac{d\left(2\ -3D_f\right)}{3(1+d)} \\ D_2 = \frac{\left(2\ -3D_f\right)}{3(1+d)} \\ D_3 = \frac{1}{3} -\ D_2 \end{cases} \tag{23}$$

$$\frac{d-1}{3d} < D_f < \frac{d^2+1}{3(d^2+d+1)}:\ P_{Y-Y_{Trap}} = \frac{dV_1^2\left(6D_f\left(d^2+1\right) - 9D_f^2\left(d^2+d+1\right) - (1-d)^2\right)}{9f_sL(1+d)^2} \tag{24}$$

$$\begin{cases} P_{Y-Y\_Trap\_min} = P_{3p\_Trg\_max} \\ P_{Y-Y\_Trap\_max} = \frac{d^2V_1^2}{9f_sL(d^2+d+1)} \end{cases} \tag{25}$$

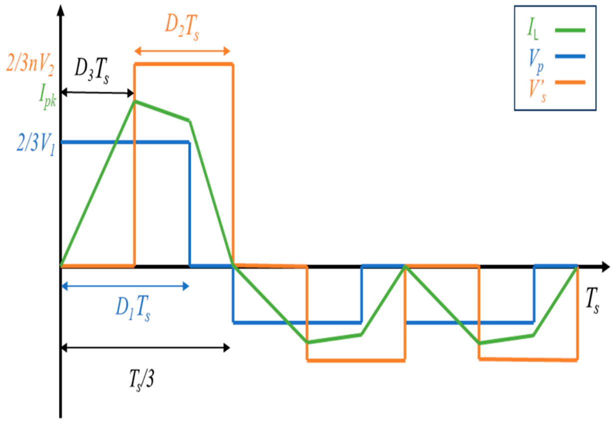


Figure 6. Y-Y three-phase trapezoidal phase-shift modulation.

3.3. The 3p DAB DC-DC Converter D-D Configuration

For a D-D transformer configuration rated at the same Y-Y transformer power, the duty-cycle expression remains the same, and the soft-switching feature remains unchanged. However, the phase inductance is three times greater than the line inductance of the Y-Y configuration, and the inductor current is reduced considerably [47]. Typical waveforms for 3p-TrgPS for a D-D transformer configuration are shown in Figure 7. The inductor current expression is given by (26) and (27). The converter transferred power expression is given by (28), where the minimum and maximum powers in this operating mode are given by (29).

$$0 < t < D_3T_s:\ i_L(t) = \frac{V_1}{L}t \tag{26}$$

$$D_3T_s < t < D_1T_s\ :\ i_L(t) = \frac{(V_1\ - nV_2)}{L}(t - D_3T_s) + \frac{V_1}{L}D_3T_s \tag{27}$$

$$0\ <\ \mathrm{D_f} < \frac{\mathrm{d}\ -1}{3\mathrm{d}}:\ \mathrm{P_{D-D_{Trg}}} = \frac{3\mathrm{dV_1^2D_f^2}}{(\mathrm{d}\ -1)\mathrm{f_sL}} \tag{28}$$

$$\begin{cases} \mathrm{P_{D-D\_Trg\_min}} = 0 \\ \mathrm{P_{D-D\_Trg\_max}} = \frac{(\mathrm{d}-1)\mathrm{V_1^2}}{3\mathrm{d}\mathrm{f_s}\mathrm{L}} \end{cases} \quad (29)$$

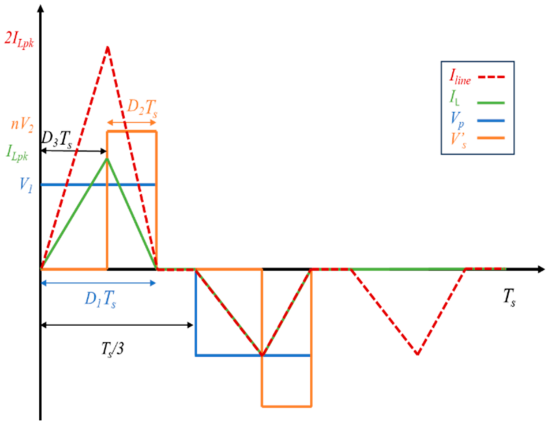


Figure 7. D-D three-phase triangular phase-shift modulation.

The 3p-TrapPS waveforms for the D-D configuration are shown in Figure 8. The inductor current for this operating mode is expressed in Equations (30)–(32), and the minimum and maximum powers are expressed in (33) and (34), respectively. Note that for both operating modes in the D-D configuration, the waveform during the second third of the period is of the opposite sign to that of the first third period and is null during the last third of the period. The line current for phase A is expressed as $i_{LA}(t) - i_{LC}(t)$.

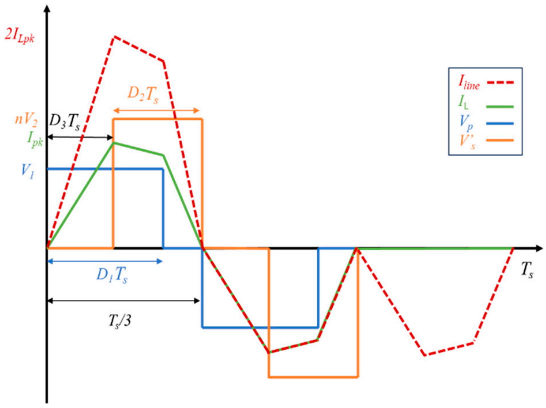


Figure 8. D-D three-phase trapezoidal phase-shift modulation.

$$0 < t < D_3T_s : \; i_L(t) = \frac{V_1}{L}t \quad (30)$$

$$D_3T_s < t < D_1T_s \; : \; i_L(t) = \frac{(V_1 - nV_2)}{L}(t - D_3T_s) + \frac{V_1}{L}D_3T_s \quad (31)$$

$$D_1T_s < t < T_s/3 : \; i_L(t) = -\frac{nV_2}{L}(t - D_1T_s) + \frac{(V_1 - nV_2)}{L}(D_1T_s - D_3T_s) + \frac{V_1}{L}D_3T_s \quad (32)$$

$$\frac{d-1}{3d} < D_f < \frac{d^2+1}{3(d^2+d+1)} : P_{D-D_{Trap}} = \frac{dV_1^2\left(6D_f\left(d^2+1\right) - 9D_f^2\left(d^2+d+1\right) - (1-d)^2\right)}{3f_sL(1+d)^2} \quad (33)$$

$$\begin{cases} P_{D-D\_Trap\_min} = P_{3p\_Trg\_max} \\ P_{D-D\_Trap\_max} = \frac{d^2V_1^2}{3f_sL(d^2+d+1)} \end{cases} \quad (34)$$

4. Magnetic Component and Power Switch Loss Models

In this section, the magnetic components and power switches of each converter variant are selected, and their loss models and loss graphs are derived. The converter parameters are V_1 = 400 V, V_2 = 800 V, n = 1, f_s = 25 kHz, P_{max} = 100 kW. The magnetic material selected is the 2605SA1 iron-based Metglas amorphous alloy with a relative permeability of μ_r = 45,000, saturation flux density of B_{sat} = 1.56 T, core loss coefficient $K_c = 1.92 \times 10^{-4}$, and other material constants α = 1.51 and β = 1.74. The different core utilization factors were fixed at K_u = 0.4. Input and output capacitor analyses are not included in this section for various reasons. First, the capacitance values must be determined based on the battery management strategy and the required minimal value to maintain the output DC bus voltage constant and the inverter in the DC-AC stage operational. Second, the input and output capacitances are usually in the form of parallel connections of similar capacitor values, which reduces the equivalent series resistance (ESR), thus making the capacitor losses negligible compared to the other component losses, which would not affect the comparative study realized in this study.

4.1. Transformer Loss Model

The transformer design methodology began by aggregating the initial specifications, including the apparent power *VA*, voltage constant K_v, frequency f_s, and utilization factor K_u. Next, the appropriate material was selected based on its saturation flux density B_{sat}, core loss coefficient K_c, and other material constants α and β. The optimal flux density B_o was calculated using the selected material. The flux density was then compared to B_{sat}. If B_o is less than B_{sat}, the process proceeds by calculating and selecting the core area product, A_p. Otherwise, it is adjusted using iterations until B_{max} is less than or equal to B_{sat}. Subsequently, the core dimensions, including the core cross-sectional area A_c, window area W_a, mean length per turn *MLT*, and magnetic path length *MPL* were extracted. Based on these dimensions, the number of primary turns N_p required for the transformer was deduced. The current density J was then calculated to ensure that the wire could handle the required current and the appropriate cross-sectional area A_w of the bare wire was selected. Subsequently, two different losses were calculated: winding loss P_w owing to the high-frequency resistance of the wire R_{AC}, and core loss P_c based on the selected material properties and operating conditions. Finally, the total loss was determined by summing the winding and core losses, and the transformer efficiency was calculated by considering the total loss and input power. A flowchart depicting the power converter transformer design methodology is illustrated in Figure 9, and all the related equations for each step are provided in detail in [53,54].

Table 1 summarizes the transformers' rated electrical specifications for the three DAB DC-DC converter layouts: the maximum RMS voltage and current and the maximum apparent power. Table 2 lists the magnetic core dimensions, and Table 3 lists the winding specifications.

Table 1. Transformer rated electrical characteristics.

Layout	V_{rms} (V)	I_{rms} (A)	Apparent Power (kVA)
1p	800	323	517
Y-Y	247	215	106
D-D	303	124	75

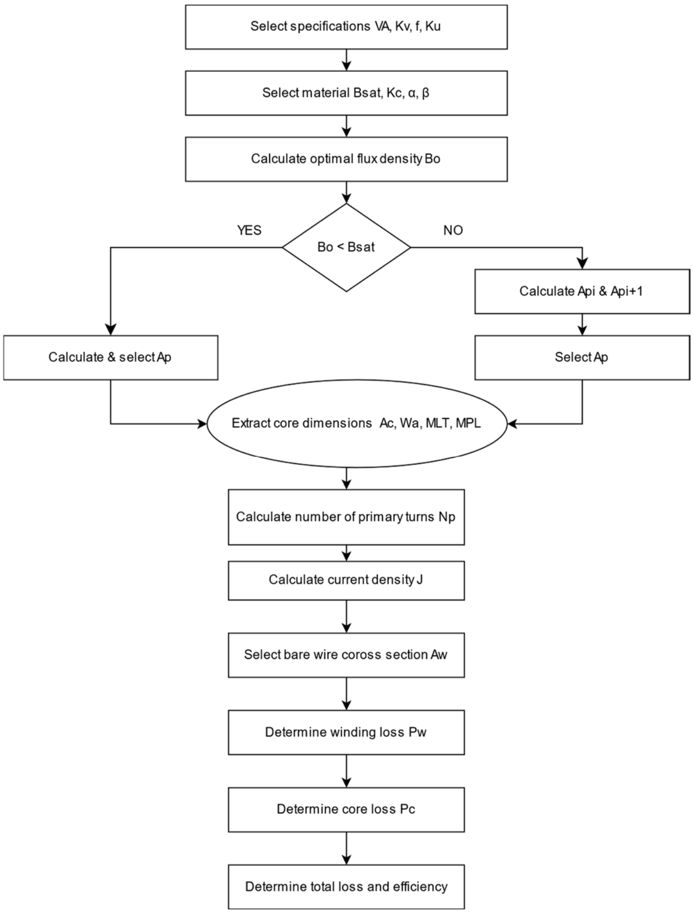


Figure 9. Transformer design methodology.

Table 2. Transformer magnetic core characteristics.

Layout	Core Number	A_p (cm^4)	A_c (cm^2)	MLT (cm)	Mass (Kg)
1p	AMCC400	348.8	11.7	17.4	2.817
Y-Y/D-D	CACC(E)47	105.75	4.5	9	0.891

Table 3. Transformer winding characteristics.

Layout	Wire Type	Profile (mm^2)	A_w (mm^2)	N_p/N_s	R_{DC} (mΩ)	R_{AC} (mΩ)
1p	4500 × 0.1	11.3 × 7	35.33	10/10	2.3	5.2
Y-Y	1380 × 0.1	7.4 × 3.4	10.84	6/6	2.8	3.4
D-D	1380 × 0.1	7.4 × 3.4	10.84	9/9	4	6.32

Because the excitation is non-sinusoidal, the core loss is calculated based on the improved General Steinmetz Equation (iGSE) using a piecewise linear (PWL) model. The expressions for the core and winding losses for the 1p architecture are given in (35). It should be noted that the peak-to-peak flux density ΔB, D_2, and I_{Lrms} expressions depend on the operating mode of the 1p-TrgPS or EPS. It should be noted that the electrical and winding specifications for the 3p Y-Y and D-D transformers were provided for only one phase. The expressions for the core and winding losses are given in (36) and (37) for the Y-Y and D-D configurations, respectively. ΔB is the peak-to-peak flux density of each phase; D_2 and I_{Lrms} expressions depend on the operating mode of 3p-TrgPS or 3p-TrapPS. The flux of each phase interacts with the others within the same core. A fair approximation of the resulting peak-to-peak flux within the core can be expressed as $\Delta\mathrm{B}/\sqrt{3}$:

$$\begin{cases} P_c = mK'_c \Delta B^{\beta - \alpha} \frac{1}{T_h} \int \left(\frac{\Delta B}{D_2 T_h} \right)^{\alpha} dt \\ K'_c = \frac{K_c}{2^{\beta - 1} \pi^{\beta - 1} \int_0^{2\pi} |cos\theta|^{\alpha} d\theta} \\ \Delta B_{Trg} = \frac{1}{N_p A_c} \int_{D_3 T_h}^{D_1 T_h} nV_2 dt \\ \Delta B_{EPS} = \frac{1}{N_p A_c} \int_{D_3 T_h}^{(D_3 + D_2) T_h} nV_2 dt \\ P_w = R_{AC} {I_{Lrms}}^2 \end{cases} \tag{35}$$

$$\begin{cases} P_c = mK'_c \left(\frac{\Delta B}{\sqrt{3}} \right)^{\beta - \alpha} \frac{1}{T_h} \int \left(\frac{\Delta B}{\sqrt{3} D_2 T_s} \right)^{\alpha} dt \\ \Delta B_{Trg} = \frac{1}{N_p A_c} \int_{D_3 T_s}^{D_1 T_s} \frac{2}{3} nV_2 \mathrm{dt} \\ \Delta B_{Trap} = \frac{1}{N_p A_c} \int_{D_3 T_s}^{\frac{T_s}{3}} \frac{2}{3} nV_2 dt \\ P_w = R_{AC} {I_{Lrms}}^2 \end{cases} \tag{36}$$

$$\begin{cases} P_c = mK'_c \left(\frac{\Delta B}{\sqrt{3}} \right)^{\beta - \alpha} \frac{1}{T_h} \int \left(\frac{\Delta B}{\sqrt{3} D_2 T_s} \right)^{\alpha} dt \\ \Delta B_{Trg} = \frac{1}{N_p A_c} \int_{D_3 T_s}^{D_1 T_s} nV_2 dt \\ \Delta B_{Trap} = \frac{1}{N_p A_c} \int_{D_3 T_s}^{\frac{T_s}{3}} nV_2 dt \\ P_w = R_{AC} {I_{Lrms}}^2 \end{cases} \tag{37}$$

4.2. Inductor Loss Model

The AC inductor design methodology began by aggregating the initial specifications, including VA, K_v, f_s, K_u, J. Next, the appropriate material was selected based on B_{sat}, K_c, α, and β. Using the selected material, A_p was calculated, and the core was selected. The core dimensions A_c, W_a, MLT, and MPL were extracted. Based on these dimensions, the number of turns N required for the inductor was calculated. The required air-gap length l_g in the core to achieve the desired inductance was then deduced, followed by the calculation of the fringing flux F resulting from the air gap. Subsequently, N was recalculated by considering the effect of F on the magnetic circuit. The flux density ΔB_L in the core was deduced based on the recalculated number of turns and the core dimensions. An appropriate A_w for the bare wire was selected to handle the required current. Then, three different losses were calculated: P_w, P_c, and the air-gap loss, P_g. Finally, the total loss was determined, and the efficiency of the inductor was calculated by considering the total loss and input power. A flowchart depicting the AC inductor design methodology is illustrated in Figure 10, and all related equations for each step are provided in detail in [53].

Table 4 summarizes the inductor-rated electrical specifications: the RMS voltage, current, maximum apparent power, and inductance. Table 5 lists the magnetic cores dimensions in addition to the core build '*a*' which is used in the gap loss calculation formula. Table 6 lists the winding specifications of the inductors. It should be noted that for the 3p configuration, the specifications were applied to three identical inductors for each phase. The expressions for the core, gap (where K_g is a geometry coefficient and its specific value for C cores is 0.0775), and winding losses are given by (38). The expressions for ΔB_L, inductor voltage $v_L(t)$, PWL integral time interval Δt, and I_{Lrms} depend on the operating mode:

$$\begin{cases} P_c = mK'_c {\Delta B_L}^{\beta - \alpha} \frac{1}{T_s} \int \left(\frac{v_L(t)}{A_c N} \right)^{\alpha} dt \\ P_g = maK'_g l_g f_s \Delta B_L \frac{1}{T_s} \int \left(\frac{v_L(t)}{A_c N} \Delta t \right) dt \\ K'_g = \frac{K_g}{2^{-1} \int_0^{2\pi} |cos\theta| d\theta} \\ P_w = R_{AC} {I_{Lrms}}^2 \end{cases} \tag{38}$$

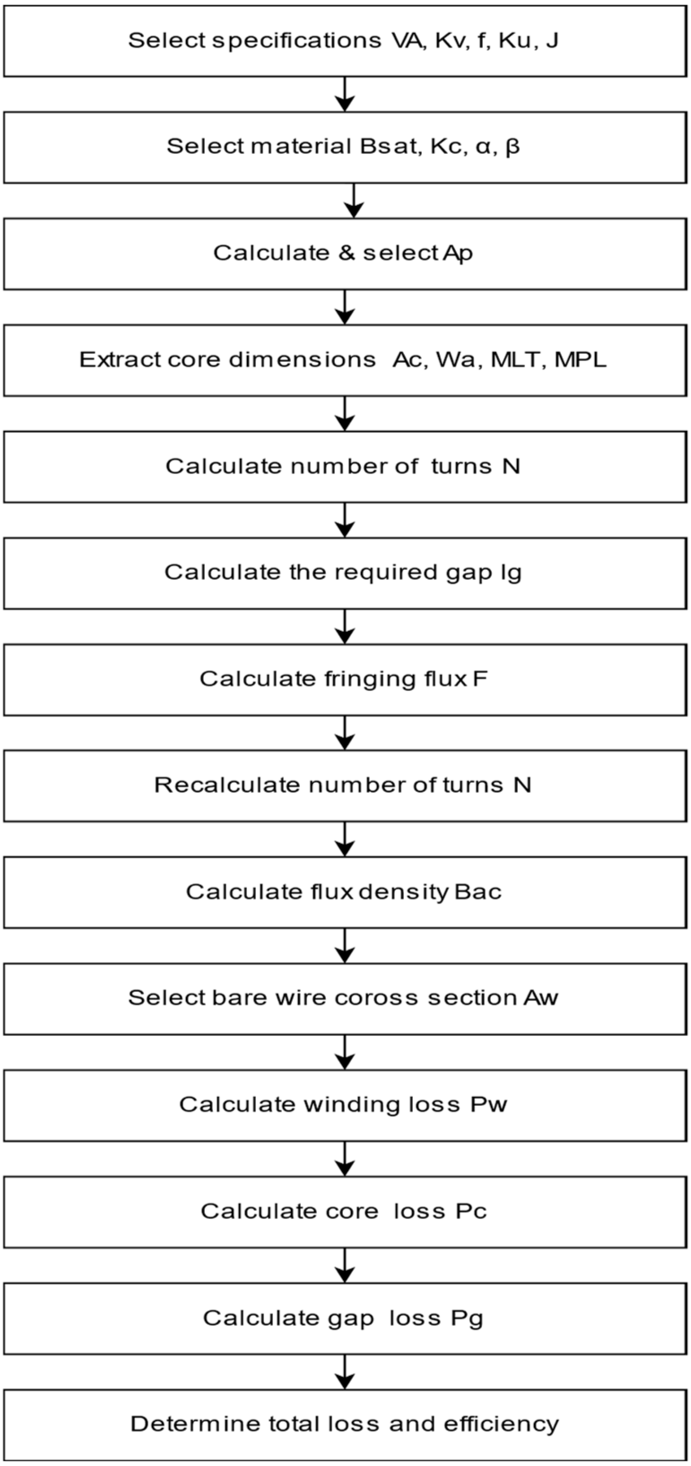


Figure 10. AC inductor design methodology.

Table 4. Inductor rated electrical characteristics.

Layout	V_{rms} (V)	I_{rms} (A)	Apparent Power (kVA)	L (μH)
1p	895	323	289	16
Y-Y	203	215	44	4.06
D-D	390	124	49	12.2

Table 5. Inductor magnetic core characteristics.

Layout	Core Number	A_p (cm^4)	A_c (cm^2)	MLT (cm)	l_g (cm)	a (cm)	Mass (Kg)
1p	AMCC312A	89.25	7.01	12.8	0.35	1.9	1.281
Y-Y	AMCC40	31.3	3.7	9.6	0.18	1.3	0.53
D-D	AMCC40	31.3	3.7	9.6	0.13	1.3	0.53

Table 6. Inductor winding characteristics.

Layout	Wire Type	Profile (mm^2)	A_w (mm^2)	N	R_{DC} (mΩ)	R_{AC} (mΩ)
1p	4500 × 0.1	11.3 × 7	35.33	8	0.76	1.54
Y-Y	3200 × 0.1	6 × 10	25.13	4	0.41	0.6
D-D	2000 × 0.1	5 × 8	15.71	6	1.05	1.33

Although the RMS current expression can be defined from the waveforms and current equations given in the previous section for each operating mode, the flux density expression also depends on the RMS voltage and K_v values, which in turn depend on the operating mode. The expression for ΔB_L is given by (39), and the expression for K_v is given by (40), where τ is the interval from the point where the flux density is zero to the point where it is at its maximum value. The expression for V_{Lrms} can be extracted from the previous section for each operational mode. The expressions for $<v_L(t)>$ are given by (41) and (42) for the 1p and 3p layouts, respectively.

$$\Delta B_L = \frac{V_{Lrms}}{K_v f_s A_c N} 10^4 \tag{39}$$

$$\begin{cases} K_v = \dfrac{\frac{V_{Lrms}}{\langle v_L \rangle}}{\tau f_s} \\ \langle v_L \rangle = \frac{1}{\tau} \int_0^{\tau} v_L(t) dt \end{cases} \tag{40}$$

$$\begin{cases} \langle v_{L_{Trg}} \rangle = \frac{1}{D_3 T_h} \int_0^{D_3 T_h} V_1 dt \\ \langle v_{L_{EPS}} \rangle = \frac{1}{D_3 T_h - t_1'} \left(\int_{t_1'}^{t_1} (V_1 + n V_2) dt + \int_{t_1}^{D_3 T_h} V_1 dt \right) \\ i_L\left(t_1'\right) = 0 \end{cases} \tag{41}$$

$$\begin{cases} \langle v_{L\_Y-Y_{Trg/Trap}} \rangle = \frac{1}{D_3 T_s} \int_0^{D_3 T_s} \frac{2}{3} V_1 dt \\ \langle v_{L\_D-D_{Trg/Trap}} \rangle = \frac{1}{D_3 T_s} \int_0^{D_3 T_s} V_1 dt \end{cases} \tag{42}$$

4.3. Power Switch Loss Model

Power switch losses are divided into two main categories: conduction and switching/commutation losses. In our case study, the power switches in all three layouts had the same peak current, estimated at 500 A. The voltage constraints on the primary and secondary bridges were 400 V and 800 V, respectively. Consequently, the SiC MOSFET half-bridge module Wolfspeed CAB530M12BM3 was selected to satisfy both current and voltage constraints. Table 7 summarizes these specifications.

Table 7. Power switch characteristics.

Rated Voltage (V)	Rated Continuous Current (A)	t_{on} (ns)	t_{off} (ns)	R_{DSon} (mΩ)
1200	530	98.11	93.71	3.96

The conduction losses in a MOSFET are defined as the product of its resistance while conducting, defined as R_{DS_on}, and the square of the RMS current passing through it, as shown in (43). It should be noted that all upper (up) and lower (lo) switches in all topologies, either on the primary (pr) or secondary (s) bridges, have the same RMS current value. The switch RMS currents for 1p-Trg and EPS are given by (44) and (45), respectively, whereas they are given by (46) and (47) for Y-Y 3p-TrgPS and 3p-TrapPS, respectively. The D-D configuration switches the RMS current expression in the Y-Y case, where only the inductor current is replaced by the line current, which is already defined in Section 2. Once the RMS current of the switches is calculated, the total conduction loss can be deduced by summing the conduction losses of each switch.

$$P_{cond} = R_{DS\_on} I_{sw\_rms}^2 \tag{43}$$

$$\begin{cases} I_{pr\_up} = I_{pr\_lo} = \sqrt{\frac{1}{T_s} \int_0^{D_1 T_h} (i_L(t))^2 dt} \\ I_{sec\_up} = \sqrt{\frac{1}{T_s} \int_{D_3 T_h}^{D_1 T_h} (i_L(t))^2 dt} \\ I_{sec\_lo} = \sqrt{\frac{1}{T_s} \left(\int_0^{D_1 T_h} (i_L(t))^2 dt + \int_0^{D_3 T_h} (i_L(t))^2 dt \right)} \end{cases} \tag{44}$$

$$\begin{cases} I_{pr\_up} = I_{pr\_lo} = \sqrt{\frac{1}{T_s} \int_0^{T_h} (i_L(t))^2 dt} \\ I_{sec\_up} = \sqrt{\frac{1}{T_s} \left(\int_0^{t_1} (i_L(t))^2 dt + \int_{D_3 T_h}^{T_h} (i_L(t))^2 dt \right)} \\ I_{sec\_lo} = \sqrt{\frac{1}{T_s} \left(\int_0^{T_h} (i_L(t))^2 dt + \int_{t_1}^{D_3 T_h} (i_L(t))^2 dt \right)} \end{cases} \tag{45}$$

$$\begin{cases} I_{pr\_up} = I_{pr\_lo} = \sqrt{\frac{1}{T_s} \int_0^{D_1 T_s} (i_L(t))^2 dt} \\ I_{sec\_up} = \sqrt{\frac{1}{T_s} \int_{D_3 T_s}^{D_1 T_s} (i_L(t))^2 dt} \\ I_{sec\_lo} = \sqrt{\frac{1}{T_s} \left(\int_0^{D_1 T_s} (i_L(t))^2 dt + \int_0^{D_3 T_s} (i_L(t))^2 dt \right)} \end{cases} \tag{46}$$

$$\begin{cases} I_{pr\_up} = \sqrt{\frac{1}{T_s} \int_0^{D_1 T_s} (i_L(t))^2 dt} \\ I_{pr\_lo} = \sqrt{\frac{1}{T_s} \left(\int_0^{\frac{T_s}{3}} (i_L(t))^2 dt + \int_{D_1 T_s}^{\frac{T_s}{3}} (i_L(t))^2 dt \right)} \\ I_{sec\_up} = \sqrt{\frac{1}{T_s} \int_{D_3 T_s}^{\frac{T_s}{3}} (i_L(t))^2 dt} \\ I_{sec\_lo} = \sqrt{\frac{1}{T_s} \left(\int_0^{\frac{T_s}{3}} (i_L(t))^2 dt + \int_0^{D_3 T_s} (i_L(t))^2 dt \right)} \end{cases} \tag{47}$$

The general switching loss expression for MOSFETs is given in (48), where V_{DS} is the drain-to-source voltage, and I_D is the drain current. All switches operating under 1p-TrgPS benefit from soft switching, except for the lower secondary bridge switches that suffer from hard switching when turned off. However, all switches suffer from commutation losses when turned off while operating under EPS. The switching losses for the 1p architecture are expressed in (49) and (50) for the TrgPS and EPS, respectively. For the 3p architecture, both the Y-Y and D-D configurations have the same soft-switching characteristics. When operating under 3p-TrgPS, the secondary upper and lower switches suffer from hard switching when turned on and off, respectively. On the other hand, when operating under 3p-TrapPS, the primary upper and secondary lower switches are soft-switched only when turned on, and the primary lower switches along with the secondary upper switches only when turned off. The expressions for the switching losses for 3p-Trg and 3p-TrapPS for the Y-Y configuration are given by (51) and (52), respectively. The switching losses of the D-D configuration are similar to those of the Y-Y configuration; only the inductor current is replaced by the line current. The total switching loss can be calculated once the commutation loss of each switch has been calculated. The total loss of the switches can also be calculated. It should be noted that the Y-Y and D-D configurations have equal conduction and switching losses because the D-D configuration inductance is three times the inductance of the Y-Y configuration; thus, the Y-Y phase current is the same as the D-D line current.

$$P_{com} = \frac{1}{T_s}\int_{0}^{t_{on},t_{off}} V_{DS} I_D dt \tag{48}$$

$$P_{com\_sec\_lo} = 2\left(\frac{1}{2}V_2 i_L(D_3 T_h) t_{off}\right) f_s \tag{49}$$

$$\begin{cases} P_{com\_pr} = 4\left(\frac{1}{2}V_1 i_L(T_h) t_{off}\right) f_s \\ P_{com\_sec\_up} = 2\left(\frac{1}{2}V_2 i_L(t_1) t_{off}\right) f_s \\ P_{com\_sec\_lo} = 2\left(\frac{1}{2}V_2 i_L(D_3 T_h) t_{off}\right) f_s \end{cases} \tag{50}$$

$$\begin{cases} P_{com\_sec\_up} = 3\left(\frac{1}{2}V_2 i_L(D_3 T_s) t_{on}\right) f_s \\ P_{com\_sec\_lo} = 3\left(\frac{1}{2}V_2 i_L(D_3 T_s) t_{off}\right) f_s \end{cases} \tag{51}$$

$$\begin{cases} P_{com\_pr\_up} = 3\left(\frac{1}{2}V_1 i_L(D_1 T_s) t_{off}\right) f_s \\ P_{com\_pr\_lo} = 3\left(\frac{1}{2}V_1 i_L(D_1 T_s) t_{on}\right) f_s \\ P_{com\_sec\_up} = 3\left(\frac{1}{2}V_2 i_L(D_3 T_s) t_{on}\right) f_s \\ P_{com\_sec\_lo} = 3\left(\frac{1}{2}V_2 i_L(D_3 T_s) t_{off}\right) f_s \end{cases} \tag{52}$$

5. Results

5.1. Dynamics Visualization

In this subsection, the converter dynamics in the start-up and load variation processes with an inductor DC offset are observed. The simulation was conducted using the MATLAB/Simulink Simscape software 2023a. The control approach uses model predictive control (MPC) for load current feed-forward control (LCFFC), which is discussed in detail in Ref. [55]. This approach provides more accurate voltage regulation along with instantaneous current tracking, particularly when the load varies widely, thereby offering more stability to the converter. The control diagram is shown in Figure 11, where i_0 is the converter output current.

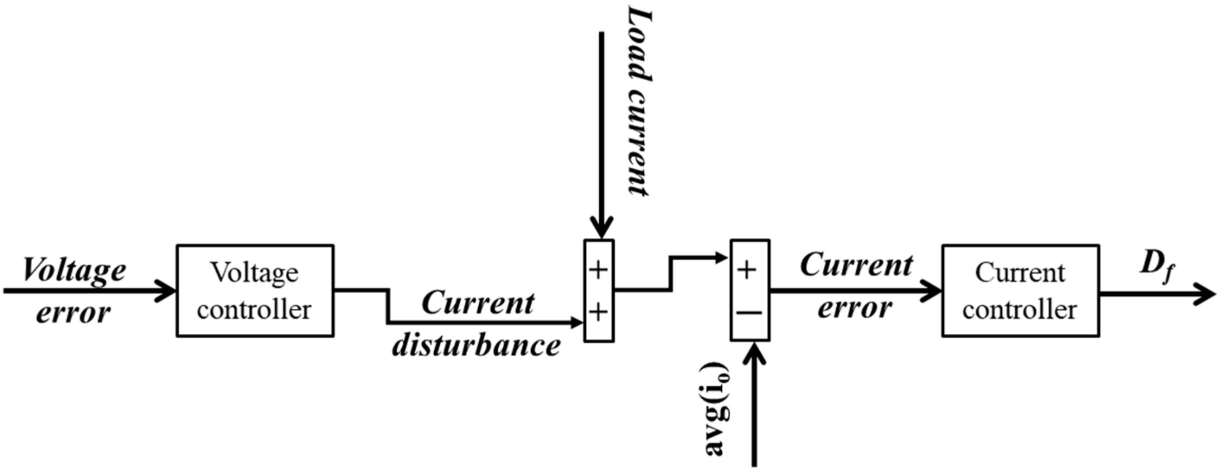
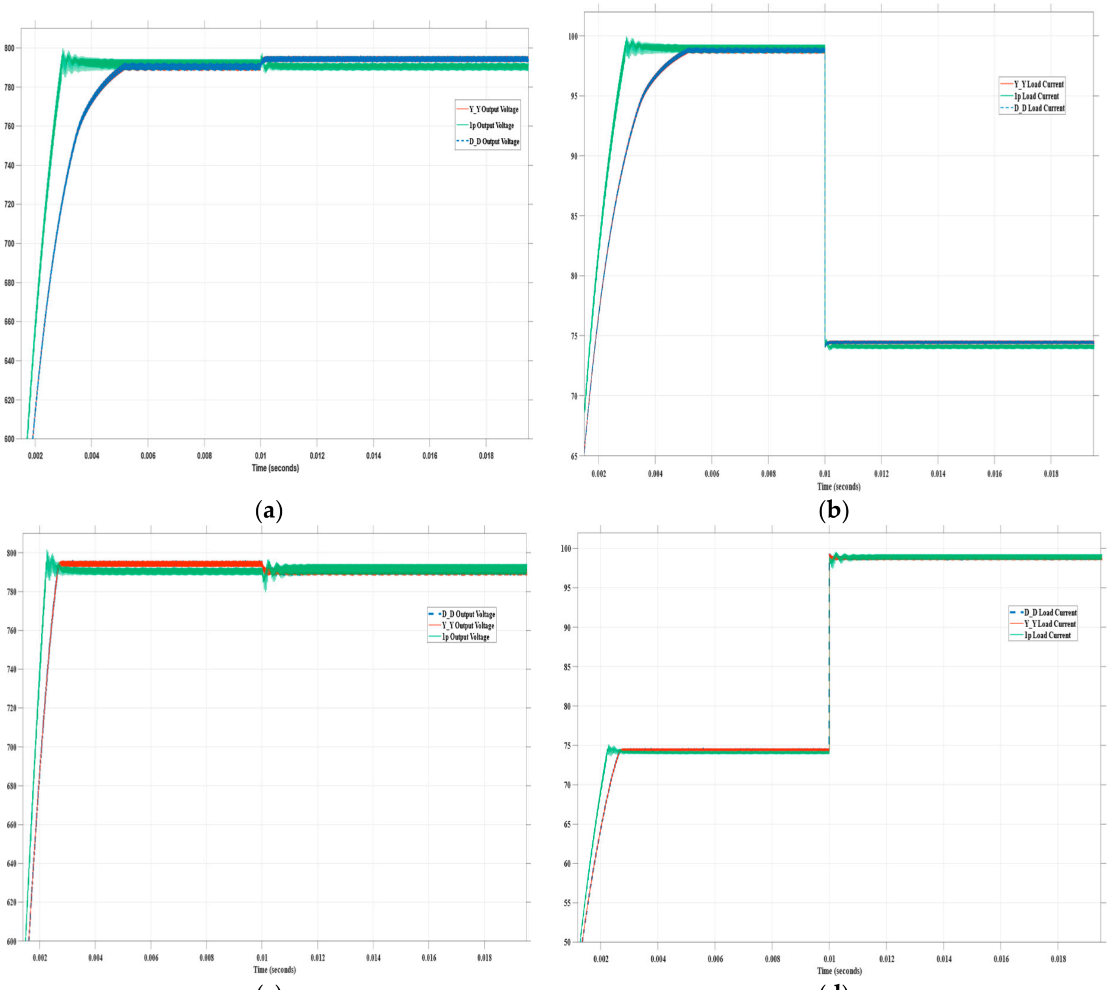


Figure 11. Voltage and average current control using LCFFC global diagram.

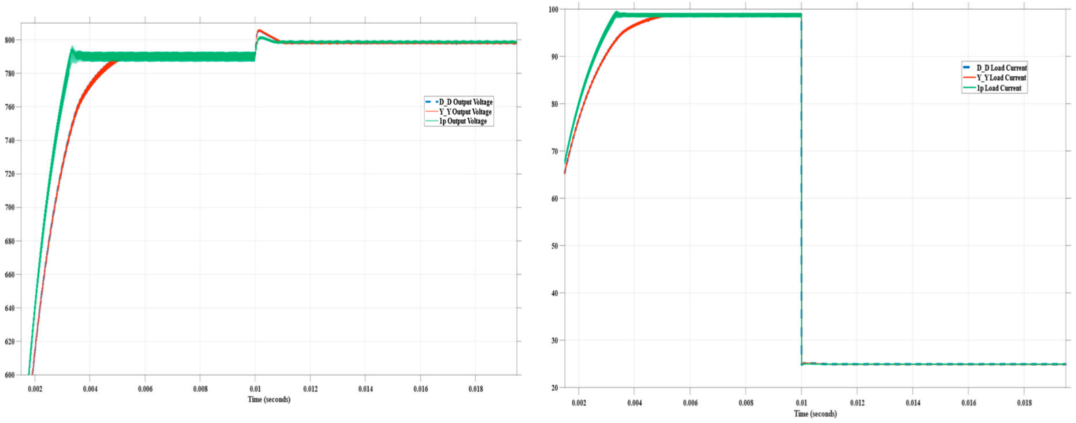
On the other hand, Figure 12 depicts the output voltage and load current response for a load variation from 80 kW to 60 kW and vice versa, and Figure 13 shows the same variables but for a load variation from 80 kW and 20 kW. The 1p and 3p architectures exhibited almost the same responses when the load was varied. However, 3p architectures suffer from a slightly higher rising time under heavy loads. The same is true for the 1p layout under light loads.



(**a**) (**b**)

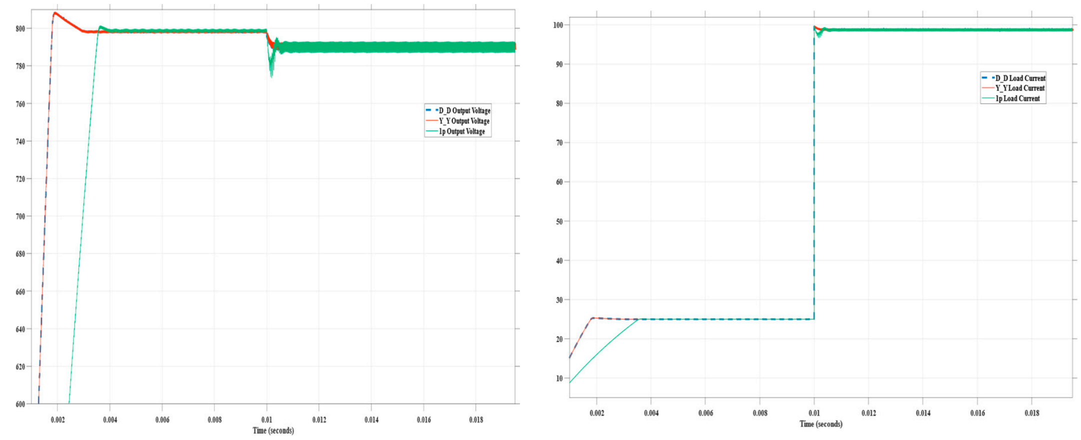
(**c**) (**d**)

Figure 12. Output voltage and load current for 80 kW and 60 kW load: (**a**) output voltage with load variation from 80 kW to 60 kW at 0.01 s; (**b**) load current with load variation from 80 kW to 60 kW at 0.01 s; (**c**) output voltage with load variation from 60 kW to 80 kW at 0.01 s; (**d**) load current with load variation from 60 kW to 80 kW at 0.01 s.



(**a**) (**b**)

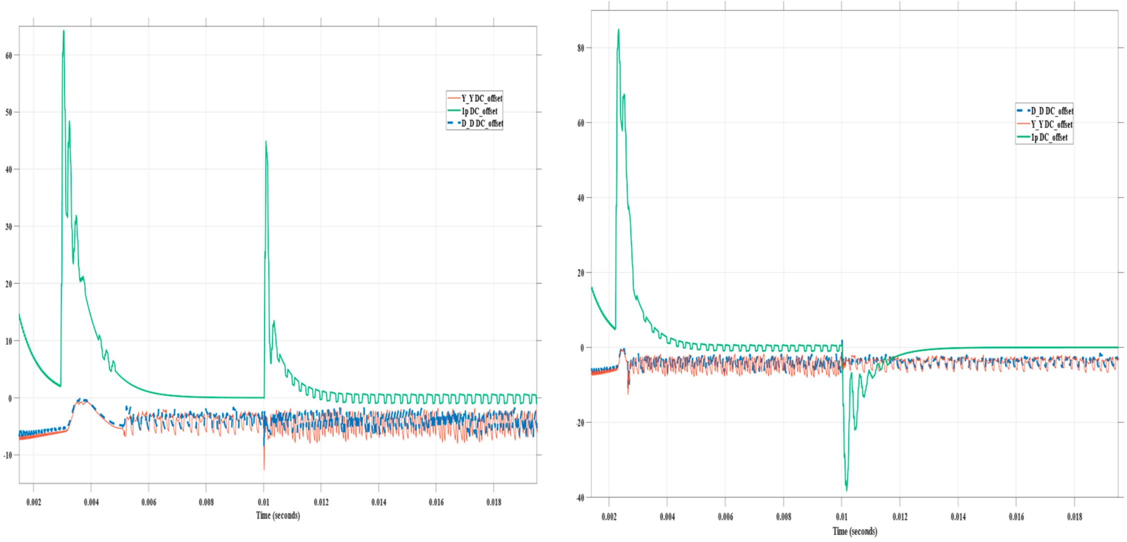
Figure 13. *Cont.*



(**c**) (**d**)

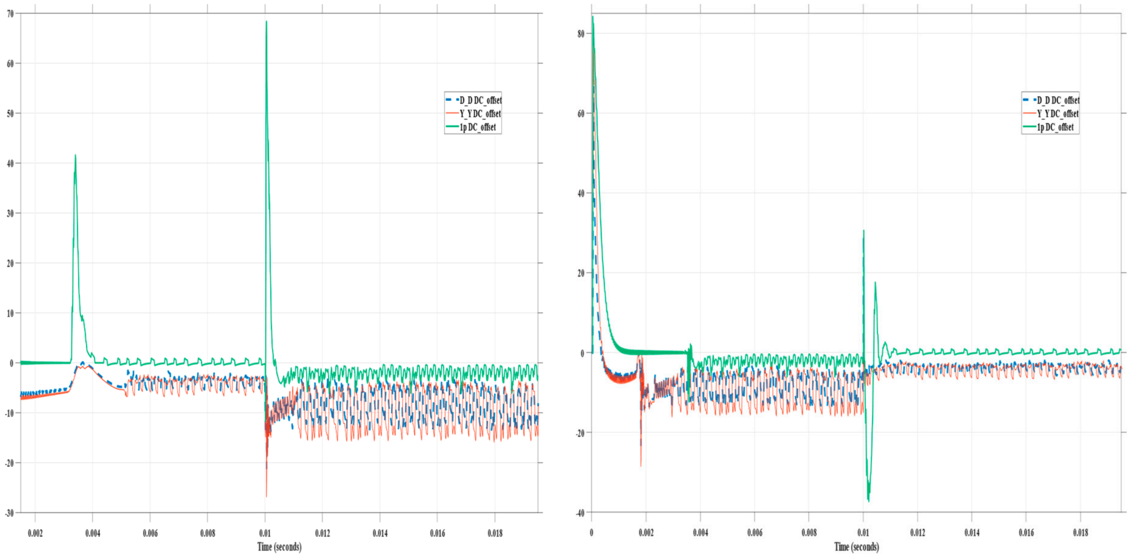
Figure 13. Output voltage and load current for 80 kW and 20 kW load: (**a**) output voltage with load variation from 80 kW to 20 kW at 0.01 s; (**b**) load current with load variation from 80 kW to 20 kW at 0.01 s; (**c**) output voltage with load variation from 62 kW to 80 kW at 0.01 s; (**d**) load current with load variation from 20 kW to 80 kW at 0.01 s.

Another crucial parameter to be considered is the DC offset of the inductor. This is illustrated in Figure 14 under the same conditions as those in Figures 11 and 12. For common ground in comparison, the DC offset is represented as a percentage relative to the inductor RMS current in each case. It is evident that for both the 1p and 3p architectures, the DC offset in the inductor is high during the start-up process. However, in the case of the 1p layout, it took more time to settle, particularly at high loads. In addition, the DC offset for the 1p architecture increases in transient modes when the system response settles and the load is varied, which is not the case for 3p layouts. However, when the system response is settled, the 1p layout exhibits a much lower inductor DC offset, regardless of heavy or light loads. In the same context, the DC offset of the inductor in the 3p layouts is higher at light loads and lower at heavy loads, and it is higher in the case of the Y-Y configuration compared to the D-D configuration.



(**a**) (**b**)

Figure 14. *Cont.*



(**c**) (**d**)

Figure 14. Inductor DC offset: (**a**) load variation from 80 kW to 20 kW at 0.01 s; (**b**) load variation from 80 kW to 20 kW at 0.01 s; (**c**) load variation from 62 kW to 80 kW at 0.01 s; (**d**) load variation from 20 kW to 80 kW at 0.01 s.

5.2. Loss Visualization

In this subsection, different graphs are provided to illustrate the converter losses using both mathematical and simulation models. The per-unit (Pu) system is used on the x-axis to normalize the power level, ranging from 0 to 1, whereas the y-axis represents the percentage of total losses relative to the input power. The simulated results were obtained using both MATLAB/Simulink 2023a and the PSIM 2024.1 thermal module using magnetic materials, windings, cores, and power switch properties.

5.2.1. Transformer Loss Visualization

The total transformer losses are illustrated in Figure 15 for the three DAB DC-DC converter variants. The derived mathematical and simulation models exhibited the same pattern of results. All three layouts exhibited high losses at extremely low power levels. This is expected because transformers are less efficient when operating at very low loads because fixed losses (such as core losses) are dominant. At mid-range loads, i.e., $0.2 < Pu < 0.8$, the 3p layouts show similar performance, with losses decreasing significantly as the load increases. Both layouts had losses below 2% throughout this range, indicating a high efficiency. The 1p layout showed higher losses than the 3p layout. Although the losses decreased as the load increased, they remained slightly higher than those of the 3p layout, indicating a lower efficiency. At high loads, when Pu converges to unity, the 3p layouts continue to show low losses, remaining below 2% even at full load, while the 1p layout exhibited an increase in losses as the load approached the maximum, rising above the 3p layout losses, making it less efficient at high loads.

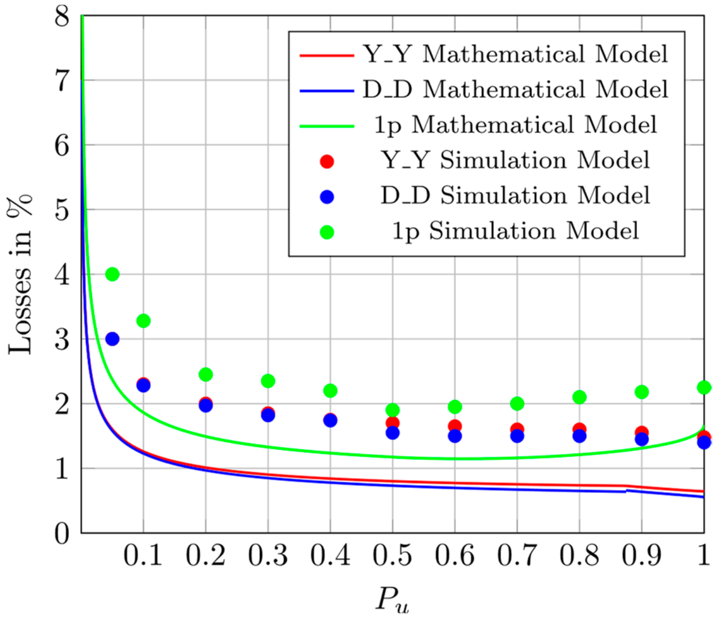


Figure 15. DAB DC-DC converter total transformer loss.

5.2.2. Inductor Loss Visualization

The total inductor losses are illustrated in Figure 16 for the three DAB DC-DC converter variants. The derived mathematical and simulation models exhibited the same pattern of results. All three layouts show high losses at very low power levels; however, the 1p layout initially shows a sharp decrease in inductor losses compared with the other two layouts, making it more efficient in very light-load operation. At mid-range loads, the D-D layout showed slightly lower losses than the Y-Y layout because of its lower phase current. However, it is still less efficient than the 1p layout because the D-D layout losses are caused by three distinct inductors, whereas the 1p layout has only one inductor. At high loads, where *Pu* was close to 1, the 3p layouts continued to exhibit stable performance, whereas the 1p layout exhibited a noticeable increase in losses as the load approached the maximum. This indicates that the 1p inductor experiences higher losses under heavy loads.

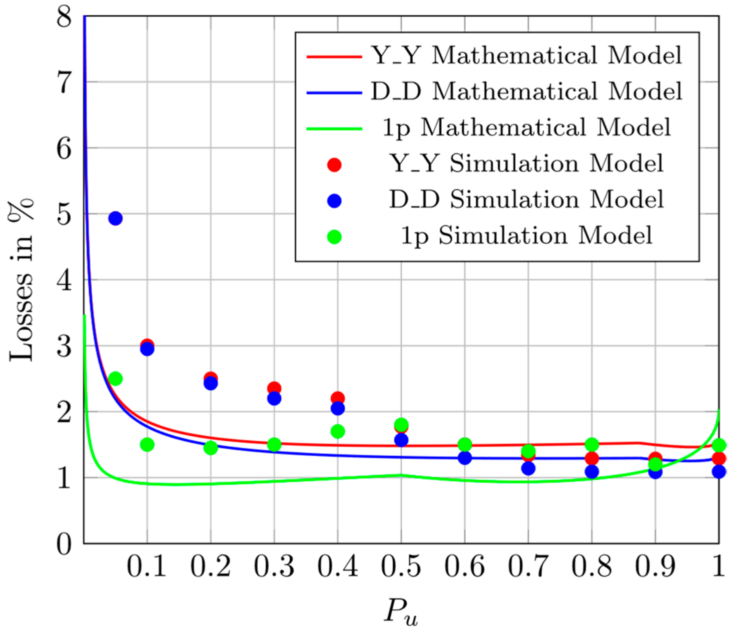


Figure 16. DAB DC-DC converter total inductor loss.

5.2.3. Power Switches Loss Visualization

The total power switch losses are illustrated in Figure 17 for the three DAB DC-DC converter variants. The derived mathematical and simulation models exhibited the same pattern of results. All three layouts show high losses at very low power levels; however, the 1p layout has much lower initial losses than the 3p layout. At mid-range loads, the losses for all the layouts decreased significantly as the load increased. The 3p layouts have a loss range between 7% and 4%, whereas the 1p layout shows a more substantial reduction in losses in the mid-range, maintaining losses below 3% and showing superior performance compared to the 3p layouts in this power range. At heavy loads, where Pu is close to unity, the losses for the 3p layouts stabilized and slightly increased from 4% to above 5%, whereas the 1p layout showed an increase in losses as the load approached the maximum. However, it still maintained a lower loss compared to the 3p layout in this power range, limited between 2% and 4%. The 3p layouts had identical performance regarding power switch losses because the D-D configuration inductance value was three times the Y-Y configuration inductance; thus, the phase current in the Y-Y case was equal to the line current in the D-D configuration.

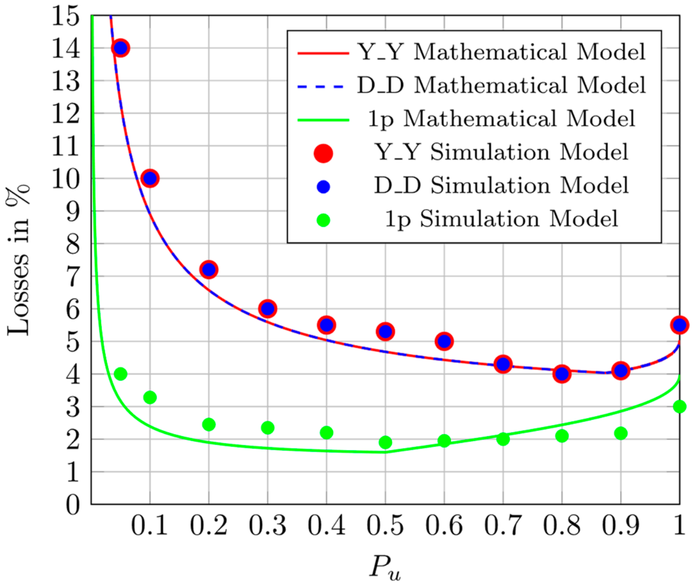


Figure 17. DAB DC-DC converter total power switch loss.

6. Discussion

The global efficiency of the power converter is illustrated in Figure 18 for the three DAB DC-DC converter variants. The derived mathematical and simulation models exhibited the same pattern of results. All three layouts showed lower efficiency at very low power levels; however, the 1p layout showed a higher efficiency of approximately 90% compared to the 3p layout with an efficiency of approximately 76–85%. At mid-range loads, the efficiency of all the layouts increased as the load increased. The 1p layout maintained higher efficiency throughout this power range, peaking at approximately 95%. The three layouts showed similar efficiency profiles, both increasing steadily and reaching approximately 90% peak efficiency. At heavier loads, the efficiency of the 1p layout started to decline slightly but remained at approximately 95%. The 3p layouts maintained a stable efficiency of approximately 95%, showing a slightly better performance compared to the 1p layout, as it started to decline at extremely heavy loads close to the maximum input power.

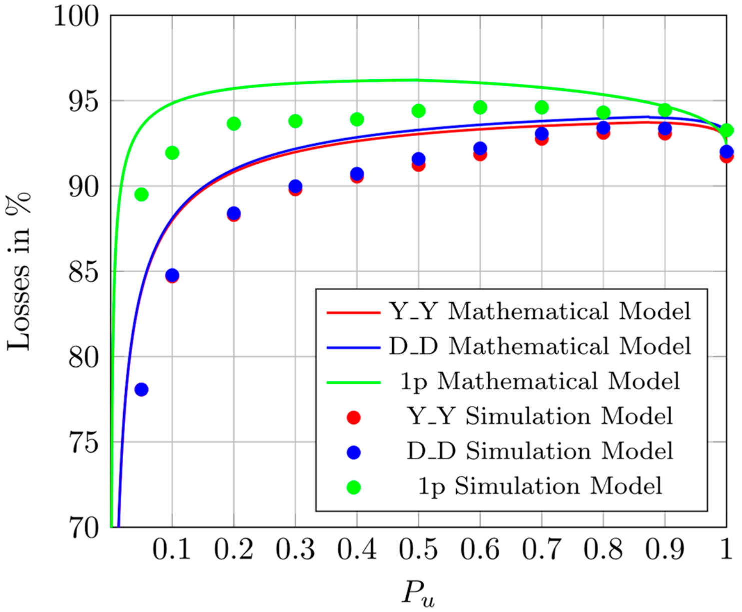


Figure 18. DAB DC-DC converter efficiency.

In summary, the 3p layouts have similar transformer and inductor loss profiles, with a slight advantage in favor of the D-D configuration. This is due to the reduced phase current in comparison with the Y-Y configuration. However, both configurations have identical power switch losses owing to the equality between their line currents. Although the 3p layouts have lower transformer losses and slightly higher inductor losses than the 1p architecture, the power switch losses represent the main difference in efficiency between them. The 3p layouts used 12 power switches compared to the 1p layout, which used only 8 power switches. It is true that the 3p DAB DC-DC architecture reduces the RMS current value per switch and provides soft-switching capability. However, the increased number of power switches causes the total energy dissipated in them to be greater than that dissipated in the 1p topology power switches. This affects the overall converter efficiency and makes the 1p topology much more efficient than the 3p architecture, especially when operating under light-load conditions, as depicted in Figure 18. In addition to the efficiency impact on the converter, the higher number of inductors and power switches makes the 3p layouts less reliable and increases their chance of failure compared with the 1p topology. Another drawback of the 3p layout is the complex design of the 3p one-core transformer. The 1p architecture uses a simple 1p transformer, which is easy to design. This represents a much more mature technology than that of the one-core 3p transformer. The 1p DAB layout suffers from a high inductor DC offset at start-up and transient loads, but it offers the advantage of a much lower offset at steady-state operation compared to 3p layouts. However, this requires further investigation. Regarding the dynamic response, both the 1p and 3p architectures showed almost the same performance when operating under the selected controller architecture used in this study. The same applies for the power density, where the heavy 1p transformer core weight is compensated by the additional power switches in the 3p architectures, making all three layouts have almost the same power density in this case study. Table 8 presents all the compared aspects in this section for better visualization.

It is true that the literature favors the 3p DAB DC-DC converter over its 1p architecture. However, it should be noted that all comparisons in the literature were based on the conventional SPS modulation technique. However, in our case study, when using optimal hybrid modulation techniques, the design complexity, low efficiency, and reduced reliability caused by the higher number of components and steady-state inductor DC offset are not favorable for 3p DAB DC-DC converter architectures. This makes the 1p DAB DC-DC converter a more favorable topology for the field of BEV powertrain applications.

Table 8. Comparison of the properties of DAB different layouts.

Rated Voltage (V)	1p DAB	Y-Y DAB	D-D DAB
Number of power switches	8	12	12
Transformer core	Simple and mature	More complex	More complex
Number of inductors	Single inductor	Three, one-phase	Three, one-phase
Total number of elements	Low	High	High
Dynamic response	Slower at heavy loads start-up	Slower at light loads start-up	Slower at light loads start-up
DC offset	Highest at transient and start-up	Highest at steady state	Slightly lower than Y-Y
Power density	Same	Same	Same
Efficiency	High especially at light loads	Lower but similar at heavy loads	Like Y-Y

7. Conclusions

This paper presents a comparative analysis of three DAB DC-DC converter variants dedicated to the DC-DC power conversion stage of a BEV powertrain. Different modulation techniques for operating converter variants were reviewed. Optimal modulation techniques were selected according to the literature. A DAB DC-DC converter mathematical loss model was derived for each of the three presented variants based on the modulation techniques selected, and a simulation model was built as well. The architecture variants were then compared based on their efficiency, element count, inductor DC offset, dynamic response, manufacturing complexity, and power density. As a result, the 1p DAB DC-DC converter topology provided higher efficiency and lower component count, which increased the converter reliability, lowered the design complexity, and lowered the inductor DC offset (still to be improved). These combined features allow the 1p DAB DC-DC converter to outperform the 3p architecture when used for the DC-DC conversion stage in a BEV powertrain, making it more suitable for this specific field of application.

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