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Evaluation of an Infinite-Level Inverter Operation Powered by a DC–DC Converter in Open and Closed Loop

Nataly Gabriela Valencia Pavón [1,*], Alexander Aguila Téllez [2], Javier Rojas Urbano [1,*], Víctor Taramuel Obando [2] and Edwin Guanga [1]

[1] Faculty of Computer Science and Electronics, Escuela Superior Politécnica de Chimborazo (ESPOCH), Riobamba 060155, Ecuador; edwin.guanga@espoch.edu.ec
[2] Electrical Engineering Career, Universidad Politécnica Salesiana, Quito 170525, Ecuador; aaguila@ups.edu.ec (A.A.T.); vtaramuel@est.ups.edu.ec (V.T.O.)
* Correspondence: nataly.valencia@espoch.edu.ec (N.G.V.P.); javier.rojas@espoch.edu.ec (J.R.U.)

Abstract: This paper evaluates the open- and closed-loop DC–DC converter operation within a DC coupling multilevel inverter architecture to obtain an infinite-level stepped sinusoidal voltage. Adding a cascade controller to the DC–DC converter should reduce the settling time and increase the number of levels in the output voltage waveform; it could decrease the speed error and phase shift concerning the sinusoidal reference signal. The proposed methodology consists of implementing an experimental multilevel inverter with DC coupling through a single-phase bridge inverter energized from a BUCK converter. Trigger signals for the two converters are obtained from a control circuit based in an ATMEGA644P microcontroller to explore its capabilities in power electronics applications. A digital controller is also implemented to evaluate the operation of the BUCK converter in open and closed loop and observe its influence in the stepped sinusoidal output voltage. The evaluation is performed to energize a resistive load with common output voltage in multilevel inverters, i.e., 3, 5, 7, 11, and infinity levels. Results show that during the design stage, fast dynamic elements, like the storage capacitor, can be used to obtain a minimum THD because the settling time is sufficiently fast, the speed error remains small, and there is no need for a controller. A digital controller requires processing time, and although in theory it can reduce the settling time to a minimum, the processor introduces latency in the control signals generation, producing the opposite effect. Controller complexity of the digital controller must be considered because it increases processing time and influences the efficiency of the closed-loop operation.

Keywords: multilevel inverter; infinite-level inverter; BUCK converter; open loop; closed loop

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1. Introduction

At present, electrical energy from renewable energy sources is one of the main research topics, especially the use of solar energy captured by photovoltaic panels. To integrate this system into the electrical power system, it is necessary to use an inverter and power converters that allow obtaining an AC voltage from a DC voltage; the simplest and most commonly used topology is known as the PWM inverter. It produces a square or quasi-square voltage waveform where the fundamental sinusoidal component predominates, acceptable in low and medium power applications, and the single-pulse PWM has high harmonic content with a THD of 48.43%. Modulation strategies improve the THD in PWM inverter output such as sinusoidal pulse width modulation (SPWM), which reduces the harmonic content using the right filters or switching frequency, and allows voltage amplitude control; however, it increases switching losses, limiting the switching frequency [1–3]. THD is an important factor in high-power applications, and harmonics can generate undesired operation effects, electromagnetic interference, and cause low efficiency. In Figure 1, the output waveform and frequency spectrum of a PWM and SPWM inverter are shown; the difference in the harmonic content can be appreciated.

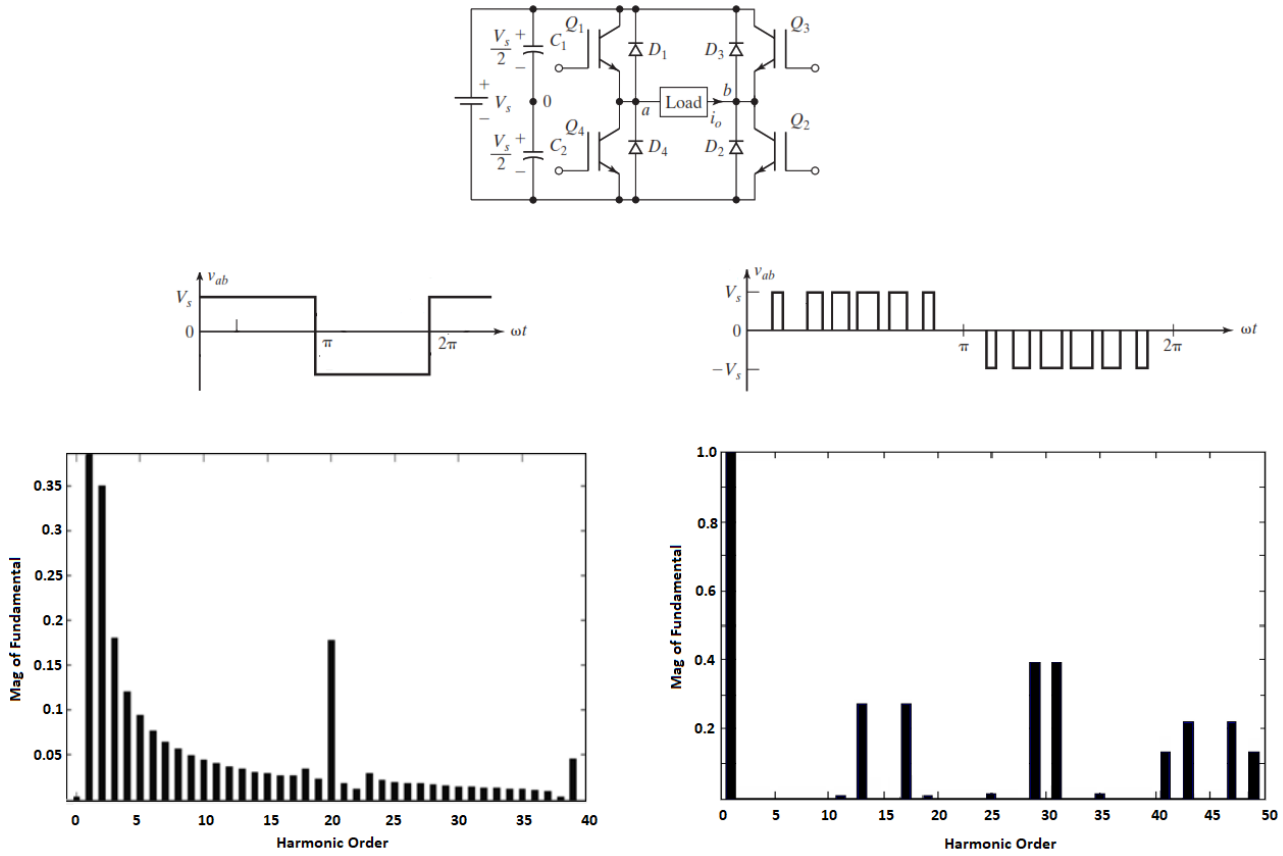

Figure 1. Inverter topology, output waveform, and harmonic spectrum. Left, PWM inverter. Right, SPWM inverter.

Multilevel inverter topologies can deal with these drawbacks. They have a topology in which a stepped voltage waveform is obtained and a low harmonic content can be reached because the waveform is more similar to sinusoidal. The THD can be controlled with the quantity of levels. It can be said that the more levels there are, the less THD there is. In this topology, modulation strategies help to improve the THD; however, this increases the complexity of the control in the power switches as well as the switching losses [1,2].

The stepped voltage waveform is obtained with an energy bank implemented with a series of connected capacitors to provide nodes where controlled switches are connected. Each capacitor has a voltage according to Equation (1), where m represents the number of levels or accessible nodes from the energy bank [2,3].

$$E_m = \frac{V_{dc}}{m-1} \tag{1}$$

A conceptual topology is shown in Figure 2. The stepped voltage waveform is generated from each energy bank node $(V_1, V_2, V_3, V_4, V_5)$ to a reference node v_0, if $v_0 = V_1$, and the positive half period output waveform is generated when switching from V_1 to V_5 and returning to V_1 with appropriate control signals. The negative half period is generated in the opposite way when $v_0 = V_5$, and switching starts in V_5 [4]. In Figure 2, the output voltage waveform is shown.

The harmonic distortion can be reduced with a high number of voltage level in the waveform. Figure 3 shows the harmonic spectrum in a nine-level inverter. Compared to the harmonic spectrum in Figure 1, a considerable reduction in the number of harmonics and its amplitude can be noted, without the need to use a modulation technique. This would allow a more noticeable THD reduction in addition to voltage control [2,3].

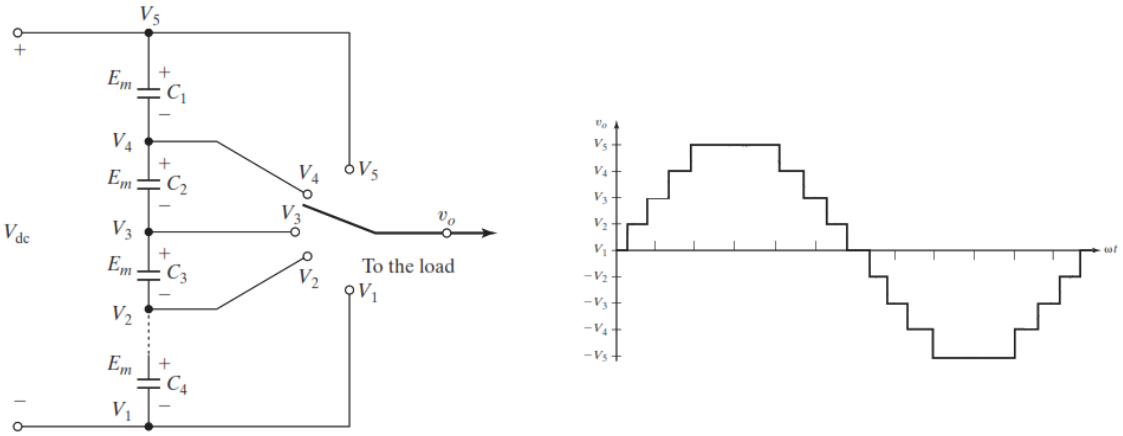

Figure 2. Multilevel inverter conceptual topology and output waveform.

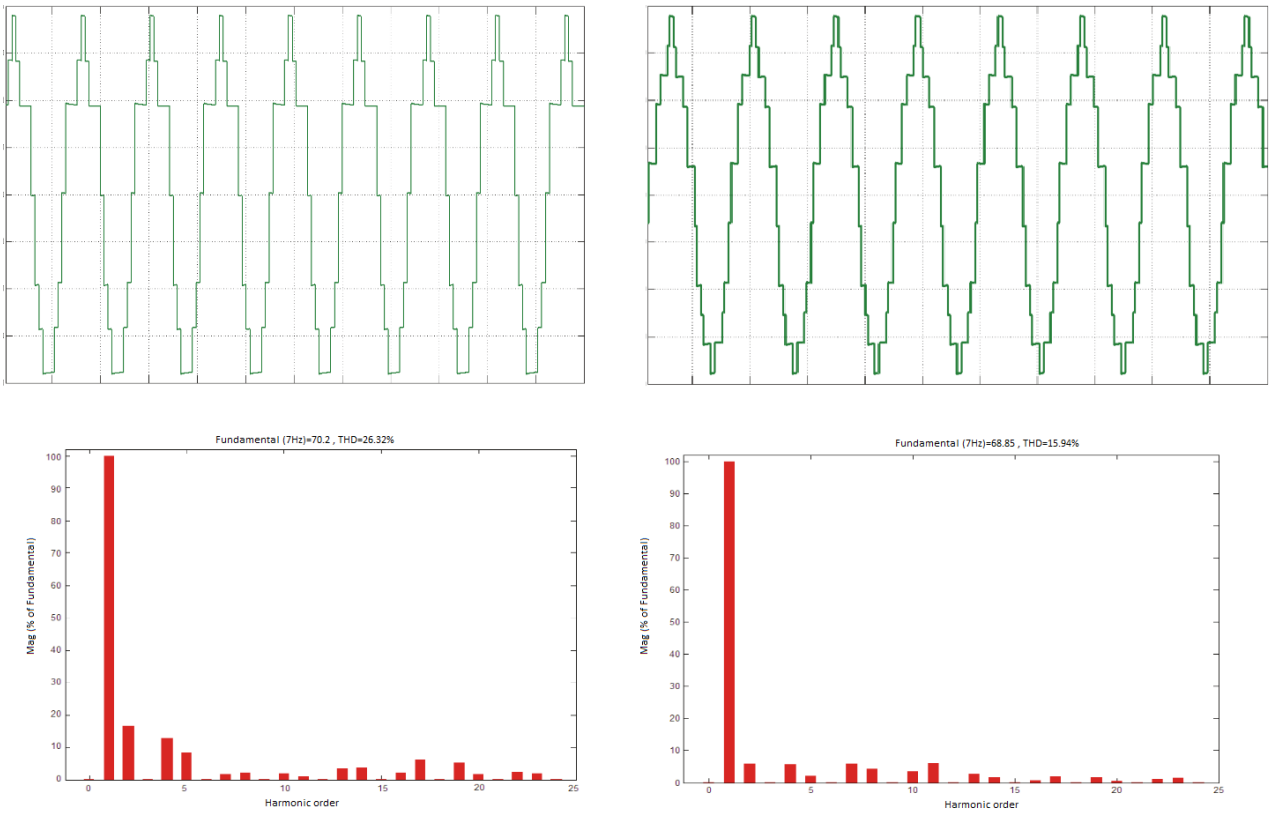

Figure 3. Harmonic spectrum in 5- and 9-level inverter [3].

Multilevel inverter topologies seek to use low breakdown voltage power switches in high-voltage applications; commonly used topologies are clamping diode, floating capacitor, and cascaded inverters. The first two topologies require a large number of power switches, in addition to other electronic components, whose numbers will increase depending on the number of levels in their output. Additionally, they introduce static and dynamic unbalances in the blocking voltages of each device, so external damping networks must be added to equalize the blocking voltages [1,3]. Single-phase cascaded inverters present a similar disadvantage in terms of the number of components; however, they present an easier implement design, but the control of each inverter must be adjusted each time, which changes the number of output voltage levels. In general terms, a multilevel AC waveform increases the amount of switching losses in power converters, so it is common to implement inverters with 15 levels as a maximum. Shown in Table 1 is the electric

components number; it can be noted that the higher the number of levels, the more complex the circuit becomes in terms of the number of devices as well as the control [5,6].

Table 1. Electric components number in m-multilevel inverter topologies [6].

Topology	Number of Switches	Number of Diodes	Number of Capacitors
Clamping diode	$2(m-1)$	$2(m-2)$	$m-1$
Floating capacitor	$(2m-2)$	0	$0.5(m-2)(m-1)$
Cascaded inverters	$(2m-1)$	0	$0.5(m-1)$

In [7], a clamping diode configuration is used, where THD values of 28.58% are obtained using a 5-level inverter. Tests are performed where the THD decreases to a value of 2.53% when using a 15-level inverter implemented with 28 switches per phase. Ref. [8] implemented a basic unit of a switched capacitor topology utilizing a cascaded H-bridge to generate 13- and 31-level output voltages with a lower number of components, and a THD 0f 2.63% was achieved. Ref. [9] showed a cascaded module configuration where the number of switches was $(n+1)$ for (n) levels at the output, and the THD obtained for an 11-level configuration (12 static switches in the bridge) was 8.61%. Ref. [10] showed a design of a full-SiC, three-level, three-phase UPS with efficiency of 97.57%. The UPS can reach a THD of 2% with the introduction of an LCL filter as an alternative to increasing the number of levels. These works evidence the use of a large number of semiconductor elements or the introduction of filters; moreover, in three-phase systems, the number of semiconductors triples and requires the use of complex controllers running extensive algorithms.

In [11,12], a topology called inifinite-level inverter (ILI) was proposed, where a DC–DC converter was cascaded with a single-phase full-bridge inverter. This topology was mentioned in [13] as a variable inverter with DC link; a stepped wave can be obtained by controlling the output voltage of the DC–DC converter while the inverter switches its switches in conduction at 180°. A topology scheme is shown in Figure 4. Through this type of operation, an infinite-level inverter can be obtained, where several levels can be reached with fewer electronic devices, reducing losses, costs, size, and complexity, and increasing efficiency.

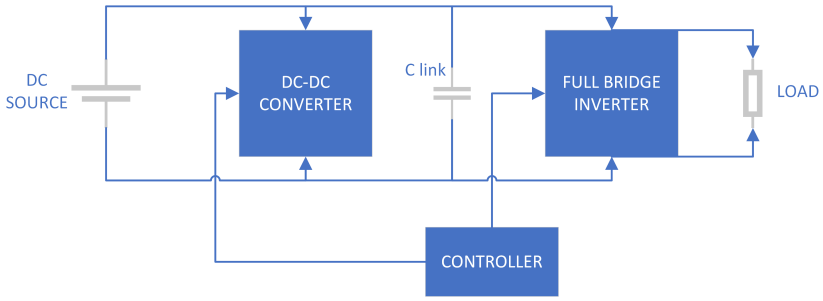

Figure 4. Infinite-level inverter schematic.

In [14,15], a BUCK-type step-down DC–DC converter with variable duty ratio in steps according to a sampled sine wave was used as a DC link, generating at the inverter output a step wave with a THD of 2.36% at a switching frequency of 10 KHz. Similar results were obtained in [16], with a THD of 1.2% and 98% efficiency in an evaluation with resistive load. In [17,18], a BUCK–BOOST converter was used to make more efficient use of the DC voltage at the input of the converter. In these works, there is no voltage feedback so the levels depend exclusively on the reference signal generated, and can be affected by disturbances, introducing distortion in the output voltage waveform. In the case of [18], a THD that varies from 2% to 8.20% depending on the load associated with the circuit at a switching frequency of 10 KHz was obtained. Ref. [19] presented a novel topology to develop a three-phase infinite-level inverter; it uses fewer semiconductors than traditional

inverter topologies and, in combination with a third-harmonic injection PWM technique, it can achieve a THD of 0.39%.

ILI has been investigated in applications such as motor management, voltage restoration, and reactive compensation; in all these works, the inverter works in open loop and the transient response to disturbances is not evaluated [16,20,21]. For infinite-level operation, the DC–DC converter output voltage must follow a sinusoidal signal reference, with it being necessary to consider the dynamics of the DC–DC converter, which has been little or not explored. If there is a speed error, there will be a phase shift in the inverter voltage signal, which would complicate control signals synchronization, especially if it works integrated into a power electrical system (PES). Also, a poor transient response could result in a poor response to disturbances or primary control strategies within a PES [21–24].

Power converters in a closed loop could improve the dynamic response in time and over impulse through a controller [25]. There are some works that include a cascade controller in DC–DC converters such as [22,26,27]; they implement PID, GPI, and H∞ controllers on high-end processors such as DSP and FPGA. The GPI controller presents a lower settling time compared to PID, of 4.64 ms vs. 13.64 ms, respectively. In addition, the GPI control shows a shorter output recovery time against sudden RL load switching and shows a higher noise decrease in the response. The H∞ controller has adaptive characteristics as it changes the $\mathcal{E}$ parameter based on the degree of error present in the output; this controller obtains a settling time of 8.62 ms.

Modern control strategies have been explored in DC–DC converters. Ref. [28] implemented a particle swarm optimization (PSO) algorithm to tune PID controller parameters and compared it with the conventional Ziegler–Nichols method. Investigation concluded that the latter strategy provided a better dynamic response; however, it was noted that this technique is effective as long as system parameters like input voltage and load do not change too much. Algorithms such as SMC (sliding mode control) implemented in [29] are a good nonlinear control strategy applied to power converters; it presents better performance compared to a dual-loop PI controller. Complex control algorithms require higher computational load, requiring complex control systems to improve system robustness but slowing down dynamic response.

In this article, a monophasic multilevel inverter with DC–DC link is implemented through a single-phase full-bridge inverter energized from a BUCK converter; it includes closed-loop operation in the BUCK converter, and the contribution given is the analysis of closed-loop operation to reduce the speed error and provide immunity to disturbances, compared with open-loop operation, in order to determine the suitability or not of this operation mode.

2. Materials and Methods

To evaluate the open- and closed-loop operation of the DC–DC converter in an infinite-level inverter topology, an experimental electronic circuit is implemented, according to Figure 5. To obtain results that can be contrasted with the work of [11,20], the circuit is able to deliver an output voltage of 30 V_{rms} for a resistive load of 30 Ω/120 W. Considering the load, a single-phase full-bridge inverter is implemented with a maximum input voltage of 30 V_{DC}; for the DC–DC converter, the BUCK topology is used with an input voltage of 30 V_{DC} from a DC source, and voltages between 0 V and 30 V can be obtained according to the duty cycle control. Switching frequency is selected considering [30]. It should be between 10 KHz and 0 KHz; however, taking as reference the work of [18] that compares several works related to multilevel waves using BUCK and BOOST topologies, switching frequency is established in 40 KHz.

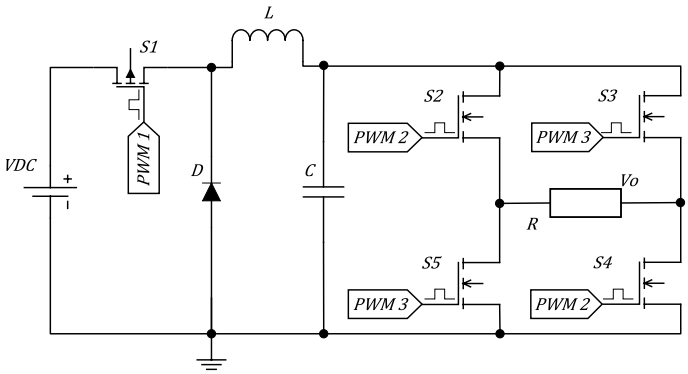

Figure 5. BUCK converter topology.

2.1. BUCK Converter Stage

According to Figure 5, the BUCK converter design has two stages, firstly, capacitor (C) and inductor (L) are selected to define an output voltage ripple and inductor current ripple; secondly, power switches ($S1$, D) are dimensioned to tolerate blocking voltages and conduction currents. Design conditions are shown in Table 2.

Table 2. BUCK converter design conditions.

Parameter	Symbol	Value
Input voltage	V_{in}	30 V
Duty ratio	δ	0.95
Output voltage ripple	ΔV_o	10 mV
Inductor current ripple	Δi_L	5%
Switching frequency	f_{PWM}	10 KHz

L and C are calculated with Equations (2) and (3) [31]. A toroidal inductor of 0.584 mH and an output capacitor of 2200 µF and 63 V are selected. Equations (3)–(6) are used for dimension power diode and MOSFET, where the breakdown voltage values (V_{BR}, V_{CE}) are determined according to the maximum blocking voltage when the circuit breaker does not conduct, while the forward current (I_F) and collector current (I_C) are determined with the output current (I_o) when there is conduction. In [31], a Hiperfast BYC15-600 diode from NXP Semiconductors (Eindhoven, The Netherlands), was used in D, which, due to its high switching speed, reduces associated MOSFET switching losses. $S1$ is a MOSFET from VISHAY Siliconix (San Jose, CA, USA), whose high speed and low switching losses make it ideal for switched mode power supply applications.

$$L_{min} = \frac{(1-\delta)R}{2f} \tag{2}$$

$$C = \frac{1-\delta}{8L\left(\frac{\Delta V_o}{V_o}\right)f^2} \tag{3}$$

$$V_{BR} = V_{in} \tag{4}$$

$$I_F = I_o\sqrt{1-\delta} \tag{5}$$

$$V_{CE} = V_{in} \tag{6}$$

$$I_C = I_o\sqrt{\delta} \tag{7}$$

2.2. Single-Phase Full-Bridge Inverter Stage

A single-phase full-bridge inverter design consists of power switch dimensioning to tolerate blocking voltages and conduction currents with Equations (8) and (10). Power switches $S1$, $S2$, $S3$, and $S4$ are IGBT's model K75H603 from Infineon Technologies AG (Neubiberg, Germany), which is a high-speed switch model ideal for power converter applications.

$$V_{CE} = V_{in} \tag{8}$$

$$I_C = \frac{I_o}{\sqrt{2}} \tag{9}$$

For a proper IGBT triggering, it is necessary to use a coupling circuit for the controller signals. HCPL 3120 from Agilent Technologies (Santa Clara, CA, USA), is a high-speed optocoupler that serves to isolate the control stage from the power stage, and its output is adequate for IGBT trigger. HCPL 3120 is used, as indicated in Figure 6.

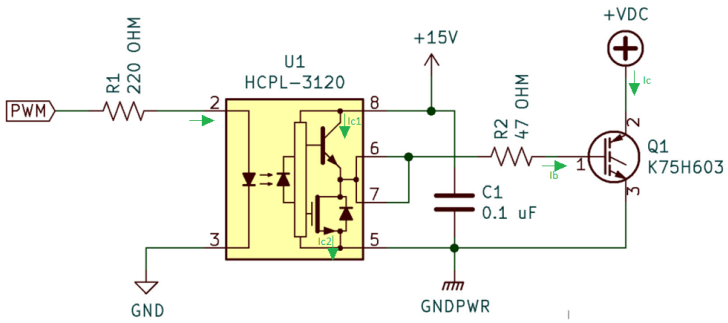

Figure 6. IGBT isolated gate driver.

2.3. Controller

The controller is the logic circuit that generates PWM signals to trigger power switches in the DC–DC converter and inverter in open- and closed-loop operation. The control program is implemented in an ATMEGA644 microcontroller from Microchip Technology Inc. (Chandler, AZ, USA), and an ADC0804 digital analog converter from Wolg Electronics (Kastl, Germany), with a voltage divider is used for feedback for the BUCK output voltage. Figure 7 shows used elements and their connections. Although there are embedded systems with better characteristics for power electronics, the ATMEGA644 microcontroller is used to explore its behavior in digital compensator implementation for power electronics as part of the research of this paper.

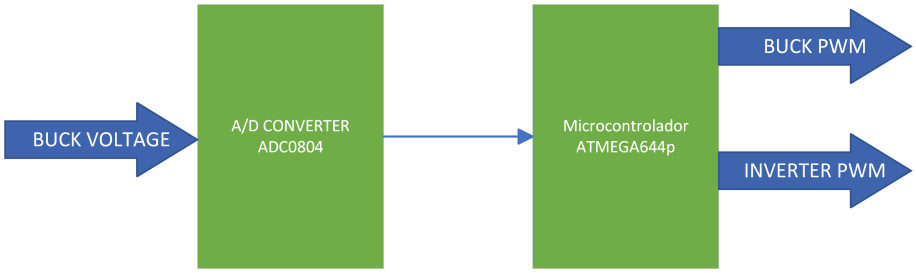

Figure 7. Controller schematic.

The developed program allows us to choose the number of levels for the inverter output voltage waveform, then the value of the BUCK PWM duty ratio and its duration is calculated using the number of levels and output frequency. For the full-bridge inverter, a PWM with constant duty ratio for 180° operation is generated. In closed-loop operation, PID parameters are from memory, the BUCK output voltage error is calculated, and it executes the compensator routine to control the BUCK duty ratio. A program flowchart can be seen in Figure 8.

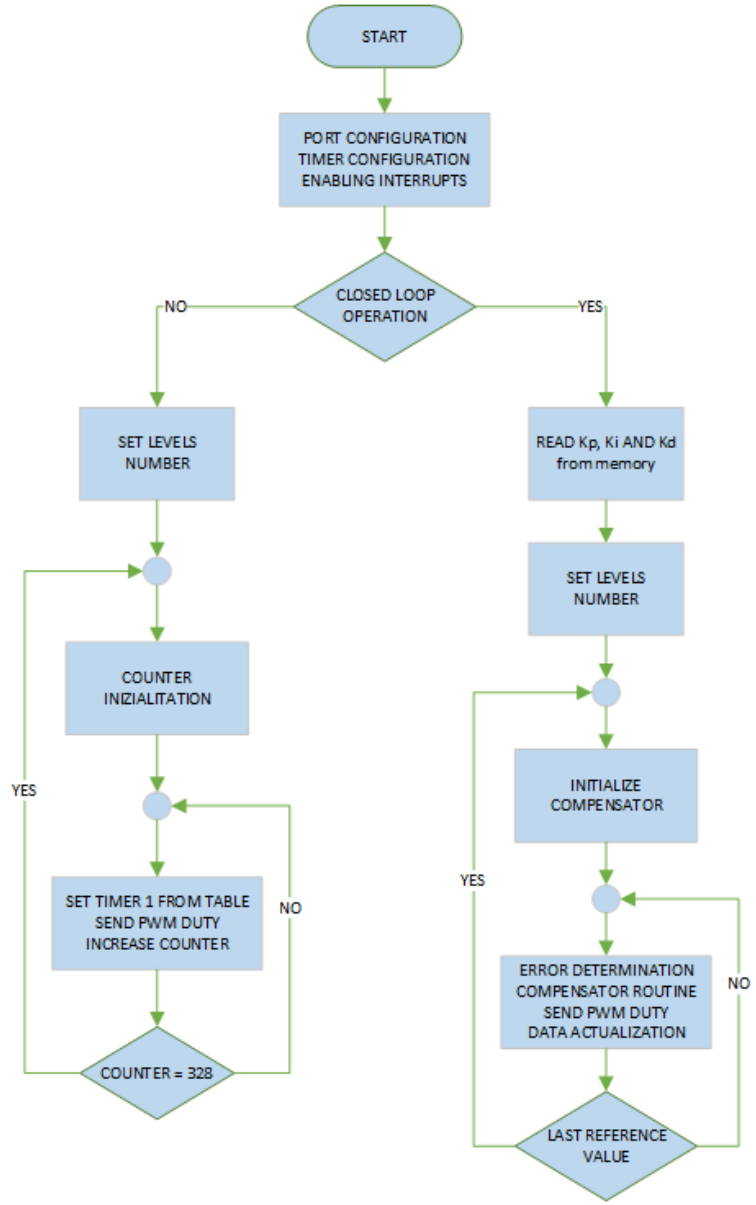

Figure 8. ATMEGA644 program flow chart.

2.4. Digital Compensator

To improve the DC–DC converter dynamics, a PID compensator is used, taking into account that the position error will be canceled and there will be fast response to disturbances as the change of reference by a sinusoidal relationship. Figure 9 shows a compensator schematic and Equations (10) and (11) mathematically describe the compensator in the time domain, where E is the voltage error; U is the BUCK converter pulse width value; KP, KI, and KD represent proportional, integral, and derivative constants that determine the compensator behavior [31].

$$PID(s) = \frac{U(s)}{E(s)} = KP + \frac{KI}{s} + KDs \tag{10}$$

$$E(s) = Vo(s) - Vin(s) \tag{11}$$

To implement the compensator digitally and to establish a controller programming routine, (10) is discretized using bilinear transform with the s to z relationship by Equa-

tion (12). The digital PID difference equation is given by Equation (13), and compensator constants are determined by Equations (14)–(16).

$$s = \frac{2(1 - z^{-1})}{Ts(1 + z^{-1})} \tag{12}$$

$$U(n) = Kp * e(n) + \frac{Ki}{2Fs}[e(n) + e(n-1)] + U_i(n-1) + 2FsKd[e(n) - e(n-1)] + U_d(n-1) \tag{13}$$

$$KP = Kp \tag{14}$$

$$KI = \frac{Ki}{2Fs} \tag{15}$$

$$KD = 2FsKd \tag{16}$$

Compensator constants are obtained experimentally by classical tuning using Ziegler–Nichols. Constants were adjusted to obtain the best transient response; the fastest response with the lowest overshoot is obtained with KP = 0.390, KI = 0.001, and KD = 0.

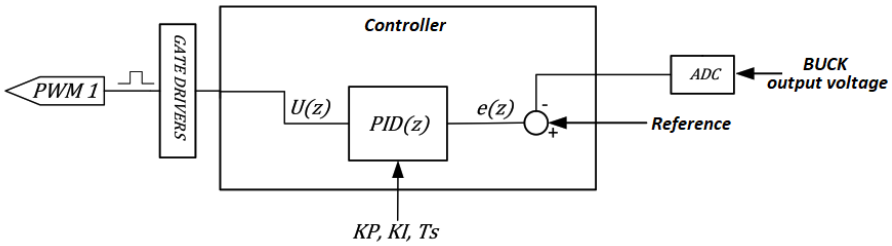

Figure 9. Controller scheme.

3. Results

To obtain data for open- and closed-loop evaluation of the BUCK converter within the infinite-level inverter, the circuit described in this section is implemented, the output voltage is analyzed and recorded using an oscilloscope, with numerical storage capability, and then the data are analyzed with the FFT powergui tool of the simscape library of MATLAB R2023b. Figure 10 shows the implemented hardware.

First, open-loop operation is evaluated to form a sine wave of infinite levels. For this duty ratio, PWM_1 varies with $sin(wt)$ for a complete period. A square waveform is obtained because the BUCK converter presents slow dynamics, with a settling time (t_{ss}) of 0.513 s. According to [18], the t_{ss} depends on capacitance value, so the value of C is modified. The results are synthesized in Figure 11, where it can be appreciated that with 2.2 µF a sine wave is obtained and t_{ss} = 4.99 ms. A BUCK converter for an infinite-level inverter must be designed with a low capacitance, and, so that this does not affect ΔV_o ripple, it must be designed with a small value of Δi_L.

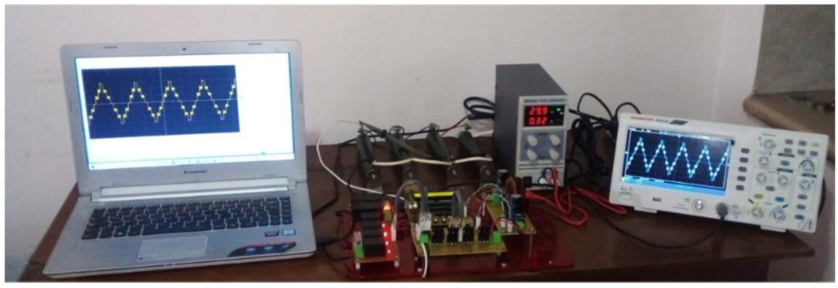

Figure 10. Experimental hardware.

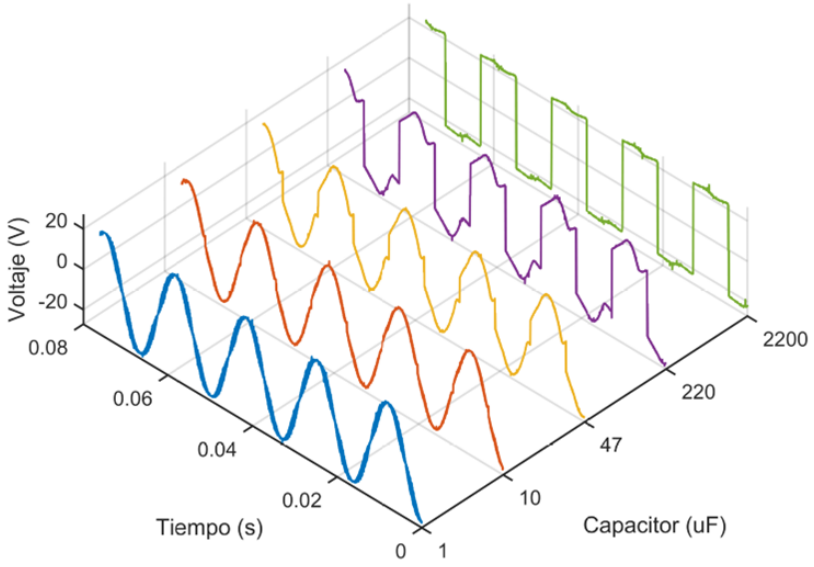

Figure 11. Capacitance effect on voltage output waveform.

The operation is evaluated with 2.2 µF for *C* to form a stepped waveform of three, five, seven, and nine levels. The obtained results can be seen in Figure 12, where it is possible to appreciate the ripple presence in the levels of the stepped wave. this is due to the low value of capacitance.

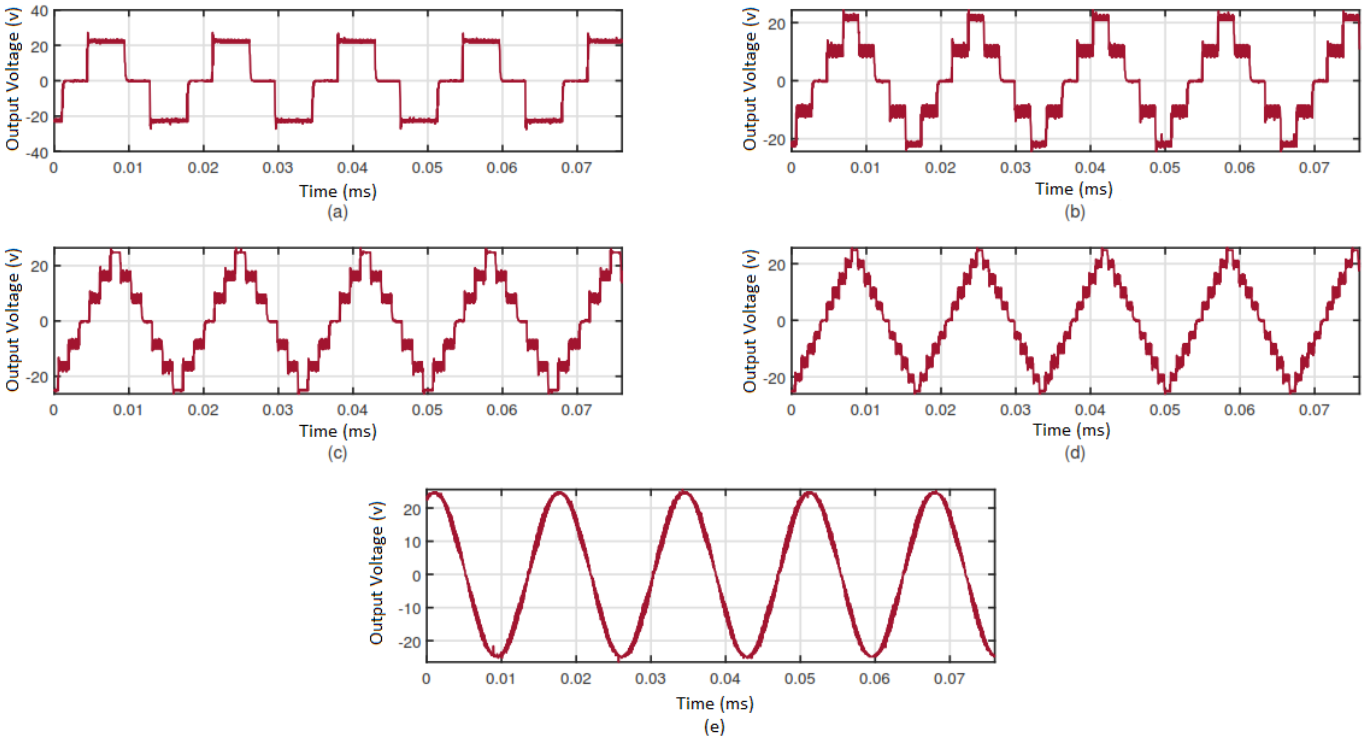

Figure 12. Inverter output voltage waveform for (**a**) 3 levels, (**b**) 5 levels, (**c**) 7 levels, (**d**) 9 levels, (**e**) infinite levels.

Each wave is analyzed in MatLab to determine the distortion, obtaining the values shown in Table 3, where a decrease in the harmonic content with respect to the increase of levels can be appreciated, obtaining a distortion of 3.47% for infinite levels and increasing to 34.28% for three levels. In the case of infinite levels, a low harmonic content is 1.26% in the third harmonic and less than 1.26% for the rest. The THD percentage value obtained

for infinite levels is within the ranges allowed by IEEE standard 519 [32] for low-voltage applications.

Table 3. Characteristics and percentage of harmonic content of voltage signals.

	3 Levels	5 Levels	7 Levels	9 Levels	∞ Levels
THD (%)	34.28	28.63	20.93	15.70	3.47
Fund. (Vrms)	16.42	12.68	14.24	14.21	17.35
DC (V)	0.05	0.16	0.13	0.14	0.08
Fundamental (%)	100	100	100	100	100
h2 (%)	0.32	0.64	0.46	0.51	0.39
h3 (%)	12.32	14.04	11.78	11.30	1.26
h4 (%)	11.11	1.18	0.79	0.80	0.16
h5 (%)	24.08	10.72	6.19	4.28	0.16
h6 (%)	0.90	0.20	0.23	0.08	0.32
h7 (%)	5.46	12.91	3.88	2.31	0.59
h8 (%)	0.56	1.56	0.52	0.25	0.08
h9 (%)	10.18	10.78	4.62	1.24	0.36
h10 (%)	1.23	0.04	0.05	0.06	0.17
h11 (%)	8.23	2.84	8.77	1.02	0.26
h12 (%)	0.42	0.54	1.33	0.27	0.17
h13 (%)	2.36	4.31	6.27	0.72	0.24
h14 (%)	1.08	0.29	0.12	0.13	0.05
h15 (%)	6.66	4.81	1.80	1.58	0.26

Before evaluating the infinite-level inverter closed-loop operation, the isolated BUCK converter closed-loop is evaluated to observe the compensator influence. The test is performed for four reference values: 5.88 V, 11.76V, 17.64 V, and 23.52 V. A comparison between open-loop and closed-loop dynamics is performed with the test results, as can be seen in Figure 13.

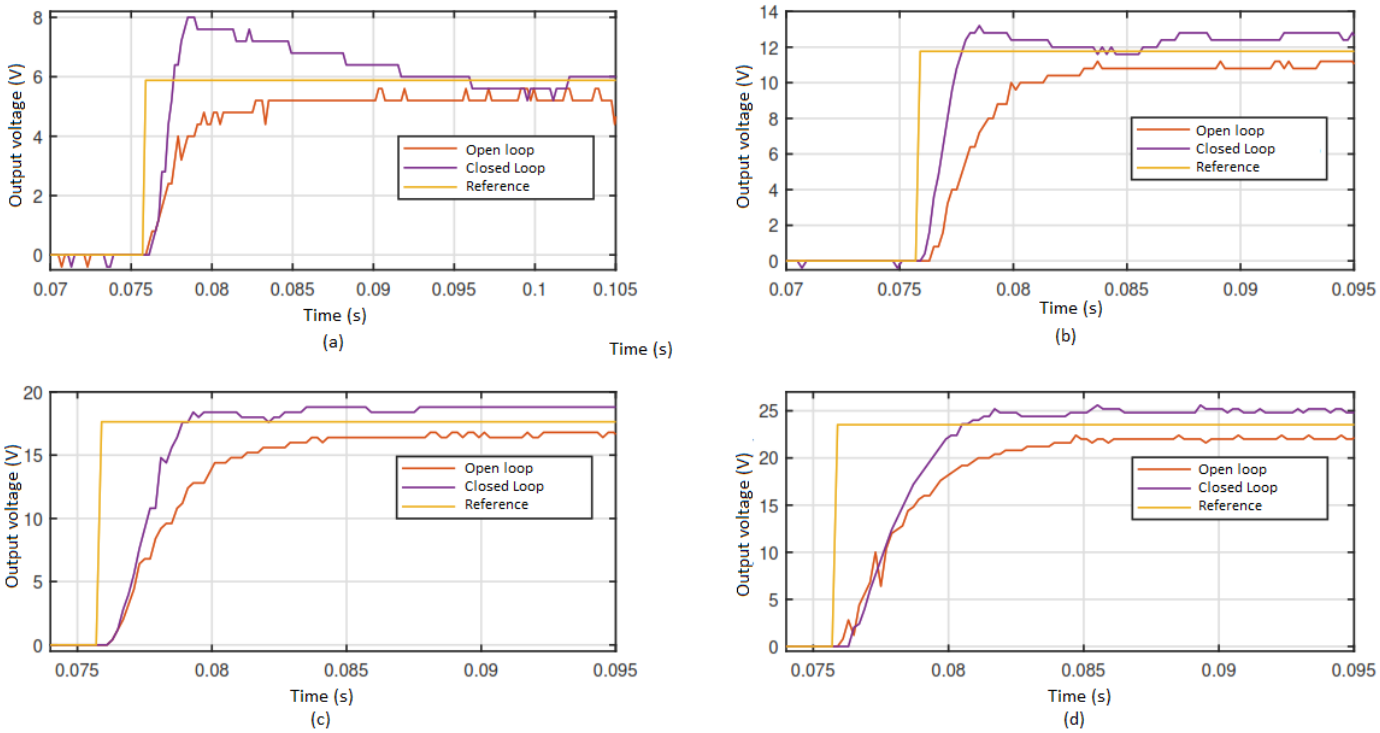

Figure 13. BUCK converter in closed- and open-loop operation for different voltage references: (**a**) 5.88 V, (**b**) 11.76 V, (**c**) 17.64 V, and (**d**) 23.52 V.

For each reference value, the maximum over impulse $MP(\%)$, settling time T_{es}, and rise time T_r are measured. To measure T_{ss}, 10% criterion is taken into account, while T_r is measured between 10% and 90% of the voltage final value. For the $MP(\%)$, the maximum value of the response is compared to the steady-state response value in underdamped response. The measured parameters for the four scenarios are shown in Table 4. There is an improvement in the T_r for closed-loop operation, as the settling time T_{is} is reduced with larger reference change. The designed compensator allows it to reduce steady-state error so that in the closed loop it is a maximum of 8.84%, while in open loop, the errors reach 18.36% for reference variations from 2.95 V to 30 V.

Table 4. BUCK converter in open- and closed-loop comparison.

	Closed Loop			Open Loop		
Voltage Reference (V)	Tr **(ms)**	T_{es} **(ms)**	Mp **(%)**	Tr **(ms)**	T_{es} **(ms)**	Mp **(%)**
5.880	1	28.9	36.05	3.2	9.21	–
11.76	1.2	19.1	12.24	4.4	9.01	–
17.64	2	9.61	–	5.2	8.41	–
23.52	3	6.41	–	4.8	9.61	–

Finally, the closed-loop operation of the infinite-level inverter is evaluated, and the evaluation conditions are the same as in the open-loop test in order to contrast the results. The results obtained can be seen in Figure 14, where a frequency of 60 Hz is achieved for the fundamental. When there is an increase of levels there is not a considerable improvement in THD, as can be seen in Table 5. The best result is presented for three levels with a THD of 33.51%, which increases to 58.04% for infinite levels. The infinite-level test measures a high presence of odd and even harmonics, so the resulting voltage waveforms have high THD and asymmetry values. As in open loop, the output voltage waves present peaks due to the low value of C and it can be said that due to the fast dynamics in open loop, the compensator does not help to improve the THD; the compensator introduces latency in the inverter operation.

Table 5. Harmonic content for infinite-level inverter in closed-loop operation.

	3 Levels	**5 Levels**	**7 Levels**	**∞ Levels**
THD (%)	33.51	34.54	32.77	58.04
Fund. (Vrms)	19.83	15.55	17.01	6.246
DC (V)	0.469	0.285	0.328	1.907
Fundamental (%)	100	100	100	100
h2 (%)	1.58	0.44	5.90	11.76
h3 (%)	6.89	14.08	7.72	4.73
h4 (%)	2.57	1.05	1.71	8.83
h5 (%)	17.85	15.70	0.75	4.27
h6 (%)	2.61	0.47	0.79	2.29
h7 (%)	4.83	12.67	1.57	2.21
h8 (%)	0.36	3.43	1.62	2.25
h9 (%)	2.54	12.21	1.31	4.23
h10 (%)	0.78	0.45	0.43	3.21
h11 (%)	0.38	3.51	1.85	1.73
h12 (%)	0.13	1.38	1.67	1.61
h13 (%)	0.11	1.72	1.38	1.54
h14 (%)	0.43	0.56	0.83	1.03
h15 (%)	1.36	0.36	0.29	0.16

Additionally, the compensator behavior with 2200 µF in the BUCK converter output was evaluated, and the results show that it is not possible to generate an output voltage with frequencies in the 50 Hz to 60 Hz range due to the converter slow dynamics. Changes in the reference at frequencies close to 60 Hz generate system instability due to the output

capacitor charging and discharging times. The frequencies generated under these test parameters allowed the generation of alternating voltage waves at the output frequency up to 0.1879 Hz and a THD of 14.24% in the best case. There are no voltage peaks, and the compensator improves the transient; these results can be seen in Figure 15.

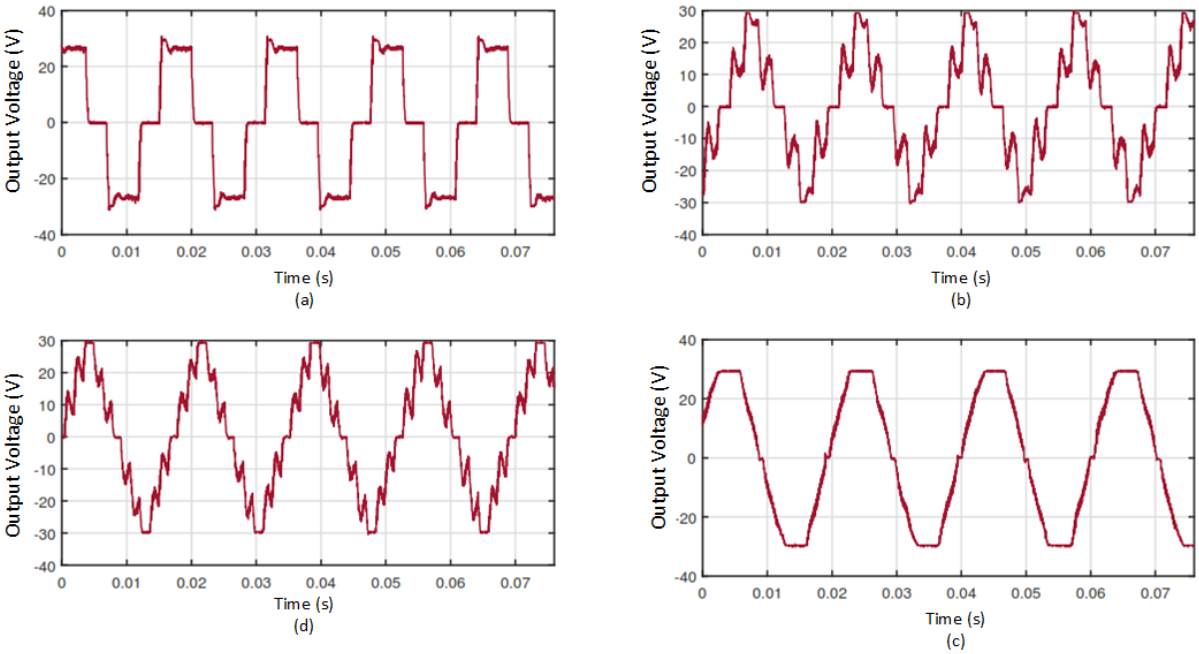

Figure 14. Results in an infinite-level inverter in closed-loop operation for (**a**) 3 levels, (**b**) 5 levels, (**c**) 7 levels, and (**d**) ∞ levels.

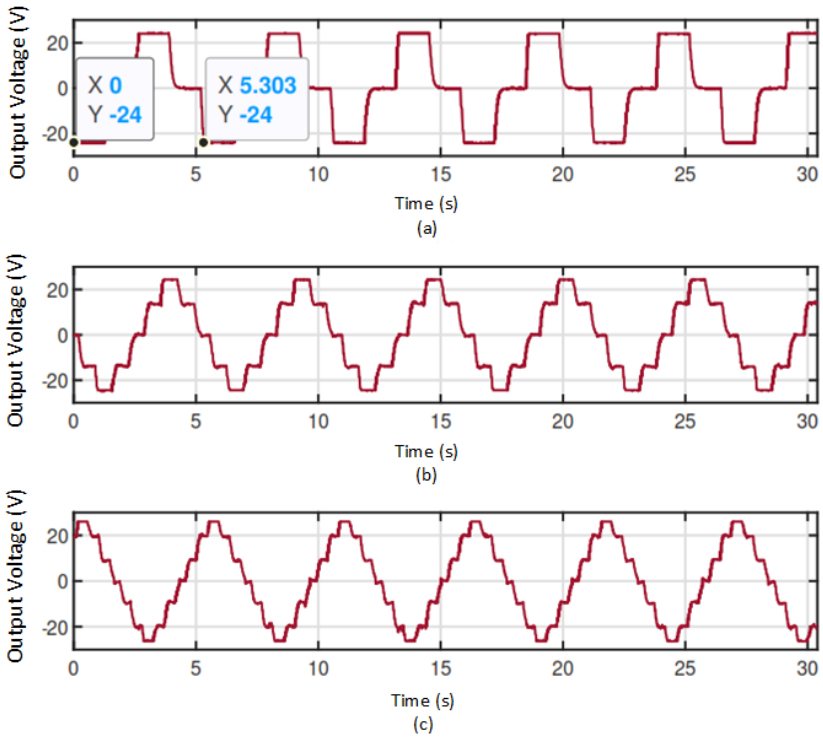

Figure 15. Results in an infinite-level inverter in closed-loop operation for (**a**) 3 levels, (**b**) 5 levels, and (**c**) 7 levels with 2200 µF.

4. Conclusions

The open-loop test results were better than the closed-loop tests results. An open-loop harmonic distortion of 3.47% was obtained, which is a distortion value accepted by IEEE std 519 in low-voltage applications. On the other hand, closed loop showed high levels of harmonic distortion as well as the presence of even harmonics, revealing low quality of the output voltage waveform generated. This shows that for an infinite-level inverter designed with a fast dynamic DC–DC converter, it is not convenient to close the loop with the DC output voltage, and future research should evaluate the behavior by closing the loop with the rms voltage at the inverter output.

The use of the controller allows a decrease in the rise times in the converter response; however, the converter output continues presenting a slow transient response, which does not satisfy the dynamics requirement for an inverter of infinite levels, so it is not possible to generate output AC voltages with frequencies between 50 and 60 Hz that are applicable to common loads. The converter presents instability when working with slow dynamics (high output capacitance) to rapid changes in the reference.

In similar works, PI controllers are used in the control loop due to simplicity, and there are problems that could cause the use of more complex controllers in their execution time. The implemented digital PI controller, in spite of improving the dynamics in open loop, did not present good results for this type of application. The compensator was experimentally tuned and adjusted to obtain the best performance, so the results show that the microcontroller ATmega644P does not have the best characteristics for this application. Modern digital compensators require high processing times, which requires that they be developed on multicore embedded or FPGA-based systems to avoid introducing speed error due to latency in this application where there is fast dynamics. The increasing use of high-end microprocessor systems operating at speeds of the order of GHz in power electronics applications will allow the development and execution of more precise control algorithms that can take advantage of different power conversion circuit topologies in more efficient ways.

The current development of more stable, fast, efficient, and high-blocking-voltage semiconductor devices will allow the more frequent use of DC–DC converter topologies to obtain inverters with low distortion at high voltages, leaving out the common inverter topologies (anchored diode, floating capacitor, and cascade bridge) due to their size, number of semiconductor elements, and control complexity.

The discharge time of a capacitor depends on the value of the capacitor and the value of the load, which can be on the order of nanoseconds (ns), milliseconds (ms), or seconds (s). For small times, the compensator has almost no effect on the dynamics of the system because the controller can use longer sampling times; in addition, the execution times used by the controller must be added to perform mathematical floating point operations and control of other peripherals.

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