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Review

Review of Voltage Balancing Techniques for Series-Connected SiC Metal–Oxide–Semiconductor Field-Effect Transistors

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Abstract: Power devices in series are low-voltage power devices used in medium- and high-voltage applications in a more direct program. However, when power devices in series are used, because of their electrical performance parameters or external circuit conditions, there are unique short-circuit voltage imbalances, a serious threat to the safety of the device. The article first summarizes the research status and characteristics of the four models of SiC MOSFETs based on the domestic and international research on the models of SiC MOSFETs in recent years; second, the voltage balancing technology of series-connected SiC MOSFETs is sorted out and summarized, and then the driving circuits of SiC MOSFETs are sorted out and summarized. Again, several voltage balancing techniques reviewed are compared in six different aspects: cost, modularity, complexity, speed of voltage balancing, losses, and effectiveness of voltage balancing. Finally, an outlook of voltage balancing techniques for series SiC MOSFETs is provided.

Keywords: silicon carbide metal–oxide–semiconductor field-effect transistors; voltage balancing technology; device in series connection; mathematical model; drive circuit

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1. Introduction

In recent years, with the rapid development of distributed generation technology, the increase in DC loads, and the increasing demand for the power supply reliability of various power-using loads, medium-voltage high-power DC converters have received extensive attention from scholars at home and abroad [1,2]. Compared with traditional medium-voltage AC converters, medium-voltage DC converters have the advantages of transmission efficiency, good stability, and easy direct access to distributed resources [3,4]. Some of the common and important applications of high-power DC converters and their corresponding voltage and power levels are given in Figure 1. Their typical applications are communication and data centers [5,6], metro traction power supply systems [7], ship power distribution fields [8], etc.

Power devices, as core electrical energy conversion devices, have been at the center of demand for their high voltage, high current, and low loss. Figure 2 shows the general development trends of power devices [9]. Compared with silicon-based MOSFETs and IGBTs, SiC MOSFETs have excellent operating characteristics such as high operating frequency, low on-resistance, high voltage and high temperature resistance, making them ideal for manufacturing high-frequency, high-voltage, and high-power devices. Although the use of silicon carbide metal–oxide–semiconductor field-effect tubes in high-voltage, high-power applications is expected, at present, due to the manufacturing process, costs, and other factors, commercial SiC power devices feature a maximum voltage level of 1700 V, and the ability of insulated gate bipolar transistors (insulated gate bipolar transistors, IGBTs) to withstand up to 6.5 kV of voltage is still a gap. There is still a gap between the device voltage. In order to solve the problem of insufficient voltage capacity in individual SiC MOSFET power devices, SiC MOSFET series operation is the most direct idea, but ensuring

the voltage balance between series-connected SiC MOSFET devices has become an urgent problem to be solved [10].

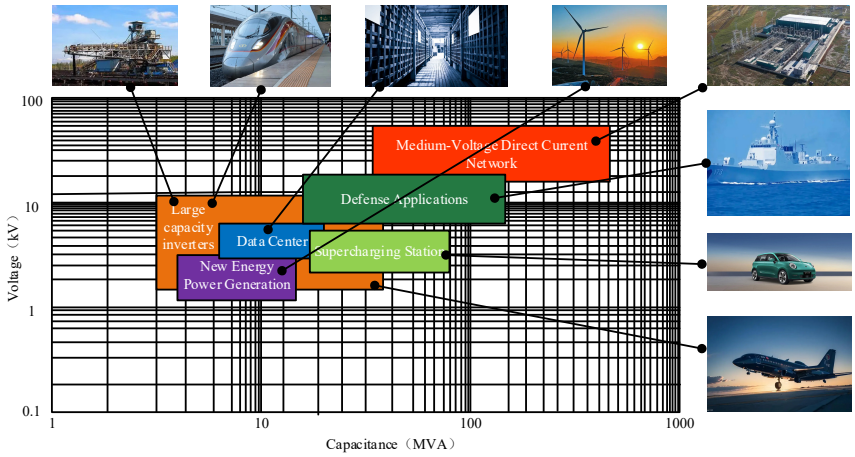

Figure 1. Typical applications and operating intervals of medium-voltage high-power equipment.

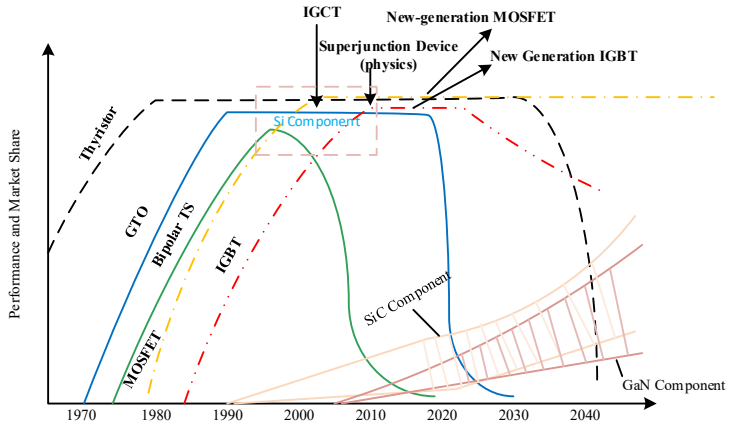

Figure 2. Trends in power devices.

In series SiC MOSFET operation, the voltage applied to each device is balanced under ideal conditions. The safe operation of the device will not be affected. However, due to the difficulty of ensuring that the internal electrical parameters of each SiC MOSFET remain consistent during the production process, as well as the nonlinear variation in the internal electrical parameters due to the influence of the peripheral circuits, unbalancing of the voltage distribution between the devices connected in series can occur, which affects the safe operation of the devices and can even result in irreversible damage [11]. The voltage imbalance that exists in series SiC MOSFETs during turn-on or turn-off is mainly categorized into static voltage imbalance and dynamic voltage imbalance. Static voltage imbalance refers to the voltage imbalance between devices due to the different volt-ampere characteristics of each SiC MOSFET device, temperature variations, etc., when the SiC MOSFET is in a turn-on or turn-off steady state [12]. Dynamic voltage imbalance refers to the fact that when SiC MOSFETs are in turn-on or turn-off transients, the differences in the electrical parameters of the SiC MOSFETs themselves, as well as the inconsistencies in the peripheral circuit parameters (stray inductance, buffer circuits, driver circuits, control signals, etc.), result in an imbalance in the voltages on both sides of the various series-connected SiC MOSFET devices [13]. If the problem of voltage unbalancing of devices connected in series can be effectively solved, low-voltage devices can be applied in series for medium- and high-voltage high-power conversion systems. The advantages of this scheme are small size and weight, simple topology, high power density, and the ability to

avoid the problems of a large number of devices and high capacitance of submodules in multi-level circuits.

In order to solve the voltage unbalancing phenomenon between series-connected SiC MOSFET devices, domestic and foreign scholars have proposed a variety of voltage balancing techniques. According to their role position, they can be divided into voltage balancing techniques on the driver side and voltage balancing techniques on the power side [14–16], as shown in Figure 3. Among them, the voltage balancing technique at the driver side mainly adjusts the gate-side input directly or indirectly through auxiliary circuits or control strategies, so as to realize the dynamic and static voltage balance of series-connected SiC MOSFETs. This technique can achieve a small unbalancing voltage, but the modulation time is long, and the reliability is not high. The voltage balancing technique on the power side mainly introduces RC/RCD snubber circuits or clamp circuits at the drain of the SiC MOSFETs, which use the peripheral circuits to absorb the overvoltage while indirectly buffering the transient action process of the device. This technique has a faster response time. However, if a small unbalancing voltage is achieved, the parameter design will become complicated. In addition, other voltage balancing techniques have been proposed, such as the voltage balancing technique based on the series connection of SiC MOSFETs and JFETs and the voltage balancing technique based on the series connection of SiC MOSFETs with a single drive signal. The voltage balancing effects are all unsatisfactory.

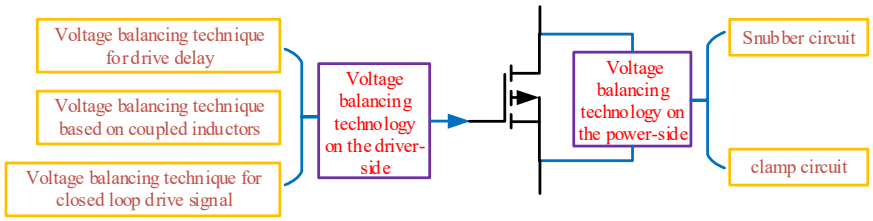

Figure 3. Trends in power devices.

In different practical applications, it is necessary to select appropriate voltage balancing techniques for series-connected SiC MOSFETs. Therefore, it is necessary to review and summarize different voltage balancing techniques for series-connected SiC MOSFETs and compare the voltage balancing effect, cost, complexity, and loss of each technique.

In order to realize the voltage balancing of series-connected SiC MOSFET devices, it is necessary to start from the study of individual MOSFET devices, including the analytical model of the device and the driving technology, etc., and then consider the principle of series operation of the device, circuit design, and optimization methods. This paper firstly summarizes the research status and characteristics of the four models of SiC MOSFETs according to the research on the model of SiC MOSFETs at home and abroad in recent years; secondly, the voltage balancing technologies of series-connected SiC MOSFETs are sorted out and summarized; then, the driving circuits of SiC MOSFETs are also sorted out and summarized; and finally, the research direction and optimization method of the voltage balancing technology of series-connected SiC MOSFETs are looked forward to. Finally, the research direction, development trend, and application prospect of voltage balancing technology for series SiC MOSFETs are summarized.

2. Models of SiC MOSFET

The safe operation of SiC MOSFET devices is a crucial consideration in practical applications, particularly during switching transients where MOSFETs are commonly exposed to overvoltage or overcurrent conditions. The occurrence of transient voltage imbalance during the operation of series-connected MOSFETs further exacerbates the voltage stress on the devices. To guarantee the safe and reliable operation of MOSFETs, accurate modeling of these devices serves as an effective means to assess their switching behavior during the design phase. Since the advent of SiC MOSFETs, research into their

simulation models has garnered extensive attention. Domestic and international scholars have continuously strived to develop simpler and more precise models for SiC MOSFETs. SiC MOSFET models can be broadly categorized into three types: behavioral models, physical analytical models, and numerical models. Additionally, some scholars have appropriately integrated these three models, leveraging their respective advantages to create a fourth type—the hybrid model.

2.1. Behavioral Model

For experts and scholars who are solely focused on the external current and voltage characteristics of SiC MOSFETs, the behavioral model is often the simplest and most direct choice. Behavioral modeling involves abstracting the actual electrical behavior of the device and fitting it to a mathematical model, without delving into the intricate physical characteristics of the device's operational process changes. The fitted mathematical formulas solely aim to mirror the functional traits of the device and often bear no direct relation to the underlying physical processes. Based on the switching characteristics of SiC MOSFETs, the switching process can be segmented into the switching delay state, current-switching state, voltage-switching state, and current/voltage oscillation state [17]. By constructing the equivalent circuit for each switching state and listing the corresponding circuit equations, one can derive the transfer function or state equation that accurately describes the SiC MOSFET's switching behavior [18–20]. This model obviates the need to consider the semiconductor's physical mechanisms and clearly delineates the state relationships at each stage of the SiC MOSFET's switching process, thereby effectively capturing its switching characteristics. Furthermore, most of the electrical parameters necessary for constructing the behavioral model can be readily obtained from the device's datasheet, enabling hardware engineers to assess design schemes early in the system design phase [21]. Behavioral models are favored in circuit and system-level simulations due to their ease of parameter acquisition. Various studies have focused on refining these models to better capture the characteristics of SiC MOSFETs. Reference [22] examines the output characteristic curves of SiC MOSFETs in the non-saturated region, specifically the relationship between drain-source voltage and drain current. By analyzing these curves, the study extracts key parameters for model building and proposes a subcircuit model based on the Level 3 MOSFET model in LTspice. This model is both structurally simple and computationally efficient. Furthermore, the authors utilize MATLAB's genetic algorithm to automate model optimization. Comparison with experimental data from double-pulse tests confirms the model's accuracy in predicting time-domain switching behavior and associated losses, making it suitable for SiC MOSFET application design. Reference [23] constructs an analytical model of the ideal switching process of SiC MOSFETs, revealing the interrelationships among different sub-states during switching. However, the model's lack of consideration for internal parasitic parameters limits its ability to accurately describe actual SiC MOSFET switching characteristics. Reference [24] addresses this limitation by optimizing the analytical model to fully account for internal MOSFET and circuit parasitic parameters, resulting in more accurate results. However, the model still neglects the nonlinearity of junction capacitance and transconductance parameters within the MOSFET. Reference [25] proposes a SiC MOSFET switching behavior model based on the finite state machine concept. The model divides the turn-on or turn-off process into five stages, defining corresponding state equations and transfer conditions based on transition relationships and state transitions between stages. It also considers the effects of nonlinear capacitance and nonlinear transconductance parameters of SiC MOSFETs during dynamic processes. Double-pulse test and simulation results demonstrate the model's accuracy in reflecting SiC MOSFET switching behavior, with voltage, current change rates, and overshoots aligning well with test results. Reference [26] introduces a behavioral model for simulating SiC MOSFET dynamic switching characteristics, consisting of a drain-source resistor and three constant inter-pole capacitances. In this model, the drain-source resistor's resistance decreases from infinity to a very small value as the gate-source voltage

increases. The model also considers the impact of system parasitic inductance on the switching process but neglects the nonlinearity of the inter-pole capacitance. Reference [27] extracts parameters such as SiC MOSFET inter-polar nonlinear capacitance using a simple device to measure the MOSFET's output characteristic curve, combined with parameter manuals provided by the device vendor. Based on this, the authors propose a SiC MOSFET behavioral model implemented in MAST language and simulate and verify its switching characteristics in the SABER platform under static and dynamic conditions. This model accounts for the effects of nonlinear conduction resistance and parasitic capacitance of the MOSFET, offering the advantage of short simulation times. In summary, these studies showcase various approaches to refining SiC MOSFET behavioral models, with each addressing specific limitations and improving the model's accuracy and applicability in different contexts.

2.2. Physical Analytical Model

Physical analytical models, often referred to as mathematical models, rely heavily on fundamental semiconductor physics theory. These models utilize three core equations from semiconductor physics to elucidate the internal operational mechanics of semiconductor devices. By solving these descriptive equations, one can derive expressions that describe the distribution and movement of carriers within the device, which in turn allow for the derivation of expressions for the device's external characteristics. In the realm of MOSFETs, several classical physical analysis models exist, notably the Hefner model, the Kraus model, and the Sheng Kuang model. Each of these offers a distinct perspective on describing the internal physical characteristics of MOSFET devices, thereby enhancing the accuracy of both steady-state and dynamic characteristic analyses. However, constructing a precise physical analytical model necessitates a thorough understanding of the MOSFET's internal structure, encompassing physical dimensions, doping concentrations within the device, and the complex parasitic parameters that arise. In practical scenarios, acquiring such detailed information can be challenging for device users, posing a significant hurdle in model development. Certain references, such as [28], have employed a voltage-controlled current source equivalent parasitic capacitor to simplify model structure and facilitate parameter extraction. Yet, this model incorporates a parallel structure of a voltage source and capacitor, which may compromise model convergence. References [29,30] have utilized segmented fitting to boost fitting accuracy, albeit at the cost of reduced model convergence. Moreover, while modeling the body diode, many studies treat it as a constant component, neglecting any inputs into the diode model. In reality, temperature influences the diode carrier diffusion rate. Consequently, some literature has incorporated the impact of temperature on the volt-ampere characteristic curve of the body diode [30]. Additionally, variations in gate-source voltage affect the concentration of diode carriers. Notably, both increased temperature and gate-source voltage shift the volt-ampere characteristic curve in the same direction, indicating that gate-source voltage is another crucial factor in diode modeling. To enhance the accuracy and convergence of SiC MOSFET models while reflecting their applicable operating conditions, reference [31] focuses on CREE's C2M0025120D (1200V/90A) as the modeling target. This study constructs a continuous function that describes the model's static characteristics as its core, and proposes a dynamic model with excellent convergence. Ultimately, a high-precision SiC MOSFET model with robust convergence is established, as illustrated in Figure 4. This model represents an advancement in capturing the complex behaviors of SiC MOSFETs under various operating conditions.

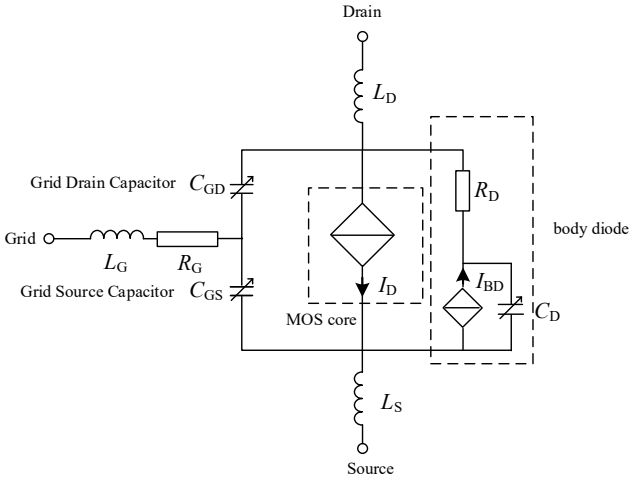

Figure 4. Mathematical model of SiC MOSFET with high accuracy and strong convergence.

2.3. Numerical Model

Unlike the aforementioned two models, the numerical model eschews the direct elucidation of the physical operating principles of carriers within the MOSFET and the external current-voltage characteristics. Instead, it employs the finite element analysis (FEA) method to construct the model, leveraging FEA software to conduct the simulation analysis. The creation of this model type necessitates the utilization of large-scale simulation software equipped with semiconductor simulation capabilities, while also demanding high precision in the internal physical parameters of the device. In practical applications, some experts and scholars have introduced a partial regional numerical modeling approach to mitigate simulation complexity. This approach applies the FEA method solely to the base region of the MOSFET, while continuing to use physical analysis methods for other parts to streamline the analysis, yielding satisfactory results. Reference [32] has developed a numerical analytical model for 6H SiC Schottky drain-source N-channel MOSFETs, grounded in research on the working mechanisms of Schottky drain-source MOSFETs. The voltammetric characteristics of the device are simulated through coupled solving, accurately depicting the effects of tunneling current and barrier reduction, thus more precisely reflecting the device's characteristics. Reference [33] utilizes semiconductor device simulation software to establish a numerical model that accurately mirrors the short-circuit failure of SiC MOSFETs and Si MOSFETs. This model analyzes the short-circuit failure mechanisms of field-effect transistors made from both SiC and Si materials. Reference [34] presents a numerical model for the surface potential of short channels, considering quantum effects. Based on this model, it analyzes the impact of source-drain bias on surface potential distribution.

2.4. Hybrid Model

All three aforementioned MOSFET models possess their unique strengths and weaknesses, yet none of them effectively balances model accuracy with simplicity, thereby limiting their broader application. In response to this limitation, some references have explored the integration of high-accuracy physical analytical models with high-simplicity behavioral models, proposing a hybrid model that incorporates all three types. For SiC MOSFET devices, a classic model outlined in reference [35] is widely adopted. This model builds upon the silicon-based Sajitang equation and the Shichman-Hodges model, while accounting for the unique resistive characteristics of SiC devices, such as channel electron mobility decay. It represents the static volt-ampere characteristics of SiC MOSFETs using a segmented function, with its *C-U* (capacitance–voltage) characteristics typical of a vertical structure capacitance model. However, due to the complexity of the segmented function, this model often fails to converge in simulation programs like SPICE (Simulation Program with Integrated Circuit Emphasis). Reference [36] complements the parameter extraction

method of the model presented in reference [35]. To address the convergence issue, reference [37] merged the models across different intervals of volt-ampere characteristics from reference [35], unifying the expressions of the current source model. However, the expressions in the linear and saturation regions of this model deviate from those in reference [35], resulting in an unsmooth transition between intervals and discrepancies with measured results. Building upon reference [37], reference [38] modifies the current source model expression to ensure that the model combines good convergence with voltammetric characteristics accuracy similar to that of the model in reference [35]. Additionally, it introduces a new Miller capacitance model that considers hierarchical depletion, accurately characterizing the *C-U* characteristics at low leakage source voltages, as illustrated in Figure 5.

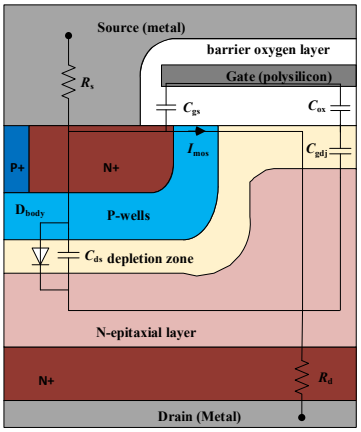

Figure 5. SiC MOSFET metameric cell profiles and modeling of aggregate elements in different regions.

3. Voltage Balancing Technique for Series-Connected SiC MOSFETs

Figure 6 shows the division of voltage balancing techniques. The following section makes an overview of voltage balancing techniques in this vein.

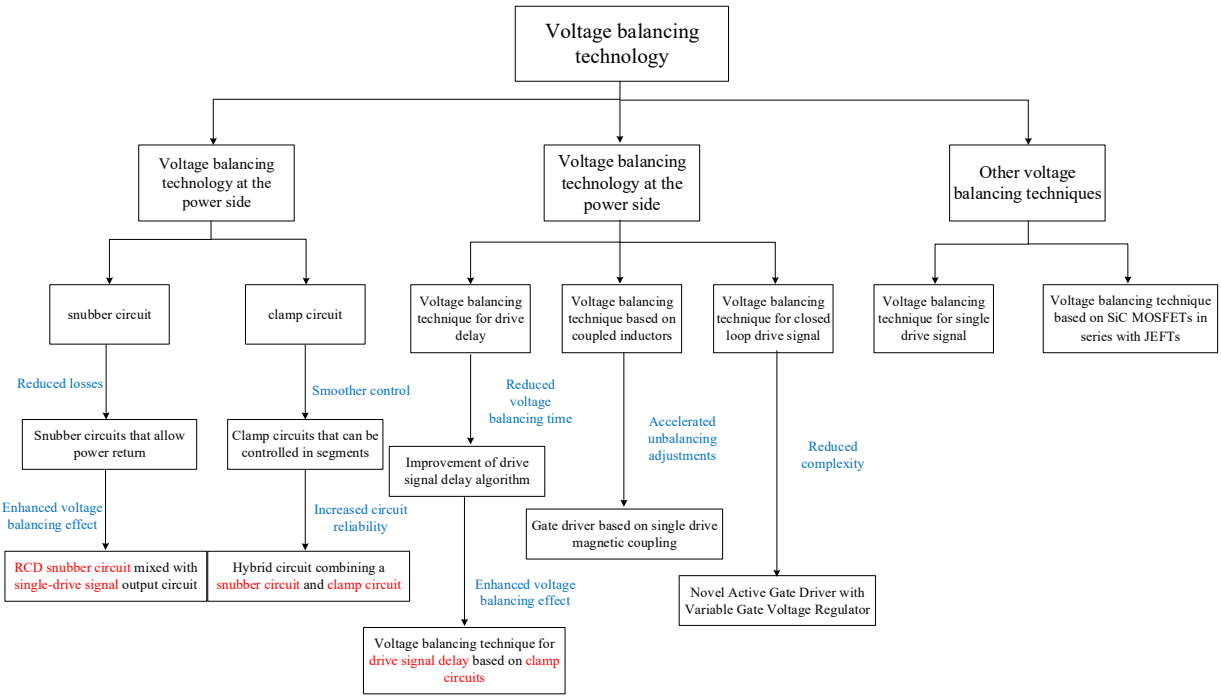

Figure 6. Voltage balancing technology division figure.

3.1. Voltage Balancing Technology at the Power Side

3.1.1. Snubber Circuit

Snubber circuits are a widely used voltage balancing technology on the power side. Common types of snubber circuits, as illustrated in Figure 7, include RC snubber circuits and RCD snubber circuits, among others [39–42]. These circuits are constructed using only passive components such as resistors, capacitors, and diodes, resulting in a simple and reliable circuit structure. However, it is crucial to match the passive components with the appropriate voltage ratings based on the device capacity. One drawback of snubber circuits is that they can slow down the switching speed of power devices. Additionally, they introduce additional losses into the system. Therefore, when designing snubber circuits, careful consideration must be given to the parameters, particularly the capacitance of the snubber capacitor. The design needs to balance the voltage balancing effect and the device switching speed, as both aspects are crucial for the overall performance of the system. To optimize the design of snubber circuits, engineers must carefully analyze the system's requirements and constraints. They must determine the appropriate values for the resistors, capacitors, and diodes to ensure that the circuit can effectively balance the voltage while minimizing losses and maintaining an acceptable switching speed. This may involve iterative testing and adjustments to find the optimal combination of parameters. In summary, snubber circuits are a valuable tool for voltage balancing in power-side applications, but their design requires careful consideration of the parameters to ensure optimal performance. By balancing the voltage balancing effect and the device switching speed, engineers can create snubber circuits that are both effective and efficient.

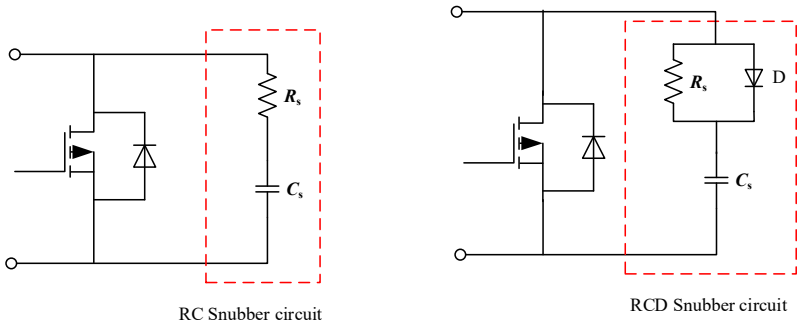

Figure 7. Typical snubber circuit structure.

The research on improved snubber circuits that combine switching devices and passive components aims to reduce the additional losses introduced by traditional snubber circuits. By incorporating switching devices, these circuits can actively manage the energy stored in the snubber during the power device's turn-off and diode recovery phases. This energy can then be fed back to the input power supply, significantly reducing snubber circuit losses and improving overall performance [43–47]. One example of an improved snubber circuit is the novel RCD snubber circuit topology proposed in reference [43], and the circuit structure is shown in Figure 8. This circuit topology uses snubber capacitors to clamp the maximum drain-source voltages of series-connected SiC-MOSFETs, ensuring highly reliable switching of the power semiconductors. Additionally, by adjusting the gate drive signal algorithm, the energy accumulated in the snubber capacitor can be actively transferred back to the power supply, effectively reducing snubber circuit losses, as shown in Figure 9. While these improved snubber circuits offer significant benefits in terms of loss reduction and performance improvement, they also come with increased complexity in circuit structure and component voltage withstand ratings. The use of switching devices and active control algorithms introduces additional design considerations and challenges. Despite these challenges, the potential benefits of reduced snubber circuit losses and improved performance make these improved snubber circuits a worthwhile area of research. Engineers must carefully balance the complexity and cost of these circuits

against the potential gains in efficiency and reliability to determine the best solution for their specific application. In summary, improved snubber circuits that combine switching devices and passive components offer a promising approach to reducing additional losses and improving performance. By actively managing the energy stored in the snubber, these circuits can significantly reduce snubber losses while maintaining high reliability. However, they also introduce increased complexity and design considerations that must be carefully evaluated.

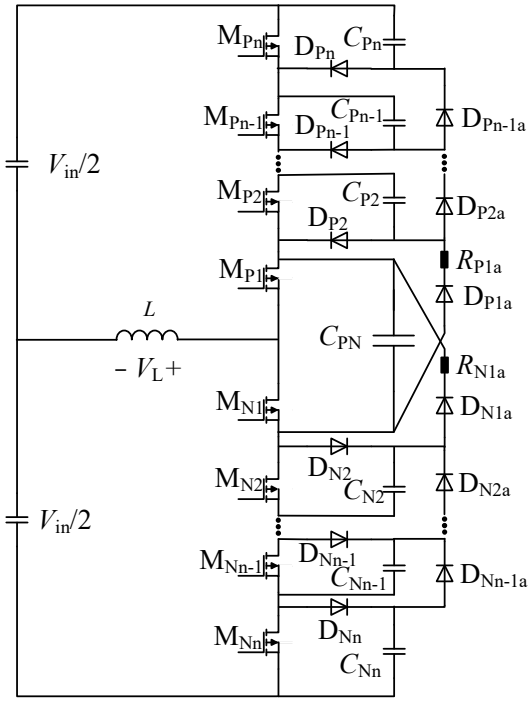

Figure 8. Snubber circuit structure with energy return function.

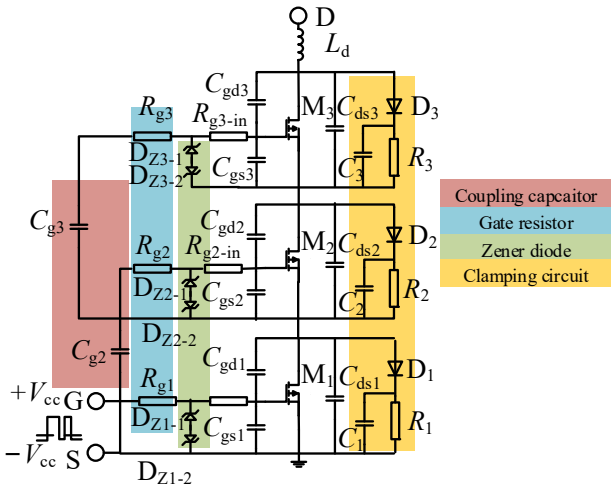

Figure 9. RCD snubber and single drive signal mixing circuit structure.

3.1.2. Clamp Circuit

The clamp circuit is a specialized circuit configuration designed to interact with the drain and gate terminals of a power device. Its purpose is to constrain the device's voltage within a predefined range, thereby guaranteeing its safe and reliable operation. The fundamental principle behind its operation is that, during the device's shutdown sequence, if the power device's voltage surpasses a specified threshold, the clamp circuit becomes

conductive. This, in turn, triggers the injection of current into the power device's gate, effectively mitigating the rate of increase of the drain-source voltage. A typical clamp circuit, as illustrated in Figure 10 [48–52], is a concept initially pioneered by Siemens [48] and subsequently adopted widely in engineering by companies like Alstom and ABB. This clamp circuit, specifically the regulator clamp, is interconnected between the MOSFET's drain and gate. When the device voltage exceeds the regulator's voltage threshold, the regulator becomes conductive, allowing a feedback current to be injected into the gate through the clamp circuit. This mechanism achieves off-peak voltage balancing for the device. However, the startup of this circuit clamp is not seamless. The voltage at the MOSFET terminal reaches V_Z before it can be controlled, limiting the ability to perform comprehensive process control. Consequently, losses increase and control becomes less effective, with the clamp circuit exhibiting significant transient power consumption. To address these issues, J. Saiz and colleagues designed a voltage slope adjustment circuit in 2021 [49], enhancing accuracy in voltage transient regulation by incorporating additional Zener diode groups. In practical applications, the voltage clamp method is often combined with RC/RCD buffer circuits. Hongfei Gong and team, in 2021, integrated an RCD snubber circuit with a Zener diode clamp circuit, analyzing its advantages from a loss perspective across different loads [50]. The circuit structure is depicted in Figure 11. In 2019, Zhe Wang and colleagues proposed a parametric design method for hybrid voltage balancing circuits that merge snubber and voltage clamp circuits. This method considers MOSFET switching losses, voltage balancing circuit losses, MOSFET voltage stress, and switching frequency, ultimately enhancing system efficiency and reliability [51]. The traditional voltage clamp method necessitates the use of multiple driver circuits, all requiring isolation from the high-voltage power supply. This results in harsh component operating conditions and complex circuits, hindering integrated applications. To tackle this challenge, Rui Wang and team designed a coupling circuit between voltage clamp equalization and single drive signal output, thereby improving the stability of the equalization circuit [52]. The clamp circuit boasts simplicity and high reliability, with relatively low requirements for MOSFET parameter consistency, making it easily applicable to multiple MOSFET series connections. However, it falls short in achieving real-time transient regulation for voltage fluctuations and necessitates the integration of passive voltage balancing to ensure effective balancing. Furthermore, akin to the snubber circuit, while the voltage clamp circuit can effectively mitigate voltage imbalances among series-connected MOSFETs, it introduces additional current into the MOSFET gate. When the MOSFET operates in the active region and the gate voltage rises, prolonged conduction and frequent activation of the voltage clamp circuit can result in extremely high switching losses for the MOSFET, alongside a significant imbalance in switching losses among series-connected MOSFETs. This imbalance in switching losses can be particularly severe.

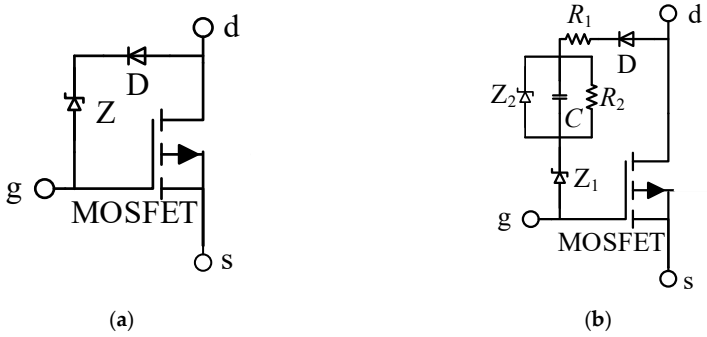

Figure 10. RCD snubber and single drive signal mixing circuit structure ((**a**) voltage regulator diode tube clamp circuit; (**b**) voltage regulator diode tube-capacitor clamp circuit).

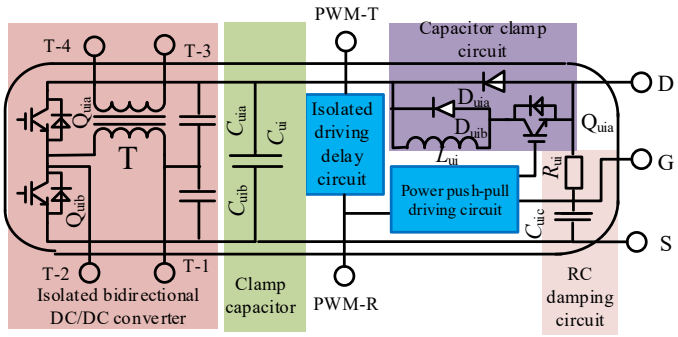

Figure 11. Hybrid circuit structure of snubber circuit and clamp circuit.

3.2. Voltage Balancing Technology at the Driver Side

3.2.1. Voltage Balancing Technique for Drive Delay

Drive signal delay is an effective technique for voltage balancing in power device drivers. The fundamental principle involves sampling the drain-source voltage of the series-connected device using a sampling circuit. This sampled voltage is then substituted into the voltage balancing algorithm computation within the controller. By adjusting the edge delay of the drive signal for the subsequent switching cycle, heterocyclic voltage balancing control of the series-connected device is achieved. Figure 12 illustrates a typical drive signal delay modulation circuit, which often employs a master-slave control approach to achieve voltage balancing by adjusting the delay of the slave signal. Current research primarily focuses on refining the implementation of the voltage balancing algorithm. Reference [53] introduces a voltage balancing algorithm with a fixed adjustment step for drive delay. This algorithm determines the direction of the voltage difference in the current switching cycle by assessing the same in the preceding cycle. If the voltage difference exceeds a positive threshold, the slave signal delay is increased by a fixed step in the subsequent switching cycle; conversely, if the voltage difference falls below a negative threshold, the delay is shortened by a fixed step. While adaptable to various voltage and current conditions, this technique suffers from slow adjustment speeds and limited accuracy. Reference [54] proposes a voltage balancing algorithm with dichotomous delay adjustment. The underlying concept is similar to that of [53], but the delay adjustment time is determined in a step-by-step, dichotomous manner through a state machine, thereby enhancing the speed and accuracy of delay adjustments. References [55–60] establish a closed-loop control relationship between signal delay and voltage difference, further improving the speed of voltage balance adjustments. However, the linear relationship between signal delay and voltage difference is derived from experimental fitting, lacking a theoretical analysis of its intrinsic link. Additionally, these references do not delve into the design of closed-loop regulation control parameters for the drive signal, and the parameter design process becomes complex when the operating point changes.

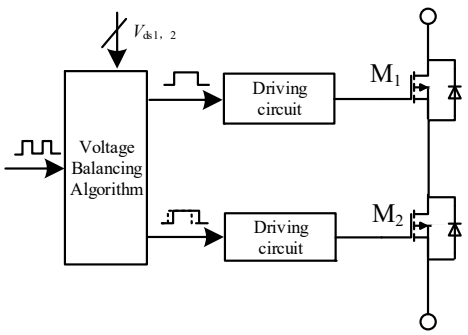

Figure 12. Typical adjustment circuit for drive signal delay.

References [61–63] propose a voltage balancing technique for drive signal delay that leverages a clamp circuit, as depicted in Figure 13. This technique represents an innovation in the sampling method employed in voltage balancing techniques for drive signal delay. Its core principle involves obtaining the clamp circuit's on-time duration (AC, or action time) by sampling the voltage drop across a series sampling resistor within the clamp circuit. The voltage balancing algorithm then adjusts the drive signal delay between devices based on this on-time duration. This method combines the clamp circuit with drive signal delay technology, aiming to prevent overvoltage damage to the device while achieving rapid voltage balancing of the series-connected device. However, the circuit implementation is relatively complex, and issues such as the additional loss introduced by the clamp circuit persist.

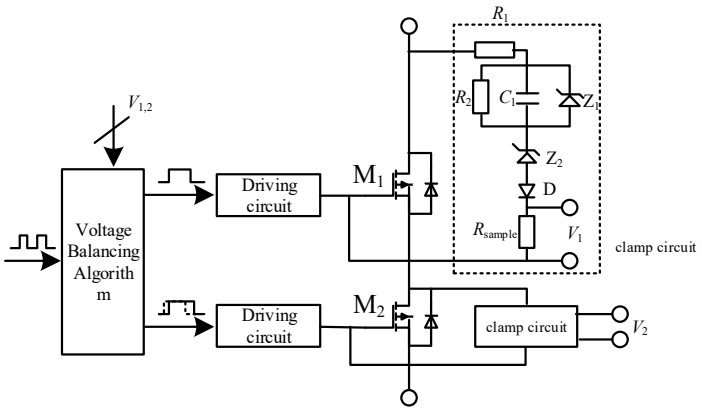

Figure 13. Circuit structure based on clamp circuits and drive delay.

3.2.2. Voltage Balancing Technique Based on Coupled Inductors

In 2002, Japanese scholars introduced a voltage balancing technique that utilizes coupled inductors. The primary principle of this technique involves employing mutual inductance to couple the gate signals, thereby suppressing discrepancies in gate currents, compensating for delays between drive signals, and ensuring synchronization of the gate signals, as illustrated in Figure 14.

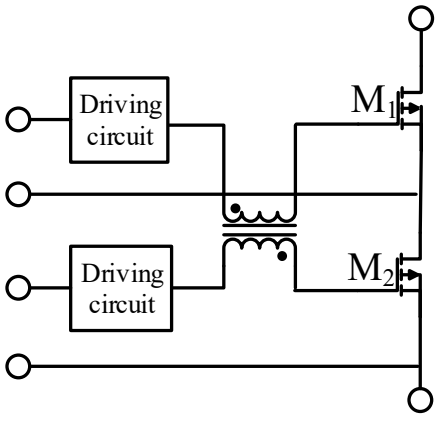

Figure 14. Voltage balancing technique based on coupled inductors.

As depicted in Figure 15, reference [64] introduces a simple, swift, and economical dynamic voltage balancing circuit designed to mitigate voltage imbalances between series-connected SiC MOSFETs. This circuit comprises an RC snubber and a coupled inductor, which efficiently detects drain-source voltage imbalances and appends a compensatory signal to the gate drive voltage. The article elaborates on the operational principles of this method and provides guidelines for selecting circuit parameters. Furthermore, it proposes an optimized layout for the circuit within a typical half-bridge SiC power module, aiming

to minimize the spurious parameters induced by the coupled inductor. The proposed method has been experimentally validated under various conditions, demonstrating that it significantly reduces the capacitance value of the buffer capacitor compared to the pure RC snubber circuit voltage equalization approach. Notably, as only passive components are utilized in the feedback loop, the proposed method is both reliable and straightforward.

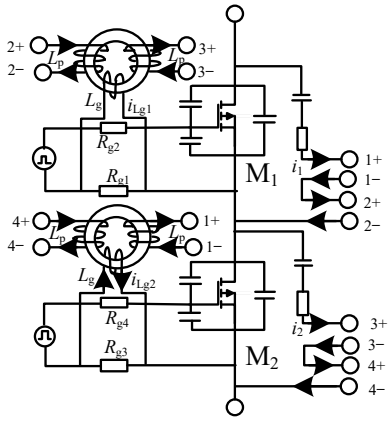

Figure 15. Circuit structure for mixing coupled inductor and RC snubber circuits.

As illustrated in Figure 16, reference [65] introduces a single-driver, magnetically coupled, voltage-source-type gate driver. With SiC MOSFETs serving as typical voltage-controlled devices, this proposed gate driver boasts a straightforward and cost-effective design, devoid of a flux reset winding on the secondary side. Thanks to the magnetic constraint, the drive voltages can achieve a high degree of synchronization, thereby minimizing the series voltage imbalance of the power devices that may arise from unsynchronized drive signals.

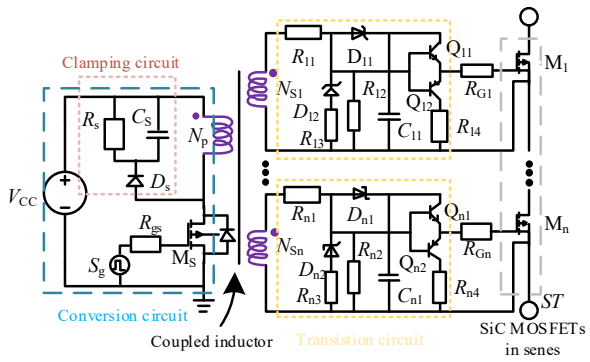

Figure 16. Single-drive magnetically coupled voltage-source gate driver.

3.2.3. Voltage Balancing Technique for Closed-Loop Drive Signal

Fully controlled power devices, such as IGBTs and MOSFETs, can be manipulated by adjusting the amplitude of their drive signals to control their switching processes. Consequently, utilizing active drive technology to achieve voltage balancing in series-connected devices is a well-established method. Compared to voltage balancing techniques at the power end, active closed-loop drive voltage balancing technology offers the advantages of minimal additional losses and numerous degrees of control freedom. The fundamental principle of this technology involves designing an active closed-loop drive circuit that utilizes the voltage difference across the series-connected devices to control hardware circuits or controllers. By modulating the gate voltage or gate current, this approach enables the regulation of the device's switching speed and the voltage balance control of the series-connected devices. The principle circuit of the active closed-loop drive, depicted in Figure 17 [66–72], primarily aims to achieve voltage balancing by sampling the device's

drain-source voltage and adjusting the drive signal through a control unit. Reference [66] introduces an enhanced control circuit shown in Figure 18, which modifies the original circuit by incorporating a bipolar transistor and pulsing the control signal. This modification ensures that the external capacitor is fully reset during each switching cycle. Additionally, the article presents a simplified model of active dv/dt control, revealing a linear relationship between the control voltage and the device's dv/dt. The article further describes a feedback control model using differential equations for stability analysis, providing a parameter selection guide for the control process. Reference [67] achieves soft turn-on and soft turn-off, along with controllable output dv/dt, by utilizing distributed resonant capacitors for dynamic voltage balancing. This eliminates the need for external dv/dt filters. In reference [68], a novel active gate driver with a variable gate voltage regulator is proposed. It employs a single P-channel MOSFET to time the connection of a pre-charge capacitor in series with the input capacitor, enabling adjustable switching transients for each device in the stack. These advantages are particularly evident when applied to low-power SiC MOSFETs with relatively small external resistances. The article presents two sampling and voltage balancing control circuits based on different processors, tailored to different switching frequencies and costs. It specifies their operating principles and design guidelines, and experimentally demonstrates their performance in voltage balancing control. On the other hand, references [69–72] adjust the compensating current source injection or extraction based on the reference voltage waveform V_{ref} of the device voltage. By comparing the difference between the VDS sampling voltage value and the given reference voltage V_{ref}, these references realize voltage balancing.

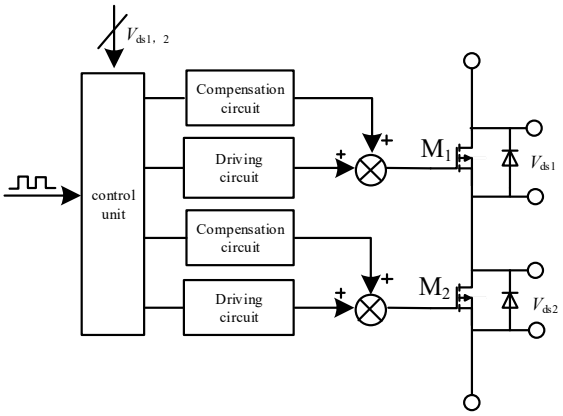

Figure 17. Voltage balancing technique for active closed-loop drives.

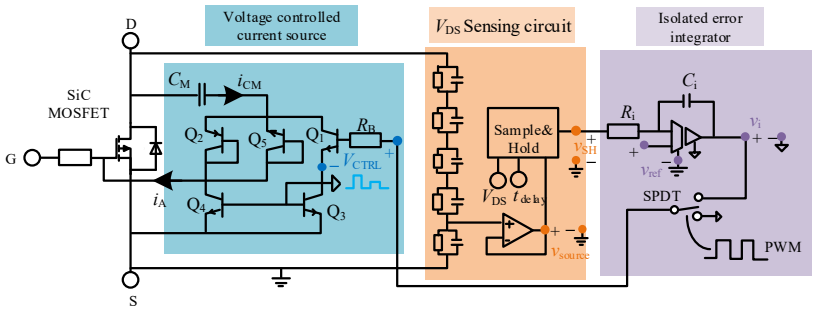

Figure 18. Active driver based on Miller capacitance compensation.

3.3. Other Voltage Balancing Techniques

3.3.1. Voltage Balancing Technique for Single Drive Signal

To address the challenge of assigning independent drive signals to multiple devices in series, which complicates the overall structure, references [73–75] propose a circuit structure for series-connected devices that operates using a single drive signal. Specifically,

reference [73] introduces a new series-connected topology for SiC MOSFETs, as illustrated in Figure 19. In this topology, three SiC MOSFETs connected in series are driven synchronously by a single gate drive. The article delves into the working principle of this topology and provides an analysis. Reference [74] presents a high-voltage series-connected SiC MOSFET module designed for use as the main switch in a repetitive high-voltage nanosecond pulse generator. This module boasts a minimal component count and requires only a single external gate driver, making it suitable for compact equipment. By analyzing the operational principle, three topologies for series MOSFET modules are proposed. Experimental comparisons of the switching behavior among three different topologies with four SiC MOSFETs connected in series are conducted. The study investigates the variations in switching characteristics of the series-connected SiC MOSFET module for different numbers of devices and optimizes the layout to reduce pulse lead time and enhance output pulse quality. Reference [75] examines the topology of series-connected power devices and introduces a novel single-signal driver. Compared to traditional driving methods, the proposed gate driver offers improved compactness, stability, and scalability. Notably, the designed structure effectively addresses and suppresses gate oscillation issues.

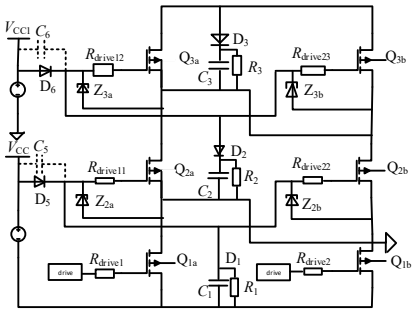

Figure 19. Circuit structure for single drive signal.

3.3.2. Voltage Balancing Technique Based on SiC MOSFETs in Series with JEFTs

Another incoming voltage balancing technique is based on SiC MOSFETs in series with JFETs, also called super JFETs [76,77]. In reference [76], in order to solve the problem of electrical parameter deviation in the series device structure, an optimized voltage control method is introduced, which can ensure voltage balancing in both static and dynamic states. In the absence of a Zener diode array, this strategy can significantly reduce the turn-off loss. As shown in Figure 20, the article also proposes this hybrid MOSFET-JFET circuit structure to suppress the parasitic capacitance effect of SiC MOSFETs. The forward gate drive voltage greatly accelerates the turn-on speed and reduces the switching losses. A FREEDM super cascade structure for a 15 kV/40 A three-terminal power switch was proposed in reference [77].

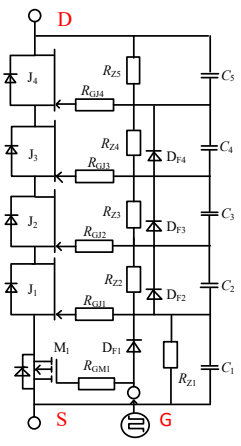

Figure 20. Circuit structure of hybrid MOSFET-JFETs.

4. Study of SiC MOSFET Driver Circuit

In addition to the effect of voltage balancing of series-connected SiC MOSFETs, which is affected by the modeling accuracy, another key factor is the SiC MOSFET driving circuit.

During the high-speed turn-on/turn-off process of SiC MOSFETs, several critical issues arise, including oscillations due to device parasitic parameters, electromagnetic interference (EMI) problems, and electrical stresses on the devices, which cannot be overlooked [78]. Typically, the most prevalent solution involves incorporating RC snubber circuits into the system's main circuit to mitigate voltage and current spikes [79]. However, it is important to note that these added snubber circuits introduce additional power loss to the entire system, along with increased size and cost. Furthermore, in high-power power system applications, the inherent structural complexity often makes it impossible to completely eliminate device spurious parameters [80]. Consequently, the optimized design of gate drivers has emerged as a focal area of research today. SiC MOSFETs and Si IGBTs are voltage-controlled switching devices; there are many similarities in the drive, so their early drive circuit design is mostly based on the existing Si device drive circuit design methods. However, there are differences between SiC and Si power devices, and the requirements for the drive circuit are also different. For example, if the SiC MOSFET gate charge Q_g is smaller, its gate-source voltage is more prone to oscillations; in addition, the SiC MOSFET short-circuit withstand time is shorter than the silicon power device, so its drive protection circuit detection time and short-circuit response time are shorter, and the response speed of the drive circuit is more demanding. At present, most SiC MOSFET drive circuit chips use IGBT driver chips, because SiC MOSFETs and IGBTs have similar characteristics, but because the IGBT works at low frequency, the existing mature IGBT driver chip drive capacity is smaller; the drive current is generally about 2A, and cannot give full play to the SiC MOSFET's high-frequency characteristics. In summary, studying a specialized circuit to drive SiC MOSFETs is worthwhile.

In foreign countries, the current mainstream SiC MOSFET driver manufacturers are ON Semiconductor, Core, Infineon, etc. These manufacturers have developed a SiC MOSFET special driver chip, rather than the IGBT driver chip, to drive the SiC MOSFET. Among them, ON Semiconductor's driver chip has the ability to drive high-voltage, high-frequency MOSFETs as well as perfect protection features, and Infineon's driver chip can do a two-stage shutdown to suppress dv/dt in the shutdown transient. Reference [81] proposes a new multistage structure of a medium-voltage gate driver, which consists of four main parts: a dc–dc isolation stage, a signal transmission stage, a gate drive stage, and a short-circuit protection stage. The article also designs a medium-voltage isolation transformer utilizing ferrite cores and windings embedded in polyamide material, implemented in the form of a printed circuit board, with high noise immunity and reliable signal transmission capability, while the driver occupies less space. However, the article lacks the design of circuit parameters and experiments with high switching frequencies and different switching tubes. An optically isolated gate driver for SiC power devices was proposed in reference [82]. The article focuses on minimizing the common mode current injection into the control circuit, thus adapting the gate circuit to higher fast switching transient $\mathrm{d}v/\mathrm{d}t$. By reducing the common mode interference with the control circuit, signal integrity can be improved, faults in the converter can be reduced, and the reliability of converter operation can be enhanced. Although the article has done experiments applied to switching tubes of different voltage and current levels, it can be seen that the voltage peaks are larger during the switching transients of the switching tubes. A new gate driver based on a multistage turn-off gate voltage application is proposed in reference [83], as shown in Figure 21. The driver reduces the impedance of the gate driver by adding an additional new auxiliary circuit with a triode series capacitor between the gate source. The article establishes an equivalent model of the driver circuit as well as design principles for the capacitor. However, it lacks experimental verification of different switching tubes as well as different switching frequencies, and from the available experimental waveforms, the driving signal waveform edge jumps slowly. Reference [84] proposes a novel single gate

driver (SGD) scheme by adding additional gate diodes to effectively mitigate unwanted gate voltage oscillations (GVOs). In the article, a small-signal model of the proposed SGD is developed, and a stability analysis is presented to reveal the intrinsic mechanism of GVOs. Based on the pole-zero plot and root-trajectory analysis, appropriate parameters of the absorber circuit were determined. However, the designed driver is not compact enough and has high losses.

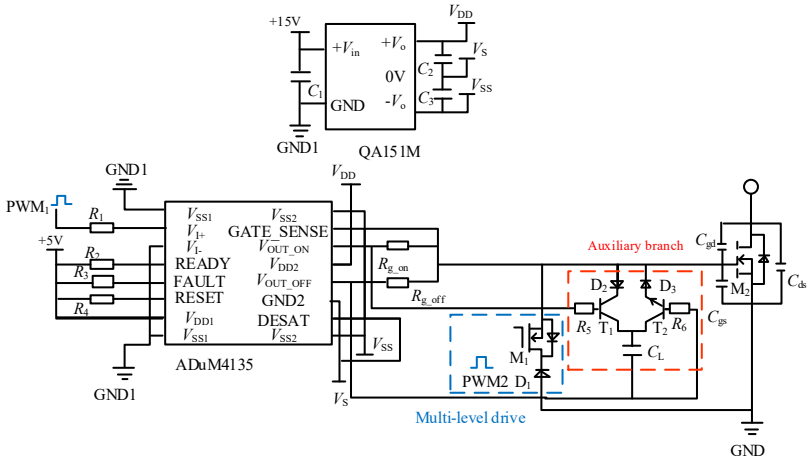

Figure 21. Reference [83] drive circuit.

In China, Qin Haihong made an overview of the current SiC MOSFET common driving technology and developments and gave a summary of whether the circuit is isolated or not, has dead time, has anti-interference ability, etc. [85]. Yuan Jie proposed a SiC MOSFET driving circuit built with discrete devices and gave detailed design ideas and simulation verification for the overcurrent protection function to achieve the overcurrent protection delay within 800 ns [86]. However, the article lacks analyses of disturbance and reactive power loss. Xu Yao reported related research for the high-speed application of SiC MOSFETs, achieving a high-speed drive of 1 MHz at 200 W with dynamic current balancing, and realizing the parallel application of SiC MOSFETs [87]. However, the article does not solve the problem of strong and weak electrical signal interference. Lei proposed a closed-loop driver chip that detects the size of chip dv/dt and di/dt through peripheral circuits, and dynamically adjusts the drive current to reduce the SiC MOSFET switching loss [88]. However, from the experimental waveforms, it can be seen that the drive signal delay is large, and the drive circuit is not designed to protect the circuit; the reliability is not high. Zhou Qi analyzed the design of series drives for SiC MOSFETs, proposed a SiC MOSFET series voltage balancing circuit, and simulated and verified its circuit [89]. Tailei Du conducted research and design for the drive of the SiC module type FF11MR12W1M1B11 of A company. On the basis of meeting the SiC drive current, active clamp protection, desaturation protection, and fault signal feedback functions were added [90]. Ke Zhao proposed a driving method and driving circuit to suppress the threshold voltage drift in response to the serious problem of threshold voltage drift in SiC MOSFETs. The driving circuit distinguishes the gate voltage between the dynamic process of shutdown of the controlled device and the gate voltage after shutdown steady state by introducing an intermediate level, so as to achieve the purpose of reducing the threshold voltage drift of SiC MOSFETs, and at the same time retaining the advantage of negative gate shutdown voltage [91]. Table 1 shows a comparison of several of these drives.

Table 1. Comparison of drive performance.

Reference	Isolated	Efficiency	Volumetric	Interference Resistance	Cost
[81]	yes	middle	small	strong	higher
[82]	yes	middle	smaller	stronger	middle
[83]	yes	low	middle	-	high
[84]	yes	high	larger	middle	middle
[86]	yes	low	middle	-	middle
[87]	yes	middle	small	-	low
[88]	yes	higher	large	stronger	middle
[90]	yes	low	larger	middle	middle
[91]	yes	middle	middle	strong	lower

5. Comparison and Perspectives of Voltage Balancing Techniques for Series Connected SiC MOSFETs

5.1. Comparison of Voltage Balancing Techniques for Series-Connected SiC MOSFETs

Different voltage balancing techniques vary in terms of voltage balancing effectiveness and ease of implementation because of different mechanisms. As shown in Table 2, this section of the article will compare them in terms of cost, modularity, complexity, speed of voltage balancing, losses, and effectiveness of voltage balancing.

Table 2. Performance comparison of voltage balancing techniques.

Voltage Balancing Technology	Reference	Experimental Data	Cost	Modularity	Complexity	Speed of Voltage Balancing	Losses	Effectiveness of Voltage Balancing
Voltage balancing technology at the power side	[43]	2.4 kV, four tubes in series, equilibrium time 200 ns, efficiency less than 90%	lower	high	lowest	faster	large	middle
Voltage balancing technique based on SiC MOSFETs in series with JEFTs	[76]	4 kV, five tubes in series, equilibrium time 800 ns, efficiency above 90%	lower	middle	lower	middle	middle	middle
Voltage balancing technique for single drive signal	[74]	10 kV, ten tubes in series, equilibrium time 600 ns, efficiency above 90%	lowest	middle	lower	fastest	middle	bad
Voltage balancing technique based on coupled inductors	[65]	1.2 kV, three tubes in series, equilibrium time 750 ns, efficiency above 90%	middle	middle	middle	faster	middle	middle
Voltage balancing technique for drive signal delay	[54]	320 V, two tubes in series, equilibrium time ns level, efficiency more than 95%	higher	low	high	slow	small	good
Voltage balancing technique for closed-loop drive signal	[71]	400 V, four tubes in series, equilibrium time ns level, efficiency above 90%	highest	low	high	slow	small	good

Comparing the cost of several voltage balancing techniques discussed in this paper, it can be clearly seen that voltage balancing technology at the power side and voltage balancing techniques based on SiC MOSFETs in series with JEFTs are cheaper. Voltage balancing techniques for a single drive signal can further reduce the cost because it requires only one power supply, unlike the conventional gate driver that requires multiple isolated power supplies for gate control. Voltage balancing techniques based on coupled inductors have a relative increase in cost and volume due to the addition of coupled inductors in the driver; finally, when comparing the voltage balancing technique for closed-loop drive signals to the delayed voltage balancing technique for drive delay, although both techniques require measurement and sampling of the device drain-source voltage, the delayed voltage balancing technique for the drive requires a stronger processor for higher gating timing calculations, and the cost is It is also more costly.

When it comes to the modularity of voltage balancing techniques, the voltage balancing technology on the power side performs the best. Voltage balancing techniques for drive signal delay, voltage balancing techniques based on SiC MOSFETs in series with JEFTs, and voltage balancing techniques based on coupled inductors can be considered to be a close second in terms of modularity. Finally, voltage balancing techniques for closed-loop drive signals and voltage balancing techniques for drive signal delays are also modular to some extent but need to be adjusted in their control phase. In addition, in practice, certain voltage balancing techniques may have limitations in terms of the number of devices connected in series.

In terms of complexity, techniques that require the measurement of drain-source voltages and the use of closed-loop controllers are much more complex than techniques consisting of passive components only. This is why in Figure 22, the voltage balancing technique with active closed-loop for the drive circuit and the voltage balancing technique with delayed drive signals are ranked higher in terms of complexity. For the voltage balancing technique with a single drive signal, the complexity lies in the fact that there must always be enough gate drive power supplied to the MOSFET, regardless of the voltage, duty cycle, and other conditions.

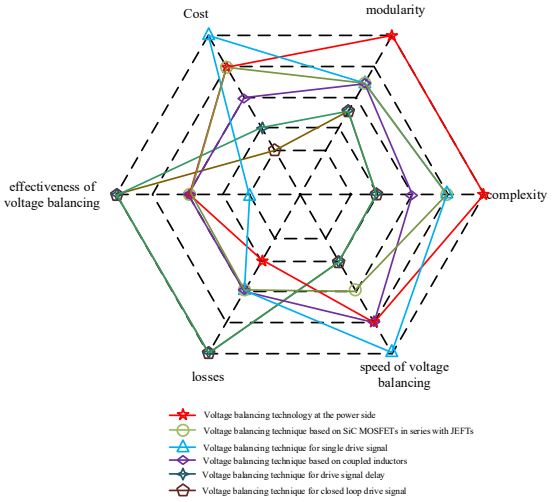

Figure 22. Summary of comparisons made between different voltage balancing techniques.

The importance of the speed of voltage balancing stems from the fact that even a small number of voltage balancing switching cycles can damage the MOSFETs in series. Techniques such as voltage balancing with active closed loops in the drive circuit or voltage balancing with delayed drive signals require several cycles to achieve proper voltage balancing. In other words, although these techniques can achieve voltage balancing, it is not straightforward compared to voltage balancing techniques on the power side.

The next comparison focuses on the additional losses incurred by the system. As previously discussed, for fast-switching SiC MOSFETs, the voltage-balancing technique on the power side inevitably results in losses that are equal to or even greater than those of the device itself, positioning this technique at the bottom of the ranking in terms of additional losses. The voltage balancing technique for a single drive signal and the voltage balancing technique based on SiC MOSFETs in series with JFETs are likely to follow closely, as they also necessitate the use of passive devices to achieve the desired voltage balance. Conversely, voltage balancing techniques on the drive side incur relatively fewer additional losses compared to the other techniques, as they do not significantly alter the switching behavior of the power device. The final comparison revolves around voltage balance. In practical applications, voltage imbalances within the range of 3% are considered acceptable. Techniques such as voltage balancing for closed-loop drive signals and voltage balancing for delayed drive signals have the potential to achieve minimal or even virtually zero

voltage imbalance. The voltage balancing technique on the power side and the voltage balancing technique based on SiC MOSFETs in series with JFETs may serve as the second-best options, as achieving better voltage balancing results through the selection of passive devices can become challenging. Lastly, the voltage balancing technique with a single drive signal yields the poorest results.

5.2. Challenges and Prospects of Voltage Balancing Techniques for Series-Connected SiC MOSFETs

The advantages and disadvantages of various voltage balancing techniques have been outlined above. With the growing diversity of converter circuit topologies utilizing SiC MOSFET series structures, voltage balancing in series-connected SiC MOSFETs presents an even more significant challenge and offers a broad scope for further development.

The disadvantage of the voltage balancing technique on the power side lies in the significant extra loss it incurs. Therefore, accurately calculating these additional losses and analyzing their causes can be instrumental in reducing the overall circuit loss from the source and enhancing efficiency. Current research lacks sufficient precision in calculating losses within the voltage balancing circuits at the power side of series-connected SiC MOSFETs. To address this, an accurate loss model for the voltage balancing circuit of SiC MOSFET devices must be established. This model should incorporate factors such as temperature to enable comprehensive loss calculations, thereby mitigating the adverse impact of the power-side voltage balancing technique on the entire circuit. The reliability of the voltage balancing technique on the driver side is relatively low. Therefore, analyzing the voltage balancing technique across various application scenarios should encompass multiple aspects, including its impact on voltage balancing and circuit reliability. While existing research has demonstrated that the voltage balancing techniques for drive signal delay and closed-loop drive signals can achieve a higher degree of voltage balancing, the complex parameter calculations and control methods they employ introduce instability into the circuit. Furthermore, current research lacks depth in analyzing circuit reliability. It is imperative to incorporate circuit reliability analysis into the parameter selection process and strive to simplify the control algorithm as much as possible. As SiC MOSFET process technology advances and SiC and other new-generation semiconductor materials are utilized, the switching speed of individual SiC MOSFETs is increasing rapidly, and their voltage withstand capabilities are becoming higher. Consequently, achieving voltage balance in series-connected SiC MOSFETs under high-voltage and high-frequency conditions has emerged as a pressing issue. Current research lacks sufficient studies on series voltage imbalance in high-voltage and high-frequency applications. For the power-side voltage balancing technique, the voltage withstand capacity of passive devices must be taken into account. For the driver-side voltage balancing technique, in addition to optimizing feedback time, exploring the benefits of combining different voltage balancing techniques can be considered to achieve superior voltage balancing effects, thereby meeting the application demands of high-voltage and high-frequency scenarios. In general, experts have achieved significant advancements in the research of voltage balancing technology in recent years. This includes the proposal of a universal analytical model for parameter extraction based on datasheets, the optimization of snubber capacitors, and the implementation of multi-segment smoothing control for clamping circuits. However, there are still some areas that require further exploration. Specifically, there is a need to enhance the accurate modeling of SiC MOSFETs. Additionally, the current voltage balancing techniques are predominantly applied to series connections of 2 to 5 devices, with a notable lack of discussion on series connections involving approximately 10 devices.

6. Conclusions

In this paper, based on summarizing the causes of voltage imbalance in series SiC MOSFETs, we first introduce four classical SiC MOSFET models. Secondly, we review the characteristics and basic theories of the existing voltage balancing techniques for series SiC MOSFETs from three aspects: voltage balancing techniques on the power side, voltage

balancing techniques on the driver side, and other voltage balancing techniques. Then, we summarize the current development status of SiC MOSFET driver circuit development status. Comparing six different aspects, i.e., the cost, modularity, complexity, speed of voltage balancing, losses, and effectiveness of voltage, the paper compared several voltage balancing technologies. The comparison results show that the simple and more traditional voltage balancing technology on the power side is less complicated to implement and has a lower cost, better modularity, and better voltage balancing effect at startup. However, when it comes to the additional loss and voltage balance of the system, the voltage balancing technique on the driver side is better than the former. Finally, the challenges and further research directions for the study of voltage balancing techniques for series-connected SiC MOSFETs are pointed out.

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Conflicts of Interest: F.C. was employed by State Grid Yuncheng Power Supply Co. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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