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Design and Simulation of a Novel Modular Converter-Transformer for AC/DC, DC/AC and DC/DC Operations

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Abstract: This manuscript describes the research and the development of a novel family of modular AC/DC, DC/AC and DC/DC converters for high-voltage interconnections between AC and DC lines or between two DC lines. Such devices are bidirectional and they integrate a three-phase power transformer. The relationship existing between AC and DC voltages in each module for rectifier and inverter operations is analogous to the one set in single-phase thyristor bridges. Due to the novelty of this topic, a low-voltage, low-power prototype was sized to make a first validation of its predicted behavior. This converter should realize all the operating modes allowed by the new family of devices, namely, AC/DC, DC/AC and DC/DC conversions. Its rated phase voltage is 230 V rms and it should be able to carry at least 1 kW. Thus, a switching model of the device was realized first. The simulated behavior of this prototype is deeply discussed in this paper during steady-state, transient and DC-fault operations.

Keywords: modular converter; multilevel converter; HVDC; converter transformer

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1. Introduction

High-voltage DC (HVDC) interconnections became interesting solutions in several countries worldwide for sub-sea and/or long transmission lines ($\ell \geq$ 600–700 km) in the last 20 years, due to their economical convenience and several technical advantages with respect to traditional three-phase AC solutions [1,2]. Among all the possible aspects in favour of long DC lines versus AC ones, it is worth mentioning the theoretical absence of skin effects on the conductors, limited harmonic content in DC quantities, no issues related to quarter-length lines and reduced number of conductors in each interconnection (i.e., two or even one active conductors instead of three). Therefore, research in power electronics focuses on the design of converters working as interfaces between AC and DC grids or directly among DC ones. These devices should aim to be efficient, safe, flexible and must provide strong reduction in both the harmonic distortion on the AC side and the ripple on the DC one. After the first studies and applications with conventional two-level converters, new solutions started to be investigated based on three- or multi-level solutions [3–6]. Indeed, the need for large passive filters was an issue with two-level devices to reduce harmonic pollution. In particular, modular multilevel converters (MMCs) became a very appreciated solution by the scientific community due to their applicability as well as scalability for several voltage levels [7]. The literature reports many case studies involving the applications of such devices, e.g., recharging stations [8], battery management systems [9] and traction [10,11] on electric vehicles [12] as well as interfaces for HVDC interconnections [13–19]. It goes without saying that multi-level converters in general ensure better approximations of sine waves with increasing number of levels, without

the need for rising the switching frequency too much. On the other hand, they may have higher costs associated with the required semiconductors compared to two-level solutions, even though each power switch has a nominal voltage which is inversely proportional to the number of installed modules. Hence, a trade-off must be found between the reduction in size of passive filters, the increase in number of switches in the converter and their associated costs [20,21].

Additionally, another big challenge in DC interconnections is the clearance of DC faults. This is still the subject of several studies carried out by the scientific community due to the intrinsic lack of any zero crossing in DC currents. Hence, typically large energy dissipation is associated with clearance events and traditional AC circuit breakers cannot be used to this aim during such faults [22]. The literature offers solutions like solid state breakers [23,24], hybrid breakers (i.e., with both semiconductors and mechanical switch) [25–27] and MMC converters with fault-blocking capabilities [28–30]. With this background in mind, Terna, the Italian Transmission System Operator (TSO), deposited a patent proposing a new family of bidirectional converter transformers (CTs) capable of working as rectifiers AC/DC, inverters DC/AC and DC/DC converters [31,32]. These new devices have multi-level and modular characteristics. However, they differ from MMCs due to the absence of batteries or capacitors as energy storage elements in each module. Moreover, these converters are characterized by the capability of transforming DC fault currents into AC ones, allowing for the exploitation of traditional AC protections for DC fault clearance.

Specifically, this paper shows the working principles of this new family of devices and reports the sizing and the first simulations of a low-voltage, low-power prototype. The digital twin of the physical device is based on a switching model of the electrical system, and it is aimed to prove the applicability of the idea proposed in the patent. Moreover, a real prototype is created based on the simulation results obtained during this research. In particular, the device could be operated in all three different working operations, namely AC/DC, DC/AC and DC/DC conversions. The realization of the actual converter and the experimental test campaign are still ongoing while writing this paper. Hence, this manuscript is organized as follows: an overview of the working principles, the main equations linking DC and AC voltages for this family of device and the fault clearing strategy are reported in Section 2. Then, Section 3 explains how the prototype was sized and shows how its switching model was realized. Section 4 reports the results for several steady-state and transient operations and for some sensitivity analyses as well. In particular, emphasis is put on the simulation runs showing the fault clearance capability of the device. Finally, a conclusion is drawn.

2. Structure and Main Equations of the New Family of CTs

Before going into the details of the design and modelling of the low-power, low-voltage prototype of the CT, this section shows an overview of its working principles. Starting form the adopted arrangement of the switches in each module and the connections between modules and transformer, the modulation logic is explained. Then, some equations are reported: they allow for estimations of electrical quantities of interest (both in terms of mean and rms values), but they also provide some information on their evolution in time. Finally, this section describes the peculiar feature of these power converters, that is, their capability of introducing zero crossings in DC currents. This ability allows for easy DC fault clearance combining the action of the modules of the CT with the operation of conventional circuit breakers currently adopted in AC grids.

2.1. Topology of the Device

The family of converters described in patent [31] are characterized by the presence of a multi-winding power transformer, which primary is directly connected to the AC grid for AC/DC and DC/AC operations. Thus, it must work at grid frequency, namely 50 or 60 Hz. Such transformers should have three primary windings and $3 \times M$ secondaries (namely,

M is the number of secondaries in each phase forming a M-level converter). Every power module has two couples of terminals, thus forming one AC port and a DC port. The AC side is connected to a secondary winding with a one-to-one correspondence, as shown in Figure 1. All the elementary power cells are then cascaded connecting their DC terminals in series. This peculiar arrangement determines a DC bus and a three-phase AC port at the primary terminals of the transformer for the whole device (see Figure 1). Therefore, the CT can be seen as an equivalent power transformer with a time-varying transformation ratio between the AC and DC ports. Moving to the topology of the $3 \times M$ power modules, it slightly depends on the adopted semiconductor technology and application. For high- and medium-voltage frameworks, Gate Turn-off Thyristors (GTOs) and Integrated Gate-Commutated Thyristors (IGCTs) are the best candidate switches. For medium- and low-voltage applications, Insulated-Gate Bipolar Transistors (IGBTs) can be used, whereas Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) are intended only for low-voltage applications. The peculiarity of all these cells is the presence of anti-series or anti-parallel switches to allow for the bidirectional control of the device during DC/AC and AC/DC operations, as well as to block the current flow in specific directions through the switches: the arrangements for the switch technologies mentioned before are reported in Figure 2. It must be said that the arrangements reported in Figure 2 show discrete switches, but monolithic bidirectional switches [33] can be used as well to help improving the power density of the devices.

Regarding the DC/DC operation, a power transformer is foreseen as well. For this specific application, it should be multi-winding both on the primary and on the secondary sides, having an inverter and a rectifier stage. Namely, the input stage works as inverter, whereas the output one operates as rectifier. The two stages are cascaded in this configuration; overall, a device working as DC/DC converter should have two DC ports. The frequency on the AC side of the modules can be much higher than 50 or 60 Hz, since no interface with the AC grid is foreseen. Therefore, the geometrical size of the transformer can be much smaller than in inverter or rectifier operations.

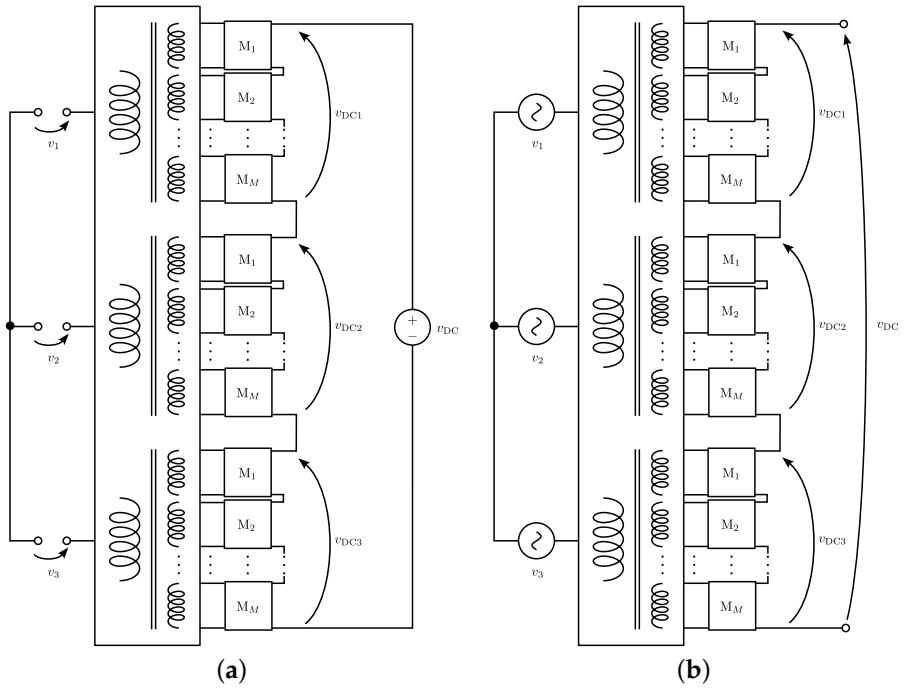


Figure 1. *Cont.*

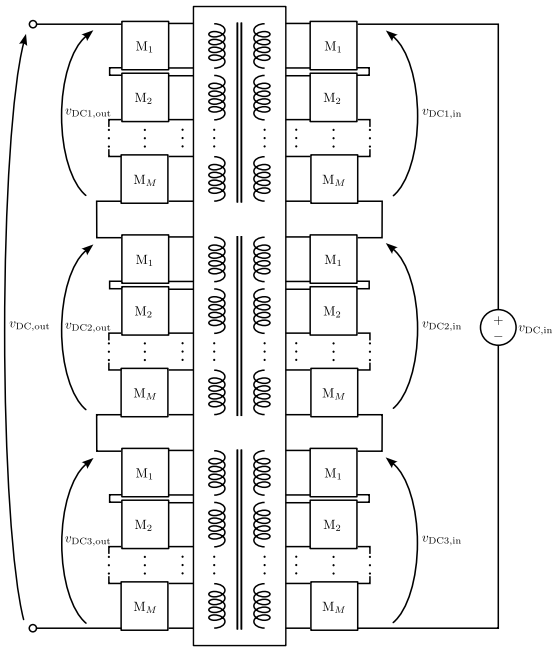


Figure 1. Equivalent circuits of the family of CTs working as: (**a**) DC/AC, (**b**) AC/DC and (**c**) DC/DC converters. Each module is connected to a secondary winding of a multi-winding transformer. Transformers must be multi-winding on both sides in DC/DC converters [32].

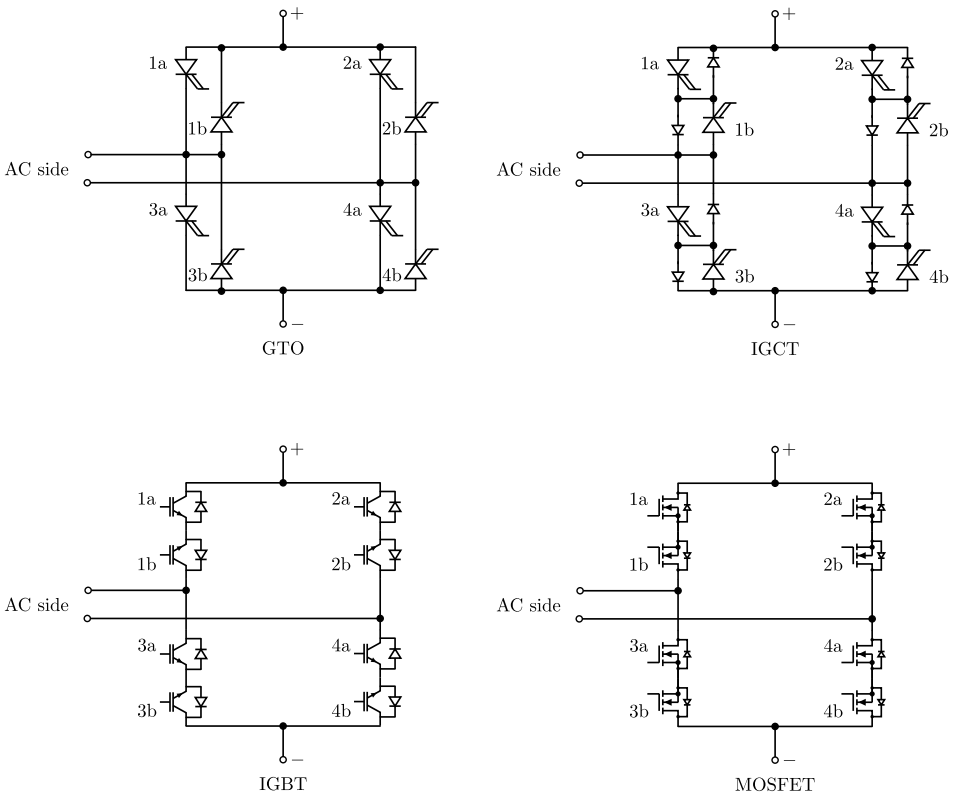


Figure 2. Arrangement of the power switches in the modules for different semiconductor technologies. AC and DC ports (this last showing + and − terminals) of the cell are highlighted [32].

2.2. Modulation Strategy

The topologies proposed in Figure 2 enable bidirectional power flow to the CTs. As already stated, the eight electronic switches are never on at the same time. Indeed, the four

semiconductors labeled with letters "a" or "b" (as reported in Figure 2) can be enabled or disabled through two signals G_a and G_b. The first activates the four modules involved in the inverter operation when set to a logic high value, whereas G_b is turned on to start rectifying operations. Then, the effective dynamic variation of the transformation ratio of the CT between its AC and DC ports is a consequence of the turn number in the power transformer and the modulation strategy adopted to drive the power electronics. This last is analogous to the nearest level control (NLC) used in MMCs [14]. Namely, three reference sinusoidal signals $v_{e,1}(t)$, $v_{e,2}(t)$, $v_{e,3}(t)$ with $2/3\pi$ mutual phase displacement and synchronization with the AC grid (if connected) are compared with constant thresholds V_h, with $h = 1, \ldots, M$ associated to each module. The $v_{e,i}(t)$ are defined as follows:

$$v_{e,i}(t) = V_e \sin(\omega t + \varphi_i + \varphi_e) \tag{1}$$

with $\varphi_i = 0, \ -2/3\pi, \ 2/3\pi$ for the considered phase $i = 1, \ 2, \ 3$. φ_e can be set $\neq 0$ to provide a phase displacement between the grid voltage and the excitation signal: the aim is to obtain a regulation effect at the output terminals for the three operations. As will be shown later in this paper, the effect of variations on φ_e is similar to the one obtained controlling firing angles in thyristor bridges. Moreover, the duty cycle of the modules can be varied by changing the peak value V_e. Since $v_{e,i}(t)$ is a quantity that acts only in the modulation algorithm and represents a normalized version of the AC voltage acting on phase i, V_e and all the V_h are interpreted as pure numbers in this paper.

Based on the result of the comparisons, a couple of switches on each module are activated at a time. Three states are allowed on a module: direct, reverse and bypass, as shown in Figure 3. The direct configuration provides a connection between AC and DC terminals such that the positive half-sine wave of AC signals is brought on DC terminals on each module during rectifier mode. Analogously, the same switch arrangement is exploited to synthesize the positive half-waveform of the AC quantities in inverter mode. Reverse state is similar to the direct one, but with a flipped connection of the AC and DC terminals. Therefore, the negative side of sine waves are mirrored with respect to the x-axis and reported on the DC terminals during rectifier operations. Instead, negative side of AC waveforms are generated using reverse state in inverter operation mode. Finally, bypass sate is a short-circuit of the DC terminals and, in principle, it should be used both to shape the AC quantities and to control the power flowing through the device.

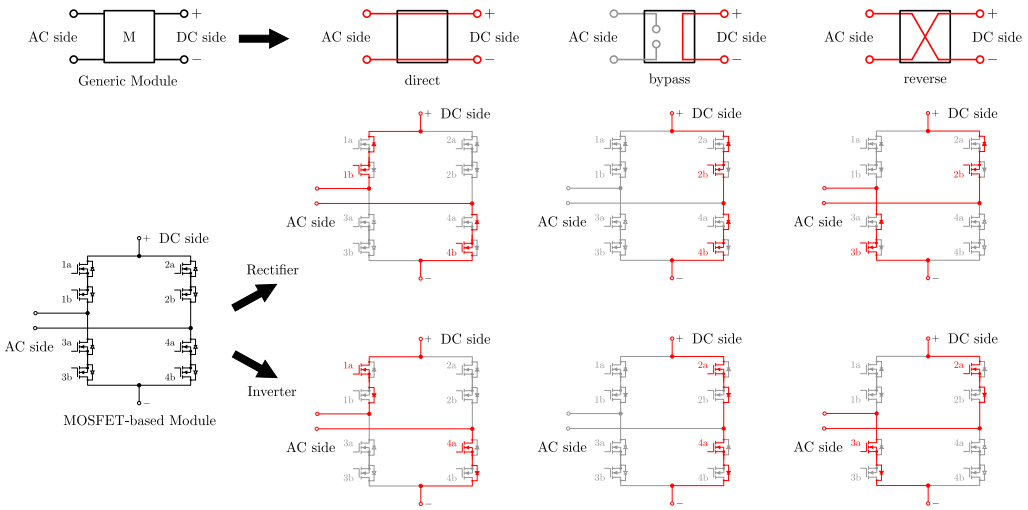


Figure 3. Allowable states of the modules (direct, bypass and reverse) and their realization in rectifier and inverter operations. Switches are here represented as short, open circuits and as MOSFETs. Red colors identifies paths where switches are turned on and, thus, on which the current can flow.

These three states are applied sequentially according the switching table reported in Table 1. This schedule is configured to include small ranges δ to allow for smooth transitions

between direct, inverse and bypass states, if needed. Namely, three switches are on for a short period of time to prevent abrupt transients between two following states. It can also be noted that all the switches are off in idle mode and the current circulation is prevented in any direction. Figure 4 reports an example of a comparison between a generic $v_{e,i}(t)$ and constant threshold V_h with $\delta = 0$ and $\varphi_e = 0$ to show how the modulation is operated. It can be observed that modules can be stressed differently based on the specific value of V_h associated to each of them. To provide a better exploitation of the power electronics, dynamic permutations of these constant values over the modules can be realized.

Table 1. Switching table of single modules on phase i based on NLC considering a generic constant threshold V_h. Values equal to 1 mean on switch, whereas 0 stands for off switch.

Operation	G_a	G_b	v_e Range	1a	1b	2a	2b	3a	3b	4a	4b	State
idle	0	0	$V_e \geq v_{e,i}(t) \geq -V_e$	0	0	0	0	0	0	0	0	idle
rectifier	0	1	$v_{e,i}(t) > V_h + \delta$	0	1	0	0	0	0	0	1	direct
rectifier	0	1	$V_h + \delta \geq v_{e,i}(t) > V_h - \delta$	0	1	0	1	0	0	0	1	transition
rectifier	0	1	$V_h - \delta \geq v_{e,i}(t) > -V_h + \delta$	0	0	0	1	0	0	0	1	bypass
rectifier	0	1	$-V_h + \delta \geq v_{e,i}(t) > -V_h - \delta$	0	0	0	1	0	1	0	1	transition
rectifier	0	1	$v_{e,i}(t) \leq -V_h - \delta$	0	0	0	1	1	0	0	0	reverse
inverter	1	0	$v_{e,i}(t) > V_h + \delta$	1	0	0	0	0	0	1	0	direct
inverter	1	0	$V_h + \delta \geq v_{e,i}(t) > V_h - \delta$	1	0	1	0	0	0	1	0	transition
inverter	1	0	$V_h - \delta \geq v_{e,i}(t) > -V_h + \delta$	0	0	1	0	0	0	1	0	bypass
inverter	1	0	$-V_h + \delta \geq v_{e,i}(t) > -V_h - \delta$	0	0	1	0	1	0	1	0	transition
inverter	1	0	$v_{e,i}(t) \leq -V_h - \delta$	0	0	1	0	1	0	0	0	reverse
idle	1	1	$V_e \geq v_{e,i}(t) \geq -V_e$	0	0	0	0	0	0	0	0	idle

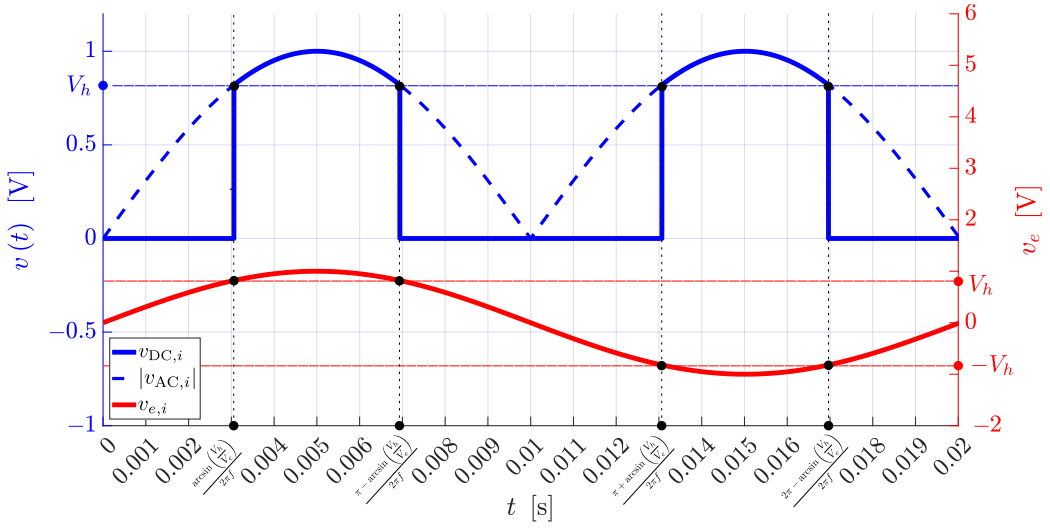


Figure 4. Ideal behavior of the rectified DC voltage on the h-th module (solid blue curve), and the corresponding comparison between $v_{e,i}(t)$ and V_h (red curves with $\delta = 0$, $\varphi_e = 0$) [32].

2.3. Analytical Model of the Devices

Simple equations can be derived to link AC quantities with the DC ones for rectifier and inverter operations. In case CTs are used as DC/DC converters, the same equations can be cascaded to provide valid estimations. The easiest relationship that can be formalized is based on a dynamic transformation ratio $k(t)$ defined as follows:

$$k(t) = \sum_{h=1}^{M} \frac{Nc_h(t)}{N_p} \tag{2}$$

where c_h is a function of time (typically a combination of square waveforms) that depends on the specific state of the h-th module. Namely, it can assume the values $-1, 0, 1$ for reverse, bypass, direct states, respectively, assumed at the specific time instant t based on Table 1. N is the number of turns of each secondary winding (assuming all of them are equal) connected to the h-th module while N_p is the total number of primary turns. Hence, the primary voltage $v_{p,i}(t) = \sqrt{2}V_p \sin(\omega t + \varphi_i)$ and the DC voltage $v_{\mathrm{DC},i}(t)$ on each phase i can be linked as follows:

$$v_{\mathrm{DC},i}(t) = k(t) v_{p,i}(t) \tag{3}$$

In three-phase systems, the waveform of the overall DC voltage $v_{\mathrm{DC}}(t)$ can be computed as follows:

$$v_{\mathrm{DC}}(t) = \sum_{i=1}^{3} v_{\mathrm{DC},i}(t) \tag{4}$$

Namely, the combination of Equations (2)–(4) provides an indication of the harmonic content in the involved quantities, assuming that (1) the supply side is a pure sine-wave or a perfect constant, (2) the switching operations are ideal and (3) all the reactive elements in the system are negligible. It can be noted that this approach has many limitations. The most important one is that $k(t)$ is a piece-wise function and it may not be easy to manage when the number of modules is very large. From this observation, a simpler relationship between AC rms voltage and DC mean value can be formalized. To this aim, a rectifier operation of the CTs is assumed; thus, the starting point is the expression of the DC voltage $v_{\mathrm{DC1}}(t)$ associated to phase 1 (i.e., $\varphi_i = 0$) through a piece-wise function dependent on the threshold levels V_h, $h = 1, 2, \ldots, M$ and $\delta = 0$:

$$v_{\mathrm{DC},1}(t) = \begin{cases} \sqrt{2}V_s \sin(\vartheta) & \text{for } \varphi_e \le \vartheta \le \arcsin\left(\frac{V_1}{V_e}\right) + \varphi_e \\ 2\sqrt{2}V_s \sin(\vartheta) & \text{for } \arcsin\left(\frac{V_1}{V_e}\right) + \varphi_e < \vartheta \le \arcsin\left(\frac{V_2}{V_e}\right) + \varphi_e \\ \vdots & \\ M\sqrt{2}V_s \sin(\vartheta) & \text{for } \arcsin\left(\frac{V_M}{V_e}\right) + \varphi_e < \vartheta \le \pi - \arcsin\left(\frac{V_M}{V_e}\right) + \varphi_e \\ \vdots & \\ 2\sqrt{2}V_s \sin(\vartheta) & \text{for } \pi - \arcsin\left(\frac{V_2}{V_e}\right) + \varphi_e < \vartheta \le \pi - \arcsin\left(\frac{V_1}{V_e}\right) + \varphi_e \\ \sqrt{2}V_s \sin(\vartheta) & \text{for } \pi - \arcsin\left(\frac{V_1}{V_e}\right) + \varphi_e < \vartheta \le \pi + \varphi_e \end{cases} \tag{5}$$

where $\vartheta = \omega t = 2\pi f t$ with f the fundamental frequency of $v_{p,i}$ (i.e., 50 or 60 Hz), V_s is the rms value of the secondary voltage of the multi-winding transformer, which can be computed from the rms value of the primary voltage V_p and the constant turn ratio:

$$V_s = V_p \frac{N}{N_p} \tag{6}$$

Focusing on $v_{p,i}$ (which are the voltages applied on the terminals of the primary windings), they can be shifted and amplified with respect to the AC grid voltages v_i depending on the connection adopted at the primary terminals of the transformer (i.e., star, delta or zig-zag). Hence, no relationship involving v_i is investigated for simplicity in this paper. Considering the same system of equations, it is possible to write a relationship

between V_s and the mean value of DC voltage on each module, each phase and the whole DC bus as well. Indeed, starting from a piece-wise integration like the following one:

$$V_{\mathrm{DC}m,h} = \frac{1}{\pi}\int_{\arcsin\left(\frac{V_h}{V_e}\right)+\varphi_e}^{\pi-\arcsin\left(\frac{V_h}{V_e}\right)+\varphi_e} \sqrt{2}V_s \sin(\vartheta)\mathrm{d}\vartheta \tag{7}$$

it follows that:

$$V_{\mathrm{DC}m,h} = \frac{2\sqrt{2}}{\pi}V_s \cos(\varphi_e)\cos\left[\arcsin\left(\frac{V_h}{V_e}\right)\right] = \frac{2\sqrt{2}}{\pi}V_s \cos(\varphi_e)\sqrt{1-\left(\frac{V_h}{V_e}\right)^2} \tag{8}$$

Reminding the expression that links AC and DC voltages in ideal single-phase thyristor bridges [34]:

$$V_{d\alpha} = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} \sqrt{2}V_s \sin(\omega t)\mathrm{d}(\omega t) = \frac{2\sqrt{2}}{\pi}V_s \cos\alpha \tag{9}$$

It can be noted that every module in the CT works exactly in the same way: φ_e can be interpreted as the firing angle of an equivalent thyristor bridge, whereas the DC voltage is regulated through V_h. Coming back to equation (8), the overall mean DC voltage of the device can be written as follows:

$$V_{\mathrm{DC}m} = 3\frac{2\sqrt{2}}{\pi}V_s \cos(\varphi_e)\sum_{h=1}^{M}\cos(a_h) \tag{10}$$

with:

$$a_h = \arcsin\left(\frac{V_h}{V_e}\right) \tag{11}$$

Equation (10) can be reversed to find V_s as a function of $V_{\mathrm{DC}m}$, φ_e, V_e and the V_h values. This relationship holds in absence of any loss:

$$V_s = \frac{\pi}{6\sqrt{2}}\frac{V_{\mathrm{DC}m}}{\cos(\varphi_e)\sum_{h=1}^{M}\cos(a_h)} \tag{12}$$

Voltage drops on the adopted switches can be included as well to provide more realistic estimations of $V_{\mathrm{DC}m}$ and V_s. For example, assuming that MOSFETs are used:

$$V_{\mathrm{DC}m} = 3\left\{\frac{2\sqrt{2}}{\pi}V_s \cos(\varphi_e)\sum_{h=1}^{M}\cos(a_h) - \sum_{h=1}^{M}\left(2R_{\mathrm{ds,on_{MOS}}}I_{\mathrm{DC}m} + 2V_{\mathrm{fw_D}}\right)\right\} \tag{13}$$

where $R_{\mathrm{ds,on_{MOS}}}$ is the on resistance of the mosfets, $V_{\mathrm{fw_D}}$ is the forward voltage of the diodes and $I_{\mathrm{DC}m}$ is the average value of the DC current. The values of $R_{\mathrm{ds,on_{MOS}}}$ and $V_{\mathrm{fw_D}}$ can be extrapolated from the datasheet of the selected switches. Similarly, the relationship linking V_s to $V_{\mathrm{DC}m}$ becomes:

$$V_s = \frac{\pi}{6\sqrt{2}}\frac{V_{\mathrm{DC}m} - M\left(2R_{\mathrm{ds,on_{MOS}}}I_{\mathrm{DC}m} + 2V_{\mathrm{fw_D}}\right)}{\cos(\varphi_e)\sum_{h=1}^{M}\cos(a_h)} \tag{14}$$

It must be said that more accurate evaluations can be performed if the time-dependent current is considered instead of its mean value. In that case, $R_{\mathrm{ds,on_{MOS}}}$ and $V_{\mathrm{fw_D}}$ should be updated based on the current flowing on each switch and its corresponding temperature. Instead, Equations (13) and (14) exploit an average approach: at least two MOSFETs and two freewheeling diodes are always conducting in the whole period of AC quantities. However, the results are satisfactory and very simple to compute. In principle, losses related to the transformer can be included in the equation as well. The authors preferred to manage them separately and to deal with expressions involving power electronic components only.

Figure 5a shows an example of ideal waveform for $v_{DC,i}(t)$ with seven levels compared to the absolute value of the AC voltage with amplitude $M\sqrt{2}V_s$ and the quadratic sine having the same peak-to-peak value. Equation (5) holds also for the other two phases and it can be proved that the rectified voltage on the i-th phase $v_{DC,i}$ can be approximated with

$$v_{DC,i}(t) \approx M\sqrt{2}V_s \sin^2(\vartheta) \tag{15}$$

if $M \to \infty$. Figure 5b reports the ideal waveform $v_{DC}(t)$ obtained during a rectifier operation of the CT through the combination of the seven-level $v_{DC,1}(t)$, $v_{DC,2}(t)$ and $v_{DC,3}(t)$. It can be noted that the ripple is very limited even in the absence of any passive filter. Ideal behaviors for inverter operations are such that $v_{DC,1}(t)$, $v_{DC,2}(t)$ and $v_{DC,3}(t)$ are flipped with respect to the x axis every 10 ms. Thus, the ideal time evolution of $v_{s,1}(t)$, $v_{s,2}(t)$ and $v_{s,3}(t)$ is obtained.

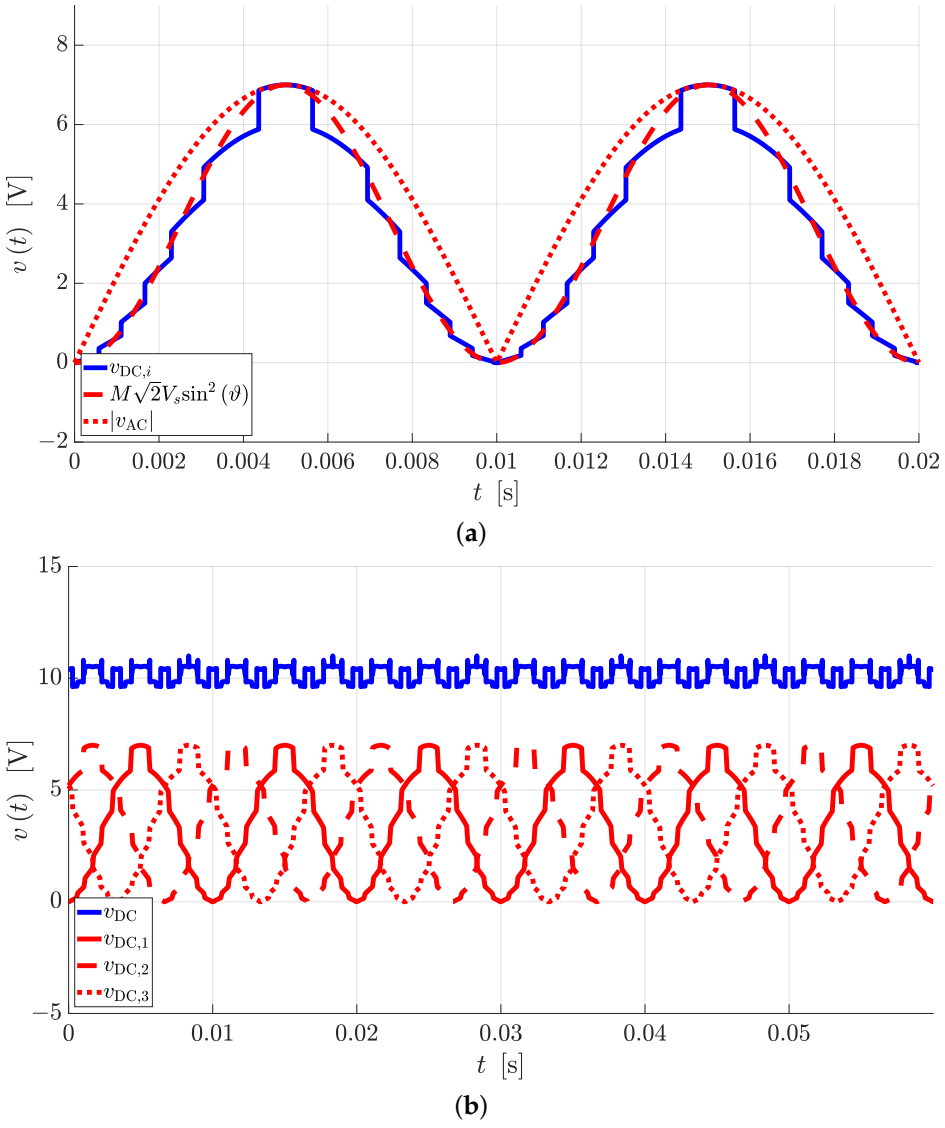


Figure 5. (**a**) Ideal behavior of the DC voltage $v_{DC,i}$ built on phase i and comparison with two possible approximations based on $|\sin(\omega t + \varphi_i)|$ and $\sin^2(\omega t + \varphi_i)$, with $v_s(t) = \sqrt{2}V_s \sin(\omega t + \varphi_i)$. (**b**) Ideal DC waveforms obtained during rectification operations [32].

2.4. Fault Clearance Strategy

The previous sections described the modulation and the ideal behavior of the device such that good rectifying and inverter performances are obtained. However, the peculiarity

of this family of devices is that they permit DC fault clearance using conventional AC protections when the CTs are operated as rectifiers or DC/DC converters. To this aim, zero crossings are introduced in DC waveforms by freezing $v_{e,i}(t)$, causing a stop in the rectification process, as shown in Figure 6a. Hence, AC voltages and currents are driven in the DC line if signals G_a and G_b are turned on and off accordingly. This feature makes it possible to try a fault clearance attempt in correspondence of the first zero-crossing of the DC current: in case the fault is still not extinguished, other opening operations can be carried out in the following zero crossings. An example of successful clearance at first zero crossing is shown in Figure 6b. It goes without saying that the CT operation with frozen $v_{e,i}$ cannot last too long, as the three phase side shows big unbalances and, possibly, may even behave as a two-phase system. Thus, this working mode is intended to last a few milliseconds only in case of faults on the DC side or for shutting the system down when working as rectifier or as a DC/DC converter. During inverter operations, DC faults are supposed to be solved by the rectifier converter placed on the other side of the line, assuming that the DC grid has no meshes. Indeed, simulations proved that the freezing strategy has no beneficial effects on DC fault clearance in such cases.

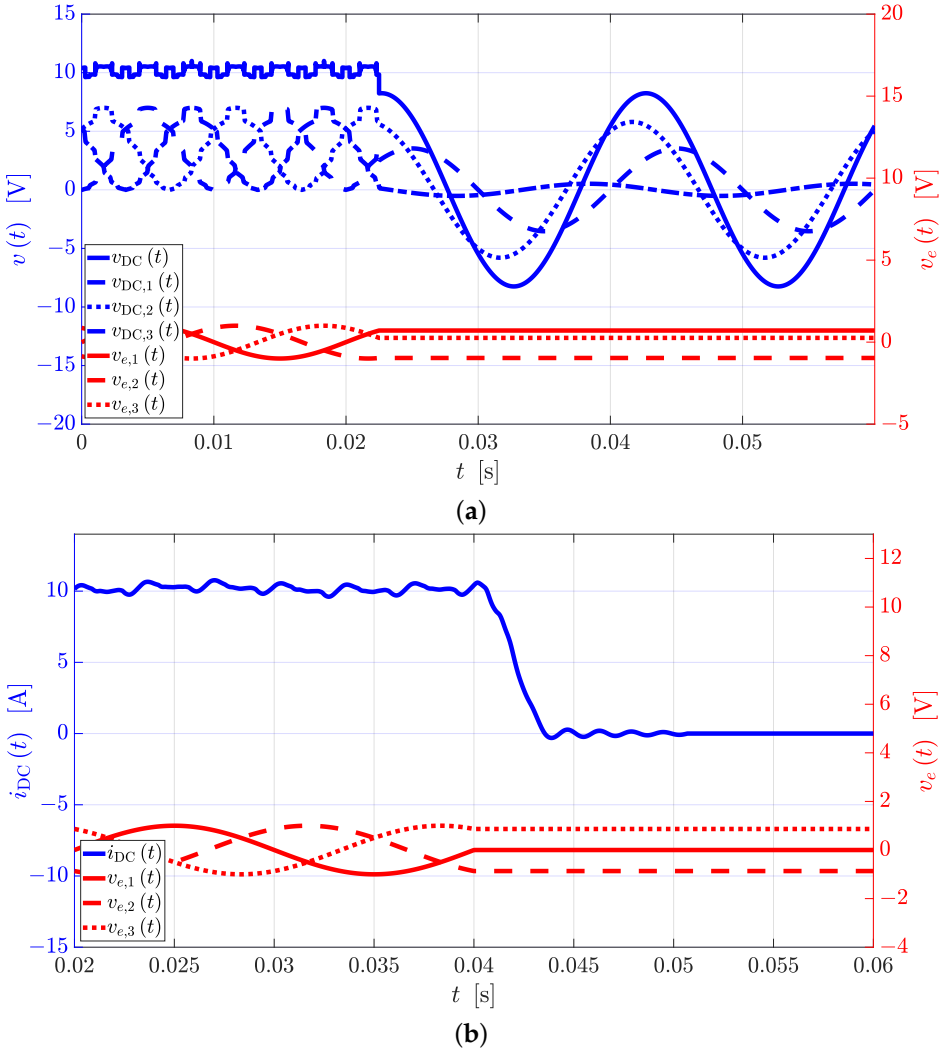


Figure 6. (**a**) Ideal waveforms obtained when the CT works as rectifier and the three $v_{e,i}(t)$ are frozen. The evolutions of $v_{DC,i}(t)$ depend on the time instant in which the variation in $v_{e,i}$ is stopped. (**b**) Example of failure clearance during a DC/DC operation [32].

3. Design and Switching Model of the Converter Transformer Prototype

In addition to the analytical equations shown in the previous section, the authors started to study a model capable of accurately representing all the elements acting in a CT. The aim was to use it for the design of a real low-voltage, low-power prototype for experimental activities and the prediction of its expected behavior during rectifier, inverter and DC/DC operations. Thus, the most immediate approach was to develop a fully detailed switching model in Simulink® including the power electronics, the multi-winding transformer and filters. This choice justifies observing the lack of preliminary knowledge on the behavior of this family of devices in terms of, e.g., loading effects, harmonic distortion and any proof of proper working of such converters.

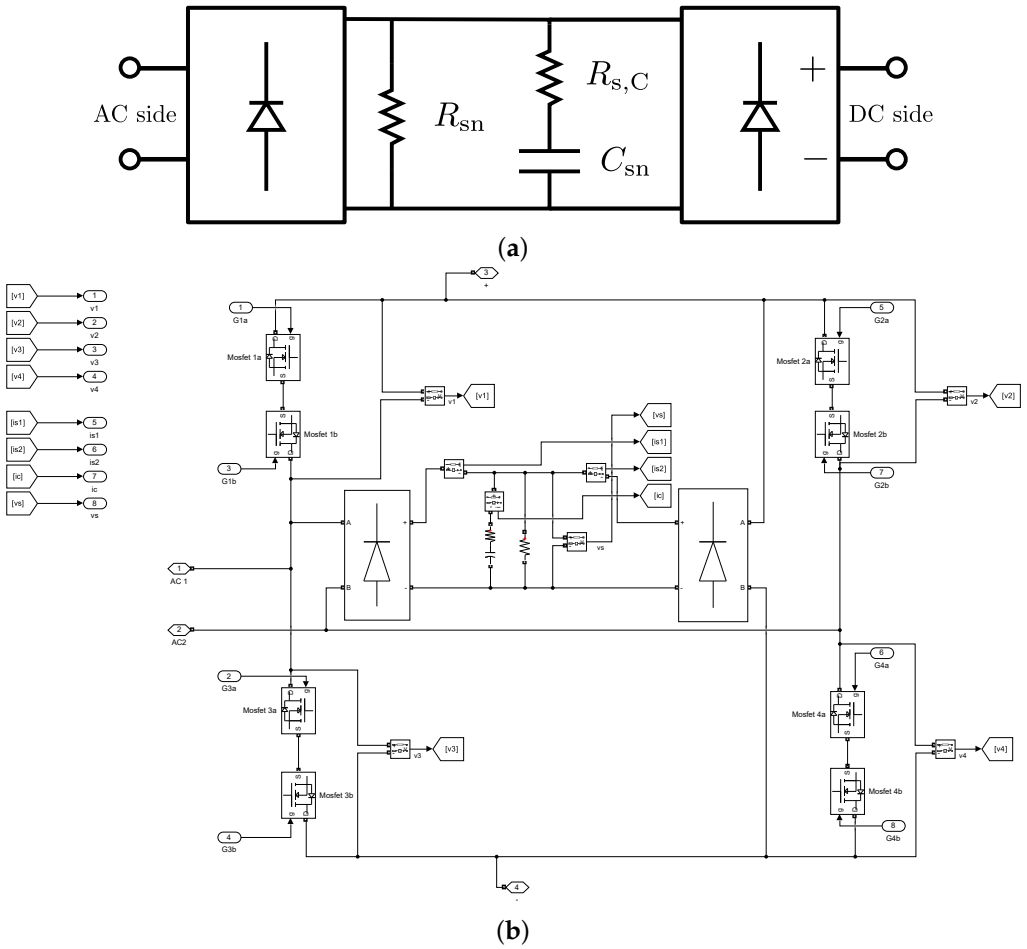


Figure 7. (**a**) Equivalent circuit of the snubbers installed on each module. (**b**) Realization of the module and its connection with the snubber in Simulink®.

The prototype should be a seven-level converter capable of working with $V_{DC,m} = 250\,V$, $V_{AC} = 230\,V$ rms phase value and it should have a rated power of $P_n = 1\,kW$. Therefore, the power electronics considered here is based on MOSFETs. The selected switches for the low voltage prototype are Infineon IRFS4229 [35]. The prototype and, thus, its model are configured with $7 \times 3 \times 2$ modules to allow for a rectifier, inverter and DC/DC converter operations with the same device. Therefore, the transformer should have two secondary sides with 21 windings each. It must be said that some simplifying hypotheses were applied to reduce the calculation burden and, thus, the simulation time due to the several non-linear characteristics of the scheme. Namely, the switching operations of the MOSFETs were considered as ideal, its $R_{ds,on_{MOS}}$ was set constant and equal to $50\,m\Omega$ and V_{fw_D} was actually modeled as a voltage drop on an equivalent resistance of $200\,m\Omega$. This approximation is rather precise at a rated current, whereas it may lead to overestimations of voltage drops

and losses at lower loading levels. Namely, the on-resistance of the MOSFET was selected slightly higher than recommended at 25 °C considering the high current rating of the chosen device. The equivalent diode resistance, on the other hand, was calculated starting from a forward voltage slightly lower than the expected one (0.7 V versus 0.8 V at 25 °C, showing decreasing $V_{\mathrm{fw_D}}$ with increasing junction temperature). Thus, $V_{\mathrm{fw_D}}$ is set equal to zero in the scheme, greatly improving simulation times and reducing the number of non-linearities of the model, albeit increasing the resistive behavior of the whole system. Key quantities can be predicted, such as input and output powers, average voltage and currents, conduction losses on the switches along with the stress on the semiconductors due to the currents and voltages they are subjected to. This approach deepened the comprehension of the device thanks to a great level of detail in the system, allowing for a precise preliminary sizing of a prototype. The main data related to the power electronics are reported in Table 2. The model of the modules reported in Figure 2 was augmented including a snubber circuit to damp possible transient due to switching operations on inductive currents. The selected snubber is shown in Figure 7a, where the two diode bridges avoid the discharge of the capacitor on the ports of the modules as well as any reverse polarity on *C*. Figure 7b shows how each module was realized in Simulink®. This subsystem receives the gate signals for every switch in input and it outputs some measurements. It also provides electrical connections with the AC and DC ports. It is worth mentioning that the gate signals driving the power electronics are obtained through logic operations and comparators based on G_a, G_b, $v_{e,i}(t)$ signals and constant V_h according to Table 1. The V_h values were selected setting $V_{\mathrm{DC}m} = 250\,\mathrm{V}$ based on the ideal Equation (10) and $V_s = 17\,\mathrm{V}$ (see Table 3). The selected secondary rms voltage is a consequence of the turn ratio selected for the transformer and the Δ connection adopted on the primary side. Moreover, $\delta = 0.02$ was adopted.

Table 2. Approximated constant on and diode resistance based on Infineon RFS4229 datasheet [35] and snubber parameters set in simulation.

Mosfet on-Resistance [mΩ]	Diode Resistance [mΩ]	Snubber Resistance [kΩ]	Snubber Capacitance [mF]
50	200	2	2

Table 3. Threshold values V_h adopted in the switching model. V_1 and V_7 were slightly modified to allow for transitions ranges with $\delta = 0.02$.

V_1	V_2	V_3	V_4	V_5	V_6	V_7
0.98	0.78	0.63	0.52	0.34	0.17	0.02

A similar level of detail can be achieved for the transformer model, namely couplings between the secondary windings are considered. Its structure is symmetrical and organized into phase equivalent subsystems like the one reported in Figure 8. Each phase is composed of the same topology with winding resistances, leakage reactances, mutual couplings and magnetizing branches so that transients, ripple and harmonic content can be estimated.

It can be noted that the circuit elements are placed in a per-unit-turn area, where the ideal transformers on each side have a turn ratio equal to $N_p : 1$ or $1 : N$ depending on whether they are primary or secondary windings. Thus, the inductances reported in this part of the circuit can also be interpreted as permeances. For practical reasons, 14 secondary coils per phase were included using a mutual inductor block to account for couplings among them. The transformer parameters were estimated starting from measurement on the device mounted on the real prototype. The secondaries are organized in shells placed radially around the iron core of three or four windings, each in the real system. Thus, the first group of seven secondaries are placed on the first two layers, whereas the windings involved in the DC/DC converters belong to the third and fourth shells. This solution is a compromise that made it possible to limit leackage flux during all the possible operations of the device. It must be noted that no separate core columns are foreseen for each secondary

winding. The realization of this machine should not be too different from the one of tap-changer transformer: the main peculiarity of this device is that all the secondary coils are isolated and the intermediate terminals are made accessible. No-load and binary short circuit tests (i.e., involving couples of windings) were carried out during the parameter identification. A linear approximation of the inductance and resistance of the magnetizing branches were estimated using a classical approach starting from no-load measurement at 50 Hz and full voltage. No core saturation was considered in this work. Instead, the short-circuit tests were performed at low voltage and allowed for the evaluation of

$$L_{sc} = L_{lk,h} + L_{lk,h+1} - 2M_{h,h+1} \tag{16}$$

where L_{sc} is the measured inductance value, $L_{lk,h}$ is the leakage inductance associated with winding h, $L_{lk,h+1}$ is the leakage inductance associated with winding $h+1$ and $M_{h,h+1}$ is the mutual inductance existing between them. The values used in the model were estimated using a constrained least square approach; that is, the values had to be compliant with equations like (16) describing the measurement process and with the constraint of the determinant of north-west minors of the overall inductance matrix (representing the mutual inductor block shown in Figure 8) greater than zero. Finally, the values of the resistances on the series branches were estimated observing that the windings were connected in series in binary tests. Table 4 reports the main data of the device. Filters were included in the system on both AC and DC sides regardless to ensure a total harmonic distortion (THD) of the AC quantities in the order of 5 % or lower and a small ripple on the DC side. Their values can be found in Table 5. The overall model is capable of simulating transient and steady-state simulations, involving power transfers from source to load and between grids. It must be said that, in the absence of any control algorithm and given the preliminary simulations required in this phase of the research, only scenarios involving power transfer on passive loads were investigated.

Table 4. Main characteristics of the transformer. Due to its complex structure, series parameters (not reported here) are not equal in each winding and phase.

	Primary	**S1**	**S2**
Number of turns	268	12×7	12×7
Rated Voltage [V]	230, 380 Y, D	17×7	17×7
Rated Current [A]	4, 2.34 Y, D	4.3	4.3
Magnetizing permeance [mH]	0.0441, 0.0516, 0.0358 (phases 1, 2, 3)		
Magnetizing resistance (primary side) [kΩ]	1.366, 2.736, 2.298 (phases 1, 2, 3)		
Rated frequency [Hz]	50		

Table 5. Low-pass filter sizes on AC and DC side.

	AC Side	**DC Side**
Filter capacitance [μF]	9.5	129
Filter Inductance [mH]	13.6	0.5

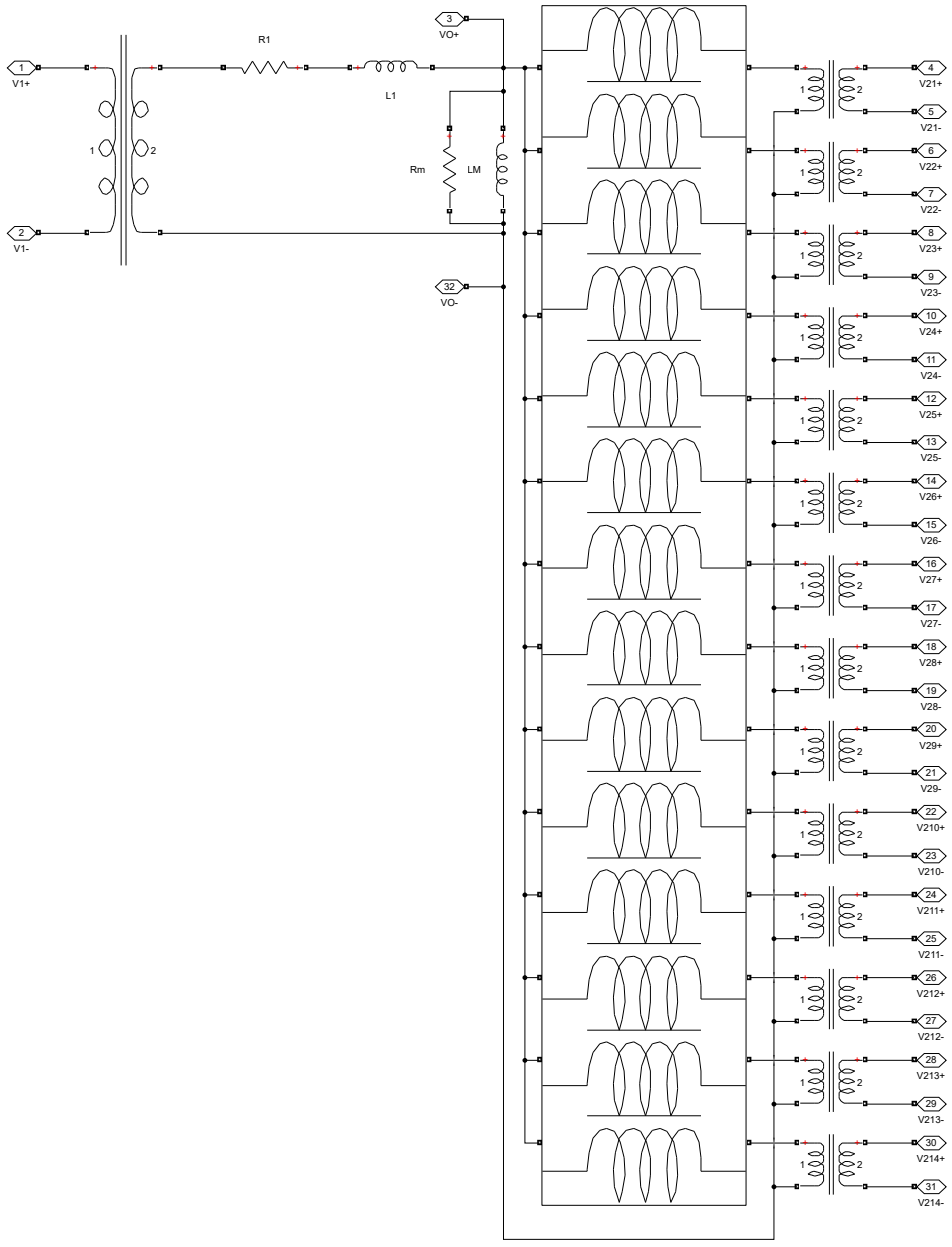


Figure 8. Equivalent phase circuit of the multi-winding transformer realized in Simulink®.

4. Simulation Results

This section is devoted to the report of some results obtained with the switching model described previously and that allowed for the prediction of the expected behavior of the real prototype working in all its possible operations (i.e., rectifier, inverter and DC/DC converter) (Tables 6–11, Figures 9–27). Different scenarios were considered. Namely, simulations of steady state, starting transients, turn off transients, $v_{e,i}(t)$ freezing, fault clearance and sensitivity analyses with respect to variations on V_e and φ_e were carried out for several loading conditions (resistive, ohmic-inductive and ohmic-capacitive loads as well as open-circuit and short-circuit at output terminals). Table 6 reports the parameters of the loading impedances.

Among all possible results, this paper shows the results obtained with ohmic-inductive loads on AC and DC sides. Finally, it is important to note that no closed loop control is developed at this stage of the research. Moreover, it is preferable to dig in the open loop

behaviour of new converters. During future research, the aim is to study and set a simplified model which should be a handy tool for designing and tuning controllers.

Table 6. AC and DC loads set in Simulink®: *RL* and *RC* loads show $\cos\varphi = 0.9$ on AC terminals.

AC Side					**DC Side**				
R	***RL***		***RC***		***R***	***RL***		***RC***	
R [Ω]	R [Ω]	L [mH]	R [Ω]	C [μF]	R [Ω]	R [Ω]	L [mH]	R [Ω]	C [μF]
158.70	142.83	220.20	142.83	46.02	62.5	62.5	96.4	62.5	105.2

4.1. Steady-State Simulations

Simulations are carried out supplying the system with voltage sources and studying the steady state of all the involved variables. The following results refer to the ohmic-inductive load only (see Table 6).

(1). Rectifier

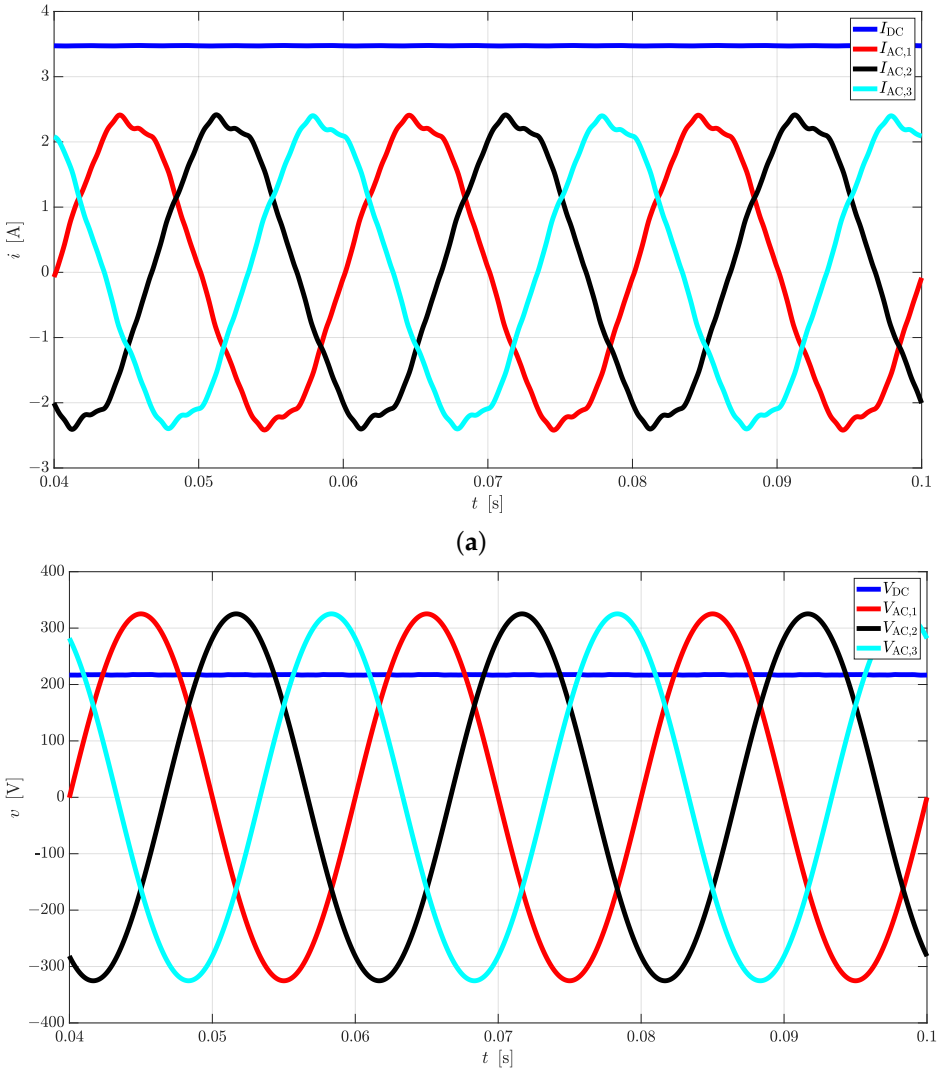


Figure 9. AC and DC (**a**) currents (**b**) and voltages at steady state obtained in simulations of the CT working as rectifier on *RL* load (see Table 6).

Table 7. AC quantities.

	$V_{AC,i}$	$I_{AC,1}$	$I_{AC,2}$	$I_{AC,3}$
RMS	230 V	1.66 A	1.66 A	1.66 A
THD	/	3.41%	3.43%	3.54%

Table 8. DC quantities (left), input and output powers and efficiency of the device (right).

	V_{DC} [V]	I_{DC} [A]	P_{in} [W]	P_{out} [W]	η
Mean	217.17	3.47	1143.5	754.59	0.66
Ripple	1.12	0.01			

(2). Inverter

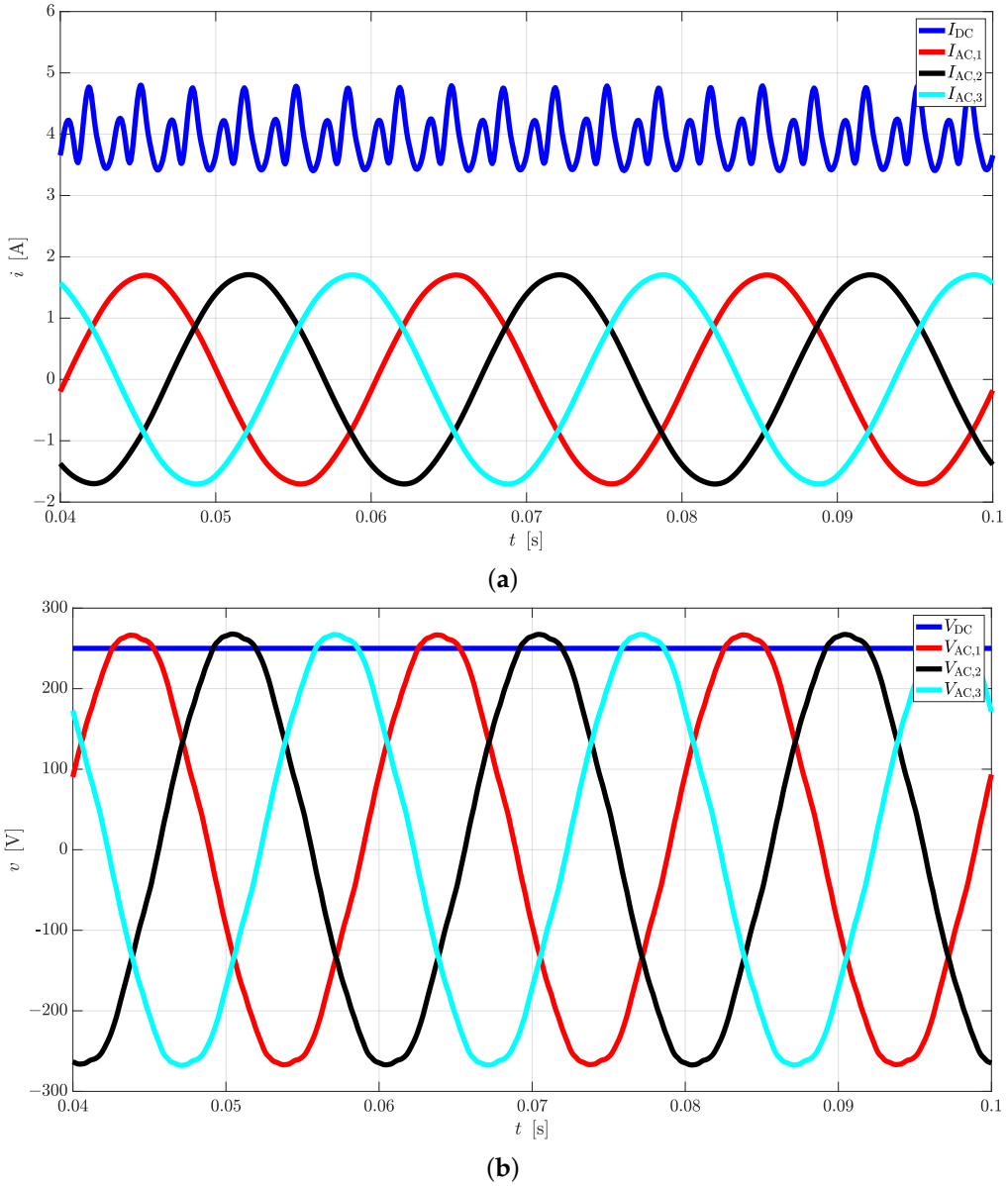


Figure 10. AC and DC (**a**) currents (**b**) and voltages at steady state obtained in simulations of the CT working as inverter on *RL* load (see Table 6).

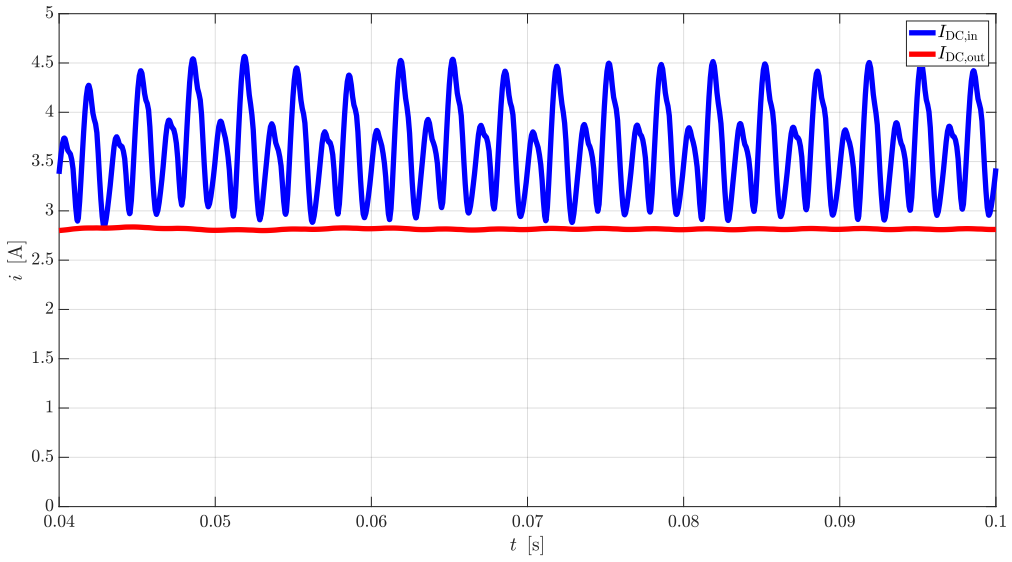
Table 9. AC quantities.

	$V_{AC,1}$	$V_{AC,2}$	$V_{AC,3}$	$I_{AC,1}$	$I_{AC,2}$	$I_{AC,3}$
RMS	190.99 V	191.63 V	191.41 V	1.20 A	1.21 A	1.21 A
THD	1.61%	1.58%	1.59%	0.55%	0.54%	0.55%

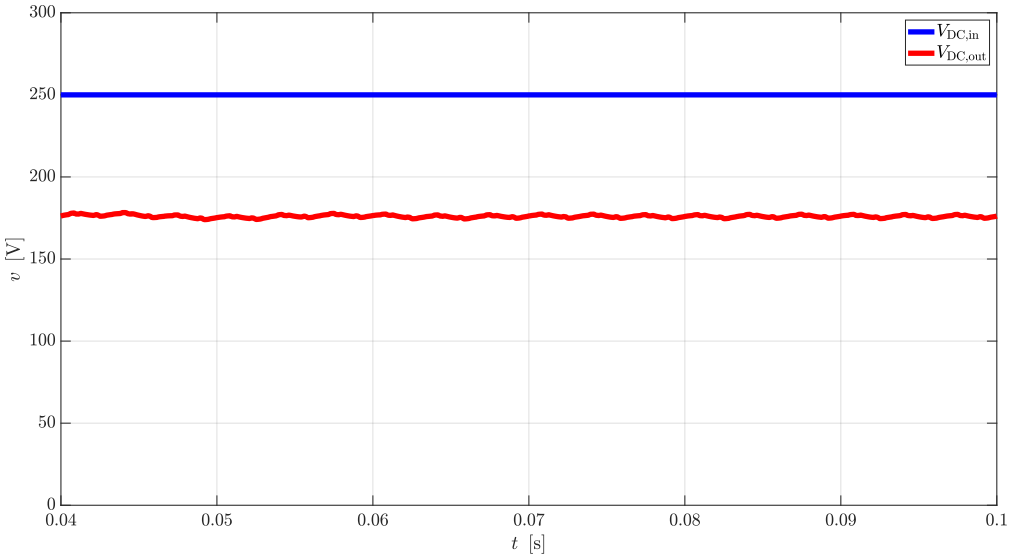
Table 10. DC quantities (left), input and output powers and efficiency of the device (right).

	V_{DC} [V]	I_{DC} [A]	P_{in} [W]	P_{out} [W]	η
Mean	250	3.96	989.04	622.59	0.63
Ripple	0	1.40			

(3). DC/DC Converter



(**a**)



(**b**)

Figure 11. AC and DC (**a**) currents (**b**) and voltages at steady state obtained in simulations of the CT working as DC/DC converter on *RL* load (see Table 6).

Table 11. DC quantities (left), input and output powers and efficiency of the device (right).

	$V_{DC,in}$	$I_{DC,in}$	$V_{DC,out}$	$I_{DC,out}$	P_{in} [W]	P_{out} [W]	η
Mean	250 V	3.63 A	176.01 V	2.82 A	907.84	495.65	0.55
Ripple	0 V	1.73 A	4.28 V	0.04 A			

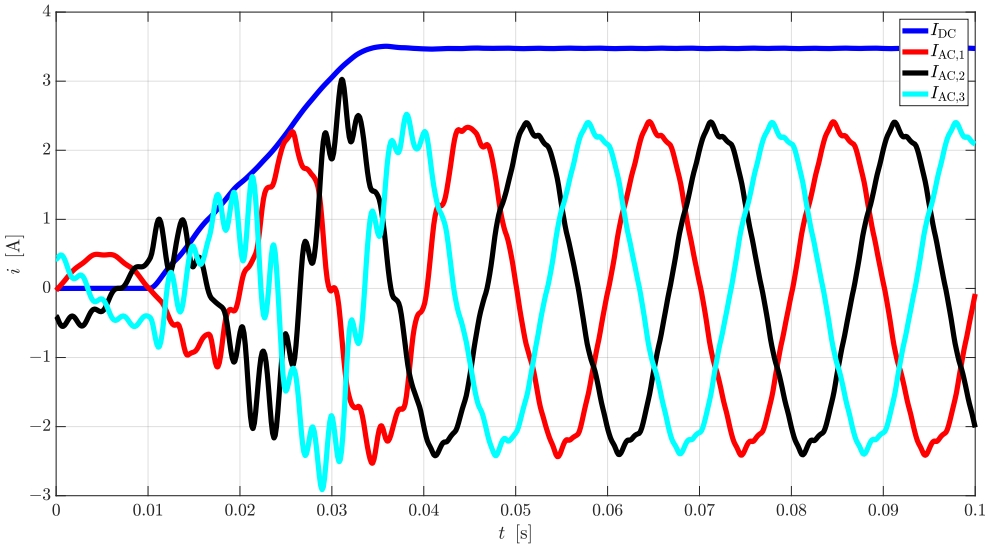
(4). Discussion on the Results

The results are satisfactory since the device behaves safely while respecting the limits set on THD for AC quantities and it is close to the predictions of Equations (13) and (14). The low efficiency is a consequence of the resistive approximation of the MOSFET and diode parameters. Moreover, the low-voltage nature of the device implies that the voltage drops on the power electronics and on the transformer (which has a resistive behavior due to its small size) have a big impact on V_{AC} and V_{DC} compared to MV and HV scenarios. Thus, CTs are expected to work more efficiently at higher voltage and power ratings.

4.2. Starting Transient Simulations

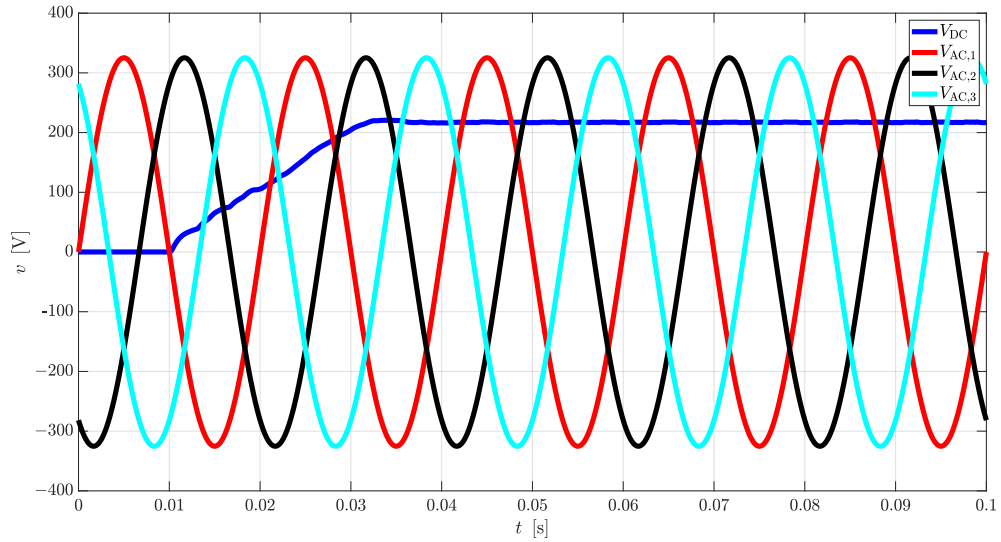
In these runs, converters are powered up from idle state to rated voltage differently depending on the specific operation. Namely, when the modules are working in rectifier mode, $V_{AC,i}$ are directly applied, whereas V_e is increased from 0 to 1 in 20 ms from $t = 10$ ms. During inverter mode, the DC voltage is assumed to be controllable and varied from 0 up to 250 V in 20 ms at $t = 10$ ms, while keeping $V_e = 1$. This scenario can be realized easily in the reality using a DC power supply in a laboratory. Moreover, this behavior is not too far from what happens in HVDC grids, considering that the DC voltage is typically realized through another controllable rectifier converter. In DC/DC converters, the ramps on V_{DC} and V_e are applied sequentially on the two groups of modules. Namely, the variation in the DC voltage is applied first at $t = 10$ ms with $V_e = 1$. Then, V_e is increased on the rectifier side at $t = 50$ ms. The results reported here in the following refer to a RL load (see Table 6).

(1). Rectifier



(a)

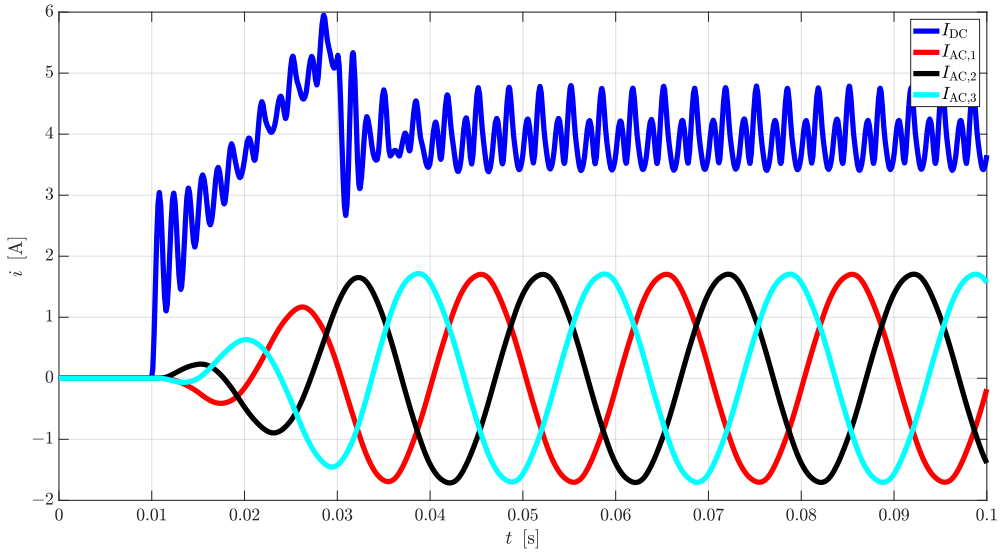
Figure 12. *Cont.*



(**b**)

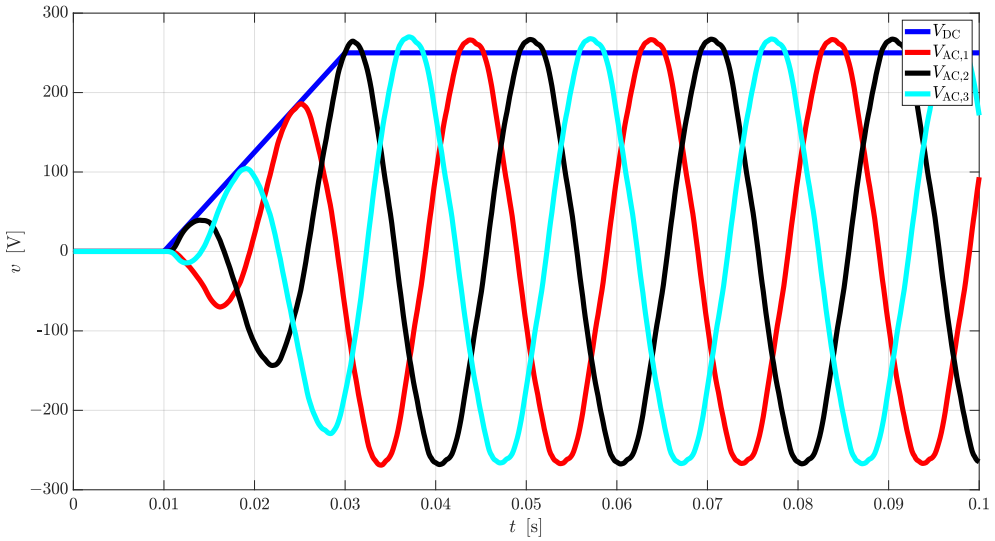
Figure 12. AC and DC current (**a**) and voltage (**b**) transients during switch-on simulations of CT working as rectifier on *RL* load (see Table 6).

(2). Inverter



(**a**)

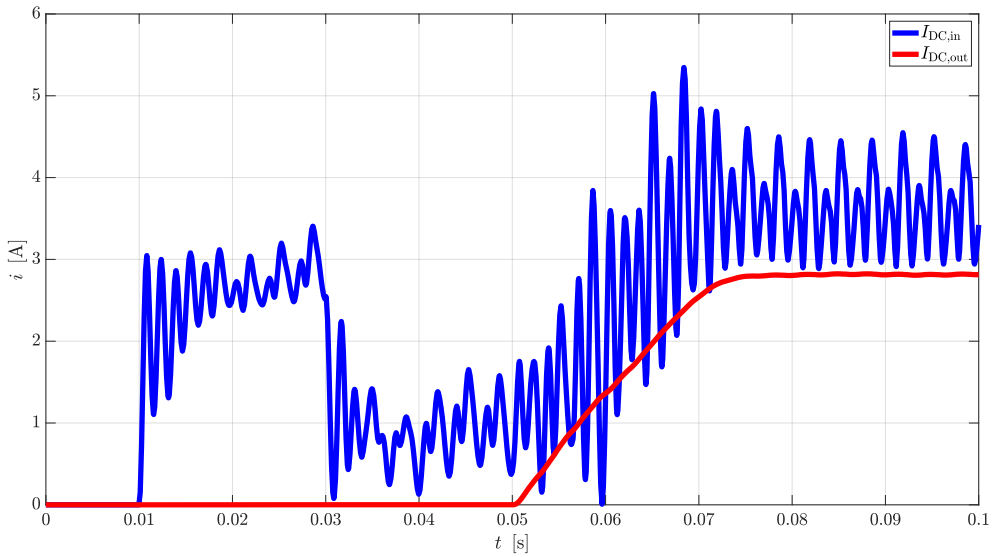
Figure 13. *Cont*.



(**b**)

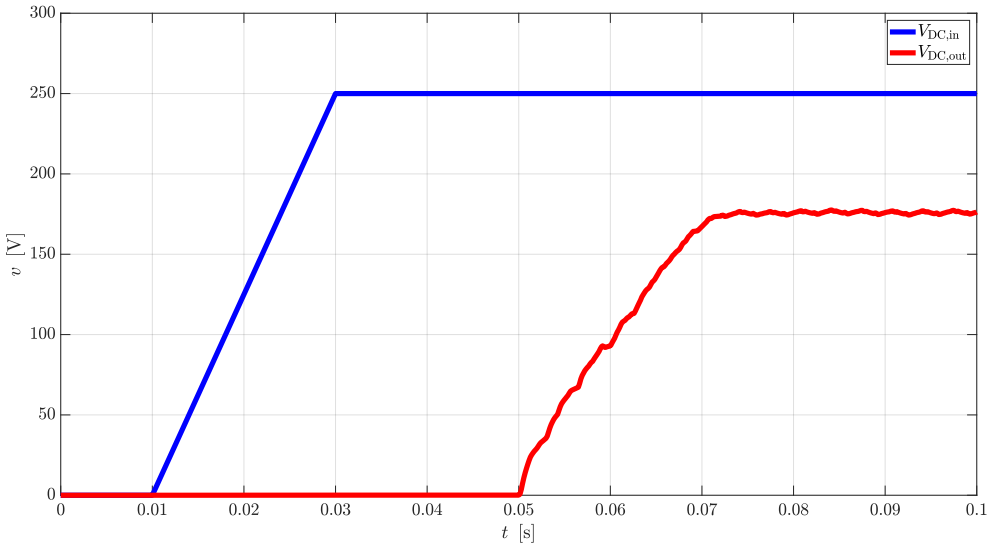
Figure 13. AC and DC current (**a**) and voltage (**b**) transients during switch-on simulations of CT working as inverter on *RL* load (see Table 6).

(3). DC/DC Converter



(**a**)

Figure 14. *Cont.*



(**b**)

Figure 14. Input and output DC current (**a**) and voltage (**b**) transients during switch-on simulations of CT working as DC/DC converter on *RL* load (see Table 6).

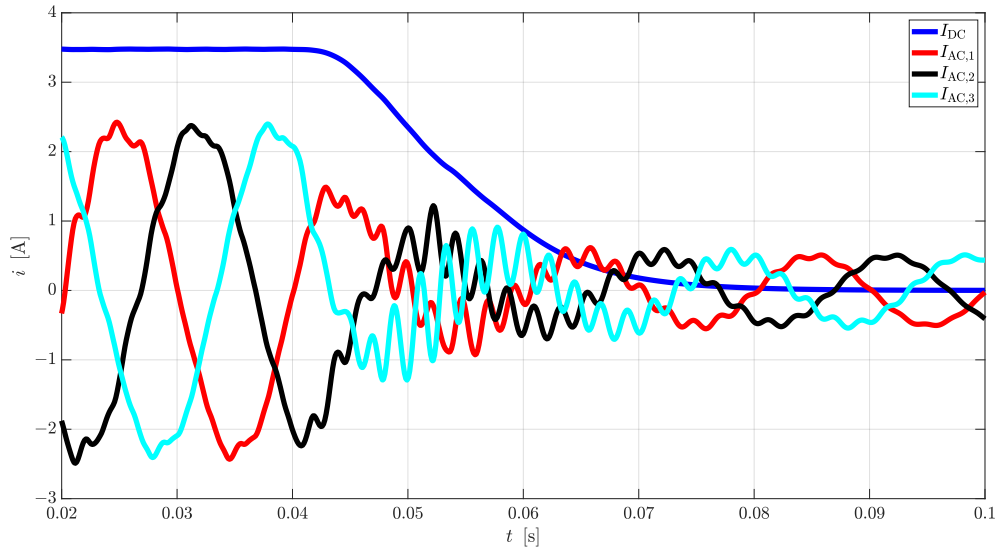
(4). Discussion on the Results

The strategies developed for powering the CT are acceptable since they do not cause overload lasting for a long time or any dangerous transient, despite the fact that the applied ramps are relatively fast. The inverter and converter are showing some peaks higher than 4 A, but they last sufficiently short not to have a big impact on the average value of the current.

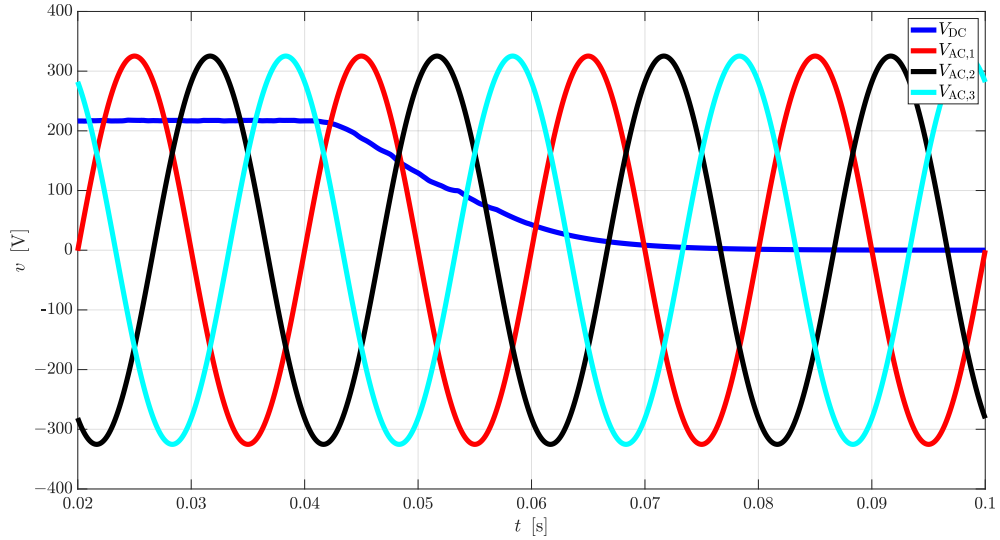
4.3. Turn-Off Transient Simulations

The virtual tests of this kind are aimed at studying strategies to zero or at least reduce AC and DC currents, thus making it possible to shut the device down safely. The procedures identified to this aim are the different for rectifier and inverter operations. During rectifications, V_e is brought down to 0 in 10 ms. After that, the current flowing on the DC side is zero, whereas $i_{AC,i}$ are strongly reduced. Therefore, an idle state can be set on the converter or either a circuit breaker can open both sides of the device. In inverter mode, circuit breakers can open the AC side during nominal load without any problem and, then, the converter can be brought to idle state. Finally, the suggested behavior for the DC/DC converter is similar to that one suggested for rectifier. Namely, V_e is reduced down to zero on the rectifier stage, making it possible to open both the DC sides at zero current and to drive the system in idle mode. It must be noted that idle mode should not be applied during operation of the device at full load as abrupt transients should appear in the system due to the presence of reactive components. All the switch-off operations start at $t = 40$ ms and decreasing ramps last 20 ms. The converter is always connected to a *RL* load (see Table 6).

(1). Rectifier



(**a**)



(**b**)

Figure 15. AC and DC current (**a**) and voltage (**b**) profiles during a transient simulation for shutting the CT down when operated as rectifier on *RL* load (see Table 6).

(2). Inverter

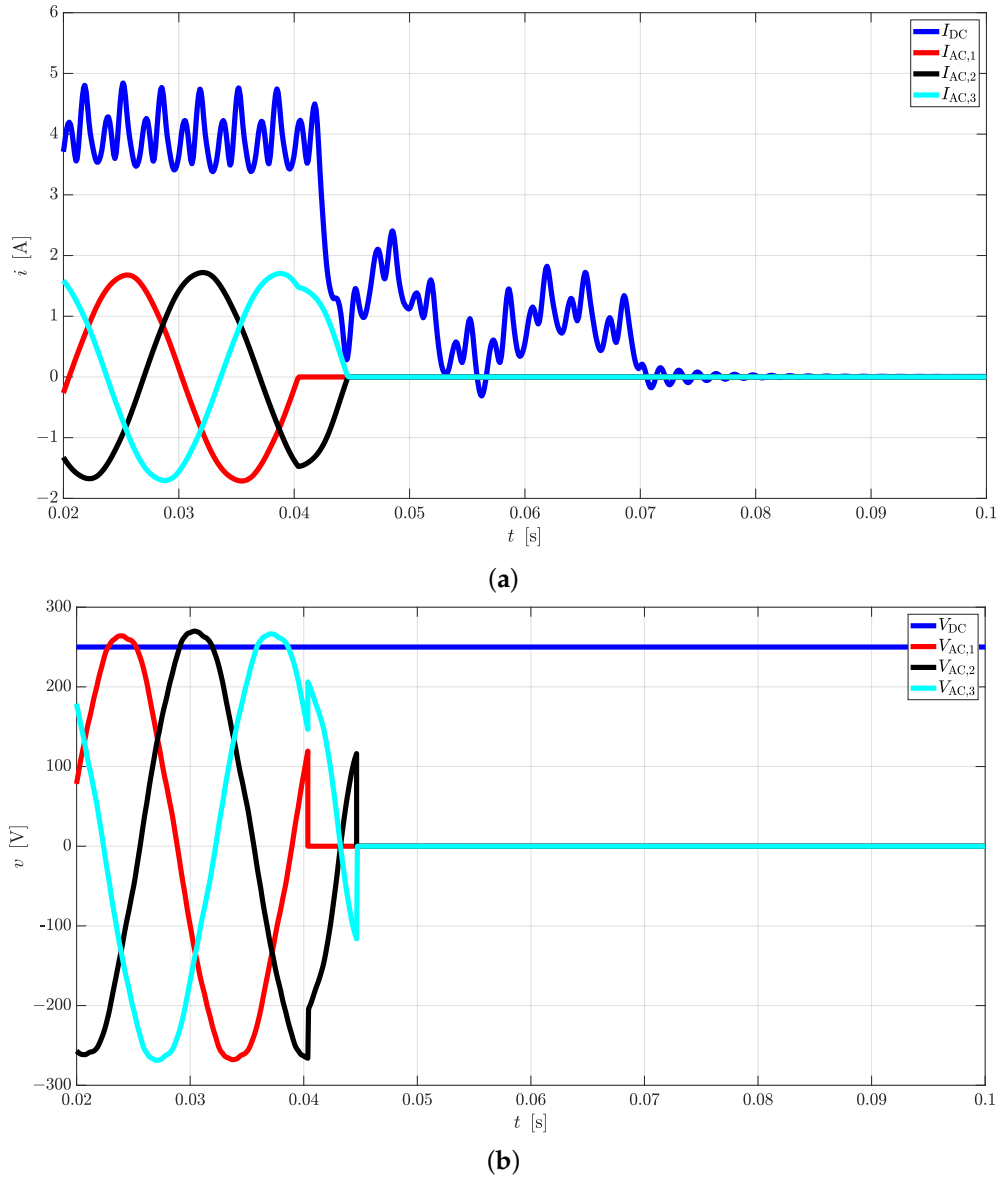


Figure 16. AC and DC current (**a**) and voltage (**b**) profiles during a transient simulation for shutting the CT down when operated as inverter on *RL* load (see Table 6).

(3). DC/DC Converter

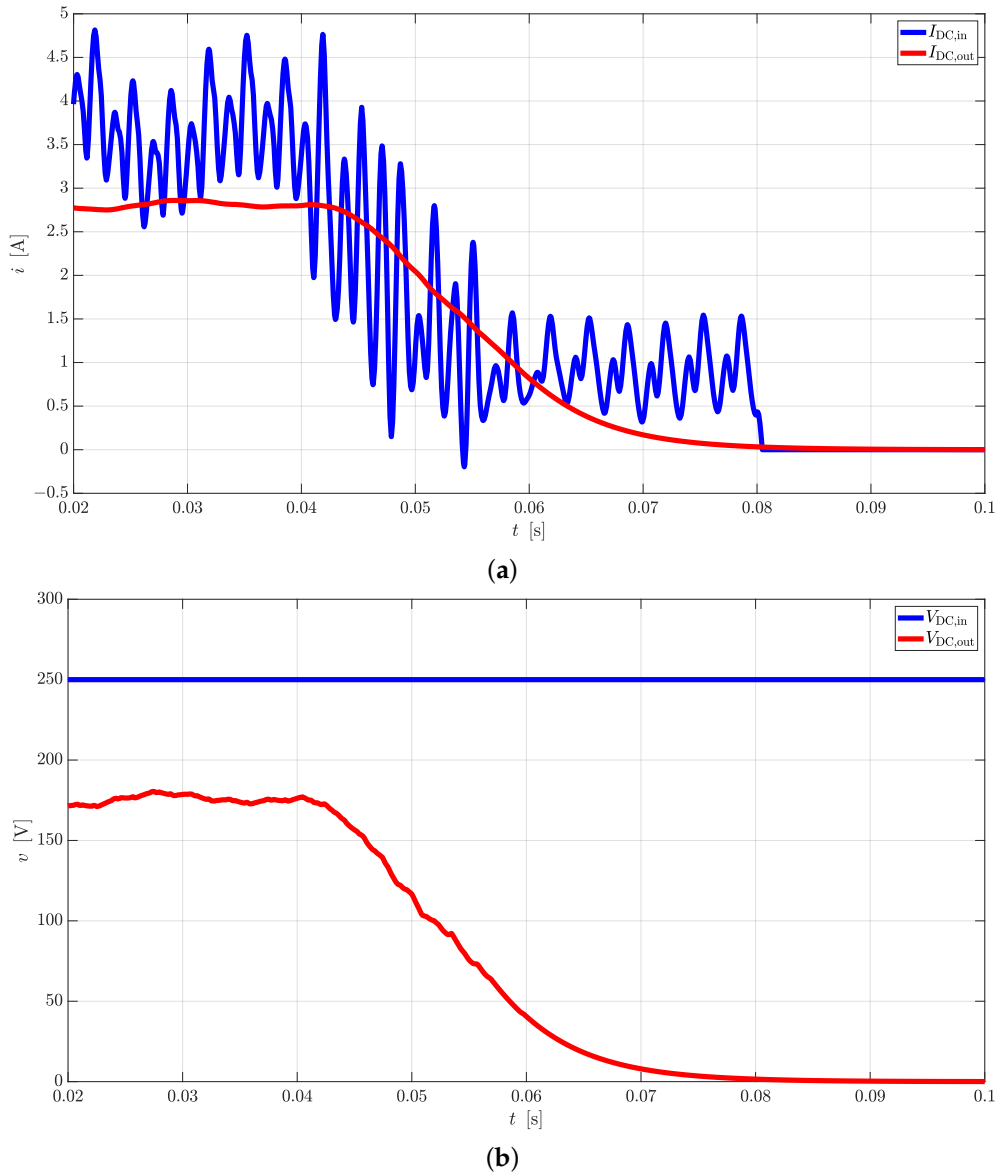


Figure 17. Input and output DC current (**a**) and voltage (**b**) profiles during a transient simulation for shutting the CT down when operated as DC/DC converter on *RL* load (see Table 6).

(4). Discussion on the Results

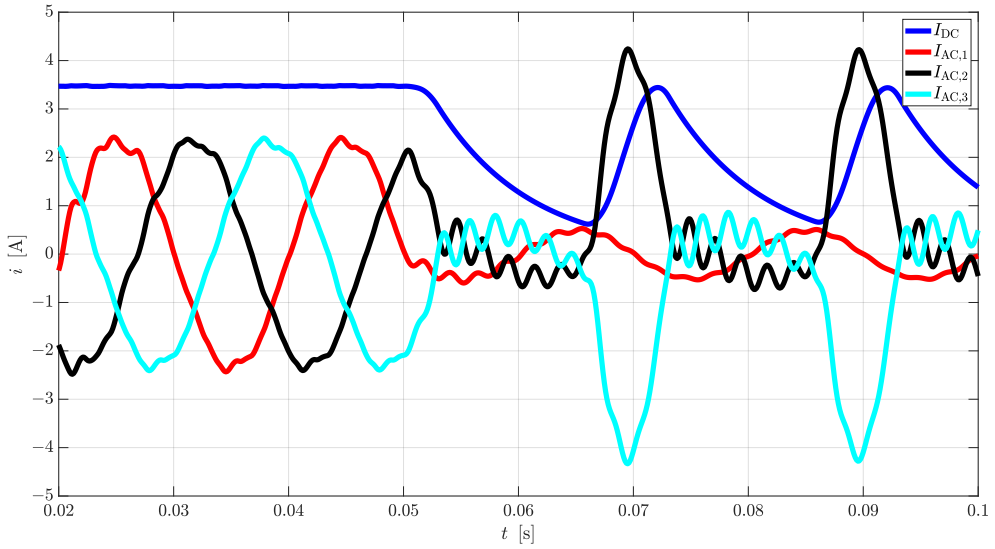
The profiles reported above do not show any dangerous transient and can bring the output current and voltage down to zero safely. Thus, the proposed turning-off strategies can be tested on the real prototype.

4.4. Reference Freezing Simulations

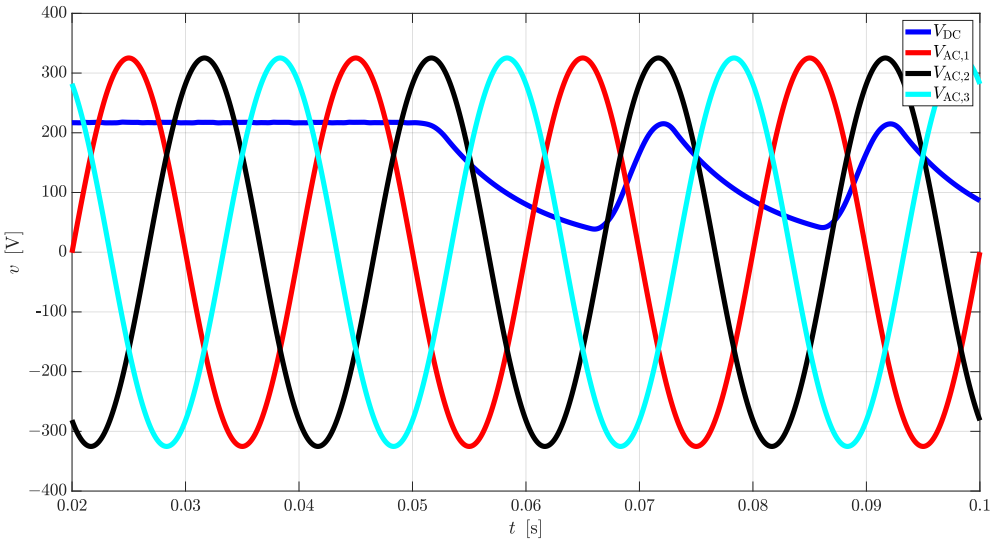
One of the peculiarity of the CT is its equivalent variable transformation ratio from AC to DC side. The results reported here in the following show what happens when $v_{e,i}$ are frozen, thus setting a constant transformation ratio between the two sides of the device. It is important to note that this strategy is dangerous during inverter operations, as transformers should not work in asymmetrical conditions, where homopolar components may arise. As previously stated in this paper, it can be seen that the AC side is strongly unbalanced and it may even behave as a two-phase system in unlucky occurrences. It can

be noted that the reference signals are frozen at 50 ms and hat the CT is connected to a RL load (see Table 6).

(1). Rectifier



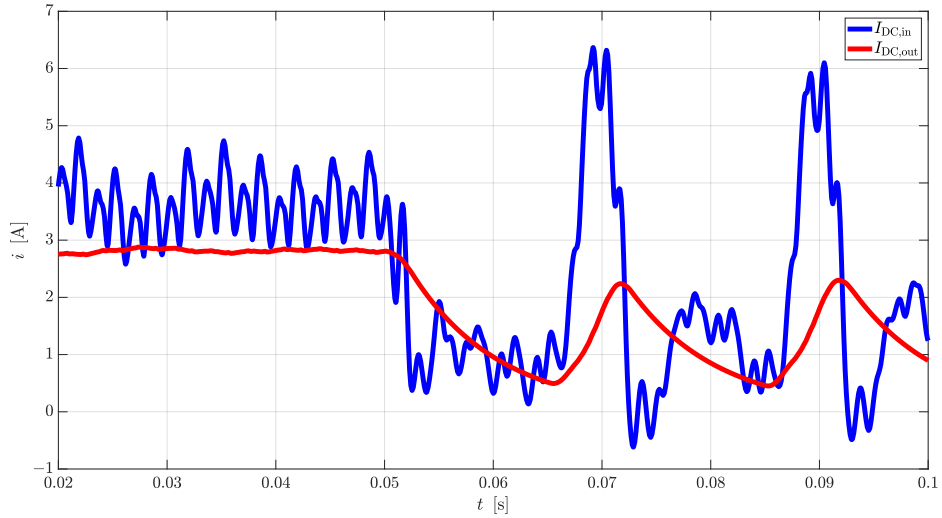
(**a**)



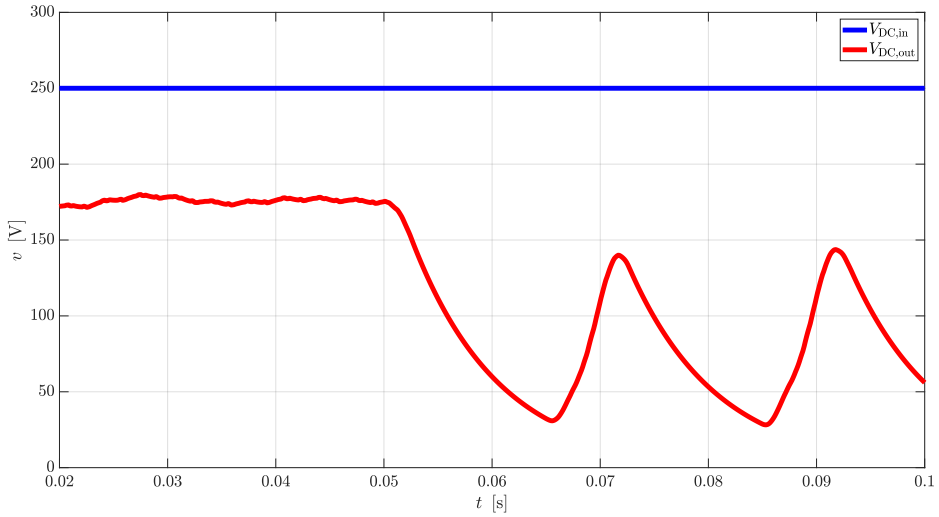
(**b**)

Figure 18. AC and DC current (**a**) and voltage (**b**) curves when $v_{e,i}$ are frozen and the CT operates as a rectifier on RL load (see Table 6).

(2). DC/DC Converter



(**a**)



(**b**)

Figure 19. Input and output DC current (**a**) and voltage (**b**) curves when $v_{e,i}$ are frozen and the CT operates as DC/DC converter on *RL* load (see Table 6).

(3). Discussion on the Results

These transients are obtained using the main peculiarity of the CT, which is its ability of freezing its equivalent transformation ratio between AC and DC sides. It is interesting to observe that virtual tests carried out on finite impedance cannot bring the DC current down to zero, whereas it is possible in case of short circuits. Therefore, to obtain intentional zero crossings on the DC line other methods (not described in this work) should be applied, such as the swap of values of G_a and G_b. As stated in Section 2.4, it can be noted that this particular operation cannot last too long, as the system is unbalanced on the AC side and high peaks of current can occur.

4.5. Fault Clearance Simulations

This section is devoted to simulations involving DC short-circuit current clearance using the ability of the converter in freezing $v_{e,i}$. Current is brought to zero in the DC side of the rectifier stages and, therefore, circuit breakers are operated in the correspondence of the first available zero crossing.

(1). Rectifier

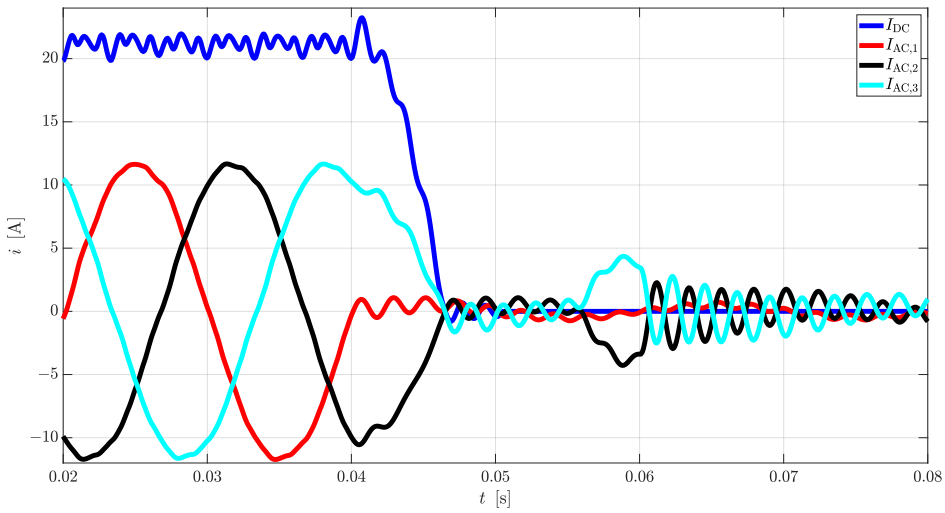


Figure 20. AC and DC currents plots during a DC fault clearance when the CT operates as a rectifier.

(2). DC/DC Converter

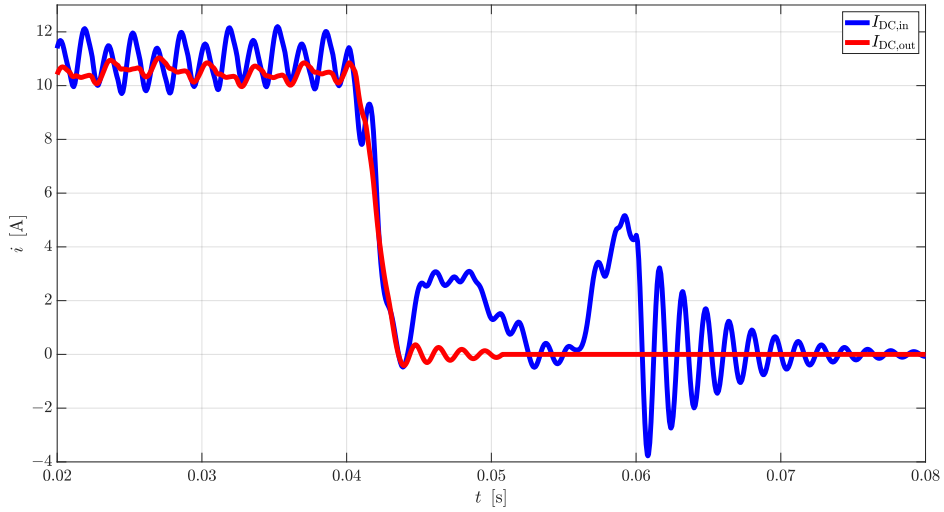


Figure 21. Input and output DC current plots during a DC fault clearance when the CT operates as a DC/DC converter.

(3). Discussion on the Results

The results reported in this subsection show the goodness of the proposed strategy for clearing DC faults during rectifier and DC/DC converter operations. Assuming that the CT is powering a short circuit, the current is brought down to zero and a circuit breaker opens the line. This operation can be applied every time the DC current has a zero crossing; hence, the same result can be achieved also when $v_e(t)$ is frozen on a finite load and the current is sent to zero using swapped G_a and G_b.

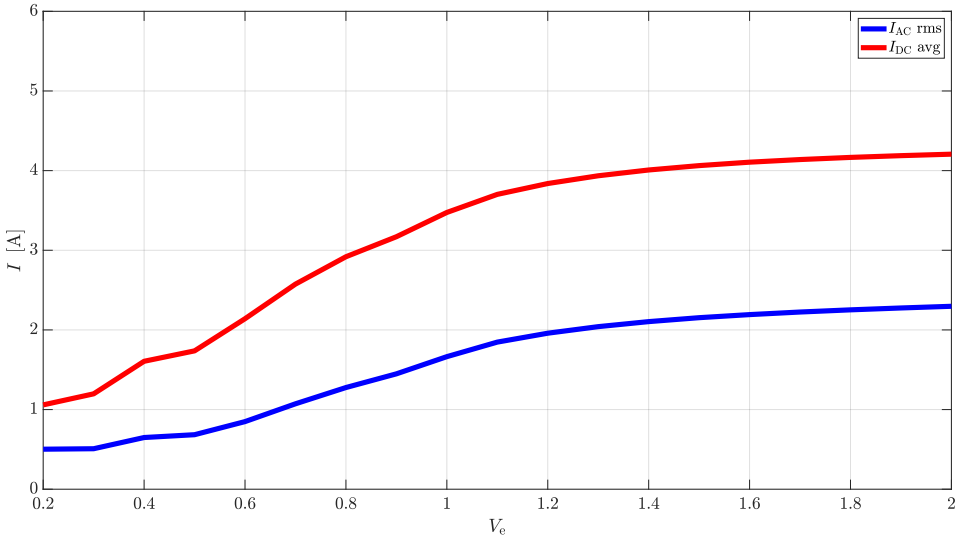
4.6. Sensitivity Analysis to Variations in the Reference Voltage

This last set of simulations is aimed at investigating the ability of the CT to control voltage and currents (hence, input and output powers) by acting on V_e and φ_e. Several steady state simulations were performed and the results are aggregated in the following plots. Two different scenarios can be set for the DC/DC converter, depending on whether the variation is performed on the rectifier or inverter side. It must be noted that the analysis

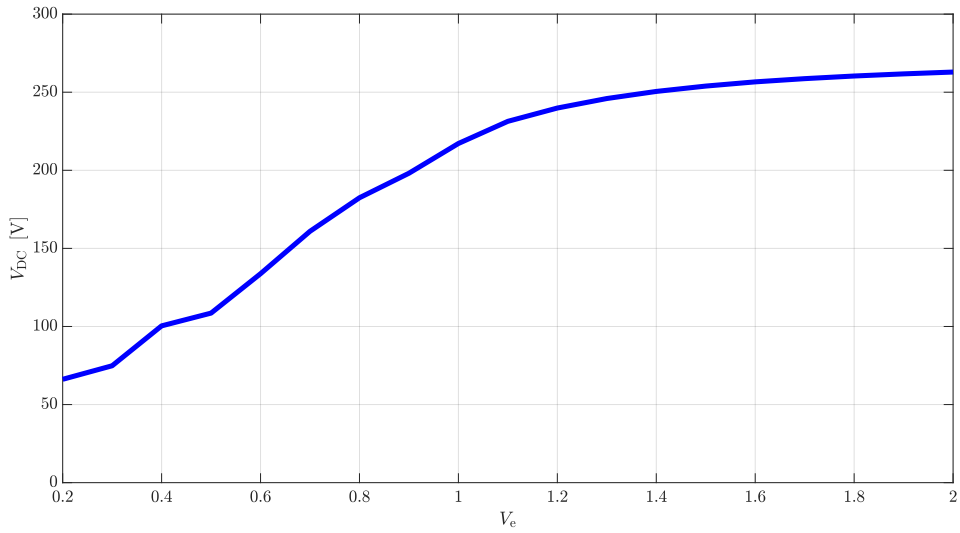
was not carried out for variations of φ_e in inverter stages since this would translate in a rigid shift of all the electric quantities on passive loads, without any additional information from the already performed steady-state runs. The results reported here in the following refer to converters working on *RL* loads (see Table 6).

4.6.1. Rectifier

Variations on V_e.



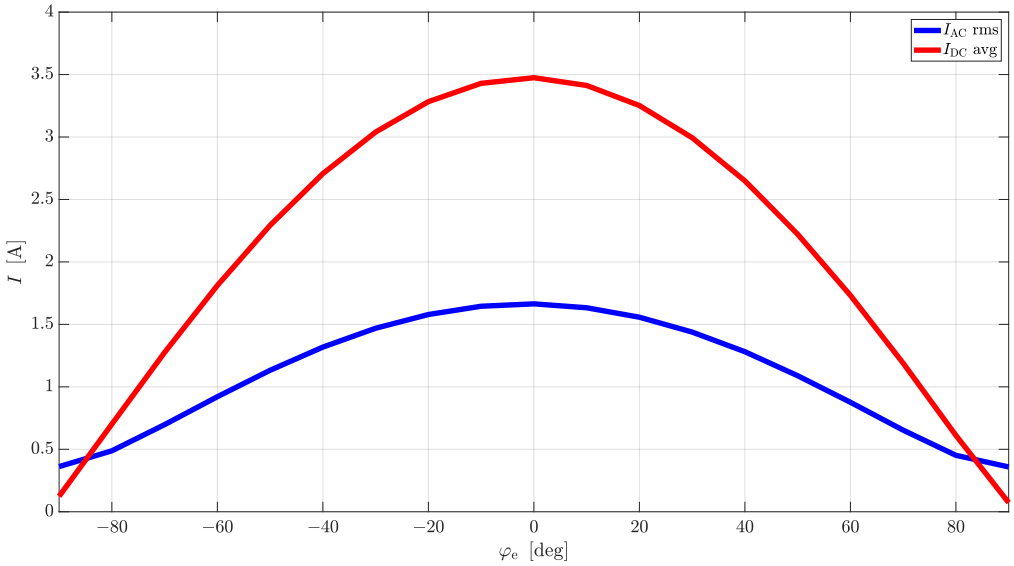
(**a**)



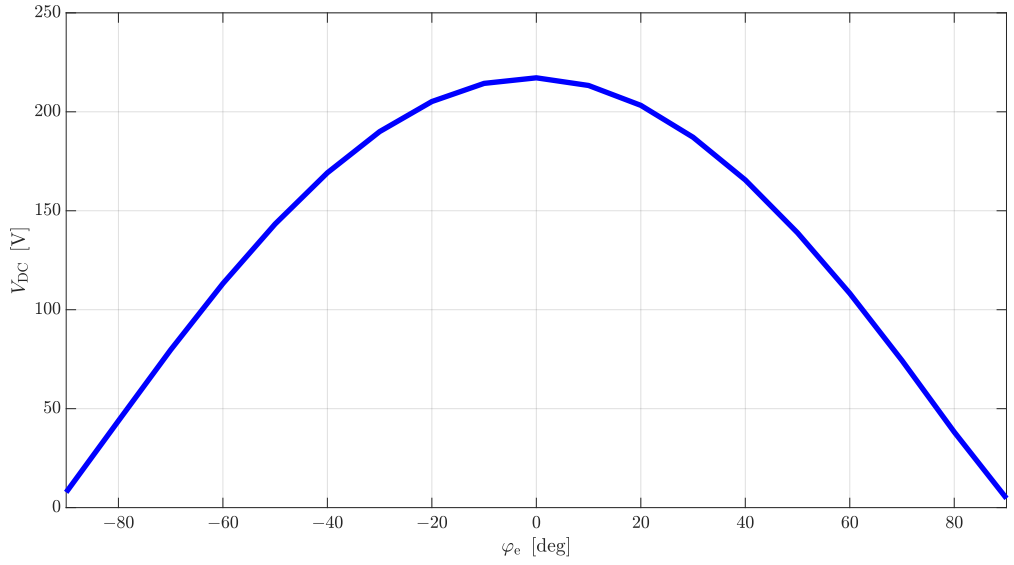
(**b**)

Figure 22. Dependency of input and output currents (**a**) and output voltage (**b**) to variations in V_e, when the CT operates as rectifier on *RL* load (see Table 6). DC quantities are expressed as average values, whereas AC ones as phase rms values.

Variations on φ_e.



(**a**)

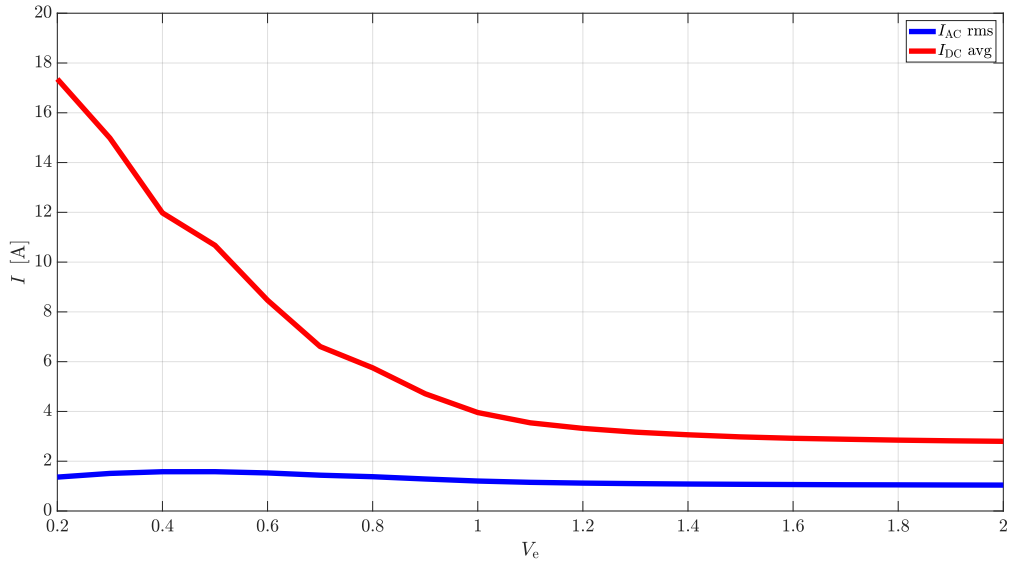


(**b**)

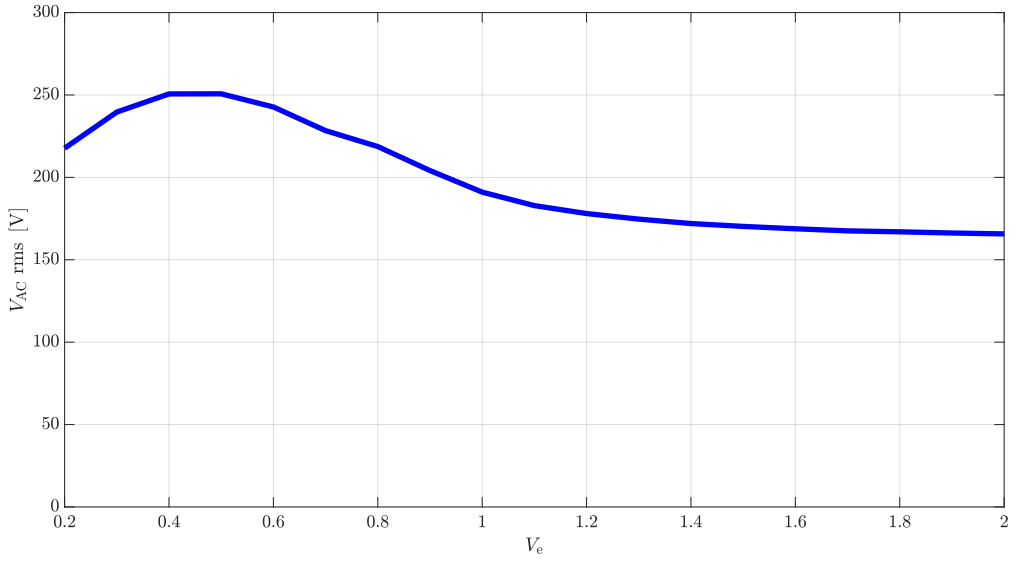
Figure 23. Dependency of input and output currents (**a**) and output voltage (**b**) to variations in φ_e, when the CT operates as rectifier on *RL* load (see Table 6). DC quantities are expressed as average values, whereas AC ones as phase rms values.

4.6.2. Inverter

Variations on V_e.



(**a**)

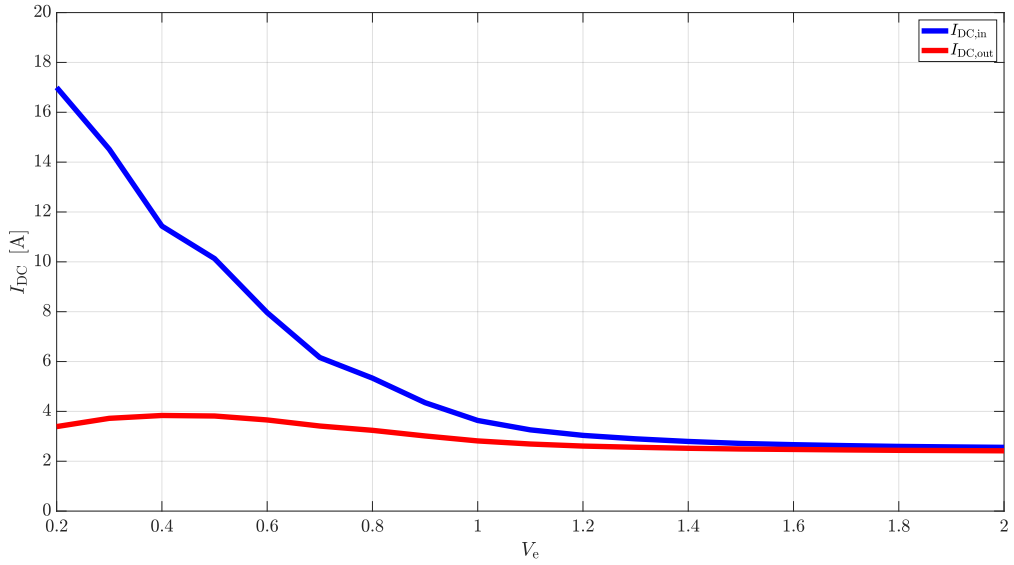


(**b**)

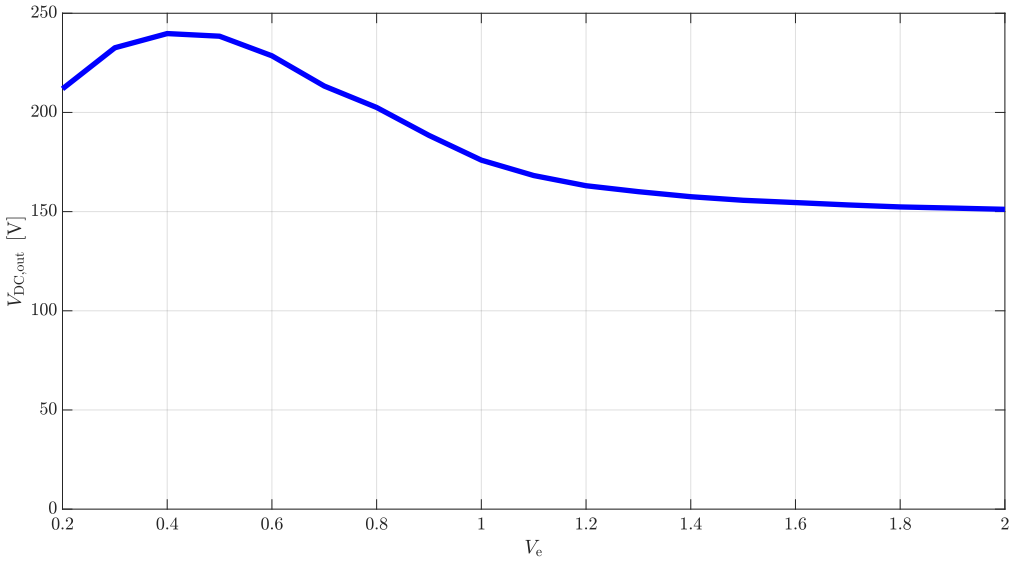
Figure 24. Dependency of input and output currents (**a**) and output voltage (**b**) to variations in V_e, when the CT operates as inverter on *RL* load (see Table 6). DC quantities are expressed as average values, whereas AC ones as phase rms values.

4.6.3. DC/DC Converter

Variations on V_e–Rectifier Stage.



(**a**)



(**b**)

Figure 25. Dependency of input and output currents (**a**) and output voltage (**b**) to variations in V_e (on the rectifier stage), when the CT operates as DC/DC converter on *RL* load (see Table 6). Quantities are expressed as average values.

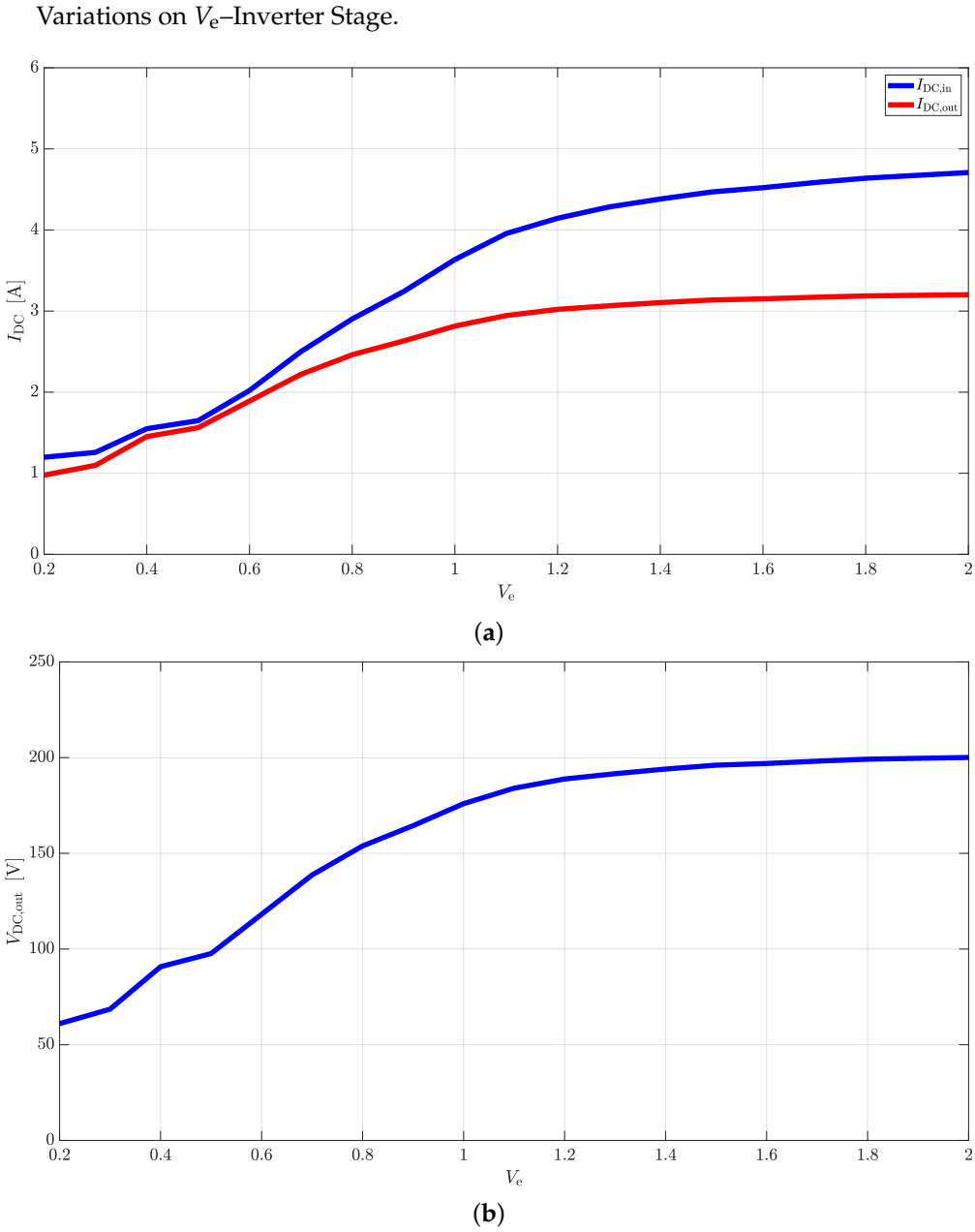


Figure 26. Dependency of input and output currents (**a**) and output voltage (**b**) to variations in V_e (on the inverter stage), when the CT operates as DC/DC converter on *RL* load (see Table 6). Quantities are expressed as average values.

Variations on φ_e–Rectifier Stage.

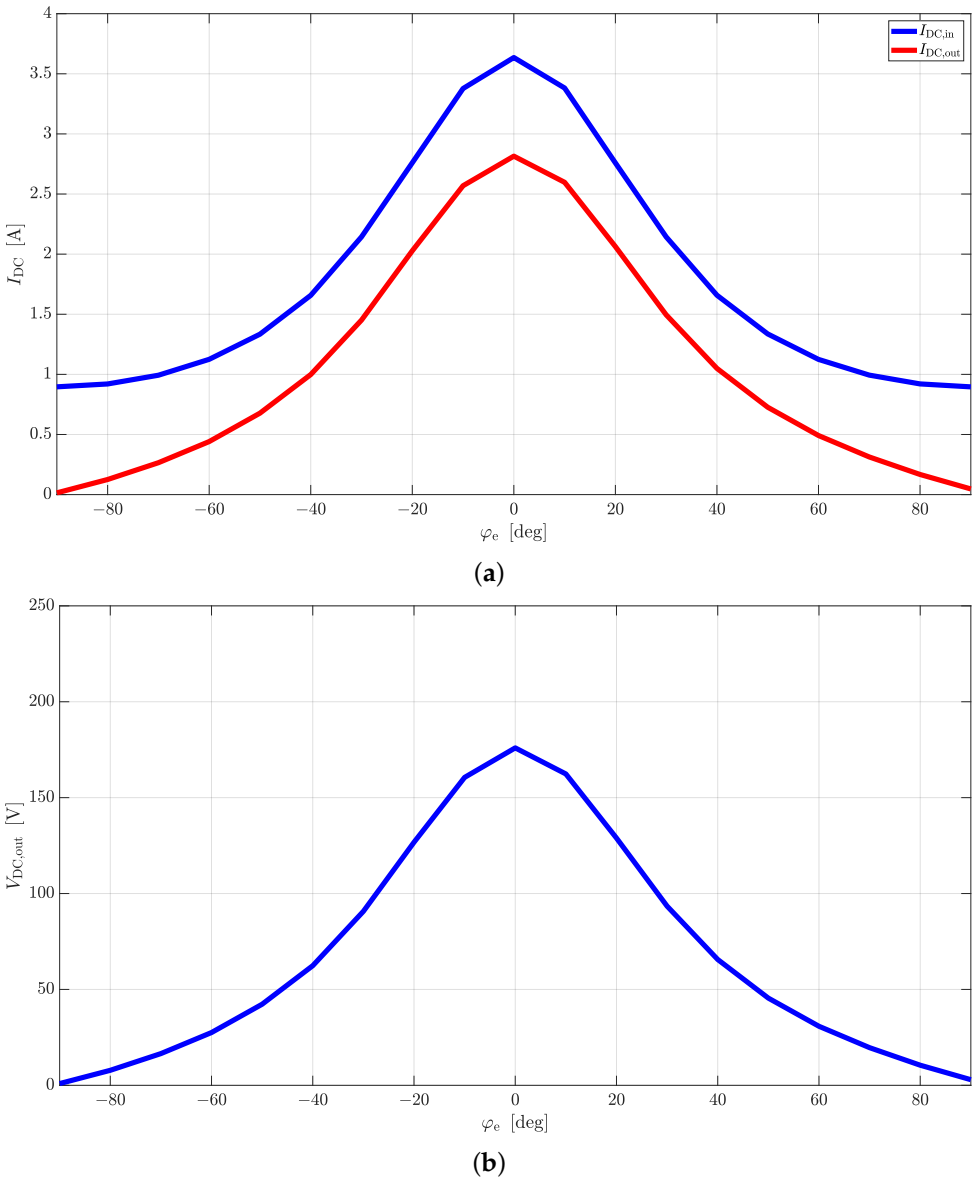


Figure 27. Dependency of input and output currents (**a**) and output voltage (**b**) to variations in φ_e (on the rectifier stage), when the CT operates as DC/DC converter on *RL* load (see Table 6). Quantities are expressed as average values.

4.6.4. Discussion on the Results

These analyses proved that voltages and currents can be controlled using $v_e(t)$ acting on the power modules. The investigations of this kind carried out for all loads shown in Table 6 will be exploited in future studies to design closed-loop control strategies for the CT prototype. By analyzing the outcomes of these sweeps, it can be observed that variations on V_e may have dangerous impacts on systems connected to inverter stages as V_e approaches 0. Indeed, abrupt increases in the input currents occur. This is justified noting that low V_e translates into a low number of on-modules; therefore, the impedance seen from the DC side reduces, possibly reaching $\approx 0\,\Omega$. This is not the case in rectifier stages. It can be noted that sweeps on φ_e show cosine-like profiles of V_{DC} on AC/DC stages, as can be predicted observing (13). Instead, it is more difficult to foresee the effects of variations in V_e on V_{DC} and V_{AC} for inverter operations, since V_e contributes in nested trigonometric functions inside a sum. Furthermore, loading effects should be accounted for solving the

whole network for providing a more realistic profile. In any case, (10) and (12) can be validated (despite representing an ideal scenario) by investigating the behavior of $\sum\cos(a_h)$ and $1/\sum\cos(a_h)$ with respect to variations on V_e. Figure 28 shows these profiles: it can be noted that V_{DC}, I_{DC}, I_{AC} in the rectifier stages show the same trends reported in Figure 28a, whereas the kind of dependency on V_e shown by I_{DC} during inverter operations is very similar to the curve reported in Figure 28a. In this context, I_{AC} and I_{DC} are more difficult to predict since they strongly depend on the loading effect acting on the multi-winding transformer and on the AC filters placed on the output stage of the inverter.

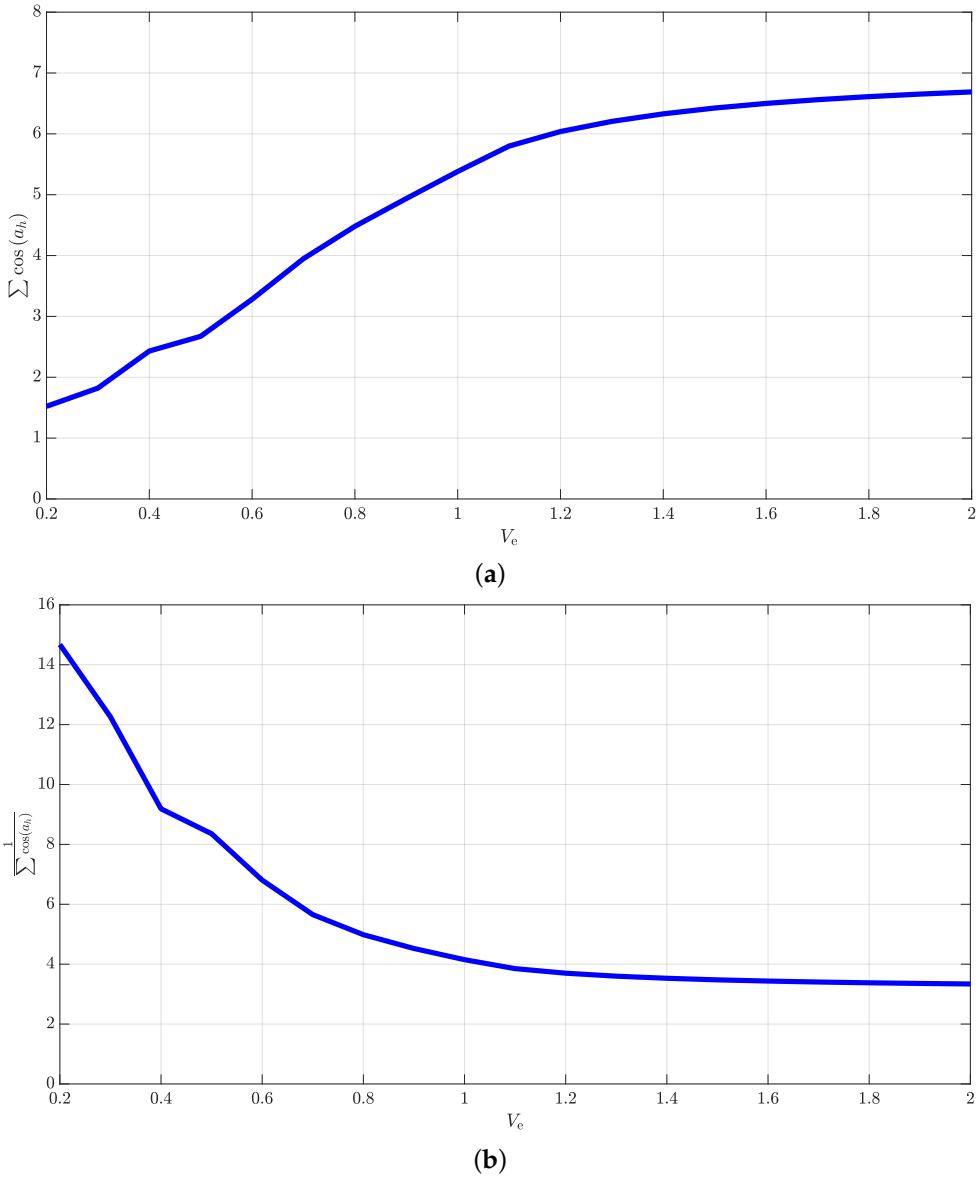


Figure 28. Dependency of $\sum\cos(a_h)$ (**a**) and $1/\sum\cos(a_h)$ (**b**) on variations in V_e.

5. Conclusions

This paper presents the CT showing its main governing equations and working principles, and a detailed switching model created in Simulink® to design and verify the behavior of a low-voltage, low-power prototype. Particularly, this research focuses on the simulation of the switching model on loading conditions reported in Table 6: this paper reports results obtained with RL loads only for brevity. However, the considerations included in this manuscript are general. The main finding of this paper is that this family of devices can operate safely in all the analyzed working conditions and no dangerous

transients occur when the CT is turned on and off as previously described. Moreover, the proposed strategy for clearing DC faults is promising on rectifier stages. Future works foresee the realization of the real prototype and a test campaign aimed at validating the simulated results.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	alternate current
DC	direct current
HV	high-voltage
MV	medium-voltage
LV	low-voltage
HVDC	high-voltage DC
MMC	modular multilevel converter
TSO	transmission system operator
NLC	nearest-level control
CT	converter transformer

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