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# A New Voltage-Doubler Rectifier for High-Efficiency LLC Resonant Converters

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**Abstract:** The LLC resonant converter is widely recognized as an effective solution for achieving high efficiency in high-frequency operations. This is primarily due to its ability to perform zero-voltage switching (ZVS) on primary switches and zero-current switching (ZCS) on secondary rectifier switches. However, implementing the secondary rectifier of an LLC resonant converter often requires the use of jumpers on the PCB to construct circuit topologies such as the center-tap rectifier (CTR), full-bridge rectifier, and voltage-doubler rectifier (VDR). In conventional VDR configurations, the source voltage of the high-side FET fluctuates according to the switching operation of the primary switch. This fluctuation necessitates auxiliary windings or bootstrap circuits to provide a floating voltage source, adding significant complexity to gate drive circuits in high-power-density applications. This complexity poses a major barrier to the practical adoption of VDRs. To address these challenges, this paper proposes a novel rectification circuit based on the VDR topology, specifically designed for LLC resonant converters, offering simplified gate drive circuitry and improved suitability for high-power-density applications.

**Keywords:** LLC resonant converter; voltage-doubler rectifier; synchronous rectifier



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## 1. Introduction

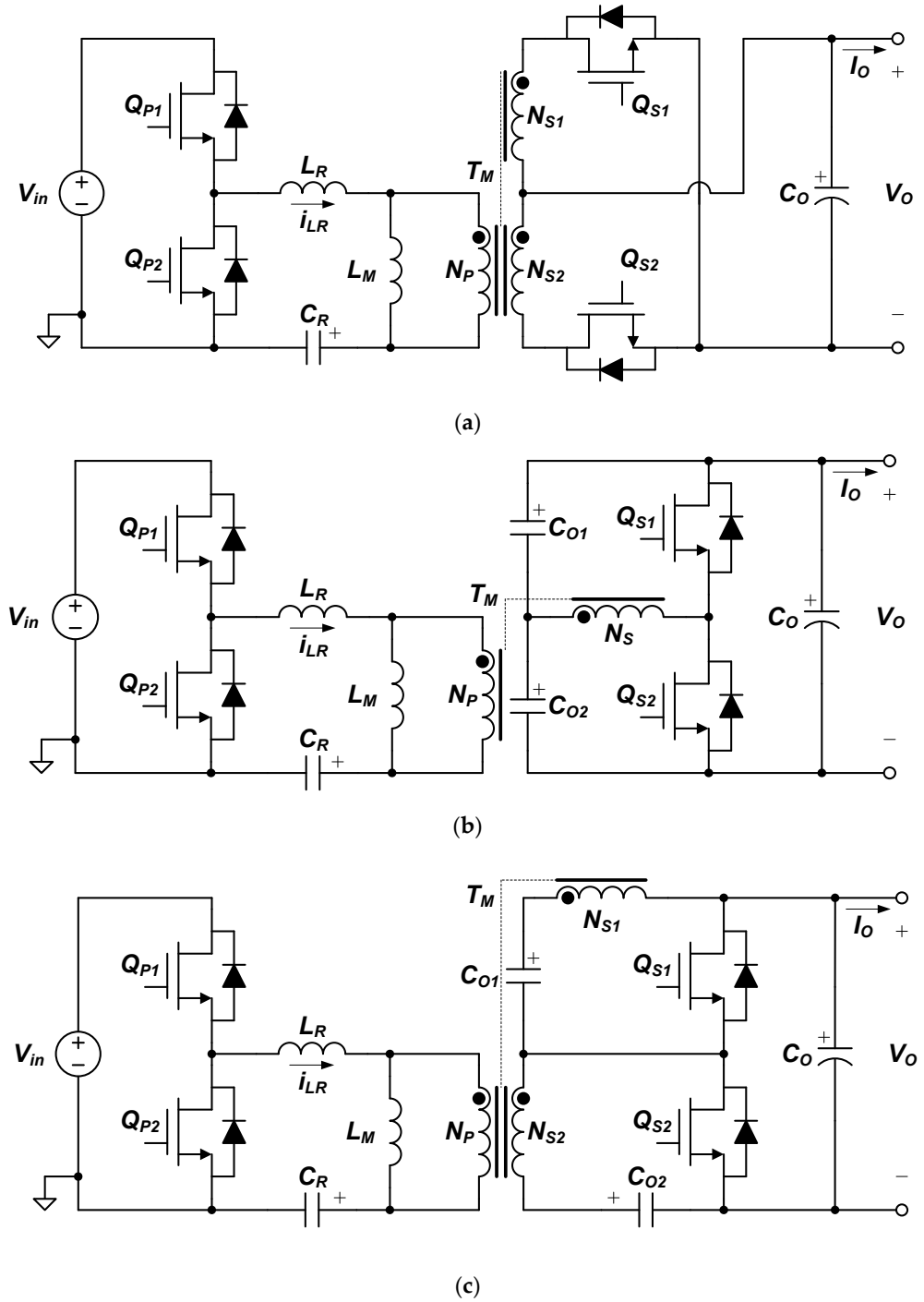
Recent advancements in semiconductor technologies, particularly silicon carbide (SiC) and gallium nitride (GaN) devices, have facilitated the development of high-frequency power modules without compromising efficiency [1–3]. Among various converter topologies, the LLC resonant converter is notable for achieving zero-voltage switching (ZVS) on the primary-side switches across the entire load range and zero-current switching (ZCS) on the secondary rectifier diodes, thereby reducing the size of magnetic components [4–8].

The LLC resonant converter is highly suited for high-efficiency and high-power-density power conversion systems [9]. Moreover, the resonant tank generates a nearly sinusoidal current waveform, minimizing power losses caused by harmonic currents compared to pulse-width-modulated (PWM) converters [10–12]. However, the LLC resonant converter encounters challenges in controlling the output voltage under no-load conditions. This limitation, which is more pronounced at high operating frequencies, arises from the junction capacitance ($C_j$) of the secondary rectifier diodes [13,14].

Furthermore, when secondary rectifiers utilize field-effect transistors (FETs) in low-voltage, high-current power modules, the larger equivalent output capacitance ($C_{oss}$) of FETs compared to Schottky diodes exacerbates the issue. Although several methods have been proposed to address light-load voltage regulation, these approaches often compromise overall efficiency [15,16].

This paper proposes a novel rectification circuit based on the voltage-doubler rectifier (VDR) topology for LLC resonant converters to address these challenges effectively.

Meanwhile, instead of a CTR shown in Figure 1a, the LLC resonant converter utilizing a VDR shown in Figure 1b exhibits a lower equivalent $C_{oss}$ value reflected to the primary resonant circuit, as analyzed in [11]. Consequently, the VDR-based LLC converter demonstrates superior regulation characteristics under light-load conditions. However, conventional VDR implementations require a high-side gate drive circuit, often involving a bootstrap or auxiliary transformer windings, which complicate the design of high-current, high-frequency power modules. To resolve these issues, a novel VDR circuit for LLC resonant converters is proposed, as shown in Figure 1c.




(**a**)

(**b**)

(**c**)

**Figure 1.** (**a**) Conventional CTR, (**b**) conventional VDR, and (**c**) proposed VDR with SR FET.

## 2. LLC Converter with New VDR

### *2.1. Operation Principles*

A circuit diagram of the proposed converter is shown in Figure 2. The primary circuit is the same as a conventional Half-Bridge LLC resonant converter, while the secondary rectifier adopts the proposed VDR structure. The proposed VDR consists of two capacitors and two rectifier diodes, similar to the conventional VDR, but with a split secondary winding, as described in [13]. The operation of the proposed converter can be divided into two symmetrical modes, akin to the conventional LLC resonant converter. In Mode 1, when $Q_{p1}$ turns on, $D_{S1}$ conducts, charging $C_{O1}$ and discharging $C_{O2}$, as shown in Figure 2a. Conversely, when $Q_{P2}$ is triggered, mode 2 enables the discharging current of $C_{O1}$ and the charging current of $C_{O2}$ to flow through $Q_{S2}$, as shown in Figure 2b.

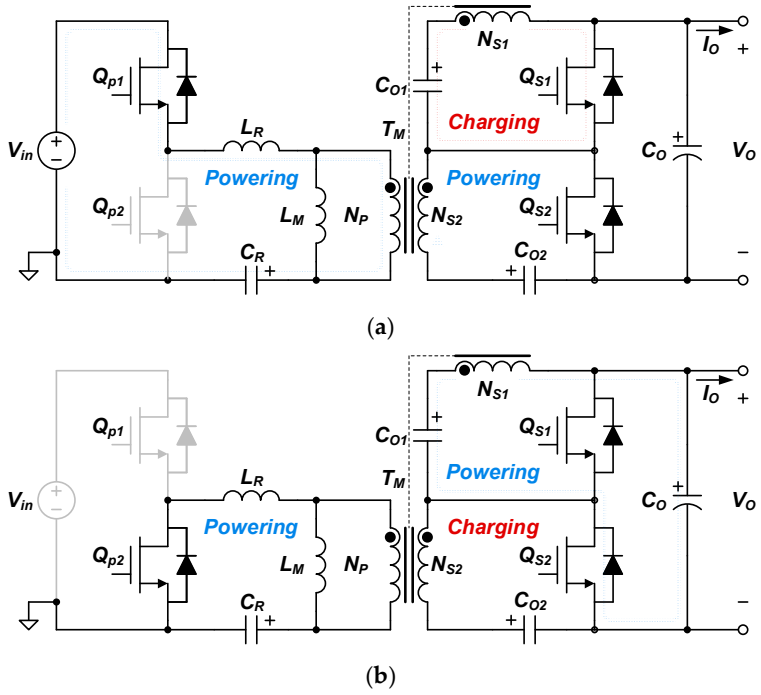



**Figure 2.** Current path of (**a**) mode 1 and (**b**) mode 2.

The main current waveforms, depicted in Figure 3, demonstrate that the resonant current flows through the two secondary windings of the transformer during both modes, resulting in a low RMS value. Assuming that $N_{S1} = N_{S2}$, during mode 1, the voltage across $N_{S1}$ is equal to $V_{CO1}$, and the voltage across $N_{S2}$ equal to $V_O - V_{CO2}$. In Mode 2, the voltage relationships are reversed. Therefore, it follows that $V_{CO1} = V_{CO2} = V_O/2$.

The proposed VDR exhibits the same low voltage stress $V_O$ as the conventional VDR. Furthermore, the proposed converter retains the fundamental operating characteristics of the conventional VDR, including the primary current and diode current waveforms. The input/output relationship equation for the LLC converter with the proposed VDR remains identical to that of the LLC converter with a conventional VDR and can be expressed as follows:

$$M = \frac{k \times f_n^2}{\sqrt{\left[(k+1) \times f_n^2 - 1\right]^2 + f_n^2 \times \left(f_n^2 - 1\right)^2 \times k^2 \times Q^2}}$$
$$\left(f_n = \frac{f_{sw}}{f_r},\ f_r = \frac{1}{2\pi\sqrt{L_r C_r}},\ k = \frac{L_m}{L_r},\ Q = \frac{1}{n^2 R_e}\sqrt{\frac{L_r}{C_r}},\ R_e = \frac{2R_o}{\pi^2}\right) \quad (1)$$

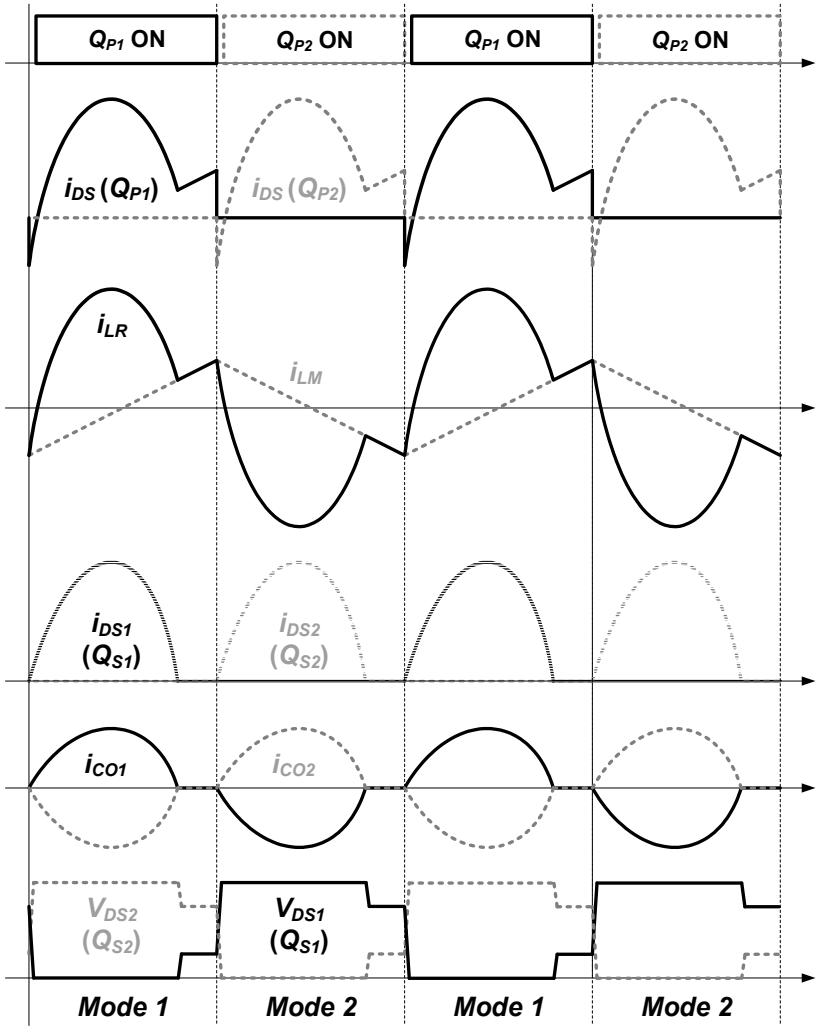



**Figure 3.** Main current waveforms of the proposed converter.

The normalized voltage gain $M$ of the LLC resonant converter is described by the equation shown above. This equation is fundamental for analyzing the input/output relationship of both the proposed VDR and the conventional VDR configurations. It highlights that the proposed VDR retains the same operational characteristics as the conventional VDR, ensuring consistent performance under various operating conditions.

In the equation, the normalized switching frequency $f_n$ is defined as the ratio of the switching frequency $f_{sw}$ to the resonant frequency $f_r$. The resonant frequency $f_r$ is determined by the resonant inductance $L_r$ and resonant capacitance $C_r$, calculated as $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$. The inductance ratio $k$ represents the ratio of the magnetizing inductance $L_m$ to the resonant inductance $L_r$, while the quality factor $Q$ quantifies the energy transfer efficiency in the resonant tank, defined as $Q = \frac{1}{n^2 R_e}\sqrt{\frac{L_r}{C_r}}$, where nnn is the transformer turns ratio and ReR_eRe is the equivalent load resistance. The equivalent load resistance $R_e$ is further expressed as $R_e = \frac{2R_o}{\pi^2}$ with $R_o$ being the actual load resistance.

The parameters $k$, $Q$, and $f_n$ collectively determine the voltage gain $M$ of the LLC converter. This equation ensures that the output voltage behavior of the proposed VDR remains identical to that of the conventional VDR under the same conditions, thus validating the compatibility of the proposed structure with standard LLC converter designs. Furthermore, the stable operating range provided by this equation supports the practical implementation of the proposed design in various power module applications.

### *2.2. Convenience of PCB Implementation with Planar Transformer*

In conventional CTR and VDR methods, jumpers are necessary to establish connections between the secondary winding and the device. This is due to the requirement for PCB traces to accommodate high-current applications with fewer layers and narrower widths. However, the proposed VDR method eliminates the need for jumpers by enabling direct connections between the secondary winding and the device. The secondary circuit can be implemented using a planar transformer with a UU Core, thereby simplifying circuit design and improving PCB manufacturing efficiency [17].

The integration of a planar transformer into the proposed VDR facilitates PCB design by eliminating jumpers and optimizing PCB layer utilization. Conventional VDR-based LLC resonant converters often encounter challenges in PCB layout due to jumper usage, which increases conduction losses resulting from pattern resistance. In contrast, the proposed VDR-based LLC resonant converter directly connects the secondary winding and rectifier diodes using a planar transformer, simplifying the design and minimizing conduction losses.

As shown in Figure 4, the differences between the conventional VDR and the proposed VDR using a planar transformer with a UU Core are demonstrated. In the conventional VDR design (Figure 4a), jumpers are required to connect the secondary winding to the rectifier diodes, which complicates the PCB layout and increases conduction losses. Moreover, the narrow PCB traces required for high-current applications further constrain overall circuit efficiency and reliability. In contrast, the proposed VDR design (Figure 4b) eliminates the need for jumpers, allowing for direct connections and reducing layout complexity. The optimized PCB layout further improves layer utilization and facilitates more efficient manufacturing processes.

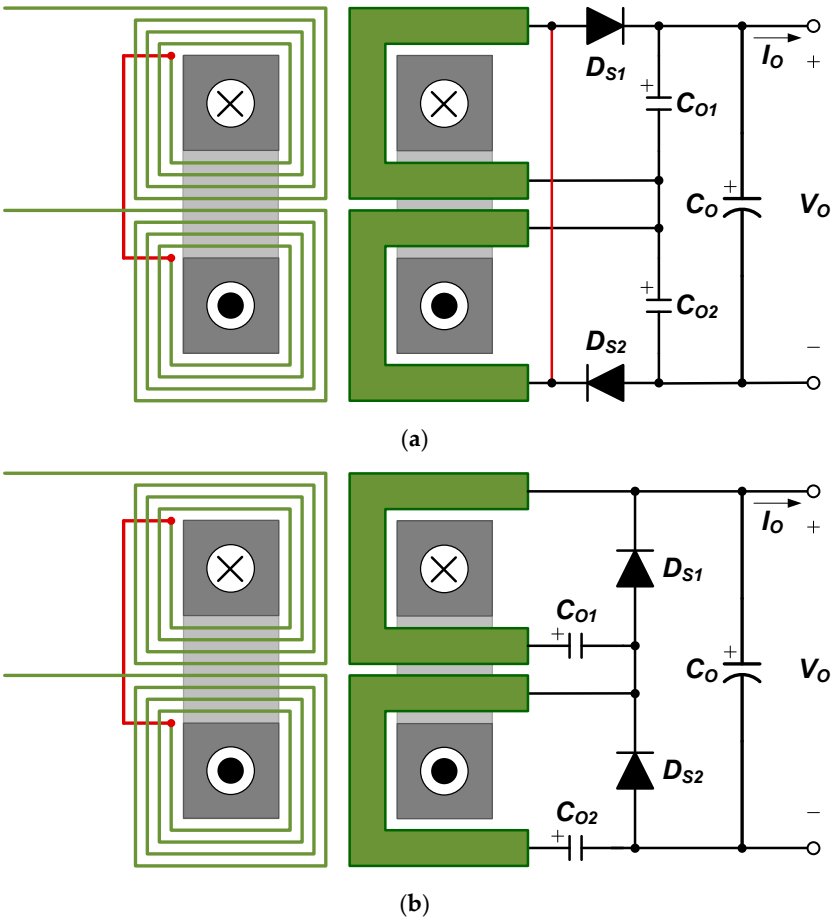



**Figure 4.** (**a**) Conventional VDR and (**b**) proposed VDR with planar transformer using UU core.

As shown in Figure 5, the layout of the proposed VDR-based LLC resonant converter using a planar transformer demonstrates these advantages. Unlike conventional VDR designs, which require jumpers and complicated PCB implementation, the proposed approach simplifies the layout while reducing complexity. This improvement not only enhances overall efficiency but also maximizes the effective utilization of PCB layers.

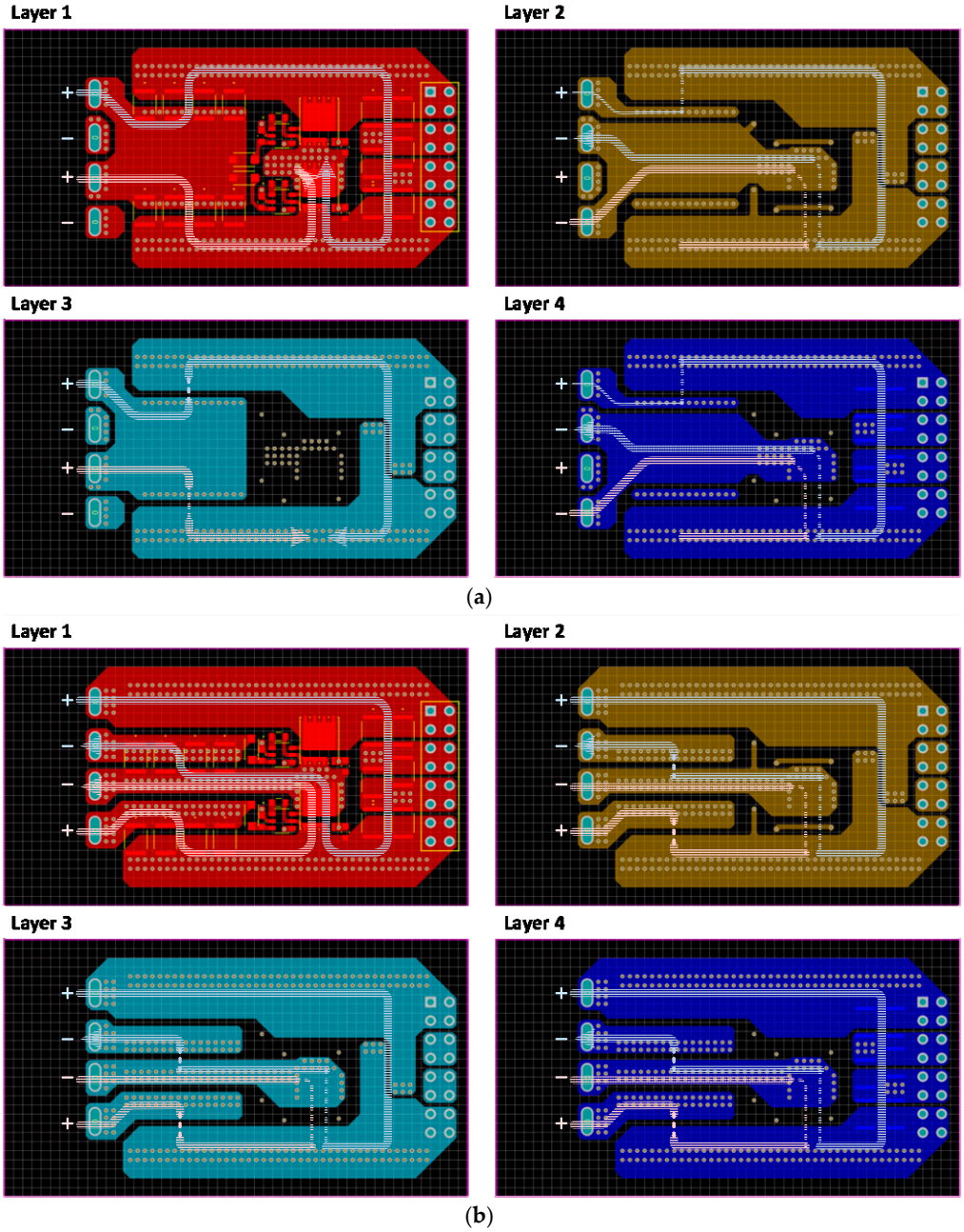



**Figure 5.** PCB implementation of (**a**) conventional VDR and (**b**) proposed VDR.

### *2.3. Simple Driving of SR FETs*

The conventional VDR configuration presents a significant challenge due to variations in the source voltage of the high-side FET caused by the switching operation of the primary-side FET, complicating gate voltage application. In the conventional rectifier configuration, the anode terminals of the rectifier diodes $D_{S1}$ and $D_{S2}$ are connected to the negative terminals of $C_{O1}$ and $C_{O2}$, respectively. This configuration increases the complexity of driving the high-side FET, necessitating additional circuits or techniques such as a bootstrap diode and a capacitor to manage the gate voltage effectively, as shown in Figure 6a.

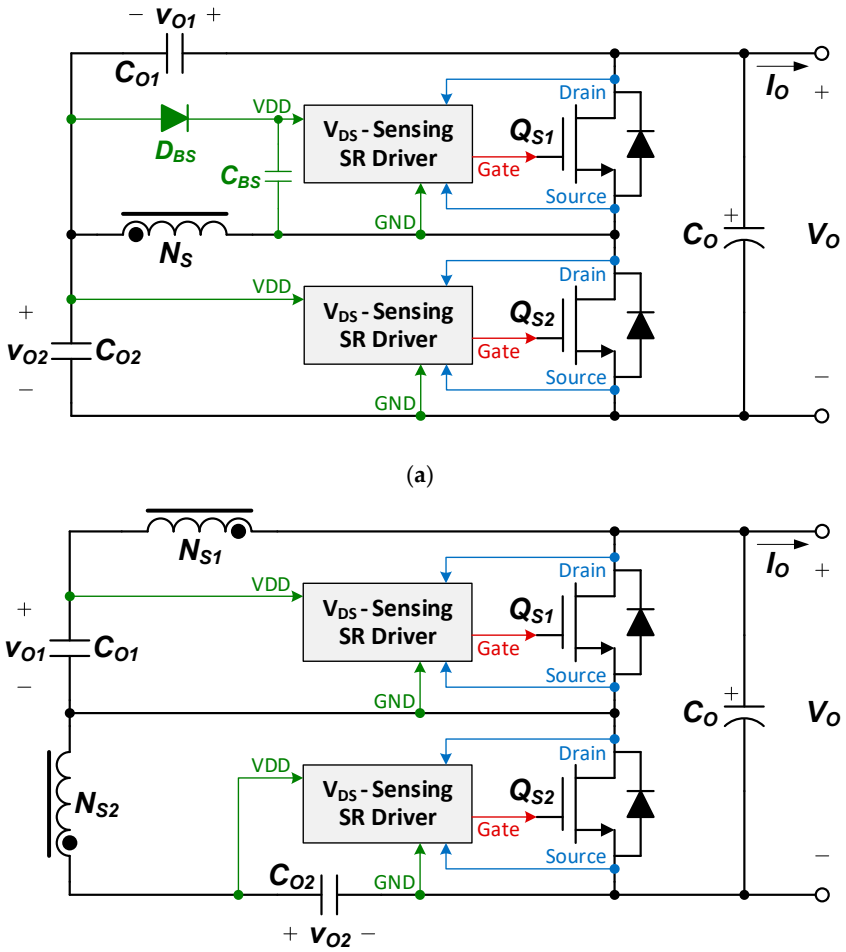



**Figure 6.** SR FET driving circuit of (**a**) conventional VDR and (**b**) proposed VDR.

In contrast, the proposed VDR structure simplifies SR FET driving when implementing the rectifier circuits for low-voltage, high-current power modules. The upper and lower FETs can be driven more easily by utilizing the voltages across $C_{O1}$ and $C_{O2}$ as power sources for the gate drive operation. This eliminates the need for a bootstrap circuit or auxiliary winding. The doubler capacitors $C_{O1}$ and $C_{O2}$ provide a stable DC voltage that can directly supply a self-driving IC for the SR FET, ensuring efficient operation without additional floating voltage sources. This novel design streamlines the system and improves efficiency in driving the SR FETs. The proposed system supports an output voltage range of 12 V to 36 V, providing sufficient gate voltage to meet the threshold voltage requirements while staying within the absolute maximum gate voltage limits.

Additionally, by using advanced SR FET gate drivers, such as the TEA2093TS (NXP Semiconductors, Eindhoven, The Netherlands) or UCC24630 (Texas Instruments, Dallas, TX, USA), the proposed VDR design can drive SR FETs more directly and efficiently compared to the conventional VDR configuration. These drivers are well suited for the simplified structure shown in Figure 6b, as they utilize the stable voltage supplied by $C_{O1}$ and $C_{O2}$ to directly operate the gates of $Q_{S1}$ and $Q_{S2}$. This direct driving capability not only enhances system performance but also reduces the complexity of gate driving circuits. Consequently, the proposed design offers a more robust and easily implementable solution for low-voltage, high-current power module applications.

As shown in Figure 6, the SR FET driving circuits of both converters are compared. While the driving circuit for the low-side SR FET is identical in both configurations, the high-side SR FET driving circuit in the conventional VDR (Figure 6a) additionally requires a bootstrap diode and a capacitor, increasing circuit complexity. In contrast, the proposed

configuration (Figure 6b) eliminates this requirement, relying instead on the doubler capacitors $C_{O1}$ and $C_{O2}$ to supply the gate drive voltage directly, simplifying the design and improving reliability.

## 3. Experimental Results

To evaluate the effectiveness of the proposed VDR, a 24 V/240 W output prototype was implemented for both the conventional VDR LLC and the proposed VDR LLC converters. The key components used in the prototypes are listed in Table 1. For the 24 V/240 W output power module, the design specifications are $V_{in}$ = 355~408 V, $P_{O,max}$ = 240 W, $V_O$ = 24 V. The experimental results obtained with the prototypes confirm the validity of the proposed circuit. As shown in Figure 7, the prototype consists of the primary side, which includes the resonant tank circuit and transformer, and the secondary side, which incorporates the synchronous rectifier SR FETs and doubler capacitors. The layout highlights the integration of essential components in a compact design for efficient operation. This physical implementation validates the compatibility of the proposed topology with the design specifications and demonstrates its capability to achieve the intended performance under experimental conditions.

**Table 1.** Experimental Parameters of 240 W prototype.

| Parameters | Value |
|---|---|
| Input voltage, $V_{in}$ | 355 V~408 V (nominal 400 V) |
| Output voltage, $V_o$ | 24 V |
| Output current, $I_o$ | 0~10 A |
| Switching frequency | $F_s$ = 87~105 kHz |
| Transformer turns ratio | $N_P$:$N_S$ = 34:2 |
| Magnetizing inductance | $L_M$ = 700 µH |
| Resonant inductance | $L_R$ = 58 µH |
| Resonant capacitor | $C_R$ = 44 nF |
| Doubler capacitor | $C_{O1}$, $C_{O2}$ = 88 µF |
| Output capacitor | $C_O$ = 1200 µF |
| Primary FET, $Q_{P1}$ and $Q_{P2}$ | TK290P60Y |
| SR FET, $Q_{S1}$ and $Q_{S2}$ | BSC016N06NST |
| SR driver | TEA1999TS |

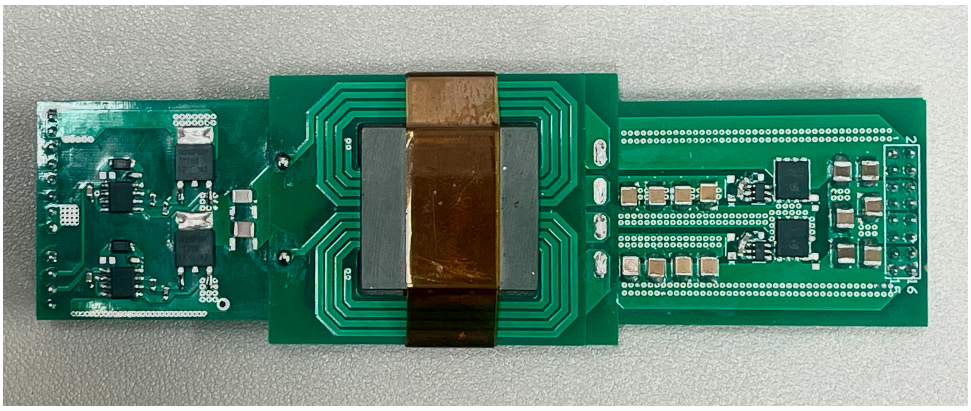


**Figure 7.** Prototype of proposed VDR LLC resonant converter module.

The proposed converter achieves the same DC gain as a conventional VDR LLC resonant converter, and its resonant tank design is comparable to that of an LLC converter with a CTR. Moreover, the proposed VDR LLC resonant converter shares common parameters with the conventional VDR LLC resonant converter, including the same turn ratio, secondary SR FETs, and doubler capacitors. The control strategy to verify the operational principles of the proposed VDR LLC resonant converter is general voltage control, as shown in Figure 8.

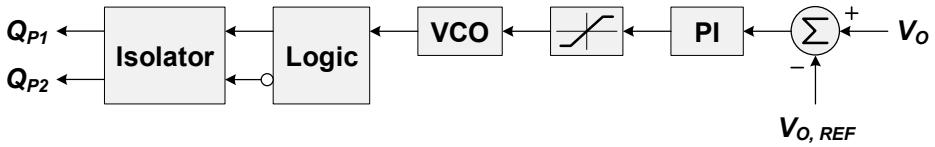



**Figure 8.** Control strategy for proposed VDR LLC resonant converter.

As shown in Figures 9 and 10, the experimental waveform of the proposed VDR converter, measured under an input voltage of 400 V, closely resembles those of the conventional VDR converter in terms of current and voltage characteristics. The performance of the proposed converter was tested under varying load conditions, specifically at 10% and 100% loads. In both cases, the primary current and rectifier diode current waveforms aligned with the theoretical predictions. Furthermore, an analysis of the resonant circuit revealed that the resonant current and voltage observed during the experiments were consistent with theoretical expectations, demonstrating reliable performance across different load conditions. Therefore, while the proposed converter shares basic operating characteristics with the conventional VDR, it distinguishes itself through simplified SR FET driving.

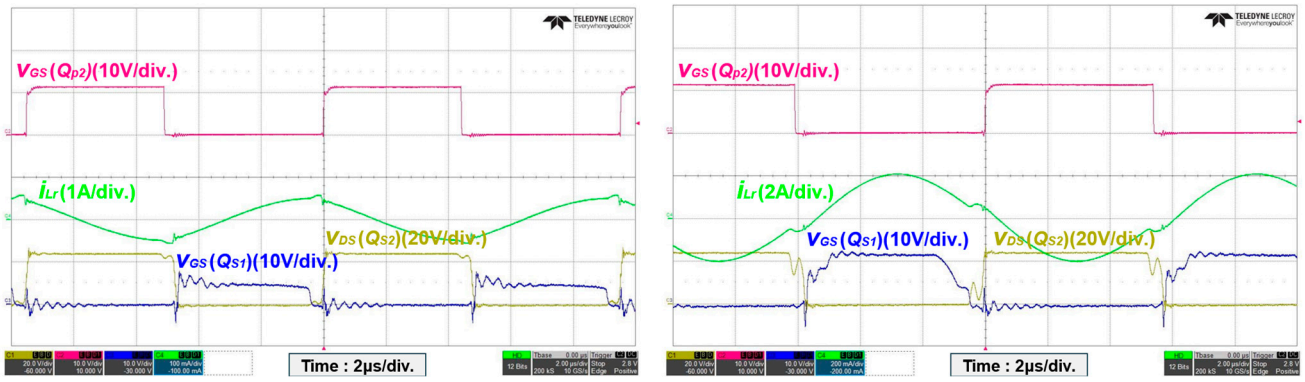



**Figure 9.** SR switching waveforms of conventional VDR under 400 V input at (**a**) 10% and (**b**) 100% loads.

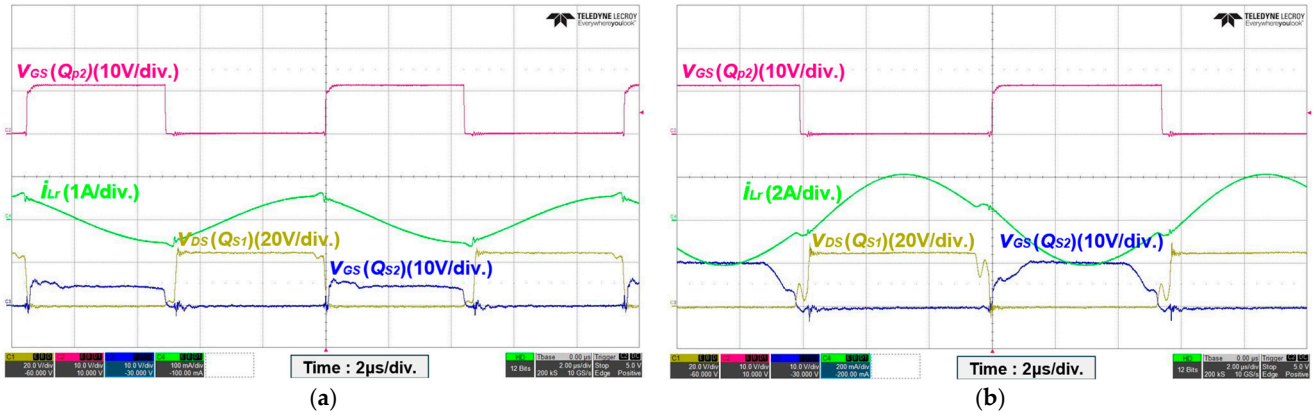



**Figure 10.** SR switching waveforms of proposed VDR under 400 V input VDR at (**a**) 10% and (**b**) 100% loads.

The simplification of SR FET driving significantly enhances the convenience of circuit design by eliminating the need for jumpers during PCB manufacturing, reducing circuit complexity, and minimizing potential manufacturing errors. Additionally, the use of SR FETs improves overall system efficiency. Unlike the conventional VDR method, which relies on complex driving circuits for high-speed switching, the proposed method simplifies the driving circuits, reducing switching losses. The reduction in switching losses trans-

lates directly to the minimization of power losses, which is a crucial factor in enhancing system efficiency.

In addition to its design advantages, the proposed converter is expected to demonstrate superior performance compared to the conventional VDR method. Simplified SR FET driving facilitates stable operation at high frequencies, enabling increased power density. Moreover, it ensures stable operation under high-voltage and high-current conditions, making it highly applicable across various fields. In conclusion, the proposed converter offers significant improvements over the conventional VDR method. The simplification of the PCB manufacturing process, increased efficiency, and ease of design through the simplification of the driving circuit are key advantages. These benefits collectively highlight the proposed converter's potential to provide a notable performance enhancement compared to the conventional VDR.

Figures 9 and 10 illustrate the measured SR switching waveform variations under different load conditions for both the conventional VDR and the proposed VDR, with measurements conducted at an input voltage of 400 V. Following this, Figures 11 and 12 present the SR switching waveforms obtained at an input voltage of 355 V in the respective VDRs.

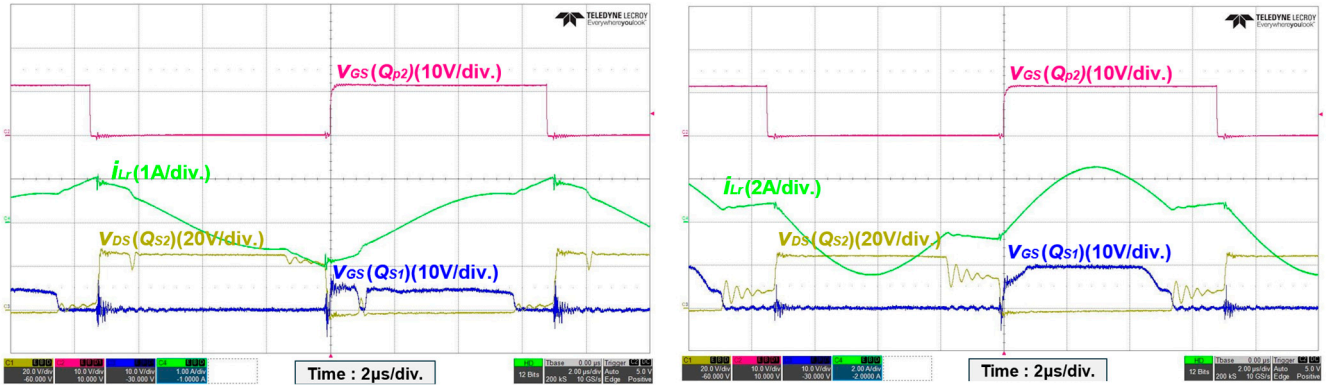



**Figure 11.** SR switching waveforms of conventional VDR under 355 V input at (**a**) 10% and (**b**) 100% loads.

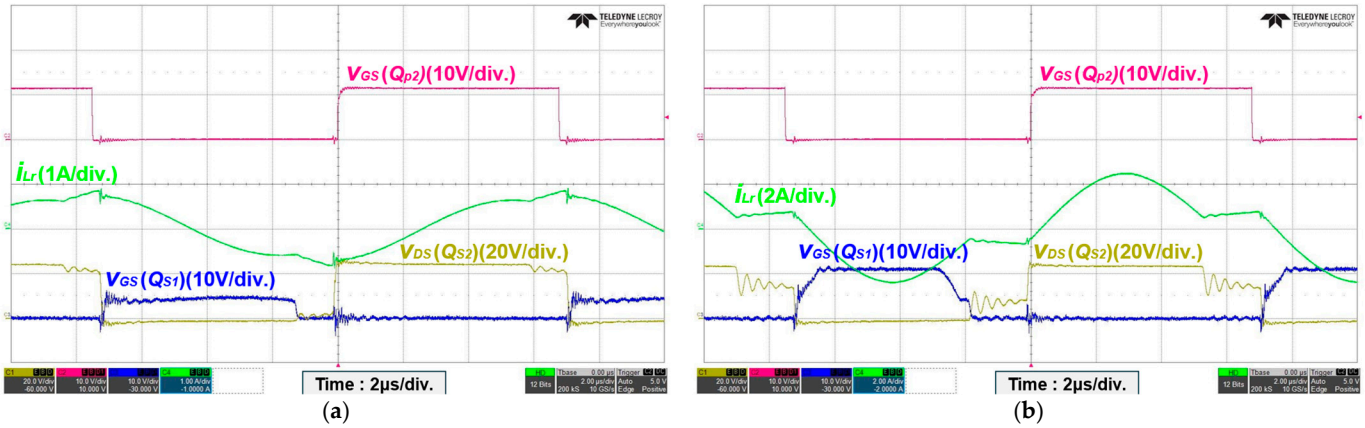
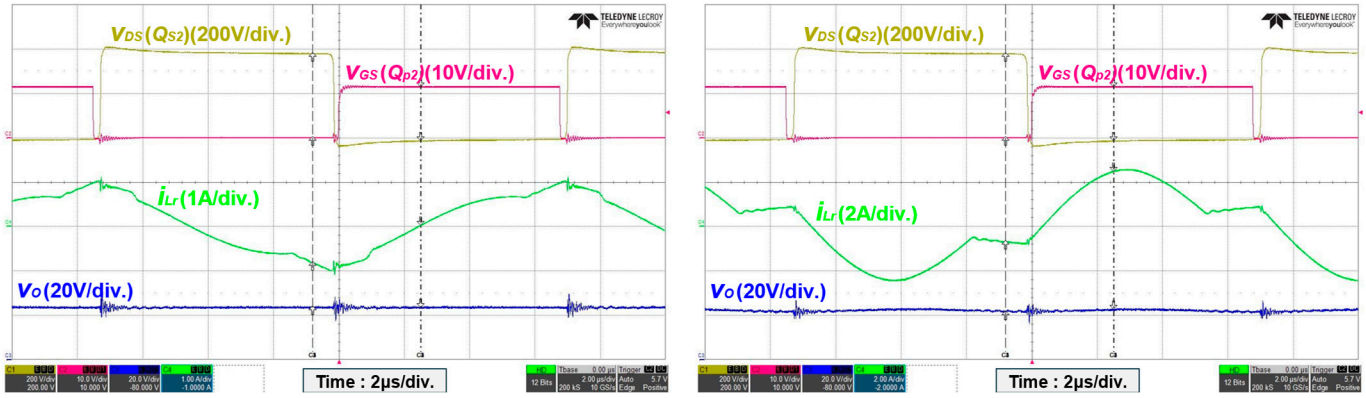



**Figure 12.** SR switching waveforms of proposed VDR under 355 V input at (**a**) 10% and (**b**) 100% loads.

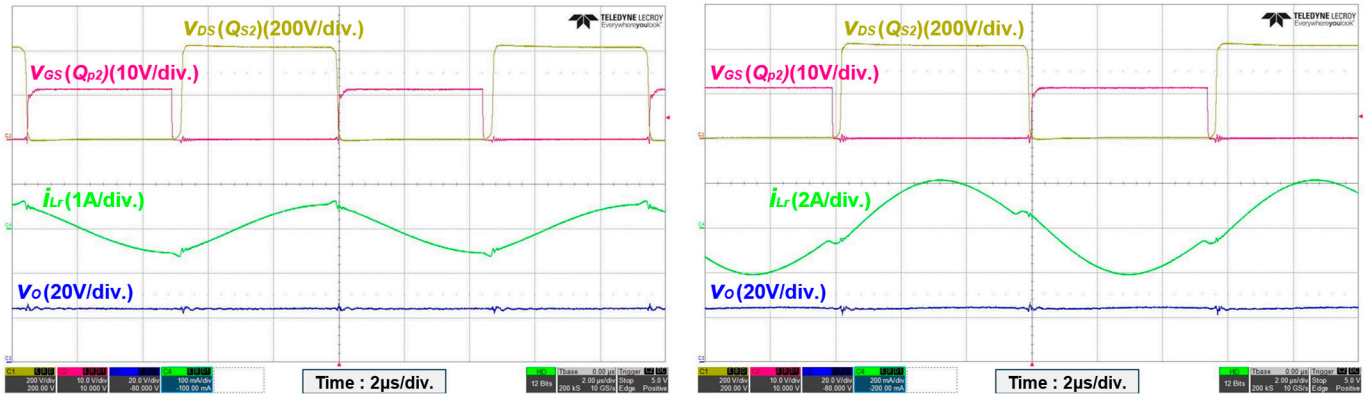
Figures 13 and 14 show primary ZVS waveforms with output voltage and primary resonant current waveforms under 355 V and 400 V inputs, respectively. Figure 15 shows the results of comparing the efficiency of the proposed and the conventional converters under different input voltage conditions. Efficiency measurements were conducted under two input voltage levels: a 400 V nominal input voltage and a 355 V minimum input voltage. Figure 15a illustrates the efficiency results at the nominal input voltage of

400 V, while Figure 15b presents the results at the minimum input voltage of 355 V. These measurements provide a comprehensive evaluation of the converters' performance across varying load conditions.




(**a**) (**b**)

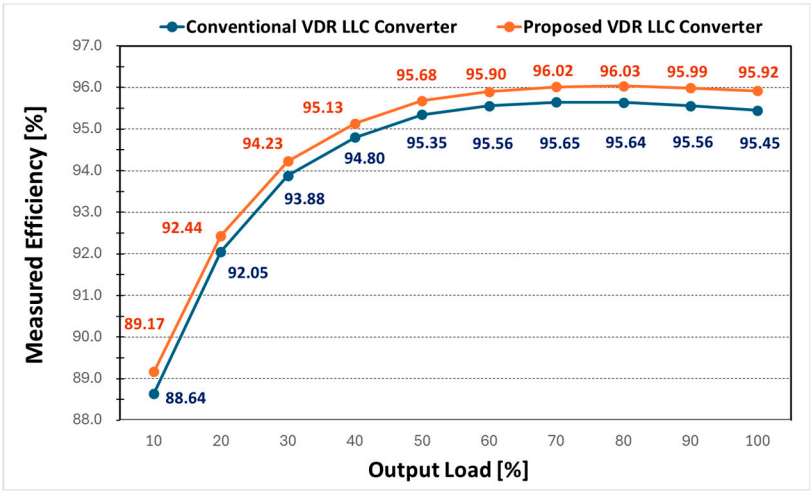
**Figure 13.** Primary ZVS and output voltage waveforms of proposed VDR under 355 V input at (**a**) 10% load and (**b**) 100% load.



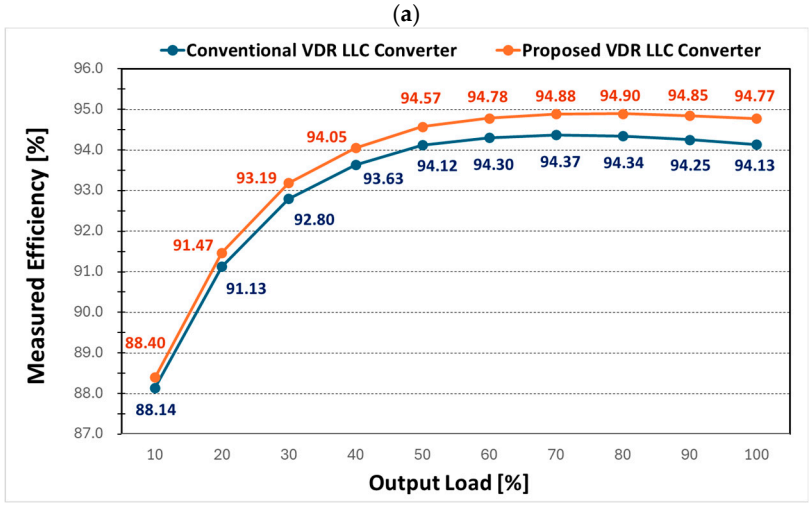

(**a**) (**b**)

**Figure 14.** Primary ZVS and output voltage waveforms of proposed VDR under 400 V input at (**a**) 10% load and (**b**) 100% load.

As shown in Figure 15a, at a 400 V input, the proposed VDR LLC converter consistently outperforms the conventional VDR LLC converter across all load conditions. At light loads, the efficiency of the proposed converter starts at 89.17%, compared to 88.64% for the conventional converter. This efficiency advantage becomes more pronounced as the load increases, with the proposed converter peaking at 95.92% efficiency at full load, while the conventional converter reaches a maximum of 95.68%. The reduced conduction losses in the proposed converter, achieved by eliminating jumpers during PCB implementation, significantly contribute to this improvement. Similarly, Figure 15b shows the efficiency comparison under a lower input voltage of 355 V. While both converters experience a slight decrease in overall efficiency due to higher conduction losses at lower input voltages, the proposed VDR LLC converter still demonstrates superior performance. At a 10% load, the efficiency of the proposed converter is 88.40%, slightly higher than the conventional converter's 88.14%. At full load, the proposed converter achieves 94.77%, compared to 94.13% for the conventional design. These results highlight the robustness of the proposed VDR design, maintaining higher efficiency across a wide range of operating conditions.




(**a**)




(**b**)

**Figure 15.** Measured efficiency of proposed and conventional VDR LLC converters under (**a**) nominal input voltage (400 V) and (**b**) minimum input voltage (355 V).

The improvement in efficiency can be attributed to the elimination of jumpers and the simplified PCB design of the proposed VDR circuit. By widening and optimizing high-current flow paths, conduction losses are minimized, leading to enhanced overall system performance. This benefit is particularly significant under high-output and high-voltage conditions, as shown in Figure 15a. Moreover, the consistent efficiency advantage at lower input voltages, as depicted in Figure 15b, demonstrates the versatility of the proposed design for applications requiring stable performance across varying voltage levels.

Furthermore, the elimination of jumpers not only reduces power losses but also enhances the convenience and flexibility of PCB implementation. This advantage allows for simplified circuit design, making the proposed converter a practical solution for high-efficiency power conversion in a wide range of applications. These results underline the potential of the proposed VDR LLC converter as a significant advancement in the design and implementation of power conversion systems.

## 4. Conclusions

In this paper, the performance improvements of LLC resonant converters adopting the new VDR method are investigated. The proposed VDR structure simplifies SR FET driving and enhances power conversion efficiency while optimizing PCB design. By incorporating UU-type planar transformers, the complexity of the PCB layout is significantly reduced, enabling greater integration and reliability. The experimental results confirm

that the proposed VDR-based LLC resonant converter retains the fundamental operating characteristics of conventional VDR LLC converters while achieving improved overall system performance. These structural enhancements demonstrate improved efficiency without compromising the inherent high efficiency and voltage stability of LLC converters.

In particular, the proposed converter exhibits excellent performance in low-voltage, high-current power module applications, indicating its potential to effectively replace conventional VDR LLC resonant converters. Furthermore, the proposed VDR-based LLC resonant converter provides a promising solution for applications requiring high-efficiency power conversion. In conclusion, the proposed VDR method significantly improves the performance of LLC resonant converters by offering a simplified structure and high implementation efficiency. These characteristics make it suitable for low-voltage, high-current power systems, underscoring its potential for broader applications in modern power electronics.

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