

Article

Low-Cost Hardware Analog and Digital Real-Time Circuit Simulators for Developing Power Electronics Control Circuits

Krzysztof Sozański 

Institute of Automation, Electronics and Electrical Engineering, University of Zielona Góra,
65-417 Zielona Góra, Poland; k.sozanski@iee.uz.zgora.pl

Abstract: The paper describes low-cost hardware-based analog and digital real-time circuit simulators for the development of power electronics control circuits. During the process of designing and developing digital control circuits for power electronics systems, preliminary verification of control algorithms is required. For this purpose, software simulators such as Pspice, Psim, Matlab-Simulink, and many others are commonly used. Afterward, the developed control algorithm is implemented in the digital control system. For further verification of the implemented control algorithms, a hardware-based analog or digital simulator can be utilized. The paper presents the author's proposed analog simulators. In the digital version of the simulator, TMS320F28388D microcontroller with 200 MHz clock was used. These simulators have demonstrated their usefulness in the development of power electronics systems.

Keywords: power electronics; real-time systems; simulation; dynamic systems; embedded systems; hardware-in-the-loop (HIL); power hardware-in-the-loop (P-HIL) test benches; mathematical model

1. Introduction

The design of power electronics systems requires significant knowledge in fields such as electrical engineering, electronics, power electronics, digital signal processing, automation, control techniques, embedded systems programming, and more. Errors made during the design and development of power electronics systems can lead to the destruction of expensive power electronics devices. Therefore, during the development and testing of digital control systems for power electronics, preliminary verification of control algorithms is essential. Commonly, software simulators such as Pspice, Psim, Matlab-Simulink, and many others are used for this purpose. After such software-based verification of the control algorithm, the developed algorithm is implemented using a microcontroller, enabling further testing within the power electronics system. However, even minor errors in the control system that are not revealed during computer simulations can result in the failure of the (often expensive) power electronics system. For this reason, an additional stage of testing is conducted using a hardware simulator.

Hardware-In-the-Loop (HIL) testing utilizes the simulation of real signals necessary for the fully functional operation of the system under test. HIL testing involves connecting actual hardware with a virtual simulation environment. This allows for realistic testing of the hardware's functionality and performance without the risk of damage, and it enables the creation of test scenarios that are very difficult or even impossible to replicate in the real world. This tool is widely used across various industries, helping to shorten product development time and eliminate errors at the design stage.

Currently, companies like OPAL-RT Technologies [1], Typhoon HIL [2], National Instruments [3], Imperix [4], Simintech, and Delta Design provide hardware and software tools for the verification of power electronics control systems. It should be noted that the need for testing digital systems and algorithms in the industry is growing, and consequently, the range of testing systems offered by companies is expanding. The topic of testing power electronics circuits using HIL systems is widely covered in the literature [5–16].



Citation: Sozański, K. Low-Cost Hardware Analog and Digital Real-Time Circuit Simulators for Developing Power Electronics Control Circuits. *Energies* **2024**, *17*, 6359. <https://doi.org/10.3390/en17246359>

Academic Editor: José Gabriel Oliveira Pinto

Received: 23 October 2024

Revised: 17 November 2024

Accepted: 13 December 2024

Published: 17 December 2024



Copyright: © 2024 by the author. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

Unfortunately, such professional HIL systems are very expensive. In this paper, low-cost hardware-based analog and digital real-time simulators for developing power electronics control circuits, proposed by the author, are described. Both analog and digital systems are discussed. In the case of digital systems, the hardware simulator of power electronics circuits was implemented using the TMS320F28388D microcontroller from Texas Instruments, Dallas, TX, USA [17]. A three-phase shunt Active Power Filter (APF) was used as a sample power electronics circuit for the developed hardware simulator.

2. Power Electronics Circuits

Power electronics systems are extensively employed for the control and conversion of electrical energy. A typical schematic representation of such a system is depicted in Figure 1. The system comprises a power electronic circuit, which incorporates components such as electronic switches (e.g., IGBTs, MOSFETs), capacitors, magnetic elements, and a digital controller. The control algorithm, executed within the digital controller, governs the functioning of the power electronic circuit [18–27]. In Figure 1, the placement of the power electronics circuit simulator is also shown; this simulator replaces the actual power electronics circuit during development work.

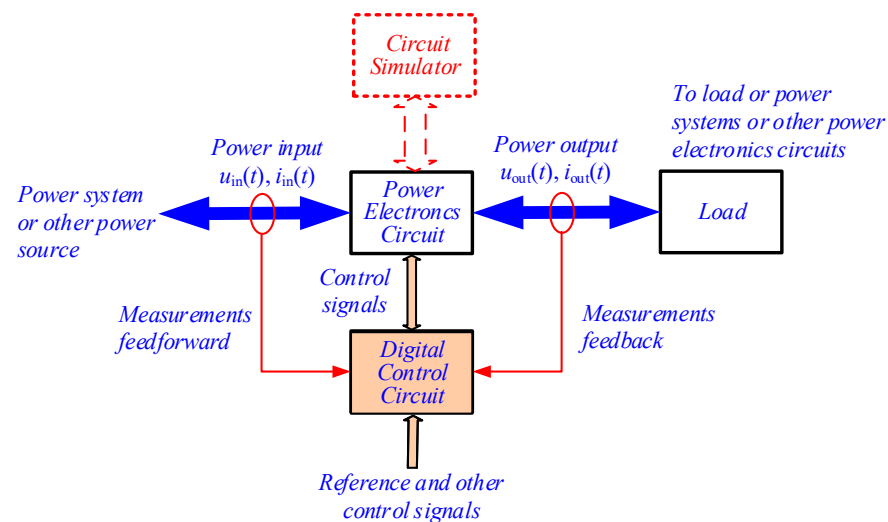


Figure 1. Block diagram of power electronics system.

The digital controller employs digital signal processing techniques to analyze input signals, generate control signals, and regulate the output of the power electronic circuit in alignment with specific performance criteria. This enables precise control of the power electronic circuit and efficient electrical power conversion across various applications, including motor drives, renewable energy systems, and power supplies.

The integration of digital controllers in power electronic systems has significantly enhanced their performance, reliability, and flexibility, facilitating the implementation of advanced control strategies and extending system functionalities.

A block diagram of the considered simulation circuit of the power electronic system is depicted in Figure 2. The circuit consists of a simulator of the power electronics circuit (analog or digital), a control circuit power electronics circuit, an arbitrary signal generator, and an oscilloscope.

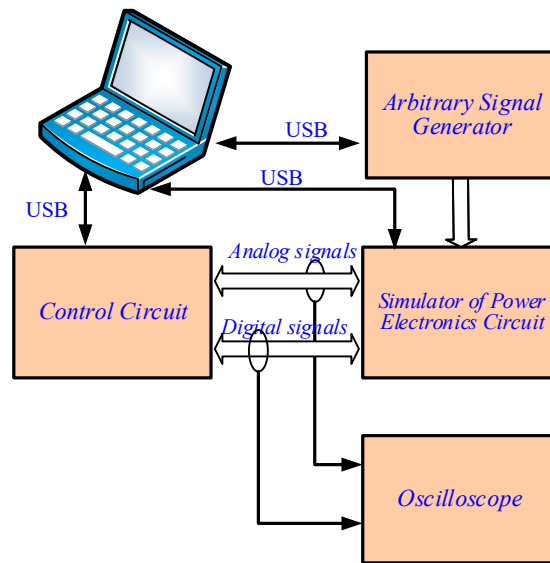


Figure 2. Block diagram of a considered simulation circuit.

3. Typical Output Circuits of Inverters

One of the main tasks of the simulation system is to replicate the operation of the power stage. Therefore, this section will present typical output circuits of inverters. These can be divided into two basic types: voltage outputs and current outputs. Figure 3 shows three circuits with first-order, second-order, and third-order voltage outputs. Voltage sources U_{DC1} and U_{DC2} supply power to the inverter, resistor R_1 represents the output resistance of the inverter and inductor L_1 , while R_L represents the load resistance. In the case of the third-order circuit, R_2 represents the resistance of inductor L_2 .

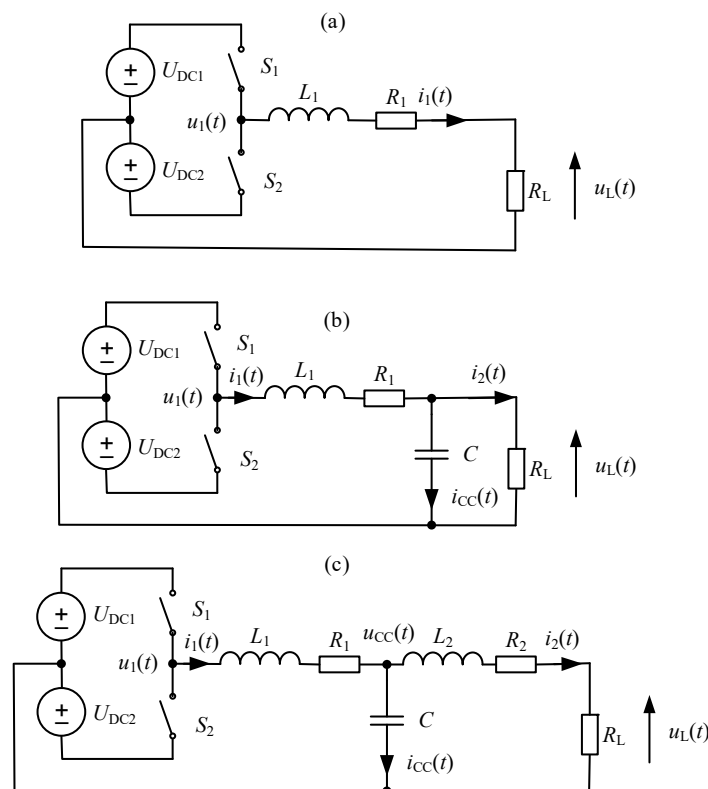


Figure 3. Examples of typical output circuits of inverters for voltage output: first-order (a), second-order (b), third-order (c).

The transfer function of the system from Figure 3a is:

$$H(s) = \frac{U_1(s)}{U_L(s)} = \frac{\frac{R_L}{R_1 + R_L}}{1 + s \frac{L_1}{R_1 + R_L}} \quad (1)$$

The transfer function of the system from Figure 3b is:

$$H(s) = \frac{U_1(s)}{U_L(s)} = - \frac{1}{1 + \frac{R_1}{R_L} + s \left(C_1 R_1 + \frac{L_1}{R_L} \right) + s^2 C_1 L_1} \quad (2)$$

The transfer function of the system from Figure 3c is:

$$H(s) = \frac{U_1(s)}{U_L(s)} = \frac{R_L}{R_1 + R_2 + R_L + s(L_1 + L_1 + C_1 R_1 R_2 + C_1 R_1 R_3) + s^2(L_2 R_1 + L_1 R_2 + L_1 R_L) C_1 + s^3 C_1 L_1 L_2} \quad (3)$$

Figure 4 shows two circuits with first-order and third-order current outputs. The voltage $e_M(t)$ represents the supply network voltage. In the case of the first-order circuit (Figure 4a), L_1 represents the inductance of the inductor and the supply network, while R_1 represents the output resistance of the inverter, the inductor L_1 , and the supply network. For the third-order circuit (Figure 4b), the situation is similar for L_2 and R_2 .

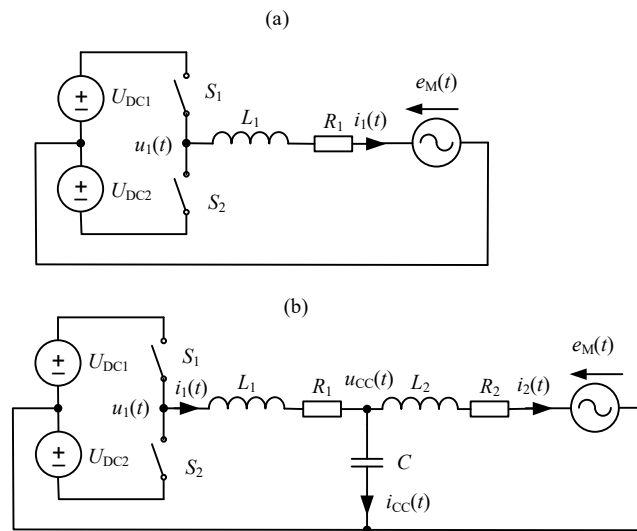


Figure 4. Examples of typical output circuits of inverters for current output: (a) first-order circuit; (b) third-order circuit.

The current transfer function of the system from Figure 4a is:

$$H(s) = \frac{I_1(s)}{U_1(s) - E_M(s)} = \frac{1}{R_1 + sL_1} \quad (4)$$

The current transfer function of the system from Figure 4b is:

$$H(s) = \frac{I_2(s)}{U_1(s)} = \frac{1}{R_1 + R_2 + s(L_1 + L_1 + C_1 R_1 R_2) + s^2(L_2 R_1 + L_1 R_2) C_1 + s^3 C_1 L_1 L_2} \quad (5)$$

For the first-order output systems depicted in Figures 3a and 4a, L_1 represents the inductance of the coil and the power supply line, while R_1 represents the resistance of the coil and the power supply line. In the case of the third-order systems shown in Figures 3c and 4b, the situation is analogous for L_2 and R_2 .

The inverter output circuits presented above do not cover all possible load combinations. For other types of output filters, the author recommends using computer software to

symbolically determine the transfer function. Examples of such software include SapWin 4 or Tina 6.02.

In Figure 5, a sample simplified schematic of an Active Power Filter (APF) is presented, which has been a subject of interest in previous studies by the author [23,28]. The APF is equipped with an LCL low-pass filter at the inverter output. This configuration was tested by the author using both analog and digital simulation tools, initially employing an L filter and subsequently an LCL filter. For improved stabilization of output currents $i_{C1}(t)$, $i_{C2}(t)$, and $i_{C3}(t)$, an algorithm version was adopted that requires additional feedback from the currents of the capacitors $i_{CC1}(t)$, $i_{CC2}(t)$, and $i_{CC3}(t)$ in the LCL output system.

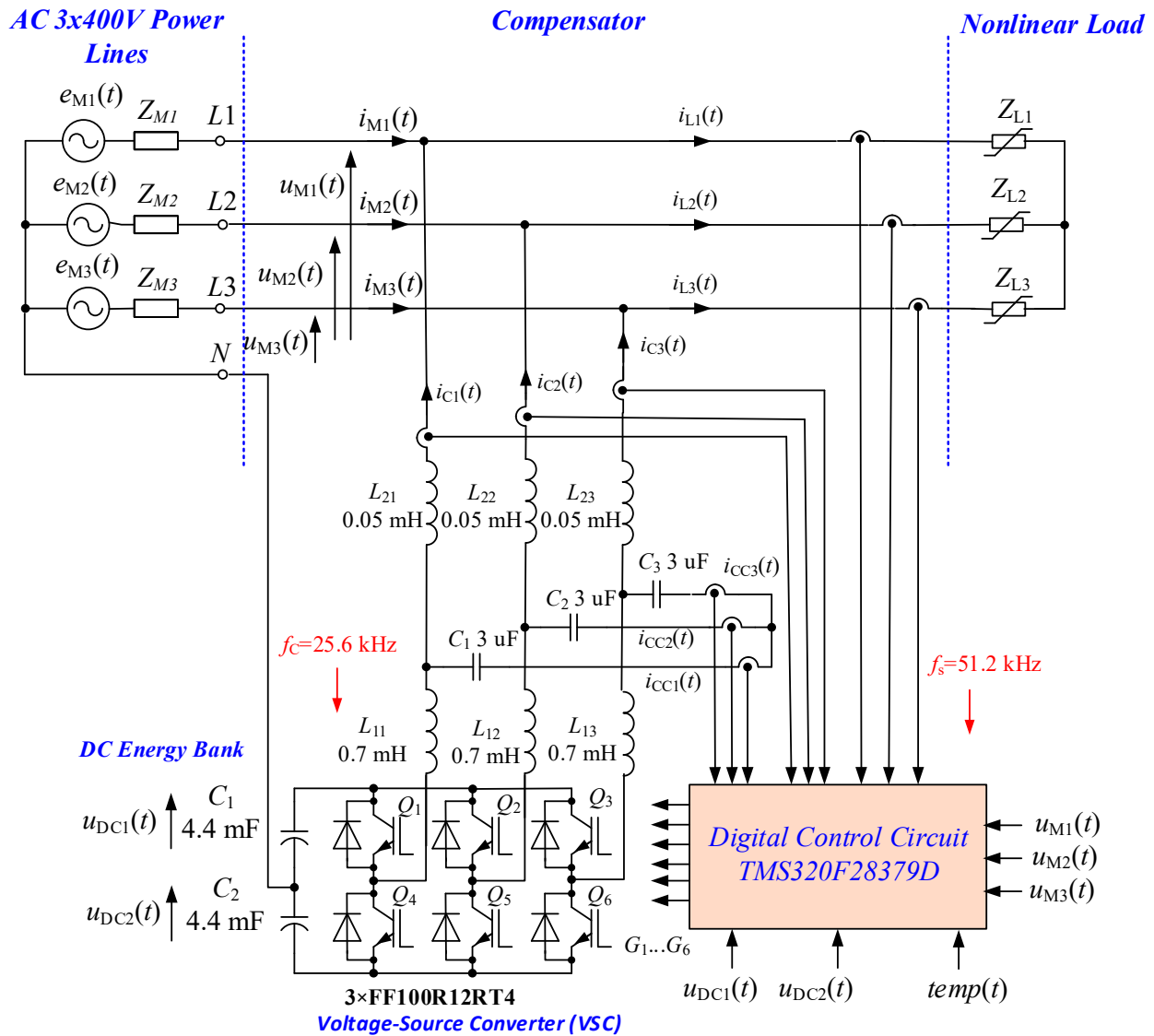


Figure 5. Diagram of the APF.

In the APF, coherent signal sampling is employed; thus, during signal sampling, a complete number of samples N is captured within one period of the power grid. For the selected value of $N = 1024$ and a grid frequency $f_M = 50$ Hz, the sampling frequency is $f_s = N \cdot f_M = 51,200$ Hz. To increase the number of processed analog signals, they are sampled every other cycle. Consequently, the effective sampling frequency is reduced to 25,600 Hz.

To avoid the occurrence of beat frequency components, the switching frequency of the inverter f_c was set to half the sampling frequency, resulting in a value of $f_c = 25,600$ Hz. For this purpose, high-speed IGBT modules of the type FF100R12RT4 from Infineon Tech-

nologies AG, Munich, Germany were utilized. The signal $temp(t)$ represents the radiator temperature and is used for controlling fan speed.

The constructed APF serves as a platform for testing algorithms in our laboratory; thus, it has been equipped with a complete set of current and voltage sensors. In some industrial applications, however, the number of sensors can be reduced to two per phase.

Currents in the APF are measured using current transducers of type ACS770LCB-050B from Allegro MicroSystems, Inc., Manchester, NH, USA while voltages are measured with AMC1311 galvanically isolated amplifiers from Texas Instruments, Dallas, TX, USA. Additionally, transistors are triggered using 2ED020I12FA galvanically isolated drivers from Infineon Technologies AG, Munich, Germany.

4. Analog Simulators

Analog simulators, in contrast to digital ones, are very simple in design and effectively replicate the simulated power elements. Therefore, in the author's opinion, their use is still recommended even when access to advanced HIL systems is available.

Figure 6 shows a very simple RC low-pass filter circuit designed for observing PWM signals that control the gate of the inverter transistors. The cutoff frequency of the RC filters should be selected based on the switching frequency of the transistors. In the author's practice, such circuits are incorporated into every control system he develops. This configuration allows for the rapid verification of waveforms generated by the PWM outputs using an oscilloscope.

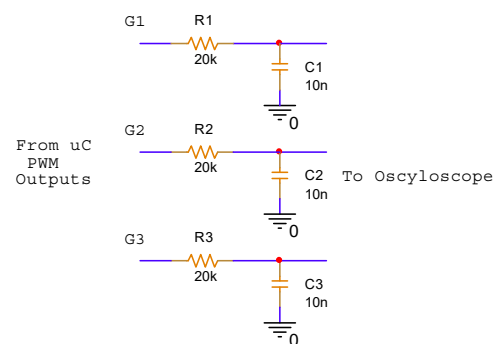


Figure 6. Simple RC low-pass filter.

Issues related to the analysis and design of analog circuits are extensively covered in the literature. Among many available sources, the author recommends the following book [29].

The diagram of the proposed first-order simulator is shown in Figure 7. Depending on the position of switch S_1 , the circuit can operate as either an integrator or an averaging circuit. Potentiometers R_{12} and R_{21} allow for the adjustment of the desired time constant.

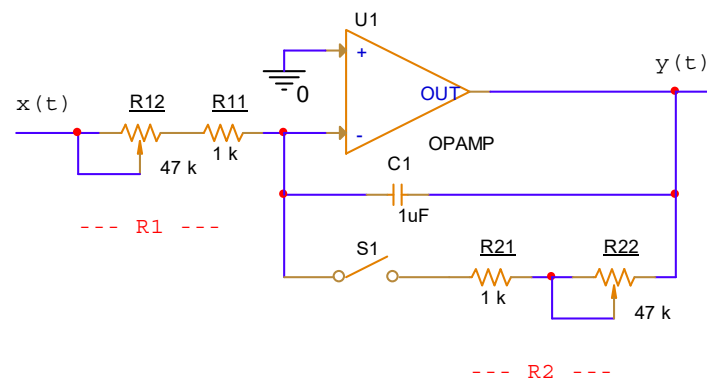


Figure 7. The diagram of a first-order analog simulator.

To avoid expanding the transfer function equations, simplifications were applied in Figures 8–10. For example, in Figure 7, the value of resistor R_1 (in red) represents the sum of resistors R_{11} and R_{12} , and the value of resistor R_2 (in red) represents the combined values of resistors R_{21} and R_{22} . The transfer functions refer specifically to the values of the resistors shown in red.

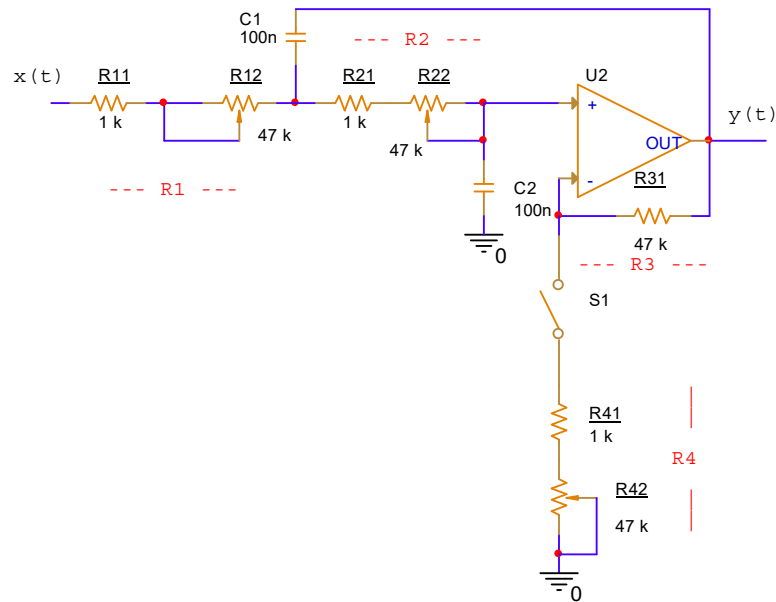


Figure 8. The diagram of a second-order analog simulator using the Sallen-Key circuit.

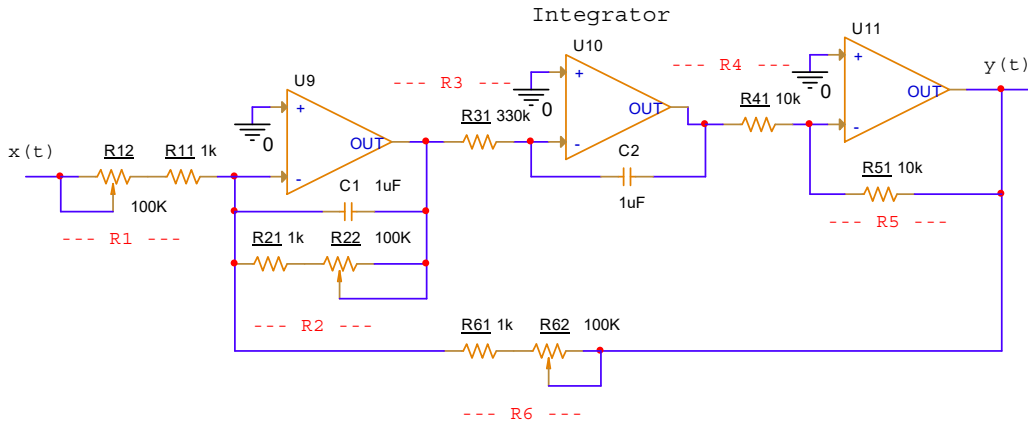


Figure 9. The diagram of a second-order analog simulator (state-variable).

The transfer function of the system when switch S_1 is in the OFF position is given by:

$$H(s) = \frac{Y(s)}{X(s)} = -\frac{1}{sR_1C_1}, \tag{6}$$

the transfer function of the system when switch S_1 is in the ON position is given by:

$$H(s) = \frac{Y(s)}{X(s)} = -\frac{R_2}{R_1 + sR_1R_2C_1}. \tag{7}$$

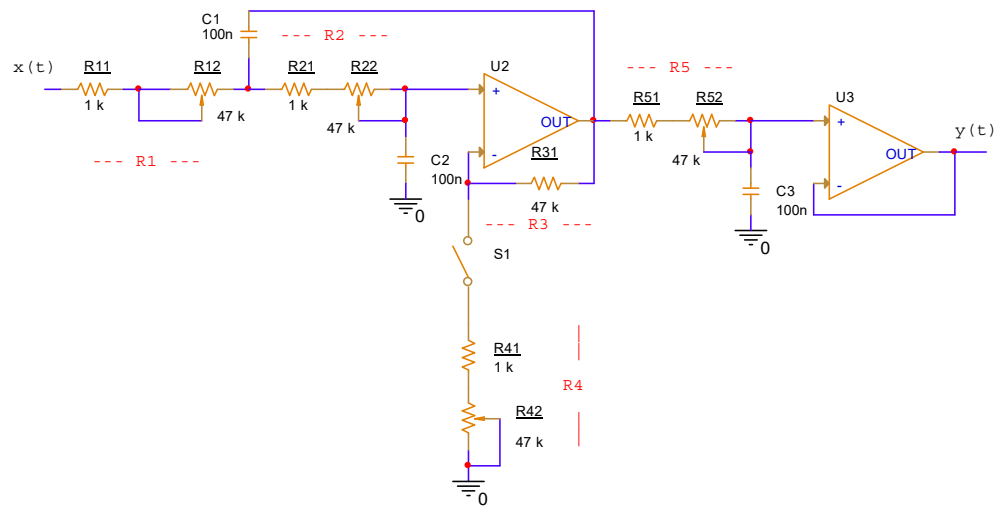


Figure 10. The diagram of a third-order analog simulator.

The second-order analog simulator using the Sallen–Key configuration is shown in Figure 8. When switch S_1 is in the OFF position, the circuit provides a unity gain for DC signals, while in the ON position, it offers adjustable gain. The transfer function of the system when switch S_1 is in the OFF position is given by:

$$H(s) = \frac{Y(s)}{X(s)} = - \frac{R_2 + R_3}{R_3 + s(R_3R_2C_1 + R_1R_3C_1 - R_1R_4C_2) + s^2(R_1R_2R_3C_1C_2)}, \quad (8)$$

the transfer function of the system when switch S_1 is in the OFF position is given by:

$$H(s) = \frac{Y(s)}{X(s)} = - \frac{1}{1 + s(R_2C_1 + R_1C_1) + s^2(R_1R_2C_1C_2)}. \quad (9)$$

Figure 9 presents the second version of the second-order analog simulator (state-variable). The transfer function of the second-order analog circuit is given by:

$$H(s) = \frac{Y(s)}{X(s)} = - \frac{R_2R_5R_6}{R_1R_2R_5 + s(C_2R_1R_3R_4R_6) + s^2(C_1C_2R_1R_2R_3R_4R_6)} \quad (10)$$

Higher-order circuits are created by cascading lower-order circuits. Figure 10 shows the schematic of a sample third-order circuit. The transfer function of the third-order analog circuit can be expressed as follows.

$$H(s) = \frac{Y(s)}{X(s)} = - \frac{1}{1 + s(R_2C_1 + R_1C_1 + R_5C_3) + s^2(R_1R_2C_1C_2 + R_2R_5C_3C_2 + R_1R_5C_3C_1) + s^3(R_1R_2R_5C_3C_2C_1)}. \quad (11)$$

The author constructed three single-phase, first-order analog simulators designed for three-phase applications. The diagram and a detailed view of the proposed solution are presented in Figures 11 and 12. The circuit incorporates two versatile fiber-optic receivers, U_1 and U_6 HFBR-2522Z from Micro-Semiconductor, Hong Kong, China, at the input; alternatively, binary inputs can be used.

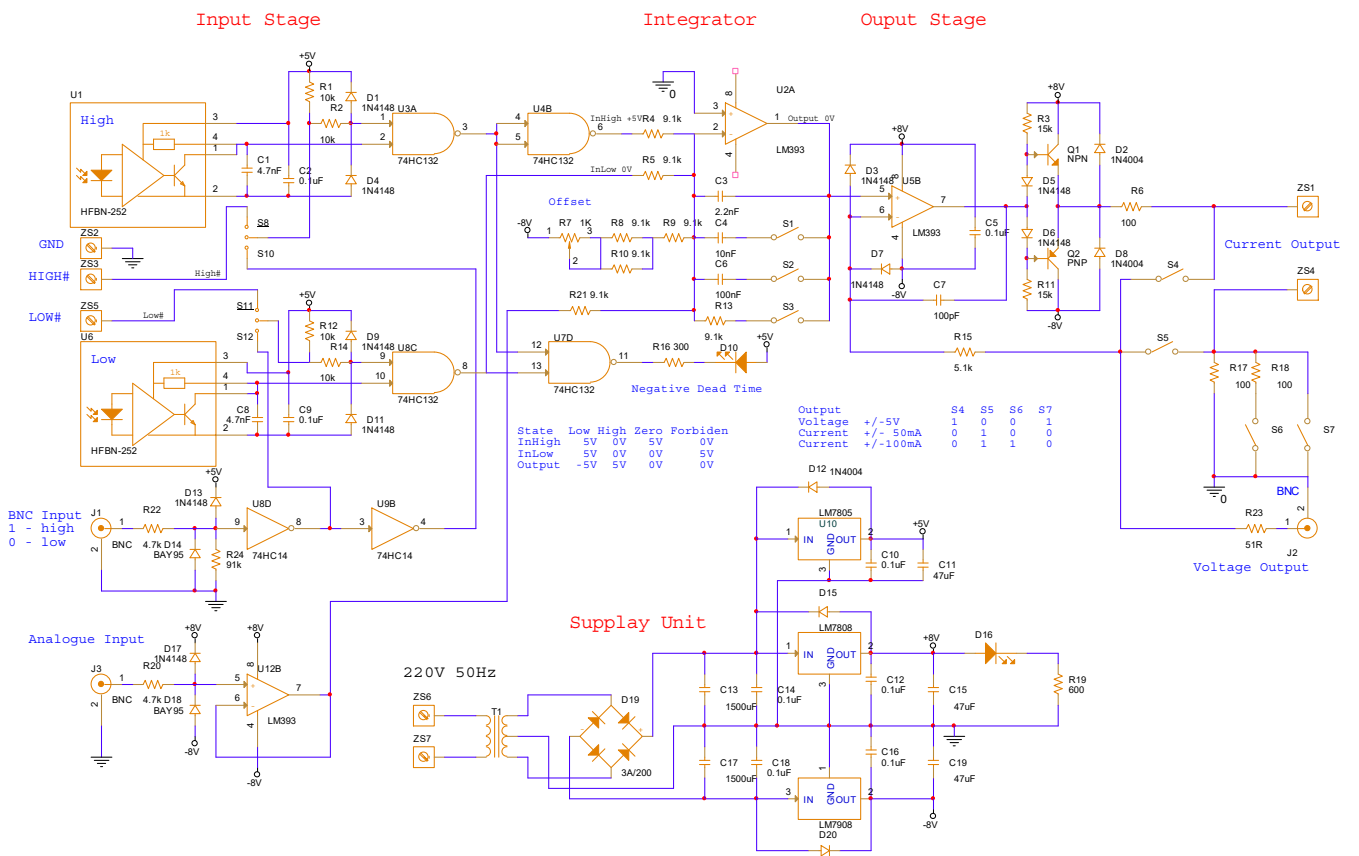


Figure 11. The detailed diagram of the analog simulator designed by the author.

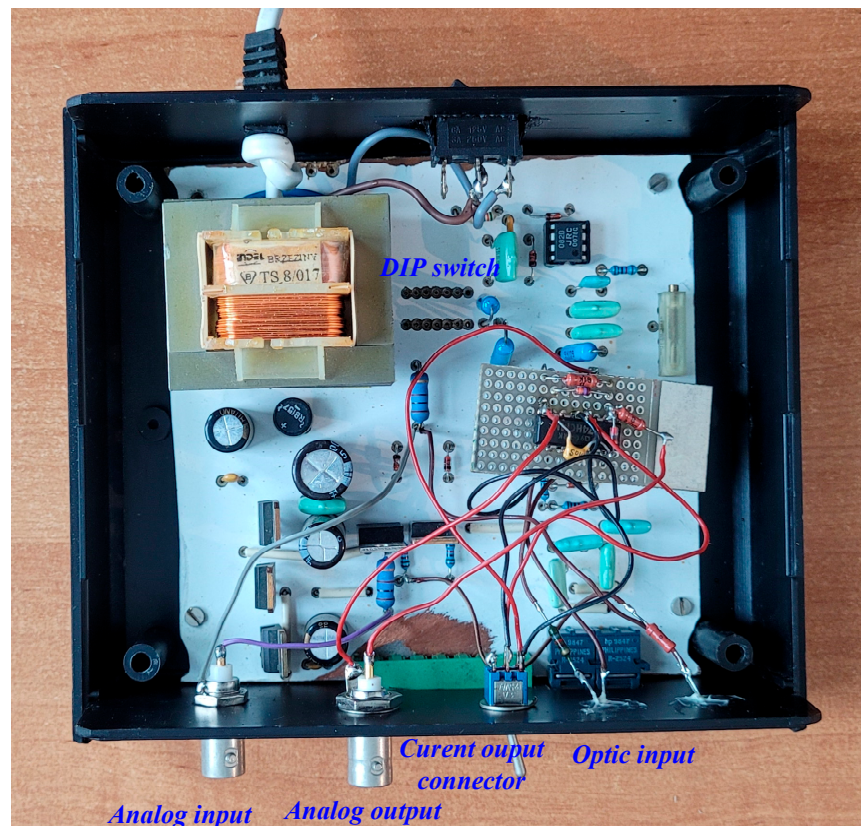


Figure 12. The view of the analog simulator designed by the author.

An integrator circuit, U_{2A} , identical to the one shown in Figure 7, is employed as the object simulator. The circuit is equipped with switches S_1 and S_2 to adjust the time constant. When switch S_3 is in the OFF position, the circuit operates as an integrator; otherwise, it functions as a first-order inertial system. Resistor R_7 allows for offset voltage adjustment of the integrator.

Additionally, an analog input has been incorporated to interface with a signal corresponding to the power grid voltage. The output can be configured as a current signal, providing ± 50 mA or ± 100 mA, similar to the output of a current transducer (e.g., LA-55-P from LEM International SA, Meyrin Switzerland), or as a voltage signal. The output circuit includes DIP switches (S_4 – S_7) for configuration adjustments.

The entire simulator circuit is powered by ± 8 V and 5 V supplies. This setup has proven effective in the development and testing of power electronics circuits.

A schematic of a simplified version of the first-order simulator designed for an analog voltage range of 0 to 3 V is shown in Figure 13.

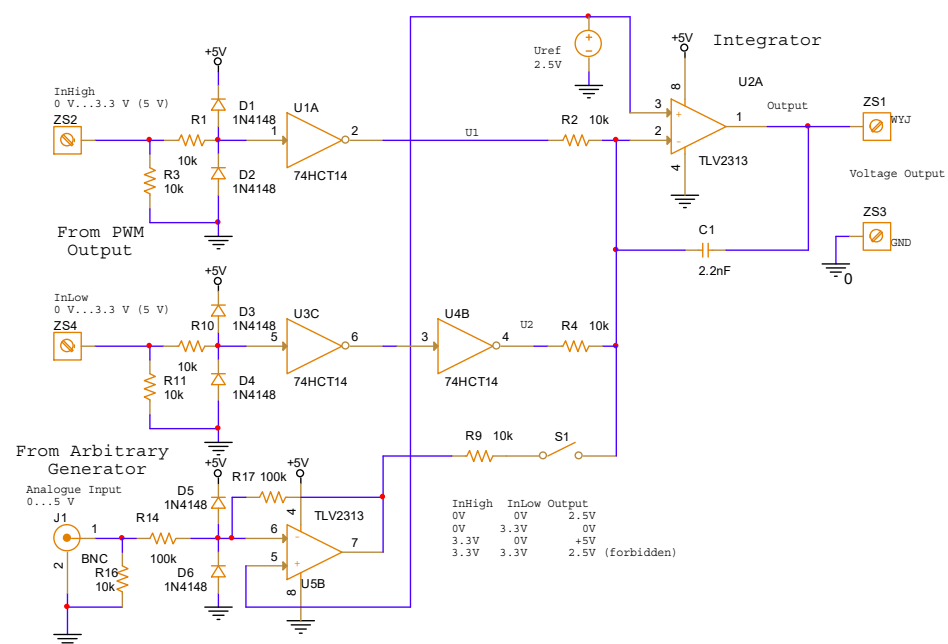


Figure 13. The diagram of an analog simulator.

The time constant values in analog simulators should be selected to appropriately represent the output system of the power electronics circuit. The adjustment of the time constant is carried out using potentiometers. Additionally, the capacitance values of the capacitors must be chosen to achieve the required range for setting the time constants.

The aforementioned analog circuits can be modified by replacing traditional potentiometers with electronic ones. This modification would enable programmability for the circuits.

5. Selected Methods of Discretization of Analog Model

Traditionally, power electronics circuits and their control circuits are described in the analog domain. Consequently, a significant portion of the digital control circuits discussed in the literature [18–28] are still represented using analog transfer functions, $H(s)$, rather than digital transfer functions, $H(z)$. Therefore, to implement a digital simulator, it is essential to convert the analog circuit to a digital circuit. Several transformation techniques can be employed for this conversion, including bilinear, matched bilinear, impulse invariant, matched pole-zero, backward integration, and forward integration methods [23,28–44]. The specific characteristics of the resulting digital circuit depend on the method selected. Among the aforementioned techniques, the bilinear method is the most versatile and

flexible, as it utilizes a first-order approximation to map the analog transfer function onto the digital domain. The bilinear transform employs first-order approximation to map the analog transfer function to a digital one.

$$H_d(z) = H_a(s)|_{s=\frac{2}{T_s} \frac{z-1}{z+1}} = H_a\left(\frac{2}{T_s} \frac{z-1}{z+1}\right). \tag{12}$$

The bilinear transformation introduces a nonlinear distortion between the analog frequency f_a and the digital frequency f_d . This distortion becomes more significant at higher frequencies, particularly near $f_s/2$, where the frequency response undergoes compression. The nonlinear relationship between the analog and digital frequencies is mathematically expressed as:

$$f_d = \frac{1}{\pi T_s} \arctan(\pi f_a T_s). \tag{13}$$

Figure 14 illustrates the process of converting a third-order analog circuit into a third-order digital circuit. The transfer function of the analog system is described by the equation:

$$H_a(s) = \frac{R_2}{R_2 + R_1 + (C_1 R_1 R_2 + L_1 + L_2)s + (C_1 L_2 R_1 + C_1 L_1 R_2)s^2 + (C_1 L_1 L_2)s^3}. \tag{14}$$

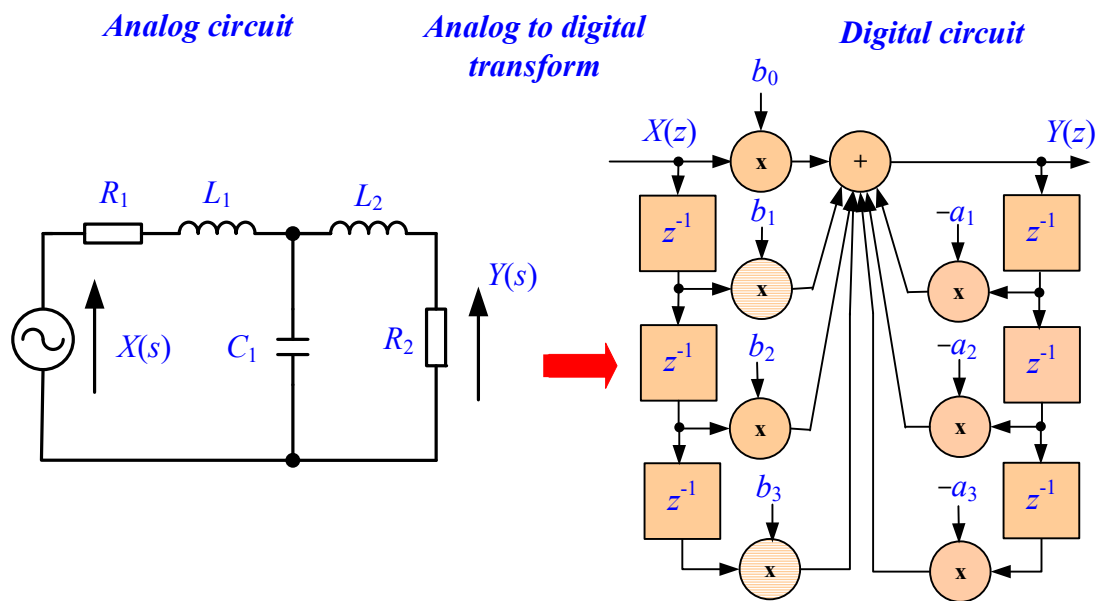


Figure 14. An example of converting a third-order analog circuit to a digital one.

The example considers a third-order Butterworth filter with a cutoff frequency of $f_g = 50$ Hz. The circuit element values are $R_1 = 1 \Omega$, $R_2 = 1 \Omega$, $L_1 = 3.183$ mH, $L_2 = 3.183$ mH, and $C_1 = 6.366$ mF. For these parameters, the transfer function of the analog system is given by:

$$H_a(s) = \frac{R_2}{2 + 0.01273s + 4.053 \cdot 10^{-5}s^2 + 6.45 \cdot 10^{-8}s^3}. \tag{15}$$

Subsequently, the analog system is converted into a digital system using bilinear transformation with a sampling frequency of $f_s = 1$ kHz. The transfer function of the resulting digital system is given by the equation:

$$H_d(z) = \frac{0.001449 + 0.004348z^{-1} + 0.004348z^{-2} + 0.001449z^{-3}}{1 - 2.374z^{-1} + 1.929z^{-2} - 0.5321z^{-3}}. \tag{16}$$

Figure 15 illustrates the frequency responses of the analog and digital circuits. Specifically, Figure 15a compares the magnitude frequency responses of the analog circuit and its digital equivalent, while Figure 15b presents their phase responses. The analog circuit exhibits a frequency response extending from zero to infinity, whereas the frequency response of the digital circuit is constrained to the range of zero to $f_s/2$. Consequently, the characteristics of analog and digital circuits diverge, particularly near $f_s/2$. As shown in the figure, the analog circuit demonstrates distinct behavior compared to its digital counterpart, with the differences becoming more pronounced as the frequency approaches $f_s/2$. However, these discrepancies may be negligible if the sampling frequency f_s and/or the power transistor switching frequency f_c are significantly higher than the highest frequency component of interest.

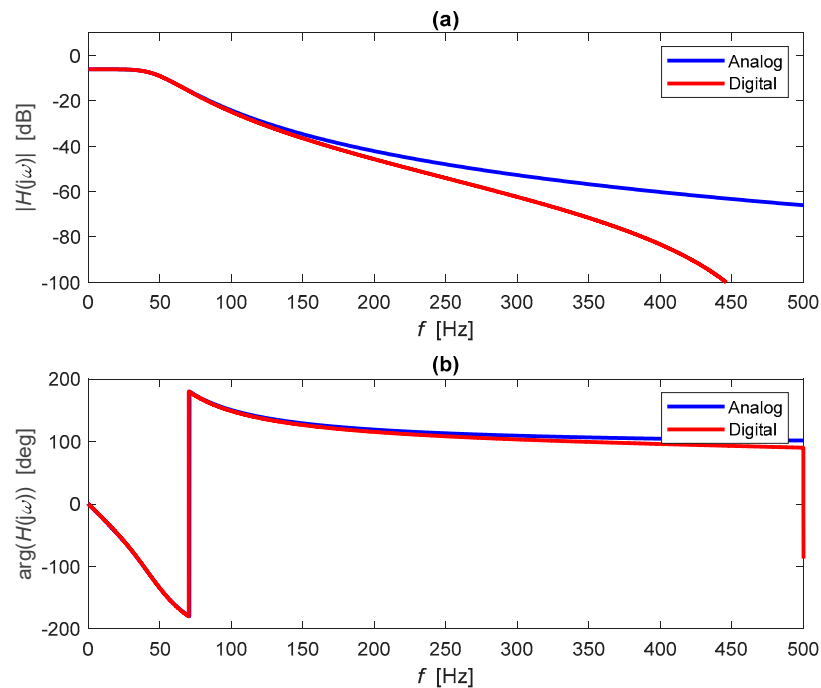


Figure 15. Frequency responses of the analog circuit and the digital circuit: (a) magnitude, (b) phase.

An alternative representation of the analog circuit is the well-known description [45–49] in the form of continuous state space (S -domain). In this framework, the system is described by the following:

$$\begin{cases} \frac{dx(t)}{dt} = Ax(t) + Bu(t) \\ y(t) = Cx(t) + Du(t) \end{cases} \quad (17)$$

To implement the digital version, Equation (12) must be discretized for a sampling period T_s . It is assumed that the sampling period is constant. The discrete state space is obtained from the continuous state space.

$$\begin{cases} x(n+1) = A_D x(n) + B_D u(n) \\ y(n) = C_D x(n) + D_D u(n) \end{cases} \quad (18)$$

where A_D , B_D , C_D , D_D —discrete version of A , B , C , D .

To determine A_D , B_D , C_D , and D_D , typical methods for converting analog systems to digital systems can be applied: Euler's method, bilinear transformation, backward integration, and forward integration, among others. The most universal method of discretization is bilinear transformation.

The coefficients A_D , B_D , C_D , D_D can be determined from the equations:

$$\begin{cases} A_D = \left(I + \frac{AT_s}{2} \right) \left(I - \frac{AT_s}{2} \right)^{-1} \\ B_D = \left(I - \frac{AT_s}{2} \right)^{-1} B \sqrt{T_s} \\ C_D = \left(I - \frac{AT_s}{2} \right)^{-1} C \sqrt{T_s} \\ D_D = D + C \left(I - \frac{AT_s}{2} \right)^{-1} B \sqrt{T_s} \end{cases} \quad (19)$$

After establishing the digital model, it is advisable to verify its performance using programs such as MATLAB, Octave, Scilab, or Python with libraries like Matplotlib and NumPy. The proposed microcontroller, equipped with a built-in IEEE 754 double-precision unit enables reliable comparisons of simulation results.

6. Digital Simulators

To simplify the construction of the simulator circuit, it has been assumed that the input and output voltage ranges will correspond to those available in the microcontroller module, specifically 0 to 3.3 V for digital signals and 0 to 3 V for analog signals. This necessitates connecting the signals directly to the control microcontroller. While it is possible to expand the simulator circuit with appropriate interface circuits (similar to the configuration shown in Figure 11), doing so at this stage of the project would significantly complicate the design. It has been assumed that a typical F28388D evaluation module MCU controlCARD from Texas Instruments, Dallas, TX, USA [50] is utilized without any modifications.

The block diagram of the proposed digital simulator is depicted in Figure 16. The microcontroller is equipped with four 16/12-bit A/D converters with simultaneous sampling and analog multiplexers at the inputs, allowing for the processing of more than four analog signals. For converting PWM signals into digital words, seven Enhanced Capture (eCAP) modules are utilized for duty cycle measurements of pulse train signals, with high-resolution capture (HRCAP) available on two of the seven eCAP modules. The output signals are processed by three 12-bit D/A converters. If there is a need to expand the number of outputs, an additional 16-bit D/A converter, specifically the DAC80504 from Texas Instruments, Dallas, TX, USA with an SPI interface, is used.

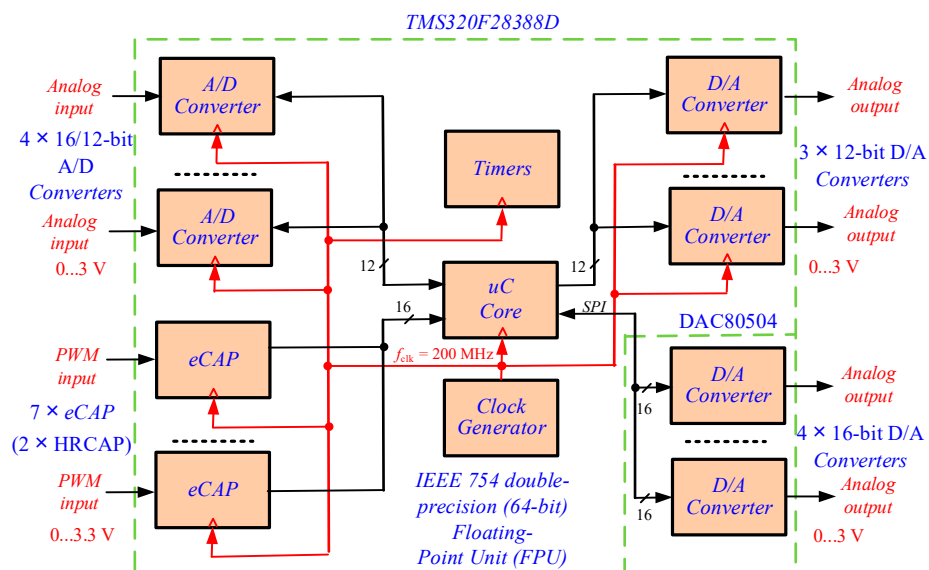


Figure 16. The block diagram of the proposed digital simulator.

In the digital simulator system, proper signal sampling is essential. In the proposed solutions, a constant sampling period (uniform sampling) has been adopted. For the

system with analog inputs and outputs, one of the microcontroller's timers is utilized to generate sampling pulses that trigger the A/D and D/A converters. Upon completion of the conversion, one of the A/D converters generates an interrupt during which data are collected from the A/D converters and calculations are performed. Subsequently, new data are sent to the D/A converters. The entire process is executed within the interrupt service routine. The timing of the analog input for the digital simulator is shown in Figure 17.

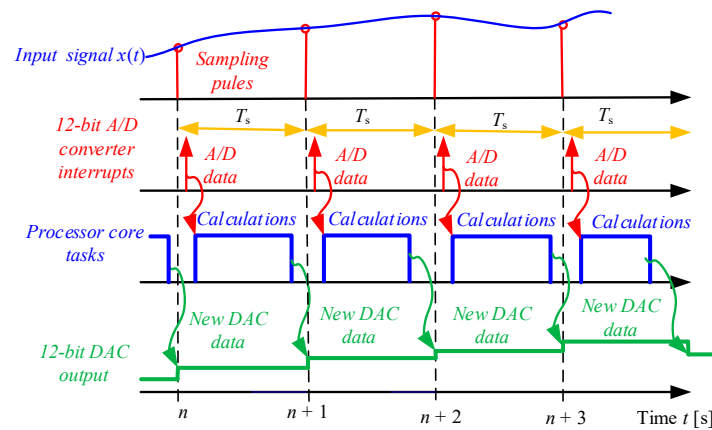


Figure 17. Timing diagram of the digital simulator for analog input.

It should be noted that when simulating the output stages of the inverter, the input signal is a PWM signal, which must be converted into a digital signal. For this purpose, the eCAP modules, integrated into the TMS320F28388D microcontroller, are used.

In the case of the simulator with a PWM input, it has been assumed that one of the PWM inputs triggers the A/D converters on the rising edge. Upon completion of the processing by the A/D converter, it generates an interrupt, during which data are collected from the A/D converters and the eCAPs, and all calculations are performed. Subsequently, new data are sent to the D/A converters. Interrupts from the eCAPs are also enabled in the microcontroller to transmit data regarding the PWM pulse widths. The timing of the digital simulator for PWM input is shown in Figure 18. In this configuration, the sampling period of the signals is equal to the period of the PWM signals. It is also assumed that the periods of the PWM signals are equal to one another.

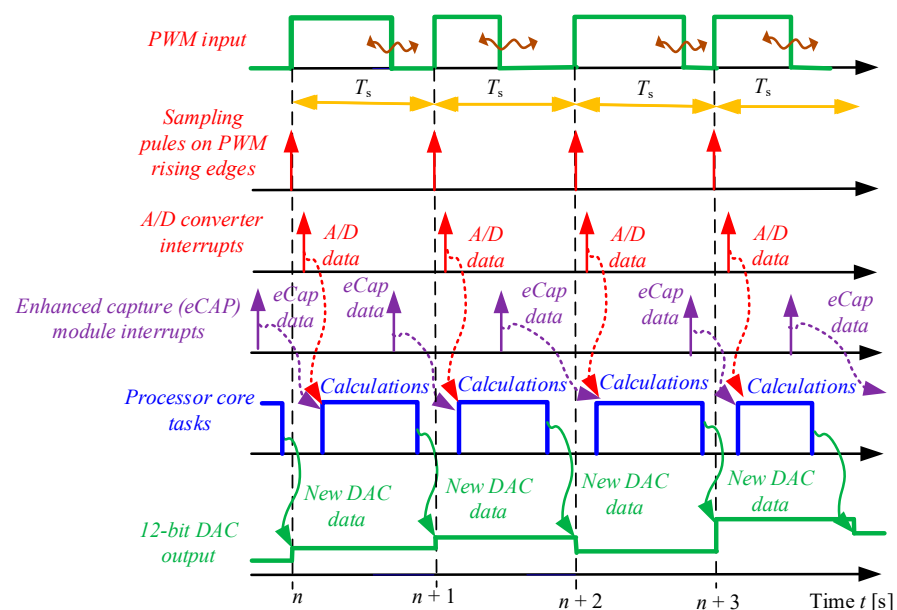


Figure 18. Timing diagram of the digital simulator for PWM input.

The implemented solutions help reduce the impact of jitter and the occurrence of ringing, which can degrade the quality of the simulation [49]. Assuming, of course, that the PWM signal generated by the control system is stable, in such a system, the sampling moment is also stable.

To verify the correct operation of the proposed digital system, laboratory tests were conducted. The schematic of the testing circuit for the digital simulator is shown in Figure 19. An APx515 Audio Analyzer from Audio Precision, Beaverton, OR, USA was used to test the simulator, enabling efficient evaluation of the frequency response. Since the analyzer has analog outputs, an analog-to-PWM converter was necessary. This converter was constructed using the TMS320F28388D microcontroller as well.

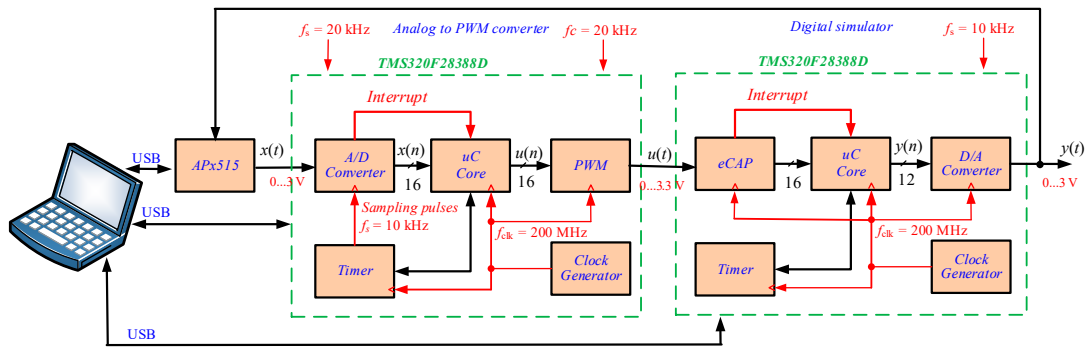


Figure 19. Testing circuit for the digital simulator.

To test the digital simulator, four exemplary eighth-order digital IIR filters were implemented: Butterworth, Chebyshev Type I, Chebyshev Type II, and Elliptic, with a cutoff frequency of $f_g = 50$ Hz and a sampling frequency of $f_s = 10,000$ Hz.

To improve the accuracy of calculations, the filters were implemented using a cascaded connection of four second-order filter stages. The block diagram of this filter implementation is shown in Figure 20. The frequency response characteristics of the filters, implemented in MATLAB R2022B, are illustrated in Figure 21.

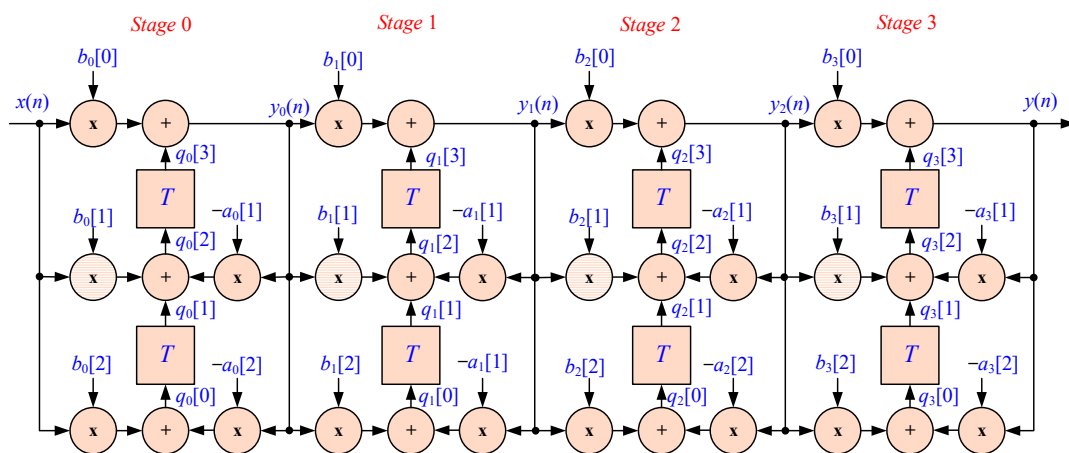


Figure 20. Block diagram of eighth-order IIR filter, cascaded connection of four second-order filter stages.

In the next step, the above filters were implemented using the TMS320F28388D microcontroller. As previously mentioned, the entire algorithm is executed during an interrupt. In this case, the interrupt is generated by the eCAP module. Listing 1 presents the C program that implements the aforementioned filters.

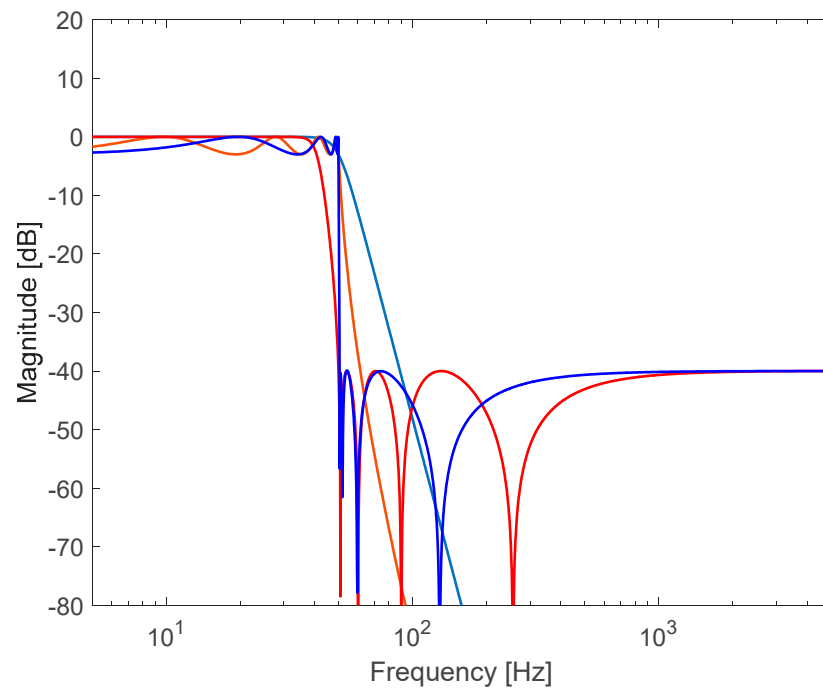


Figure 21. Numerically calculated frequency response of the exemplary object, eighth-order IIR filters, for $f_g = 50$ Hz, and $f_s = 10,000$ Hz; Butterworth (orange), Chebyshev Type 1 (green), Chebyshev Type 2 (red), Elliptic (blue).

Subsequently, the implemented filters were tested in the test setup shown in Figure 19. The frequency response characteristics of the implemented filters are illustrated in Figure 22. As shown in the graph, an excellent match was achieved between the characteristics of the digital filters and those presented in Figure 21.

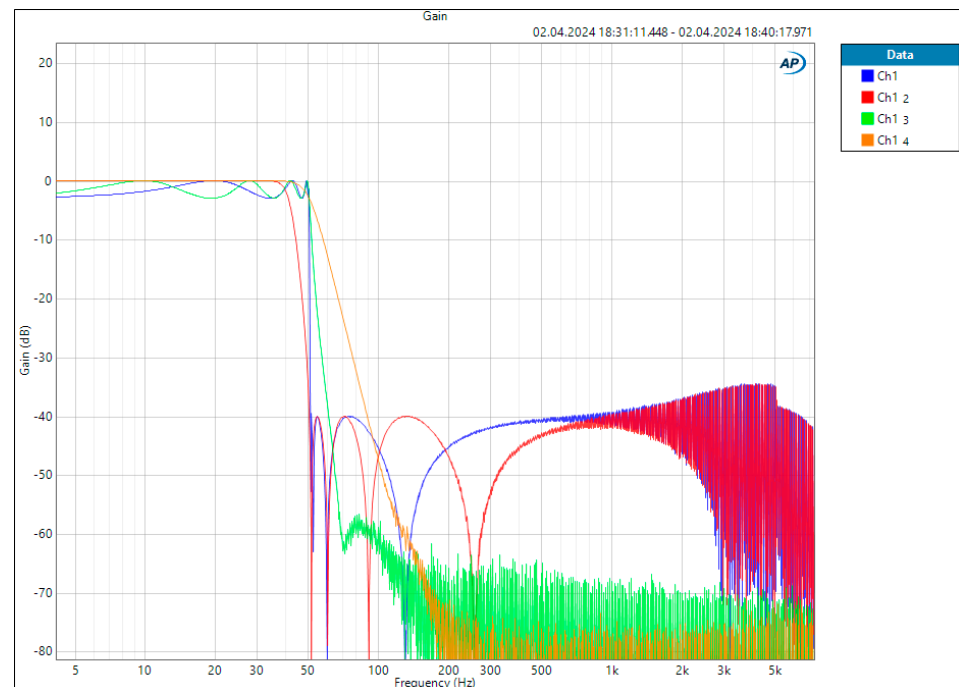


Figure 22. Measured frequency response of the exemplary object, 8th-order IIR filters, for $f_g = 50$ Hz, and $f_s = 10,000$ Hz; Butterworth (orange), Chebyshev Type 1 (green), Chebyshev Type 2 (red), Elliptic (blue).

Listing 1. An eighth-order IIR filter, implemented during an interrupt generated by the A/D converter.

```

1. x = (float) (adc_val); // data from A/D converter or eCAP
2. //stage 0
3. y0 = x*b0[0] + q0[3];
4. q0[2] = x*b0[1] - y0*a0[1] + q0[1];
5. q0[3] = q0[2];
6. q0[0] = x*b0[2] - y0*a0[2];
7. q0[1] = q0[0];
8. //stage 1
9. y1 = y0*b1[0] + q1[3];
10. q1[2] = y0*b1[1] - y1*a1[1] + q1[1];
11. q1[3] = q1[2];
12. q1[0] = y0*b1[2] - y1*a1[2];
13. q1[1] = q1[0];
14. //stage 2
15. y2 = y1*b2[0] + q2[3];
16. q2[2] = y1*b2[1] - y2*a2[1] + q2[1];
17. q2[3] = q2[2];
18. q2[0] = y1*b2[2] - y2*a2[2];
19. q2[1] = q2[0];
20. //stage 3
21. y = y2*b3[0] + q3[3]; // output signal
22. q3[2] = y2*b3[1] - y*a3[1] + q3[1];
23. q3[3] = q3[2];
24. q3[0] = y2*b3[2] - y*a3[2];
25. q3[1] = q3[0];

```

Returning to the APF system shown in Figure 2, Figure 23 presents the schematic of the simulation for the output stage with the LCL filter. In the APF control circuit, two analog signals are processed: one from the capacitor current $i_{CC}(t)$ and the other from the output current $i_2(t)$. Additionally, the circuit is synchronized with the supply voltage $e_M(t)$. The control system generates two signals, G_1 and G_4 which control the power transistors of the inverter. A simplified analog model of the output circuit is depicted in Figure 24 [51–54]. This model has been discretized and implemented in the TMS320F28388D microcontroller of the digital simulator.

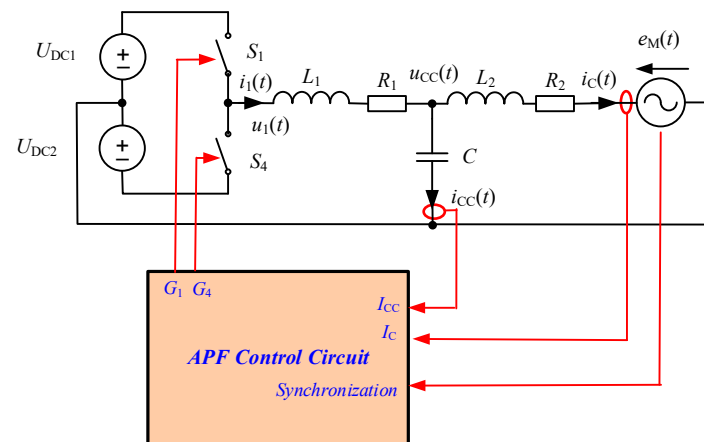


Figure 23. Simplified diagram of the single-phase output system of the Active Power Filter (APF) circuit.

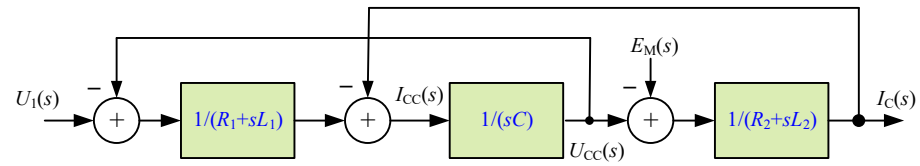


Figure 24. Simplified diagram of the analog model of the single-phase Active Power Filter (APF) output system.

Figure 25 illustrates the diagram of the digital simulation of the single-phase APF output system. The system is designed to incorporate an arbitrary signal generator or the supply voltage as the signal input $e_M(t)$.

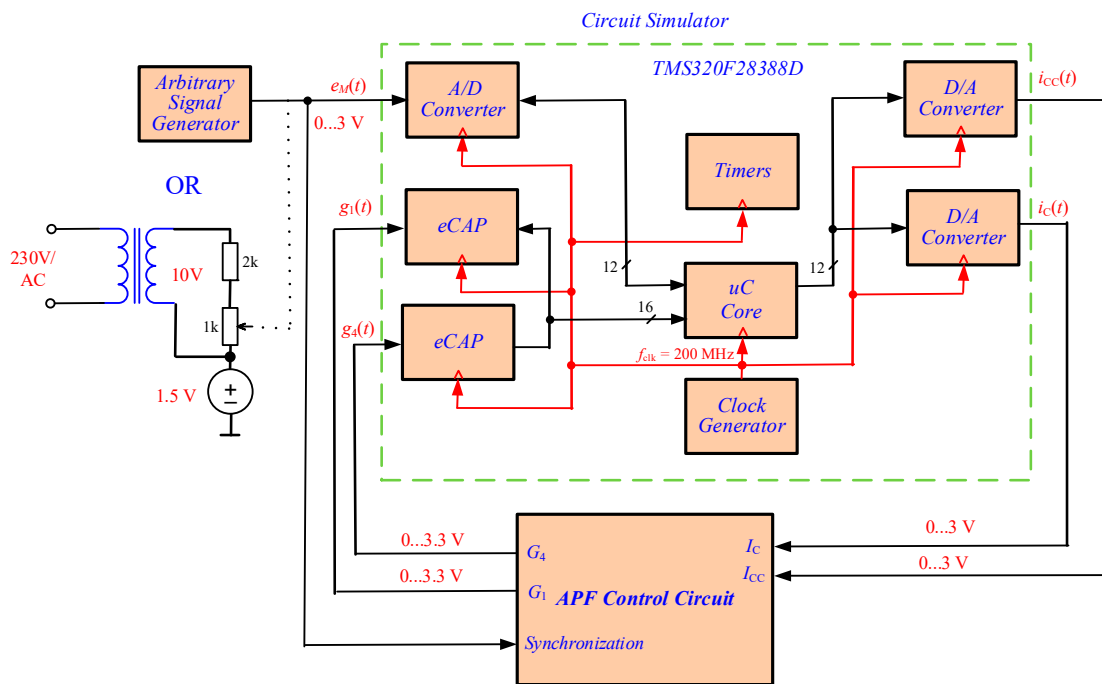


Figure 25. Diagram of digital simulation of the single-phase Active Power Filter (APF) output system.

Laboratory tests of the simulator system (Figure 25) were conducted, confirming its utility for the developing and testing of the control system.

7. Conclusions

This paper presents a low-cost alternative for power electronics circuit simulators. Analog systems have a relatively simple structure, but are not suitable for simulating more complex circuits. The accuracy of representing simple circuits with analog systems is relatively good. Additionally, analog systems do not require programming skills from the user, and their operation is straightforward. In contrast, the proposed concept of using a popular microcontroller as a digital simulator for power electronics circuits necessitates knowledge in programming and signal processing.

While this low-cost circuit simulator has limited capabilities compared to commercial HIL solutions and is not as user-friendly, I believe that an experienced embedded systems programmer can create an efficient simulation environment. The proposed solution utilizes the TMS320F28388D microcontroller due to its advanced eCAP systems, which allow for precise measurement of the duty cycle of the control pulses for the inverter’s power transistors. An additional advantage of the microcontroller is its IEEE 754 double-precision (64-bit) Floating-Point Unit (FPU), which enables the use of programs like Matlab, Octave, Scilab, and Python, with libraries Matplotlib and NumPy, for verifying implemented simulation algorithms.

It is important to note that using an advanced programmable device like an FPGA, as seen in commercial HIL systems, could provide higher system functionalities. However, this requires the designer to possess a strong understanding of programming such systems.

However, it is important to note that, as with any simulation, the results should be approached critically and continuously verified.

The analog simulators presented in the paper are a simple alternative to digital simulators. Based on the author's experience, they perform excellently for simulating simpler cases.

The proposed solution, of course, cannot replace professional simulators with extensive capabilities. However, it can serve as an excellent solution for simplified applications, offering a fraction of the cost compared to professional alternatives. An additional advantage is the high degree of flexibility in creating custom simulation algorithms.

Funding: This research received no external funding.

Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of Interest: The author declares no conflicts of interest.

References

- Available online: https://www.opal-rt.com/power-hardware-in-the-loop/?gad_source=1&gclid=CjwKCAjw1NK4BhAwEiwAVUHPUOiStyjej-b5e6gUODtwKPwZ_D-7ijuaMDrR6jISpSIDzstROKZPKdRoC_wwQAvD_BwE (accessed on 1 June 2024).
- Available online: <https://www.typhoon-hil.com/> (accessed on 1 June 2024).
- Available online: <https://www.ni.com/en/solutions/industrial-machinery/hil-testing.html> (accessed on 2 June 2024).
- Available online: <https://imperix.com/> (accessed on 2 June 2024).
- Peralta, J.; Calderon, D.; Estrada, L.; Ortega, J.; Vazquez, N.; Limones, C. Semi-Custom HIL Simulation of a Three-Phase Power Inverter. In Proceedings of the 2023 IEEE International Conference on Engineering Veracruz (ICEV), Boca del Río, Veracruz, Mexico, 23–26 October 2023; pp. 1–6. [\[CrossRef\]](#)
- Maurya, S.; Binod, S.; Srivastava, A.; Baluni, A.; Poddar, S.; Mathew, L. Controller Hardware in Loop Simulation (C-HIL) for Grid-Connected Photovoltaic System. In Proceedings of the 2021 IEEE 2nd International Conference on Smart Technologies for Power, Energy and Control (STPEC), Bilaspur, Chhattisgarh, India, 19–22 December 2021; pp. 1–6. [\[CrossRef\]](#)
- Pop, A.A.; Ruba, M.; Nemeş, R.O.; Raia, R.; Martiş, C.; Husar, C. Benchmarking methods for parameters identification of supercapacitors using Typhoon HiL. In Proceedings of the 2022 IEEE 20th International Power Electronics and Motion Control Conference (PEMC), Brasov, Romania, 25–28 September 2022; pp. 167–173. [\[CrossRef\]](#)
- Brandis, A.; Pelin, D.; Topić, D.; Knežević, G. Half-Bridge Voltage Source Inverter Control Development Using HIL System. In Proceedings of the 2021 21st International Symposium on Power Electronics (Ee), Novi Sad, Serbia, 27–30 October 2021; pp. 1–6. [\[CrossRef\]](#)
- Roshandel Tavana, N.; Dinavahi, V. A General Framework for FPGA-Based Real-Time Emulation of Electrical Machines for HIL Applications. *IEEE Trans. Ind. Electron.* **2015**, *62*, 2041–2053. [\[CrossRef\]](#)
- Saito, K.; Akagi, H. A Power Hardware-in-the-Loop (P-HIL) Test Bench Using Two Modular Multilevel DSCC Converters for a Synchronous Motor Drive. *IEEE Trans. Ind. Appl.* **2018**, *54*, 4563–4573. [\[CrossRef\]](#)
- Park, N.K.; Forsyth, P.; Kuffel, R.; Tara, E. Hardware in the loop (HILS) testing of a power electronics controller with RTDS. In Proceedings of the IECON 2013—39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, Austria, 10–13 November 2013; pp. 5386–5391. [\[CrossRef\]](#)
- Funaki, H.; Noge, Y.; Shoyama, M.; Yonezawa, Y.; Miyazawa, A. Construction of HILS System for LLC Resonant Converter Using LPV Model. *IEEE Trans. Ind. Appl.* **2024**, *60*, 3297–3305. [\[CrossRef\]](#)
- Lauss, G.; Strunz, K. Accurate and Stable Hardware-in-the-Loop (HIL) Real-Time Simulation of Integrated Power Electronics and Power Systems. *IEEE Trans. Power Electron.* **2021**, *36*, 10920–10932. [\[CrossRef\]](#)
- Liu, T.; Xu, R.; Jiang, Q.; Li, B.; Blaabjerg, F.; Wang, P. Multiple Switching Functions Based HSS Model of LCC Considering Variable Commutation Angle and Harmonic Couplings. *IEEE Trans. Power Deliv.* **2023**, *38*, 3820–3833. [\[CrossRef\]](#)
- Viehweider, A.; Lauss, G.; Felix, L. Stabilization of Power Hardware-in-the-Loop simulations of electric energy systems. *Simul. Model. Pract. Theory* **2011**, *19*, 1699–1708. [\[CrossRef\]](#)
- De Souza, I.D.T.; Silva, S.N.; Teles, R.M.; Fernandes, M.A.C. Platform for Real-Time Simulation of Dynamic Systems and Hardware-in-the-Loop for Control Algorithms. *Sensors* **2014**, *14*, 19176–19199. [\[CrossRef\]](#)
- TMS320F28388x Real-Time Microcontrollers with Connectivity Manager, Data Sheet, Texas Instruments. 2023. Available online: <https://www.ti.com/lit/ds/symlink/tms320f28388d.pdf> (accessed on 10 June 2024).
- Mohan, N.; Undeland, T.M.; Robbins, W.P. *Power Electronics, Converters, Applications and Design*; John Wiley & Sons, Inc.: Hoboken, NJ, USA, 1995.
- Kazmierkowski, M.P.; Kishnan, R.; Blaabjerg, F. *Control in Power Electronics*; Academic Press: Cambridge, UK, 2002.

20. Trzynadlowski, A. *Introduction to Modern Power Electronics*; Wiley-Interscience a John Wiley & Sons, Inc.: Hoboken, NJ, USA, 2010.
21. Bose, B.K. *Power Electronics and Motor Drives: Advances and Trends*; Academic Press: Cambridge, UK, 2006.
22. Bataarseh, I.; Harb, A. *Power Electronics Circuit Analysis and Design*, 2nd ed.; Springer: London, UK, 2018.
23. Sozański, K. *Digital Signal Processing in Power Electronics Control Circuits*, 2nd ed.; Springer: London, UK, 2017.
24. Erickson, R.W.; Maksimovic, D. *Fundamentals of Power Electronics*; Kluwer Academic Publishers: New York, NY, USA, 2004.
25. Rashid, M. *SPICE for Power Electronics and Electric Power*, 3rd ed.; CRC Press Taylor & Francis Group: Abingdon, UK, 2012.
26. Emadi, A.; Khaligh, A.; Nie, Z.; Lee, Y. *Integrated Power Electronic Converters and Digital Control*; CRC Press Taylor & Francis Group: Abingdon, UK, 2009.
27. Rashid, M. (Ed.) *Power Electronics Handbook Devices, Circuits, and Applications*, 3rd ed.; Elsevier Inc.: Amsterdam, The Netherlands, 2011.
28. Sozanski, K.; Szczesniak, P. Advanced Control Algorithm for Three-Phase Shunt Active Power Filter Using Sliding DFT. *Energies* **2023**, *16*, 1453. [[CrossRef](#)]
29. Moschytz, G.S. *Analog Circuit Theory and Filter Design in the Digital World*; Springer: Berlin/Heidelberg, Germany, 2019.
30. Rabiner, L.R.; Gold, B. *Theory and Application of Digital Signal Processing*; Prentice Hall Inc.: Hoboken, NJ, USA, 1975.
31. Crochiere, R.E.; Rabiner, L.R. *Multirate Digital Signal Processing*; Prentice Hall Inc.: Hoboken, NJ, USA, 1983.
32. Oppenheim, A.V.; Schaffer, R.W. *Discrete-Time Signal Processing*; Prentice Hall: Hoboken, NJ, USA, 1999.
33. Proakis, J.G.; Manolakis, D.M. *Digital Signal Processing, Principles, Algorithms, and Application*; Prentice Hall Inc.: Hoboken, NJ, USA, 1996.
34. Orfanidis, S.J. *Introduction to Signal Processing*; Prentice Hall, Inc.: Hoboken, NJ, USA, 2010.
35. Lyons, R. *Understanding Digital Signal Processing*, 3rd ed.; Pearson: New York, NY, USA, 2010.
36. Mitra, S. *Digital Signal Processing: A Computer-Based Approach*, 4th ed.; McGraw-Hill: New York, NY, USA, 2010.
37. Owen, M. *Practical Signal Processing*; Cambridge University Press: Cambridge, UK, 2007.
38. Bateman, A.; Paterson-Stephens, I. *The DSP Handbook: Algorithms, Applications and Design Techniques*; Prentice Hall: Hoboken, NJ, USA, 2002.
39. Wanhammar, L. *DSP Integrated Circuit*; Academic Press: Cambridge, UK, 1999.
40. Flige, N. *Multirate Digital Signal Processing: Multirate Systems, Filter Banks, Wavelets*; John Wiley & Sons: New York, NY, USA, 1994.
41. Vaidyanathan, P.P. *Multirate Systems and Filter Banks*; Prentice Hall Inc.: Hoboken, NJ, USA, 1992.
42. Lyons, R.; Fugal, D. *Essential Guide to Digital Signal Processing*; Pearson: New York, NY, USA, 2014.
43. Lyons, R. *Streamlining Digital Signal Processing: A Tricks of the Trade Guidebook*, 2nd ed.; Wiley-IEEE Press: Hoboken, NJ, USA, 2012.
44. Hussain, Z.; Sadik, A.; O'Shea, P. *Digital Signal Processing. An Introduction with MATLAB and Applications*; Springer: London, UK, 2011.
45. Astrom, K.J.; Wittenmark, B. *Computer-Controlled System, Theory and Design*, 3rd ed.; Prentice Hall, Inc.: Hoboken, NJ, USA, 2013.
46. Williamson, D. *Digital Control and Implementation*; Prentice Hall Inc.: Hoboken, NJ, USA, 1991.
47. Franklin, G.F.; Powell, D.J.; Workman, M.L. *Digital Control of Dynamic Systems*, 3rd ed.; Prentice-Hall: Hoboken, NJ, USA, 1997.
48. Laakso, T.; Valimaki, V. Splitting the Unit Delay. *IEEE Signal Process. Mag.* **1996**, *13*, 30–60. [[CrossRef](#)]
49. Sozański, K. Overview of Signal Processing Problems in Power Electronic Control Circuits. *Energies* **2023**, *16*, 4774. [[CrossRef](#)]
50. TMS320F28388D controlCARD Information Guide, Texas Instruments, May 2020. Available online: https://www.ti.com/lit/ug/spruil8b/spruil8b.pdf?ts=1733044901006&ref_url=http%253A%252F%252Fwww.ti.com%252Flit%252Fpdf%252Fspruil8b (accessed on 1 June 2024).
51. Montagner, V.F.; Maccari, L.A.; Oliveira, R.C.L.F.; Santini, C.L.A. Contribution to model LCL filters connected to the grid with uncertain parameters. In Proceedings of the 2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC), Fortaleza, Brazil, 29 November–2 December 2015; pp. 1–4. [[CrossRef](#)]
52. Wang, B.; Xu, Y.; Shen, Z.; Zou, J.; Li, C.; Liu, H. Current Control of Grid-Connected Inverter with LCL Filter Based on Extended-State Observer Estimations Using Single Sensor and Achieving Improved Robust Observation Dynamics. *IEEE Trans. Ind. Electron.* **2017**, *64*, 5428–5439. [[CrossRef](#)]
53. Bolsi, P.C.; Prado, E.O.; Sartori, H.C.; Lenz, J.M.; Pinheiro, J.R. LCL Filter Parameter and Hardware Design Methodology for Minimum Volume Considering Capacitor Lifetimes. *Energies* **2022**, *15*, 4420. [[CrossRef](#)]
54. Routimo, M.; Tuusa, H. LCL Type Supply Filter for Active Power Filter-Comparison of an Active and a Passive Method for Resonance Damping. In Proceedings of the 2007 IEEE Power Electronics Specialists Conference, Orlando, FL, USA, 17–21 June 2007; pp. 2939–2945. [[CrossRef](#)]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.