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# A Comprehensive Review on Space Vector Based-PWM Techniques for Common Mode Voltage Mitigation in Photovoltaic Multi-Level Inverters

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**Abstract:** Nowadays, transformer-less photovoltaic (PV) multi-level inverters (MLIs) are commonly employed in both industrial and residential settings. This structure has attracted increased attention due to its unique advantages, such as higher efficiency, lower cost and size, better waveform quality, and inherent fault tolerance. However, due to the removal of the transformer, the common mode voltage (CMV) becomes one of the crucial issues in transformer-less PV MLIs. The high-frequency variation in CMV results in a leakage current that deteriorates the line current quality, increases the PV power system losses, leads to severe electromagnetic emissions (EMI), reduces the PV array lifespan, and causes personal safety problems. In this regard, this paper presents a review of the existing and recent research on modulation techniques based on space vector pulse width modulation (SVPWMs) that overcome this issue in transformer-less three-level NPC-MLIs (3L-NPC-MLIs). The reduced CMV-SVPWM (RCMV-SVPWM) can be mainly categorized as an RCMV-SVPWM based on the vector type, based on virtual vectors, and based on the two-level SVPWM (2L-SVPWM). Their features and their limitations in terms of several main criteria are discussed. In the final section of this paper, some challenges and future trends for this research area are projected.

**Keywords:** photovoltaic inverters; multi-level inverters; space vector modulation; common mode voltage; leakage current



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## 1. Introduction

Recently, the focus on power generation from renewable and sustainable energy sources is notably growing, driven by the rising energy needs and the imperative for environmental protection [1,2]. As photovoltaic (PV) energy is presented as a clean and noise-free source, a significant increase in power penetration from PV systems within the global electricity industry is noted [3,4]. Certainly, this expansion has stimulated the advancement of PV power converters. These converters play a crucial role in connecting PV modules to AC loads and to the grid, as depicted in Figure 1. Consequently, they are employed to guarantee effective and dependable energy conversion. While the configuration of PV power converters may vary, their primary functions persist consistently. Over the last few years, multi-level inverters (MLIs) have dominated the industrial world thanks to their outstanding characteristics. They are widely utilized in medium- to high-power applications in grid-connected PV power generation systems.

Their foremost benefits are increased efficiency, great power density, improved waveform quality, and built-in fault tolerance [5–10]. The MLIs are essentially constructed through the integration of switching components and DC sources/capacitors. This configuration allows the generation of multiple voltage levels while requiring a lower voltage draw from each switch in comparison with the conventional two-level inverter. As illustrated in Figure 2, various MLI topologies have been proposed in the literature [9–13]. These topologies are classified into main categories: transformer-based, and transformer-less

MLIs. These two categories can also be distributed among two distinct subgroups: single DC source MLIs and multiple DC source MLIs. Certainly, in addition to the commonly recognized benefits of multilevel inverters, eliminating the transformer decreases both cost and weight of the power conversion system, thereby enhancing its overall efficiency [14,15]. The multiple DC source MLI configurations are constructed by employing multiple isolated DC power sources such as a rectifier, a battery bank or a PV panel. Nevertheless, their significant drawback is the potential for unequal power distribution among the feeders, resulting in power losses and system malfunctions [16], whereas the single DC source MLIs achieve proper operation by effectively managing the voltage across the auxiliary capacitors through the careful selection of switching states. Furthermore, there is no need for adjustment in the controller design, as they only require the regulation of a single DC link voltage [17].

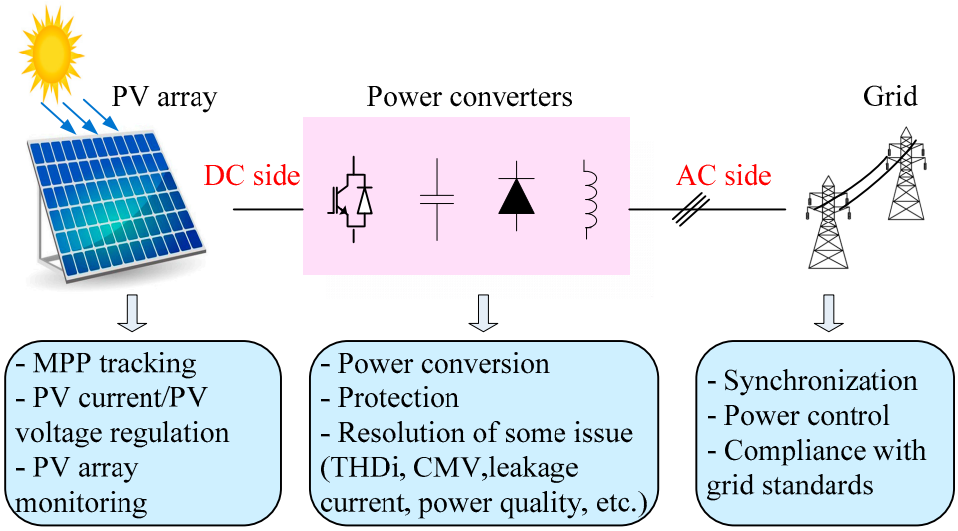



**Figure 1.** Synoptic diagram of PV conversion system.

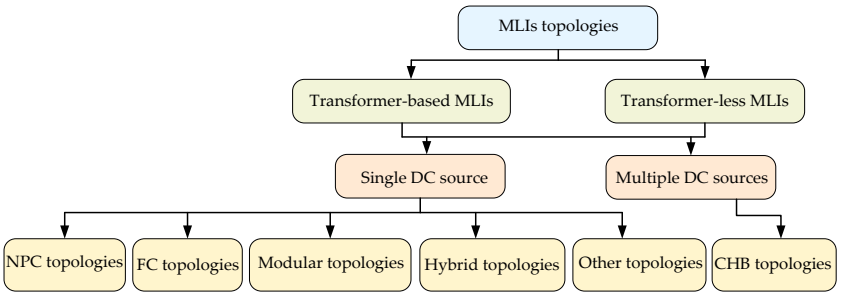
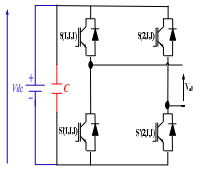
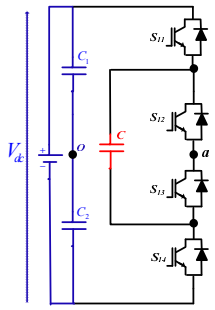
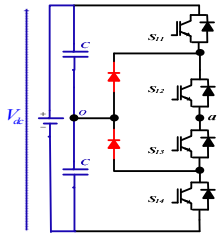



**Figure 2.** Classification of MLIs.

Among the used transformer-less MLIs based on a single DC source configuration, the neutral point clamped (NPC) inverters have become an attractive solution to feed different loads or to connect DC sources to the grid such as the PV panels [6,18,19]. This topology was, firstly, introduced in 1970 for low-power applications and then, it was suggested for medium-voltage applications in 1980 [20,21]. From a hardware perspective, when compared to other multilevel converters, the NPC MLI requires relatively few capacitors despite the use of clamping diodes. This results in cost savings, reduced converter dimensions, and an enhanced power system density [6]. The advantages and disadvantages of the NPC topology in comparison to the commonly recognized topologies, namely the cascaded H-Bridge (CHB) inverter and the flying capacitor (FC) inverter, are presented in Table 1. While there is a continued pursuit of enhanced efficiency in transformer-less PV power converters, the growing utilization of these converters in several conversion systems has revived concerns regarding one of the principal challenges inherent to these systems which

is the common mode voltage (CMV) issue [22–25]. Substantial common-mode leakage currents can be generated due to the high switching frequencies of MLI power devices. Although several proposals [2–6,8,11–13,17] have been put forward in the literature, there has not been a comprehensive review of CMV-related issues dedicated to transformer-less PV NPC inverters. Accordingly, the aim of the presented article is to give a comprehensive review of the existing and recent research on modulation techniques based on space vector pulse width modulation (SVPWM) that, in particular, overcome the CMV issue in transformer-less PV three-level NPC-MLIs (3L-NPC-MLIs).

**Table 1.** Features and limitations of the main MLI topologies.

| MLI Topology | Schematic Representation | Features | Limitations |
| --- | --- | --- | --- |
| Cascaded H-Bridge (CHB) |  | -Modular<br>-No floating capacitors<br>-High reliability<br>-Simple control | -More power devices<br>-Isolated DC sources are required |
| Flying Capacitor (FC) |  | -Cost-effective in high level structure | -High number of floating capacitors<br>-Complicated control<br>-High stored energy in capacitors<br>-High voltage ripple<br>-Bulky and weighty<br>-More voltage sensors are needed<br>-Low reliability |
| Neutral Point Clamped (NPC) |  | -No floating capacitors<br>-Good dynamic response<br>-Simple design<br>-Compact 3L structure with low cost | -Unequal losses among switches<br>-Low reliability in high-level structure |

In the case of the transformer-less MLIs in PV conversion system, the CMV issue can be introduced due to the lack of galvanic isolation. A leakage current can be induced and may circulate to the ground via the leakage capacitor that connects the PV panels to the grounded frame. This current deteriorates the quality of the line current, raises the power conversion system's losses, contributes to EMI, and could potentially reduce the lifespan of the PV panels [3,13,26,27].

To deal with the CMV issue, various modulation strategies have been discussed in different academic works [28–31]. The most common strategies employed for CMV reduction in MLIs are outlined in Figure 3. These strategies are classified into two distinct types: hardware approaches and software approaches. Concerning the initial type, passive filters and specific VSI configurations are frequently used to address CMV. In [32], a custom-designed filter is utilized to suppress the common-mode voltage, while in [33], a novel inverter topology is proposed with the objective of maintaining a constant CMV. Nevertheless, these approaches lead to increased expenses and larger physical dimensions, primarily because of the requirement for additional hardware components. Accordingly, the application of software approaches is generally preferred due to the fact that the CMV reduction is achieved without the need of auxiliary components. Recently, the space vector based-PWM (SVPWM) technique is a software approach that is extensively employed in MLI-based conversion system. The latter allows not only the CMV reduction, but also superior DC-link voltage balancing, self-neutral point equilibrium, improved-quality

harmonics profile, and minimization of switching losses [34,35]. The reduction of CMV can be achieved efficiently by simply excluding the switching states that generate high CMV.

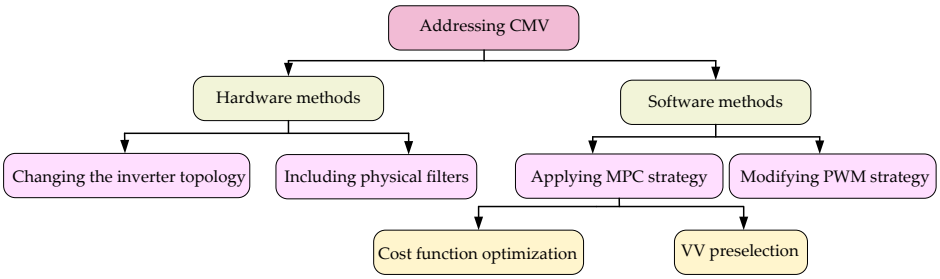



**Figure 3.** General classification of CMV reduction methods in transformer-less inverters.

The conventional SVPWM method applied to the three-level NPC (3L-NPC) inverter is named as the nearest three-vector SVPWM (NTV-SVPWM) [36,37]. This modulation technique divides the space vector diagram (SVD) of the 3L-NPC inverter into six sectors. Each sector is decomposed into four triangles, also named as regions. To generate the desired output voltage, the latter employs the closest three states. With the aim to restrict the CMV amplitude to $\pm V_{dc}/3$, the NTV-SVPWM is modified by eliminating the switching state of the zero vector (PPP) which produces the highest CMV amplitude [38,39]. Because of the SVD of the 3L-NPC inverter consists of different types of space vectors, which generate different CMV levels, various SVPWM were suggested based on space vectors type. Utilizing small vectors for generating the reference voltage vector results in a significant fluctuation in the CMV. Therefore, these vectors are generally excluded from the CMV reduction (CMVR) methods and they exclusively focus on the utilization of large, medium, and zero vectors [40,41]. The CMVR method that uses the large, medium and zero vectors was proposed to decrease the CMV amplitude to the level $\pm V_{dc}/6$. This method is referred to LMZV method [42,43]. Another CMVR method can completely eliminate the CMV through the application of two medium vectors and one zero vector, since the latter produce a zero CMV. This CMVR method is denoted as 2M1ZV [44]. However, three nearest active medium vectors are applied to synthesize the reference vector in three medium vectors (3MV) method [42,44].

Virtual Space Vector PWM (VSVPWM) introduces a fresh concept for addressing the CMV issue. This alternative is mainly dedicated to the neutral point voltage (NPV) control where medium vectors which are responsible for neutral point fluctuation, are eliminated and created virtual vectors are employed instead of them. The creation of the virtual vector is based on two small vectors and one medium vector in the corresponding sector [45]. An improved VSVPWM was suggested for CMV mitigation by choosing only the pulse patterns that are able to control both NPV and CMV [46].

Recently, a novel VSVPWM is proposed to commonly reduce the CMV. A set of new virtual vectors is produced by choosing basic vectors with reduced CMVs [47]. For the purpose of CMV reduction, an enhanced version of VSVPWM is introduced by incorporating continuous adjustment of variable coefficients within the constructed virtual vectors. This approach achieves Active Neutral-Point Voltage Control and reduces CMV. The proposed innovative VSVPWM accomplishes CMV suppression by excluding small vectors with high CMV. It also includes an analysis of the potential risk of CMV suppression failure when employing the equal phase duty-ratio method. Additionally, it outlines a restricted range for variable coefficients to guarantee effective CMV suppression.

Since the SVD of MLI can be considered as a multiple SVD of a two-level (2L) inverter, the SVPWM of 3L-NPC inverter can be achieved in a similar manner as the 2L-SVPWM. Accordingly, the 3L-SVD is decomposed into six hexagons which individually represents the SVD of 2L inverter. The 3L-SVPWM based on this approach is named as the hexagon method [36]. With the aim to mitigate the CMV, this simplified approach is performed by eliminating the zero vector state with the high CMV level. Consequently, a simple

and fast 3L-SVPWM is achieved with CMV reduction. In the same context, an improved SVPWM algorithm based on the 2L hexagon method was recommended as a simple and fast 3L-SVPWM that decreases the CMV variation [48]. This approach is based on the principle of active zero state PWM (AZS-PWM) applied to 2L inverter. To achieve CMV reduction, the zero state is avoided and it is virtualized by using two active vectors.

In this regard, the objective of this review article is as follows:

- To discuss the SVPWM techniques for CMV reduction in 3-phase-3L-NPC inverter.
- To examine the advantages and drawbacks of each approach.
- To provide recommendations for future research and development.

The rest of this paper is structured as follows. In Section 2, the configuration and the operating principle of the 3L-NPC inverter are described. The CMV issues in 3L-NPC inverters is presented in Section 3, and then the conventional SVPWM designed for 2L inverters and 3L-NPC inverters are studied in detail in the same section. In Section 4, classical and recently proposed SVPWM-based CMV reduction methods are classified and comprehensively reviewed. Challenges and future trends of the RCMV-SVPWM are projected in Sections 5 and 6, respectively. Finally, some concluding remarks are provided in Section 7.

## 2. Three-Phase Three-Level NPC Inverter Topology and Its Operating Principle

Overall, NPC inverters are favored in PV systems due to their ability to provide clean, reliable power with low distortion and reduced stress on components, contributing to improved PV system performance and longevity [49]. Typically, a three-phase n-level NPC inverter is comprised of three legs, each of which consists of 2(n − 1) power transistors along with accompanying free-wheeling diodes and 2(n − 2) clamping diodes. To achieve (n − 1) floating DC potentials, (n − 1) capacitors are interconnected in a series configuration across the DC bus. As depicted in Figure 4, the 3L-NPC inverter is equipped with a total of 12 switches and 6 diodes. Each leg of the inverter is composed of four switches, with two switches in the upper leg, two switches in the lower leg, and two clamping diodes for each leg. The two DC terminals are linked to a DC voltage source, $V_{dc}$ [50]. Thanks to the utilization of two identical series-connected capacitors, this source is divided into two distinct floating potentials, which are sequentially referred to as $V_{Po}$ and $V_{No}$. Essentially, each leg of the inverter has three distinct switching states, described as follows [51]:

- In State P, both upper switches are in the ON state, as illustrated in Figure 5a. Consequently, the pole voltage $Vxo$ ($x = a, b, c$) is equal to $+V_{dc}/2$.
- In State N, both lower switches are in the ON state, as shown in Figure 5b. As a result, the pole voltage $Vxo$ ($x = a, b, c$) is equal to $-V_{dc}/2$.
- In State O, the two middle switches are in the ON state, as illustrated in Figure 5c. Therefore, the pole voltage $Vxo$ ($x = a, b, c$) is equal to 0.

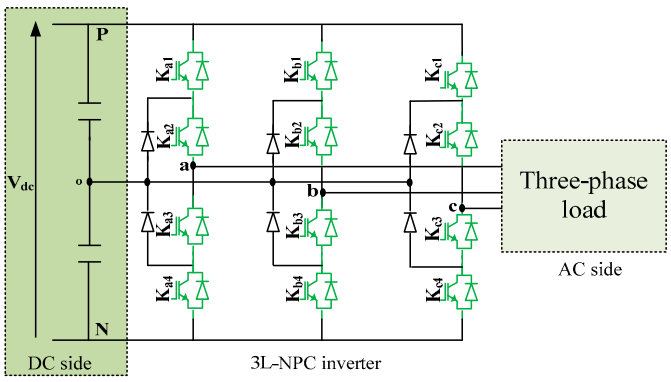



**Figure 4.** Schematic circuit of 3L-NPC inverter.

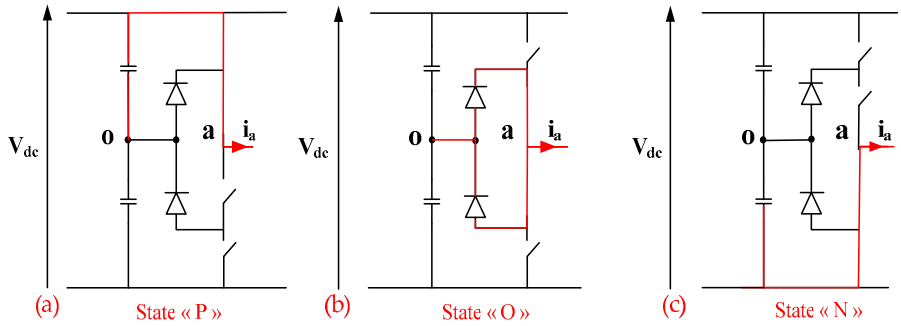



**Figure 5.** Schematic circuit of phase "a" for the following switching states: (**a**) P state, (**b**) O state, and (**c**) N state.

Hence, the total number of switching states for the converter equals $3^3 = 27$, resulting in the generation of 27 space vectors. These vectors are categorized into four groups as depicted in Table 2.

**Table 2.** Space vector types and their amplitudes.

| Space Vector States | Type | Amplitude |
|---|---|---|
| $V_o$ (PPP, NNN, OOO) | Zero | 0 |
| $V_1$ (POO/ONN); $V_2$ (PPO/OON); $V_3$ (OPO/NON); $V_4$ (OPP/NOO); $V_5$ (OOP/NNO); $V_6$ (POP/ONO) | Small | $V_{dc}/3$ |
| $V_8$ (PON); $V_{10}$ (OPN); $V_{12}$ (NPO) $V_{14}$ (NOP); $V_{16}$ (ONP); $V_{18}$ (PNO) | Medium | $V_{dc}/\sqrt{3}$ |
| $V_7$ (PNN); $V_9$ (PPN), $V_{11}$ (NPN); $V_{13}$ (NPP); $V_{15}$ (NNP); $V_{17}$ (PNP) | Large | $2V_{dc}/3$ |

## 3. CMV Issue in 3L-NPC Inverter and Conventional 2L and 3L SVPWM

### *3.1. CMV Issue in 3L-NPC Inverter*

Figure 6a provides an overview of the general structure of the transformer-less 3L-NPC inverter and the leakage current path [52]. As depicted in this figure, the CMV in 3L-NPC inverter is typically designated as the voltage difference between the load's neutral point 'n' and the negative DC bus rail 'N', as given hereafter [13,43]:

$$V_{cm} = V_{nN} = \frac{1}{3}(V_{aN} + V_{bN} + V_{cN}) - (V_{an} + V_{bn} + V_{cn}) \quad (1)$$

where $V_{an}$, $V_{bn}$, and $V_{cn}$ are denoted as the inverter's voltages with reference to the neutral point 'n'. Simultaneously, $V_{aN}$, $V_{bN}$, and $V_{cN}$ represent the inverter's voltages with reference to the negative rail 'N.'

It has been noted that the second term on the right-hand side of (1) equals zero when considering the balanced operating conditions. Consequently, the CMV can be formulated as:

$$V_{cm} = \frac{1}{3}(V_{ao} + V_{bo} + V_{co}) + V_{oN} \quad (2)$$

The voltage $V_{oN}$ represents the potential across the lower capacitor of the DC bus, essentially constituting a steady DC signal. Consequently, the amplitude and frequency of its AC ripple components are significantly smaller than those of the AC components of the CMV, in such a way that they can be disregarded [15]. Therefore, the CMV can be written as [53–55]:

$$V_{cm} = \frac{1}{3}(V_{ao} + V_{bo} + V_{co}) = V_{no} \quad (3)$$

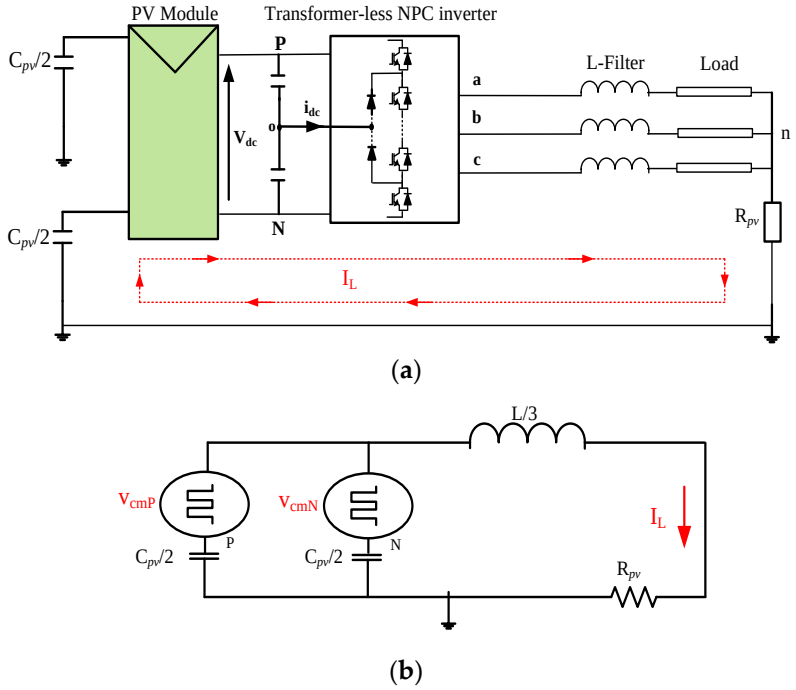



**Figure 6.** (**a**) Path of the leakage current. (**b**) Equivalent common mode circuit.

The voltages across the AC terminals can assume three levels: $-V_{dc}/2$, 0 and $+V_{dc}/2$. Therefore, The CMV can take 8 different levels that depend on the type of vector used to synthesize $\overline{V}_r$ as shown in Table 3. A zero CMV is provided by the zero vector (OOO) and the medium vectors. Two levels of CMV equal to $\pm V_{dc}/6$ are provided by the large vectors. The small vectors provide four different levels: $\pm V_{dc}/6$, $\pm V_{dc}/3$. The zero vectors with switching states (PPP) and (NNN) provide the largest amplitude of CMV that is equal to $+V_{dc}/2$ and $-V_{dc}/2$, respectively.

**Table 3.** Vector type effects on CMV.

| Vector's Type | Voltage Vector | CMV Level |
|---|---|---|
| Zero | NNN | $-V_{dc}/2$ |
| | OOO | 0 |
| | PPP | $+V_{dc}/2$ |
| Small | ONN, NON, NNO | $-V_{dc}/3$ |
| | OON, NOO, ONO | $-V_{dc}/6$ |
| | POO, OPO, OOP | $+V_{dc}/6$ |
| | PPO, OPP, POP | $+V_{dc}/3$ |
| Medium | PON, OPN, NPO, NOP, ONP, PNO | 0 |
| Large | PNN, NPN, NNP | $-V_{dc}/6$ |
| | PPN, NPP, PNP | $+V_{dc}/6$ |

The equivalent common mode circuit can be represented as shown in Figure 6b. The variation of the CMV at higher rate produces unwanted leakage current that circulates through the filter inductor L, leakage resistor $R_{pv}$, and leakage capacitor $C_{pv}$. This current can be expressed as follows [56]:

$$I_L = \frac{V_{cm}}{\frac{j2\pi f_{cm}L}{3} + \frac{1}{j2\pi f_{cm}C_{pv}} + R_{pv}} \quad (4)$$

where $f_{cm}$ is the frequency of the CMV.

It is imperative to keep this leakage current to a minimum because it can exacerbate system losses, deteriorate the quality of the current being fed into the grid, result in severe conducted and radiated EMI, and pose risks to personal safety [13,42]. According to the German standard VDE 0126-1-1 [57], if the RMS value of the leakage current exceeds 300 mA, the PV system must be disconnected from the grid within 0.3 s [58,59].

### *3.2. Conventional 2L and 3L SVPWM*

The SVPWM approach is a digital modulation method that produces PWM signals based on the vector representation of the desired output voltage. The vectors are arranged in a hexagonal structure to represent both magnitude and phase of each vector. The first step to carry out the SVPWM is to define the reference voltage vector $\overline{V}_r$ in α-β stationary-frame using the conventional Clark transformation, as mentioned hereafter.

$$\begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{5}$$

Also, the vector $\overline{V}_r$ can be defined in the following complex form:

$$\overline{V}_r = V_{r\alpha} + jV_{r\beta} \tag{6}$$

Therefore, the magnitude and the phase of $\overline{V}_r$ can be deduced:

$$\begin{cases} |V_r| = \sqrt{V_{r\alpha}^2 + V_{r\beta}^2} \\ \theta = \tan^{-1}\left(\frac{V_{r\beta}}{V_{r\alpha}}\right) \end{cases} \tag{7}$$

#### 3.2.1. Conventional 2L SVPWM

The 2L-SVPWM involves a total of 8 available switching states resulting in 8 space vectors [60,61]. These vectors are sorted into two groups: zero vectors and active vectors, which form the 2L-SVD of Figure 7a. To synthesize the desired voltage vector $\overline{V}_r$, the 2L-SVD is divided into six sectors. As an example, we consider that $\overline{V}_r$ is located at the first sector as shown in Figure 7a. In this case, the two nearest vectors $\overline{V}_1$ and $\overline{V}_2$ with the zero vector $\overline{V}_0$ are applied with the corresponding application times $T_1$, $T_2$ and $T_0$, respectively. These vectors are distributed within a switching period as shown in Figure 7b considering the following restrictions [62]:

- The power semiconductors should not undergo more than two transitions between their ON and OFF states during one switching period.
- The neutral point voltage must be maintained near to zero.

To calculate the application times, the Volt-Second equation is used and it is written as follows:

$$\begin{cases} T_s.\overline{V}_r = T_1.\overline{V}_1 + T_2.\overline{V}_2 + T_0.\overline{V}_0 \\ T_s = T_0 + T_1 + T_2 \end{cases} \tag{8}$$

where $T_s$ is the sampling period.

According to Equation (8) and the 2L-SVD, we can write:

$$\begin{cases} T_s|V_r|\cos\theta = T_1|V_1| + T_2|V_2|\cos 60^\circ \\ T_s|V_r|\sin\theta = T_2|V_2|\sin 60^\circ \end{cases} \tag{9}$$

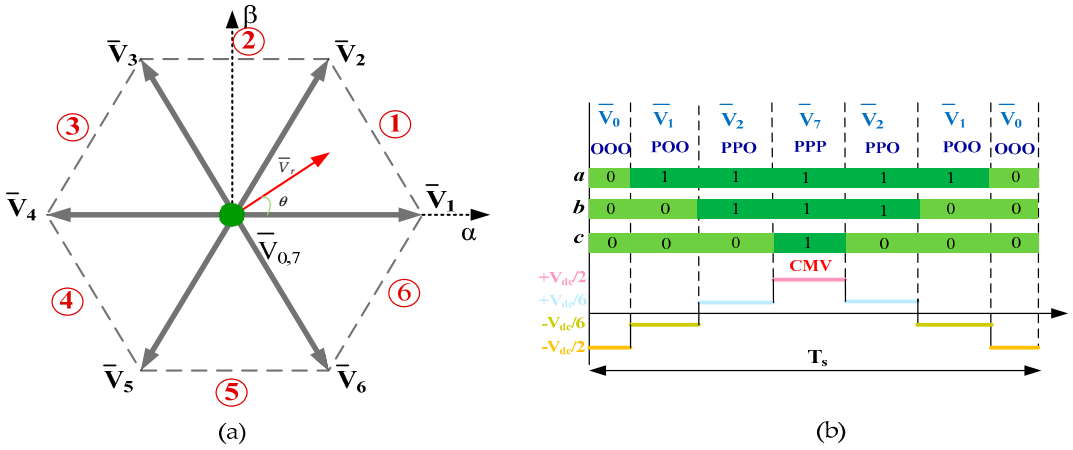



**Figure 7.** (**a**) 2L space vector diagram and (**b**) switching sequence distribution for sector 1.

By solving Equation (9), the application times can be obtained as:

$$\begin{cases} T_1 = \frac{\sqrt{3}}{V_{dc}} |V_r| T_s \sin(\frac{\pi}{3} - \theta) \\ T_2 = \frac{\sqrt{3}}{V_{dc}} |V_r| T_s \sin(\theta) \\ T_0 = 1 - (T_1 + T_2) \end{cases} \tag{10}$$

By extending this principle to all operating sectors, the general expressions of the application times for a 2L-inverter are given by:

$$\begin{cases} T_x = \frac{\sqrt{3}}{V_{dc}} |V_r| T_s \sin(k_v \frac{\pi}{3} - \theta) \\ T_y = \frac{\sqrt{3}}{V_{dc}} |V_r| T_s \sin(\theta - (k_v - 1)\frac{\pi}{3}) \\ T_z = 1 - (T_x + T_y) \end{cases} \tag{11}$$

where $k_v$ is the sector number.

Table 4 gives the conventional switching sequences of the 2L-SVPWM for all operating sectors. While the 2L-SVPWM is relatively straightforward to use, it comes with several drawbacks. The 2L-inverters are limited to low-power and low-frequency applications [6]. To address high-power and high-frequency requirements, the 3L-inverter has been introduced.

**Table 4.** Conventional switching sequences for 2L-SVPWM.

| Sector Number | Switching Sequence |
|---|---|
| 1 | $V_7$-$V_1$-$V_2$-$V_0$-$V_2$-$V_1$-$V_7$ |
| 2 | $V_7$-$V_2$-$V_3$-$V_0$-$V_3$-$V_2$-$V_7$ |
| 3 | $V_7$-$V_4$-$V_3$-$V_0$-$V_3$-$V_4$-$V_7$ |
| 4 | $V_7$-$V_4$-$V_5$-$V_0$-$V_5$-$V_4$-$V_7$ |
| 5 | $V_7$-$V_6$-$V_5$-$V_0$-$V_5$-$V_6$-$V_7$ |
| 6 | $V_7$-$V_6$-$V_1$-$V_0$-$V_1$-$V_6$-$V_7$ |

Figure 8 exhibits the simulation waveforms of the 2L SVPWM modulation technique. As it is observed, the phase-to-neutral modulated voltage Van draws different levels and the currents are balanced with a sinusoidal shape. As for the generated CMV, its amplitude reaches the value of $V_{dc}/2$, which is produced by the zero vector. As a result, the variation in the CMV amplitude leads to an important leakage current. Using an extended range of the modulation index m, The RMS values of CMV and the leakage current are displayed

in Figure 9. It is obviously concluded that changing the modulation index significantly affects the performance of CMV and the leakage current, with a higher modulation index resulting in a noticeably reduced CMV and reduced leakage current.

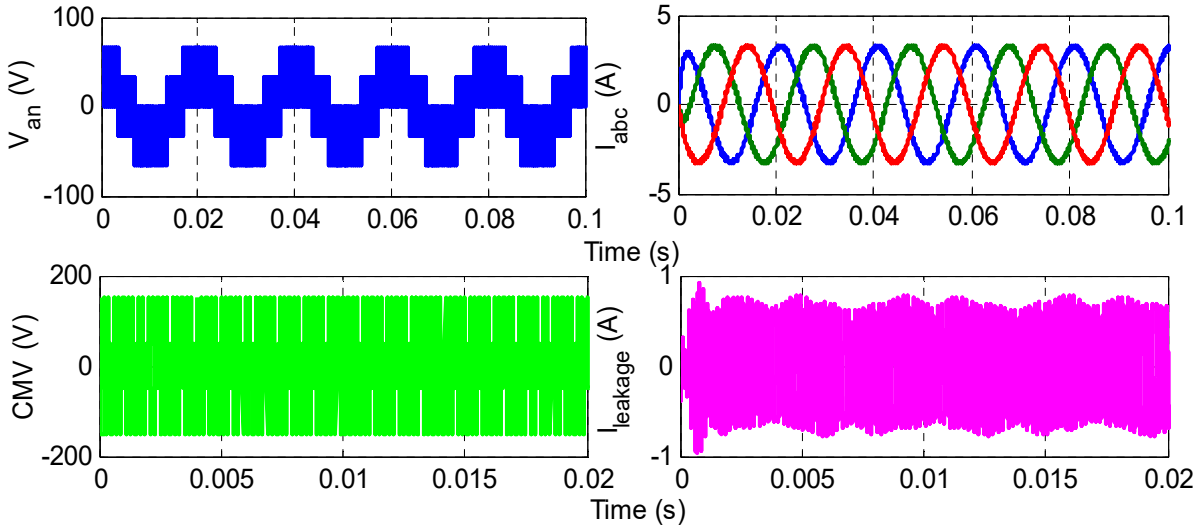



**Figure 8.** Obtained results of 2L SVPWM method for m = 1 and $V_{dc}$ = 300 V.

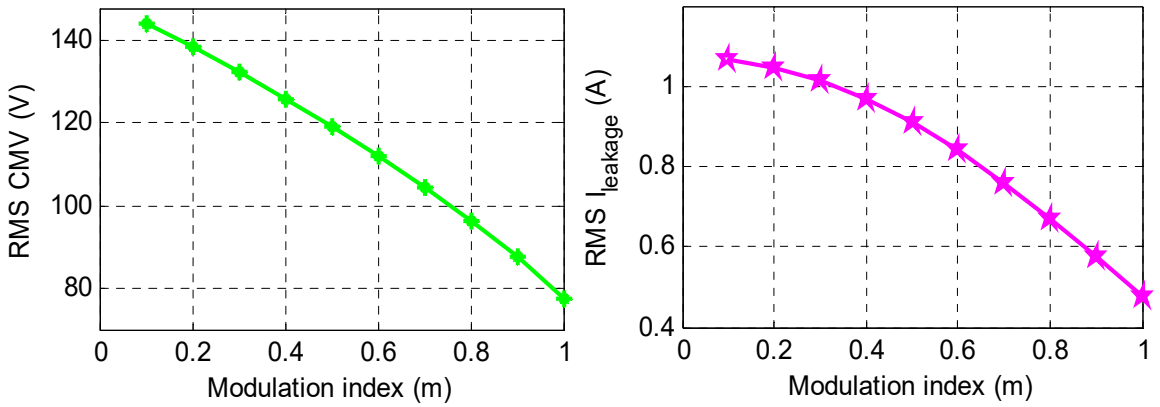



**Figure 9.** The variation of RMS values of CMV and $I_L$ versus m variation.

3.2.2. Conventional 3L SVPWM

a. NTV SVPWM

The NTV-SVPWM is the conventional modulation technique applied to the 3L inverter [36,63]. It consists to apply the three nearest vectors to $\overline{V}_r$ in each triangle. As in 2L-SVPWM, the 3L-SVPWM decomposes the 3L-SVD of Figure 10a to six basic sectors. Each sector is divided into four triangles, as shown in Figure 10b.

To pinpoint the correct triangle number 'T', it should initially calculate the generalized reference-vector coordinates $V'_\alpha$ and $V'_\beta$, as indicated in the equation system below.

$$\begin{cases} V'_{r\alpha} = |V_r| cos(\theta - (k_v - 1)\frac{\pi}{3}) \\ V'_{r\beta} = |V_r| \sin(\theta - (k_v - 1)\frac{\pi}{3}) \end{cases} \quad (12)$$

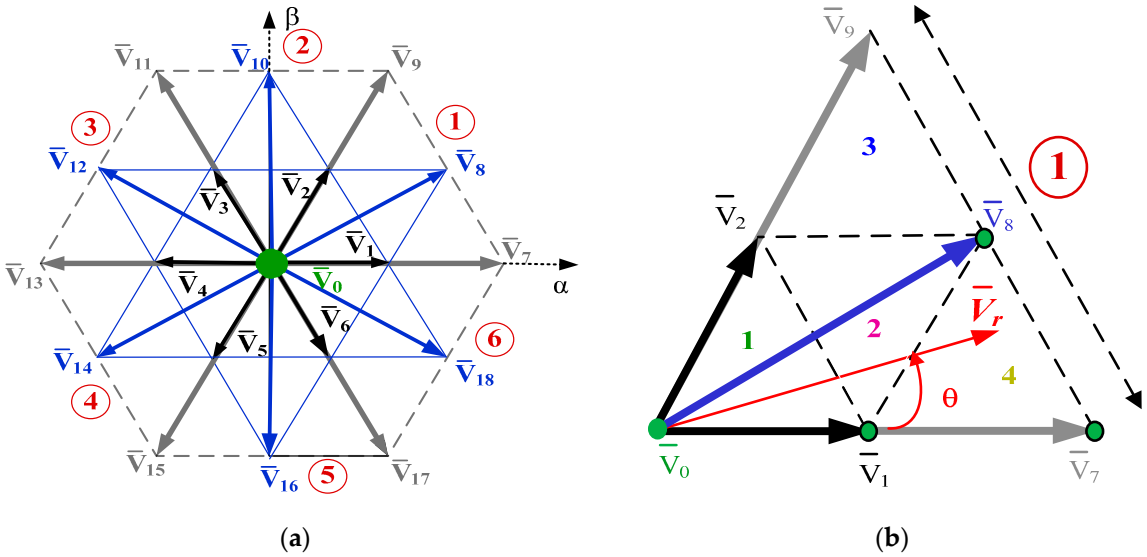



**Figure 10.** (**a**) 3L space vector diagram and (**b**) sector division.

Therefore, the triangle number can be determined using the new $\overline{V}_r$ coordinates $V'_{r\alpha}$ and $V'_{r\beta}$ according to the following algorithm:

$$\begin{cases} if\ V'_{r\alpha} \prec \frac{V_{dc}}{3} - \frac{\sqrt{3}}{3}V'_{r\beta} & then\ T = 1 \\ Else\ if\ V'_{r\alpha} \succ \frac{V_{dc}}{3} + \frac{\sqrt{3}}{3}V'_{r\beta} & then\ T = 4 \\ Else\ if\ V'_{r\beta} \prec \frac{\sqrt{3}}{6}V_{dc} & then\ T = 2 \\ Else & T = 3 \end{cases} \tag{13}$$

After the triangle has been recognized, it should apply the closest three vectors to $\overline{V}_r$ that form the selected triangle. The application times of these vectors are calculated with the same manner as in 2L-SVPWM. For a further explanation, assuming that $\overline{V}_r$ is located at the triangle 2 within sector 1. Accordingly, the three nearest vector to be applied in this case are $\overline{V}_1$, $\overline{V}_2$ and $\overline{V}_8$ with their corresponding application times $T_x$, $T_y$ and $T_Z$, respectively.

The calculated application times for the four possible locations of $\overline{V}_r$ are provided in Table 5 and they are valid for all operating sectors. Table 6 exhibits the adequate applied three nearest vector for each triangle within sector 1.

**Table 5.** Expressions of the duty cycles for the four possible positions of $\overline{V}_r$ within one sector.

| | $T_x$ | $T_y$ | $T_z$ |
|---|---|---|---|
| T = 1 | $T_s - \rho\sin\left(\theta - (K_v - 2)\frac{\pi}{3}\right)$ | $\rho\sin\left(K_v\frac{\pi}{3} - \theta\right)$ | $\rho\sin\left(\theta - (K_v - 1)\frac{\pi}{3}\right)$ |
| T = 2 | $T_s - \rho\sin\theta - (K_v - 1)\frac{\pi}{3}$ | $-T_s + \rho\sin\left(\theta - (K_v - 2)\frac{\pi}{3}\right)$ | $T_s - \rho\sin\left(K_v\frac{\pi}{3} - \theta\right)$ |
| T = 3 | $2T_s - \rho\sin\left(\theta - (K_v - 2)\frac{\pi}{3}\right)$ | $-T_s + \rho\sin\left(\theta - (K_v - 1)\frac{\pi}{3}\right)$ | $\rho\sin\left(K_v\frac{\pi}{3} - \theta\right)$ |
| T = 4 | $2T_s - \rho\sin\left(\theta - (K_v - 2)\frac{\pi}{3}\right)$ | $-T_s + \rho\sin\left(K_v\frac{\pi}{3} - \theta\right)$ | $\rho\sin\left(\theta - (K_v - 1)\frac{\pi}{3}\right)$ |
| $\left(\rho = 2\sqrt{3}T_s\frac{\lvert V_r\rvert}{V_{dc}}\right)$ | | | |

**Table 6.** The appropriate nearest three vectors for sector 1.

| | $\overline{V}_x$ | $\overline{V}_y$ | $\overline{V}_z$ |
|---|---|---|---|
| T = 1 | $\overline{V}_0$ | $\overline{V}_1$ | $\overline{V}_2$ |
| T = 2 | $\overline{V}_1$ | $\overline{V}_8$ | $\overline{V}_2$ |
| T = 3 | $\overline{V}_2$ | $\overline{V}_9$ | $\overline{V}_8$ |
| T = 4 | $\overline{V}_1$ | $\overline{V}_7$ | $\overline{V}_8$ |

Similar to the 2L-SVPWM, the same constraints must be considered to distribute the switching sequences. An example of pulse patterns is drawn in Figure 11 when $\overline{V}_r$ is situated in triangle 4 within the first sector.

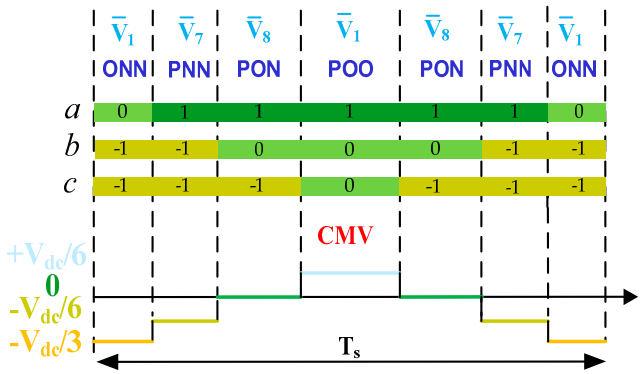



**Figure 11.** Switching sequence distribution for sector 1 and triangle 4.

Numerical results obtained with the NTV-SVPWM algorithm are depicted in Figure 12. These results show that the phase-to-neutral voltage waveform has a quasi-sinusoidal shape and the load currents provide high quality waveforms which are quite sinusoidal and balanced. Regarding the CMV waveform, for m = 1.15, it fluctuates between the negative and positive values of $\pm V_{dc}/3$. These peak values are generated by the small vectors. Indeed, the CMV amplitude depends on the value of m. As for the leakage current, it is always important with an amplitude that exceeds 1A. The measured RMS values of CMV and the leakage current are shown in Figure 13. By inspecting the variation of the RMS value of CMV, it can be observed that, when m increases, the latter decreases slightly for low values of m (m changing from 0.1 to 0.6), whereas it decreases significantly for high values of m, while with the increase of m, the RMS value of the leakage current increases for the low values of m and decreases for the high value of the latter. Certainly, the leakage current is influenced not only by the reached magnitude of CMV but also by its fluctuations.

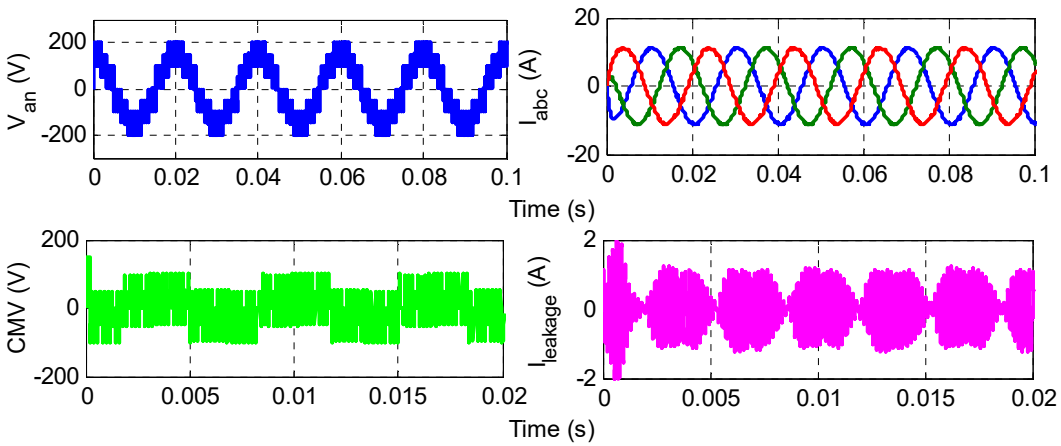



**Figure 12.** Obtained results of 3L NTV-SVPWM method for m = 1.15 and $V_{dc}$ = 300 V.

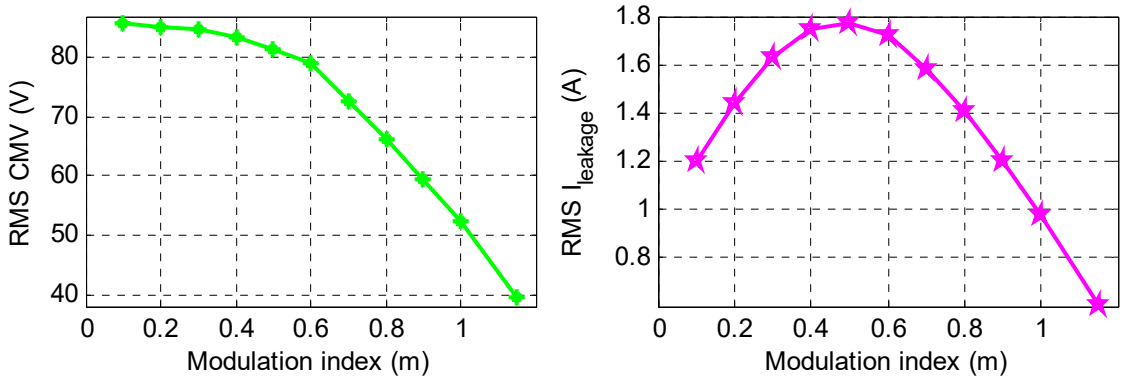



**Figure 13.** The variation of RMS values of CMV and $I_L$ versus m variation.

b. SVPWM based hexagon method

The 3L SVPWM based hexagon method is a simple and fast method compared to the 3L-NTV method [11,36]. The NTV-SVPWM seems to be complicated when the number of level is more than 3 [64]. Therefore, to obtain a simplified 3L-SVPWM, the 3L-SVD is transformed to six small hexagons as depicted in Figure 14a, while, each one corresponds to 2L-SVD [11,36,45,48]. Table 7 depicts the angle boundaries for the small hexagon selection.

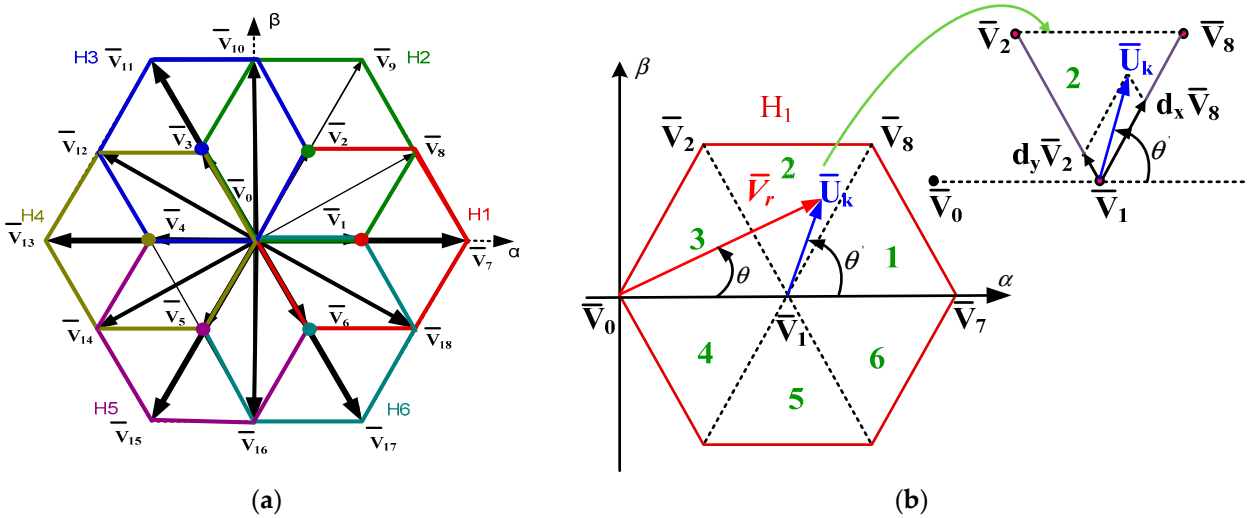



**Figure 14.** (**a**)Transformation of the 3L-SVD into six 2L-SVD; (**b**) Translation of $\overline{V}_r$ to the center of the small hexagon.

**Table 7.** Small hexagon selection.

| Phase Angle of $\overline{V}_r$ | Small Hexagon Number |
|---|---|
| $-\pi/6 < \theta < \pi/6$ | 1 |
| $\pi/6 < \theta < \pi/2$ | 2 |
| $\pi/2 < \theta < 5\pi/6$ | 3 |
| $5\pi/6 < \theta < 7\pi/6$ | 4 |
| $7\pi/6 < \theta < 3\pi/2$ | 5 |
| $3\pi/6 < \theta < -\pi/6$ | 6 |

Once the latter is identified, the same steps of the 2L-SVPWM have to be applied. Similarly, the 2L hexagon is decomposed into six subsectors in which the vector $\overline{V}_r$ can be located. To identify the appropriate subsector, the vector $\overline{V}_r$ is translated to the center of the selected small hexagon, obtaining a novel reference vector $\overline{U}_k$, as depicted in Figure 14b. This novel vector is defined as:

$$\overline{U}_k = \overline{V}_r - \frac{V_{dc}}{3} e^{j(\frac{H-1}{3}\pi)} \tag{14}$$

where H is the small hexagon number.

Hence, we need to determine the subsector that contains the new reference vector $\overline{U}_k$. Afterwards, the adequate three vectors to be applied are selected and their application times are computed. Taking the example when the vector $\overline{U}_k$ is located at the subsector 1 within the first small hexagon. Using the theory of 2L-SVPWM, the vectors $\overline{V}_7$ and $\overline{V}_8$ are applied as active vectors while $\overline{V}_1$, which is the center of the small hexagon 1, is applied as a zero vector. The selected vectors ($\overline{V}_7$, $\overline{V}_8$ and $\overline{V}_1$) are thereafter embarrassed with the application times $T_x$, $T_y$ and $T_z$, which are expressed as follows:

$$\begin{cases} T_x = 2 * \frac{\sqrt{3}}{V_{dc}} |U_k| T_s \sin(k'_v \frac{\pi}{3} - \theta') \\ T_y = 2 * \frac{\sqrt{3}}{V_{dc}} |U_k| T_s \sin(\theta' - (k'_v - 1)\frac{\pi}{3}) \\ T_z = 1 - (T_x + T_y) \end{cases} \tag{15}$$

where $\theta'$ is the phase-angle of $\overline{U}_k$ and $k'_v$ is the subsector number within the small hexagon.

In the last step, the suitable switching sequences are provided at each sampling period. An example of switching sequences distribution is depicted in Figure 15 when the novel reference vector $\overline{U}_k$ is situated in subsector 1 and small hexagon 1.

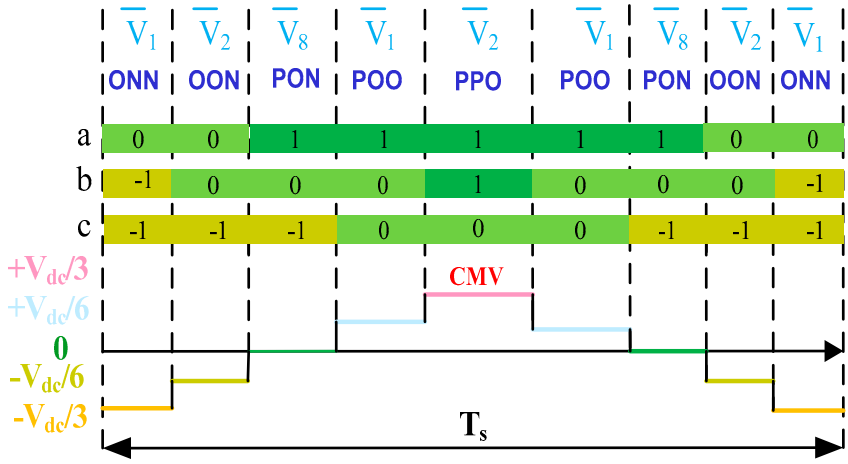



**Figure 15.** Switching.sequence distribution when $\overline{U}_k$ is situated in subsector 1 of the first small hexagon.

The achieved results with the conventional hexagon method are displayed in Figure 16 for m = 0.8. As with the NTV method, similar waveforms are drawn. The obtained CMV fluctuates between positive and negative values and it reaches $V_{dc}/3$. These CMV fluctuations result in an important leakage current with an amplitude of 2A for this operation point. The variation of the RMS values of the leakage current and the CMV are also traced in Figure 17. The obtained waveforms are different from the ones obtained with the NTV method. This is due to that the reference vector is examined and synthesized within a two-level hexagon. For low values of m, the RMS values of CMV and leakage current increase with the increase of m. However, they decrease with the increase of m for the high values of the latter.

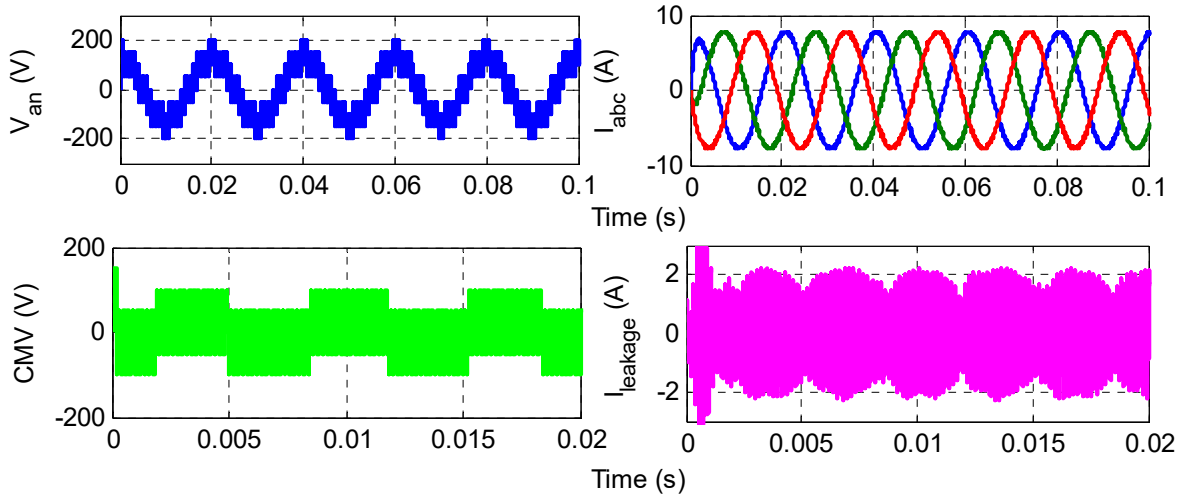



**Figure 16.** Obtained results of 3L hexagon SVPWM method for m = 0.8 and $V_{dc}$ = 300 V.

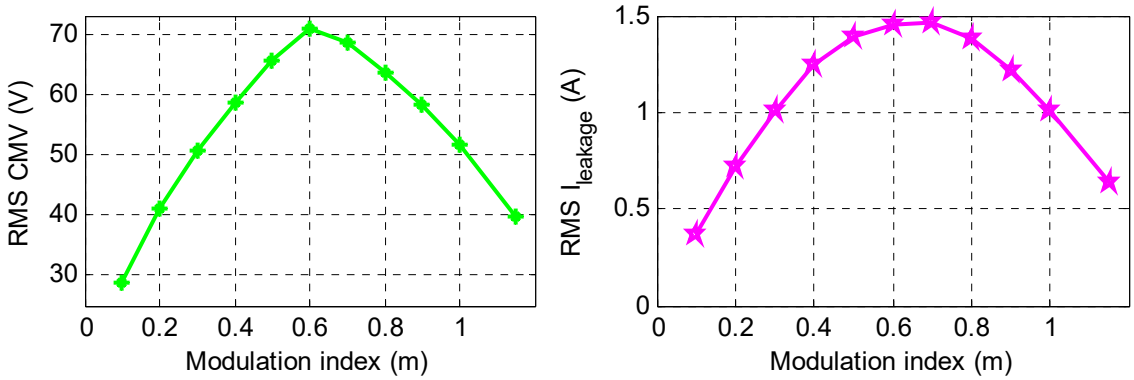



**Figure 17.** The variation of RMS values of CMV and $I_L$ versus m variation.

## 4. CMVR Methods Based SVPWM

A review of the classical and recently proposed SVPWM based CMV reduction methods is presented in this section. Particularly, this review is built on the modified conventional 3L-SVPWM, the CMVR Methods based on vectors type selection, virtual vectors based SVPWM and CMVR methods based on 2L-SVPWM.

### *4.1. Modified Conventional 3L-SVPWM*

As previously mentioned, the zero vectors with the switching states (PPP) and (NNN) produce the most important level of CMV ($\pm V_{dc}/2$). Accordingly, to reduce the CMV and to restrict it to $\pm V_{dc}/3$, these zero vectors are excluded when synthesize the reference vector $\overline{V}_r$ in the 3L-NTV-SVPWM and 3L-SVPWM based on small hexagons [36,38,39]. In 3L-NTV-SVPWM, if the vector $\overline{V}_r$ is located at the triangle 1 in any operation sector, only the zero vector with the state (OOO) will be applied, whereas in the 3L-SVPWM based on small hexagon, the switching states (PPP) and (NNN) are replaced by the state (OOO) depends on the position of $\overline{V}_r$ as presented in Table 8.

**Table 8.** Positions where the switching states (PPP) and (NNN) are substituted by (OOO).

| Small Hexagon Number | Region Number | Small Hexagon Number | Region Number |
|---|---|---|---|
| $H_1$ | $R_3$ and $R_4$ | $H_4$ | $R_6$ and $R_1$ |
| $H_2$ | $R_4$ and $R_5$ | $H_5$ | $R_1$ and $R_2$ |
| $H_3$ | $R_5$ and $R_6$ | $H_6$ | $R_2$ and $R_3$ |

*4.2. 3L-SVPWM CMVR Methods Based on Vectors Type*

Various 3L-SVPWM techniques have been presented based on the changing of the switching method and the vectors type. The idea is to eliminate the space vectors that generate the highest CMV variation whatever for CMV reduction or for completely CMV suppression. To maintain the CMV oscillate between the levels $-V_{dc}/6$, 0, and $+V_{dc}/6$, the space vectors that produces only these levels are selected. These approaches are denoted in this paper as variable CMV (VCMV) methods. In certain situations, even when the magnitude of CMV is decreased, the leakage current may remain significant due to high-frequency variations of the CMV. To obtain a constant CMV with a fixed frequency, zero CMV (ZCMV) methods are adopted [11]. These approaches apply only the vectors that produce zero CMV. Moreover, to keep the CMV to the positive level $+V_{dc}/6$, only space vectors that produce this level are chosen. This SVPMM approach is named as positive CMV (PCMV) method [56], while the SVPWM which applies only the vectors with the negative CMV level $-V_{dc}/6$ with the aim to restrict the CMV to $-V_{dc}/6$, is referred as negative CMV (NCMV) method [56]. The aforementioned SVPWM methods will be developed in details below.

4.2.1. VCMV Methods

Large, Medium and Zero (LMZ) Method

In this approach, the large, medium, and zero vectors are exclusively applied. Furthermore, to ensure minimal fluctuations in CMV, only the "OOO" state is selected as the zero vector [42,43,56]. Consequently, the 3L-SVD is divided into 12 equal sectors of 30°, as illustrated in Figure 18a.

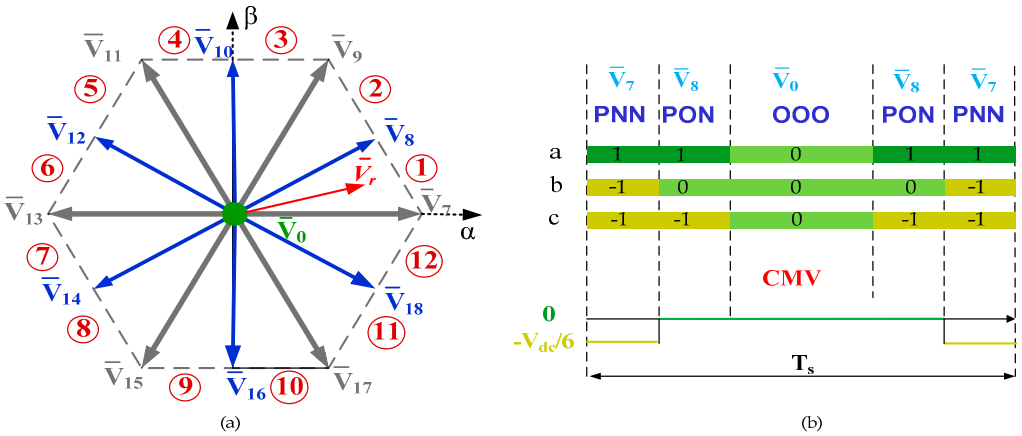



**Figure 18.** (**a**) 3L SVD using LMZ method; (**b**) Switching se quence distribution for sector 1.

As an example, let us consider that $\overline{V}_r$ is situated within sector 1. The target reference vector is generated by employing the large vector $\overline{V}_7$, the medium vector $\overline{V}_8$, and the zero vector $\overline{V}_0$ (OOO) [3]. Accordingly, the vector $\overline{V}_7$ is utilized during the time interval $T_1$, vector $\overline{V}_8$ during $T_2$, and vector $\overline{V}_0$ during $T_0$. The application times $T_0$, $T_1$, and $T_2$ are calculated according to the Volt-Second equation given as:

$$\begin{cases} T_s.\overline{V}_r = T_1.\overline{V}_7 + T_2.\overline{V}_8 + T_0.\overline{V}_0 \\ T_s = T_0 + T_1 + T_2 \end{cases} \quad (16)$$

The switching sequences distribution as well as the generated CMV of this example are shown in Figure 18b. It can be observed that the CMV oscillates between two levels: $-V_{dc}/6$, 0. The zero level is generated by the medium and zero vectors. While the level $-V_{dc}/6$ is produced by the large vectors.

4.2.2. ZCMV Methods

- Two Medium One Zero (2M1Z) Method

This alternative aims to completely suppress the CMV by applying two medium vectors and one zero vectors that produce zero CMV [42,44,65]. The 3L-SVD is therefore split into six basic sectors of 60° as shown in Figure 19a. Let us consider the example when the vector $\overline{V}_r$ is located at the first sector. The two medium vectors $\overline{V}_8$ and $\overline{V}_{18}$ with the zero vector $\overline{V}_0$ with the state (OOO). The application times $T_1$, $T_2$, and $T_0$ that correspond to $\overline{V}_8$, $\overline{V}_{18}$, and $\overline{V}_0$, respectively are computed using the Volt-Second equation given by:

$$\begin{cases} T_s.\overline{V}_r = T_1.\overline{V}_8 + T_2.\overline{V}_{18} + T_0.\overline{V}_0 \\ T_s = T_0 + T_1 + T_2 \end{cases} \quad (17)$$

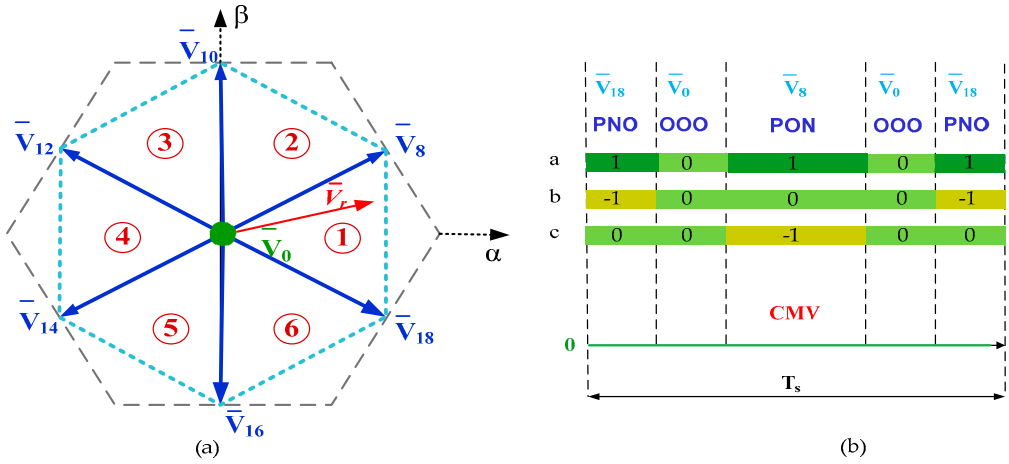



**Figure 19.** (**a**) 3L SVD using 2M1Z method; (**b**) Switching sequence distribution for sector 1.

The pulse patterns of this example as well as the generated CMV are depicted in Figure 19b. It is observed that the CMV is always equal to zero.

- Three medium (3M) method

The 3M-SVPWM uses only one vector's type. The three nearest medium vectors to $\overline{V}_r$ are applied to synthesize the target output voltages [42,44,65]. As in the NTV-SVPWM, the approach divides the 3L-SVD into six sectors of 60° as illustrated in Figure 20a. If the vector $\overline{V}_r$ lies in the first sector, the medium vectors $\overline{V}_8$, $\overline{V}_{10}$ and $\overline{V}_{18}$ are selected and applied during $T_x$, $T_y$, and $T_z$, respectively, which can be determined using the Volt-Second equation as:

$$\begin{cases} T_s.\overline{V}_r = T_x.\overline{V}_8 + T_y.\overline{V}_{10} + T_z.\overline{V}_{18} \\ T_s = T_x + T_y + T_z \end{cases} \quad (18)$$

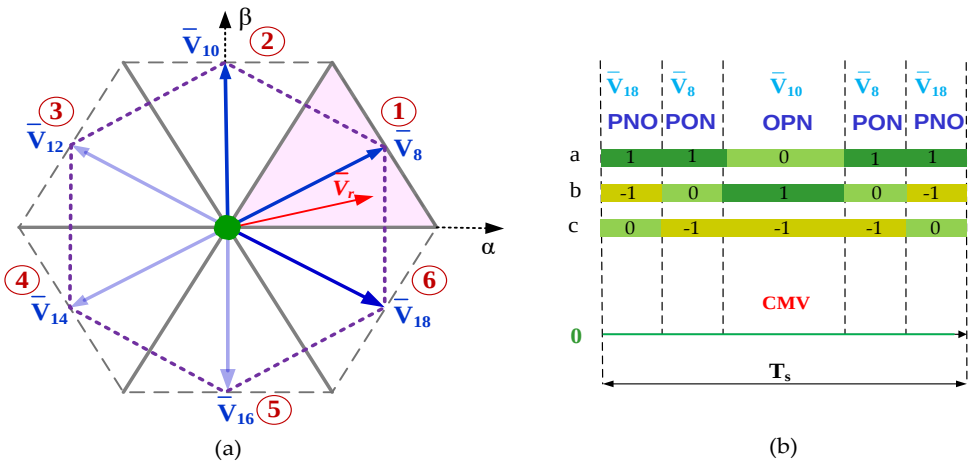



**Figure 20.** (**a**) 3L SVD using 3M method; (**b**) Switching sequence distribution for sector 1.

The three medium vectors are distributed as shown in Figure 20b. Commonly, the delivered CMV is illustrated in the same figure and it is stuck at zero.

- Three Medium (3M120) Method

This technique utilizes 3 medium vectors that are offset from each other by 120° [65]. As in the 3M method, the 3L-SVD is decomposed into six sectors as seen in Figure 21a. In this case, the medium vectors $\overline{V}_8$, $\overline{V}_{12}$ and $\overline{V}_{16}$ are selected when $\overline{V}_r$ is located in the sectors 2, 4 and 6, whereas the other vectors, $\overline{V}_{10}$, $\overline{V}_{14}$ and $\overline{V}_{18}$ are chosen for the sectors 1, 3 and 5. An example of switching sequences distribution and the resulting CMV are shown in Figure 21b, when $\overline{V}_r$ is situated in the first sector. During the switching period, the CMV remains at zero, thus the leakage current can be eliminated as described in Equation (3).

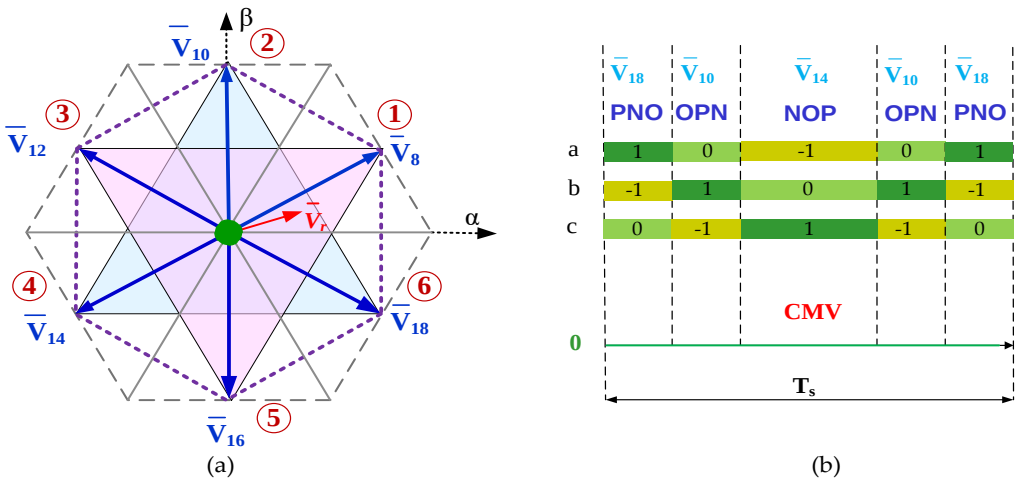



**Figure 21.** (**a**) 3L SVD using 3M120 method; (**b**) Switching sequence distribution for sector 1.

#### 4.2.3. PCMV and NCMV Methods

The PCMV approach aims to clamp the CMV level at a positive value [56]. If only the large and small vectors with CMV of $+V_{dc}/6$ are used in vector synthesis, the CMV can be maintained at $+V_{dc}/6$ during a switching period. In this case, the 3L-SVD is split into only 3 sections as illustrated in Figure 22a. The vector $\overline{V}_r$ located as in this figure is synthesized using the two small vectors (POO) and (OPO) and the large vector (PPN). The dwell times of these vectors can be determined using Equation (19):

$$\begin{cases} T_s.\overline{V}_r = T_{POO}.\overline{V}_1 + T_{PPN}.\overline{V}_9 + T_{OPO}.\overline{V}_3 \\ T_s = T_{POO} + T_{PPN} + T_{OPO} \end{cases} \quad (19)$$

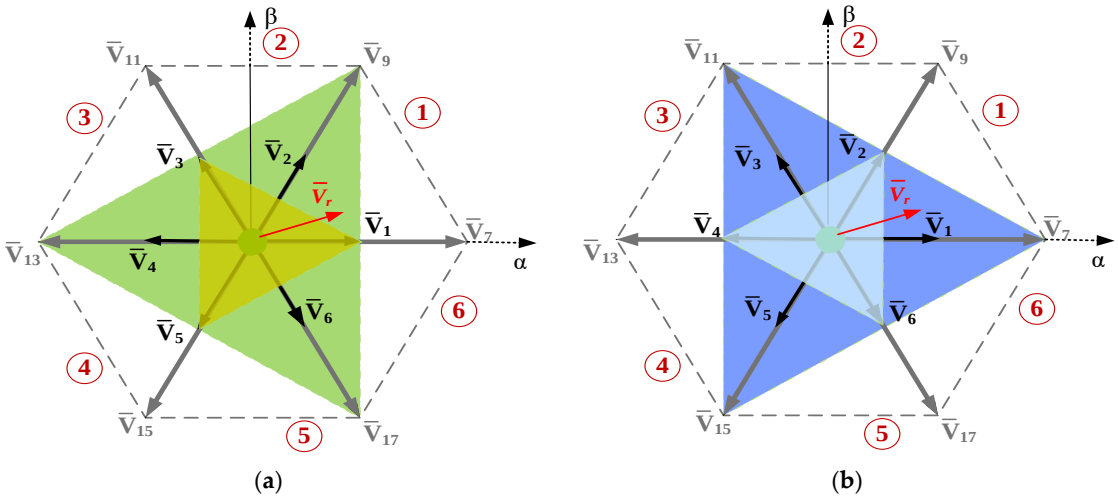



**Figure 22.** *Cont.*

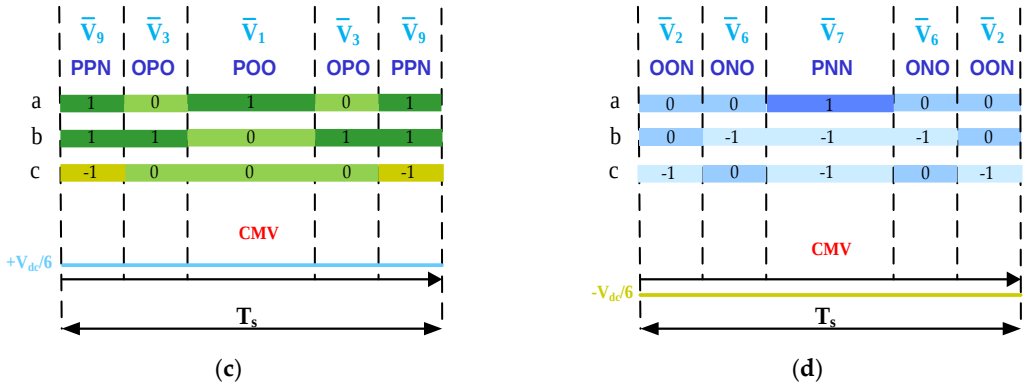



**Figure 22.** (**a**) 3L SVD using PCMV method; (**b**) 3L SVD using NCMV method; (**c**) Switching sequence distribution for PCMV method; (**d**) Switching sequence distribution for NCMV method.

The distribution of these switching states with the resulting CMV are depicted in Figure 22c.

Conversely, the NCMV method aims to clamp the CMV level to a negative value [56]. If only the large and small vectors with CMV of $-V_{dc}/6$ are applied, the CMV can be kept at $-V_{dc}/6$ during a switching period. The NCMV method decomposes the 3L-SVD into 3 sections as depicted in Figure 22b. The $\overline{V}_r$ in this figure is composed by applying the two small vectors $\overline{V}_2$ (OON) and $\overline{V}_6$ (ONO) combined with the large vector $\overline{V}_7$ (PNN). The application times of the applied vectors are calculated as below.

$$\begin{cases} T_s.\overline{V}_r = T_{ONO}.\overline{V}_6 + T_{PNN}.\overline{V}_7 + T_{OON}.\overline{V}_2 \\ T_s = T_{ONO} + T_{PNN} + T_{OON} \end{cases} \quad (20)$$

Their distribution as well as the produced CMV are drawn in Figure 22d. The selected vectors for each sector of PCMV and NCMV methods are depicted in Table 9. To operate in the six sections, the PCMV and the NCMV RCMV-methods are combined.

**Table 9.** Applied vectors for NCMV and PCMV methods.

| CMVR Method | Sector Number | Applied Vectors |
|---|---|---|
| NCMV | 1 | OON-ONO-PNN |
| | 3 | NOO-OON-NPN |
| | 5 | ONO-NOO-NNP |
| PCMV | 2 | PPN-OPO-POO |
| | 4 | NPP-OOP-OPO |
| | 6 | PNP-POO-OOP |

### *4.3. 3L-SVPWM CMVR Methods Based on Virtual Vectors*

The virtual vectors concept is originally used to control the NPV of the 3L-NPC inverter. Recently, improved and modified VSVPWM are introduced for CMV reduction objective. Three types of VSVPWM will be discussed below, which are denoted, here, as VSVPWM 1, VSVPWM 2 and VSVPWM 3.

#### 4.3.1. VSVPWM 1

The virtual space vectors are defined as a linear combination of the real vectors corresponding to certain switching states. In VSVPWM1, an improved virtual medium vector is created using the original medium vector and the adjacent two pairs of the small vectors [45,66]. This virtual vector can be defined as follows:

$$\overline{V}_{NM0} = k_{A0}\overline{V}_8 + k_{A1}\overline{V}_1 + k_{A2}\overline{V}_2 \quad (21)$$

where $k_{A0}$, $k_{A1}$, $k_{A2} \in [0,1]$ and $k_{A0} + k_{A1} + k_{A2} = 1$.

From Equation (21), it is evident that the enhanced $\overline{V}_{NM0}$ comprises two sets of small vectors, namely $\overline{V}_1$ (POO/ONN) and $\overline{V}_2$ (PPO/OON). The manipulation of the duty cycles for $k_{A0}$, $k_{A1}$ and $k_{A2}$ and consequently, the duration of medium and small vectors, can be employed to achieve NP balancing and address other control objectives such as the CMV reduction. If $k_{A0} = k_{A1} = k_{A2} = 1/3$, the 3L-SVD can be as shown in Figure 23a. Each sector of the 3L-SVD is divided into five regions ($R_1$, $R_2$, $R_3$, $R_4$, $R_5$), as illustrated in Figure 23b. During each switching cycle, a specific group of space vectors must be chosen for synthesizing the reference vector $\overline{V}_r$. Table 10 gives the applied vectors for all regions of the first sector. If $\overline{V}_r$ is located in the region $R_3$ within the first sector, there are two possible pulse sequences including the constructed virtual vector $\overline{V}_{NM0}$, as shown in Figure 23c,d. The difference between the two sequences is that the first one (Figure 23c) apply the small vector (PPO) which produces the CMV level of $+V_{dc}/3$, while the second one (Figure 23d) apply the small vector (OON) that produces the CMV level of $+V_{dc}/6$. However, they possess an equal total switching times. Accordingly, the CMV can be reduced when the pulse sequence of Figure 23d is selected since the produced CMV with (OON) is smaller than the one produced with (PPO). To conclude, the negative small vectors that produce a reduced CMV ($\pm V_{dc}/6$) with the zero vector (OOO) are used for CMV reduction in the grey areas of Figure 23a, whereas only the negative small vectors are applied to decrease the CMV in the white areas of Figure 23a.

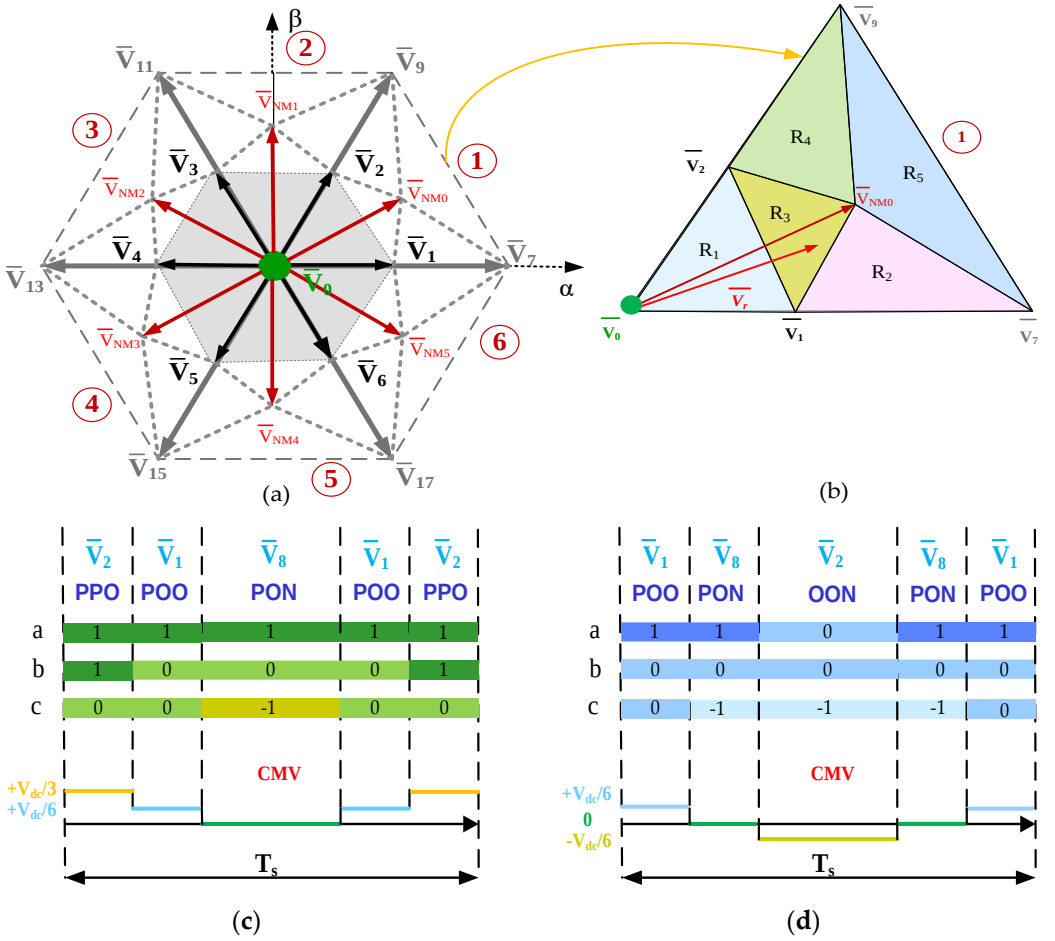



**Figure 23.** (**a**) 3L SVD using VSVPWM1; (**b**) Sector division; (**c**)and (**d**) Possible Switching sequences distribution for region 3 of the first sector.

**Table 10.** Applied vectors for all regions of sector 1.

| Region Number | Applied Vectors | Associated States |
|---|---|---|
| $R_1$ | $V_0$, $V_1$, $V_2$ | PPP, OOO, NNN, POO, ONN, PPO, OON |
| $R_2$ | $V_1$, $V_{v1}$, $V_7$ | POO, ONN, PON, PPO, OON, PNN |
| $R_3$ | $V_1$, $V_{v1}$, $V_2$ | POO ONN PON PPO OON |
| $R_4$ | $V_2$, $V_{v1}$, $V_7$ | PPO OON PON POO ONN PPN |
| $R_5$ | $V_7$, $V_{v1}$, $V_9$ | PNN PON POO ONN PPO OON PPN |

4.3.2. VSVPWM 2

To reduce both CMV and NPV oscillation, a new virtual space vector modulation strategy is suggested [46]. The guiding principle for CMV reduction is to exclude the space vectors that produce the highest CMV level while keeping the NPV control. For further explanation, we consider the example when $\overline{V}_r$ is situated in the first sector, falling within the range of 0° to 60°, four novel virtual vectors are constructed using small and medium vectors, as given by the following:

$$\begin{cases} \overline{U}_{NZS11} = \frac{1}{2}\left(\overline{V}_8 + \overline{V}_{6(\mathrm{ONO})}\right) \\ \overline{U}_{NZS12} = \frac{1}{2}\left(\overline{V}_{18} + \overline{V}_{2(\mathrm{OON})}\right) \\ \overline{U}_{NZS21} = \frac{1}{2}\left(\overline{V}_8 + \overline{V}_{3(\mathrm{OPO})}\right) \\ \overline{U}_{NZS22} = \frac{1}{2}\left(\overline{V}_{10} + \overline{V}_{1(\mathrm{POO})}\right) \end{cases} \tag{22}$$

It should be noted that the virtualized vectors are built based on the original vectors with reduced CMV. Figure 24a,b illustrate the division of the SVD of the RCMV-VSVPWM, introducing the novel virtual vectors. The regions $A_1$, $A_2$, $A_1'$ and $A_2'$ are identified using the alpha-beta frame, as shown in Table 11. Assuming that $\overline{V}_r$ is located in the region $A_1$. In this case, the zero vector $\overline{V}_0$ (OOO) and the large vector $\overline{V}_9$ (PPN) are used with the virtualized vector $\overline{U}_{NZS11}$ or $\overline{U}_{NZS12}$ to synthesize the vector $\overline{V}_r$. The distribution sequence of these vectors and the produced CMV are illustrated in Figure 24c. Moreover, when $\overline{V}_r$ is located in the region $A_1'$, the vectors $\overline{V}_0$ (OOO) and $\overline{V}_7$ (PPN) with the virtualized vector $\overline{U}_{NZS21}$ or $\overline{U}_{NZS22}$ are applied, as shown in Figure 24d.

As can be observed, in both case, the CMV level is restricted to $\pm V_{dc}/6$ since only the vectors with CMV level of $\pm V_{dc}/6$ and the virtual vectors are applied.

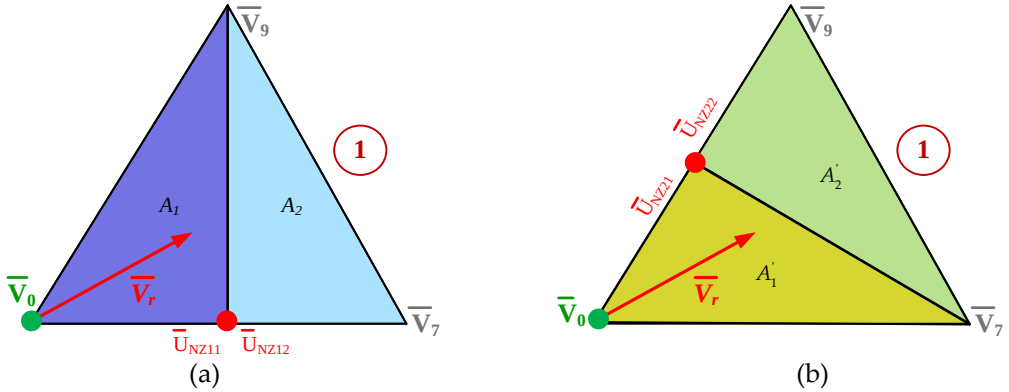



**Figure 24.** *Cont.*

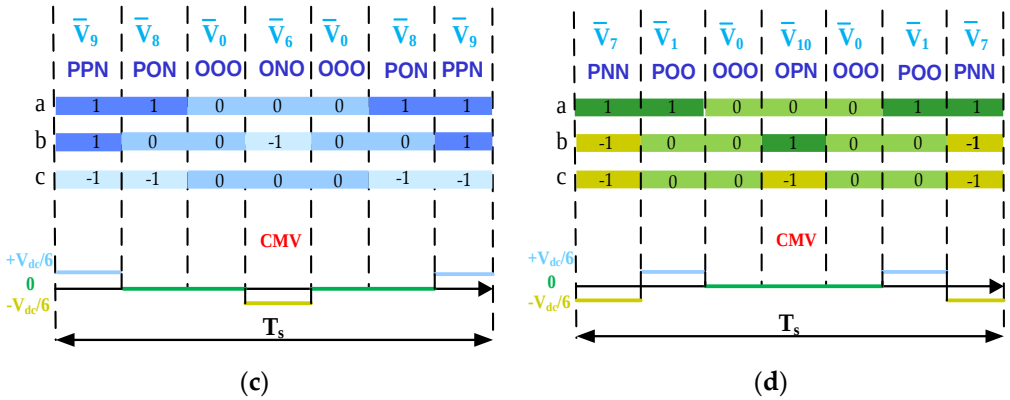



**Figure 24.** (**a**,**b**) Sector division and virtual vectors localization using VSVPWM2; (**c**) Switching sequence distribution for the region $A_1$; (**d**) Switching sequence distribution for the region $A_1'$.

**Table 11.** Region judgment.

| Region | Region Judgment |
|---|---|
| $A_1$ | $u_\alpha < V_{dc}/2\sqrt{3}$ |
| $A_2$ | $u_\alpha > V_{dc}/2\sqrt{3}$ |
| $A_1'$ | $u_\alpha + 2u_\beta/\sqrt{3} < V_{dc}/\sqrt{3}$ |
| $A_2'$ | $u_\alpha + \sqrt{3}u_\beta/2 > V_{dc}/\sqrt{3}$ |

#### 4.3.3. VSVPWM 3

An enhanced RCMV-VSVPWM is proposed in [47,67,68] with the aim to provide active NPV (ANPV) control and CMV suppression since the CMV variation is also affected by the NPV. Accordingly, new virtual vectors are construed. Taking sector 1 as an example, the zero vector with the state (OOO) is used as a zero virtual vector as well as the original large vectors are virtualized to be two virtual large vectors. Two virtual small vectors are created using three nearest small original vectors that produce CMV level of $\pm V_{dc}/6$. One virtual medium vector is also constructed using three nearest basic medium vectors. The new created virtual vectors are given as:

$$\begin{cases} V_{ZS1} = \frac{k_1}{3}\overline{V}_{6(\mathrm{ONO})} + \frac{3-2k_1}{3}\overline{V}_{1(\mathrm{POO})} + \frac{k_1}{3}\overline{V}_{2(\mathrm{OON})} \\ V_{ZS2} = \frac{k_2}{3}\overline{V}_{1(\mathrm{POO})} + \frac{3-2k_2}{3}\overline{V}_{2(\mathrm{OON})} + \frac{k_2}{3}\overline{V}_{3(\mathrm{OPO})} \\ V_{ZM1} = \frac{k_3}{3}\overline{V}_{10(\mathrm{OPN})} + \frac{3-2k_3}{3}\overline{V}_{8(\mathrm{PON})} + \frac{k_3}{3}\overline{V}_{18(\mathrm{PNO})} \end{cases} \quad (23)$$

where $k_1$, $k_2$ and $k_3$ are comprised between 0.5 and1.5.

The positions of the novel created virtual vectors are shown in Figure 25a. The novel virtual vectors split each sector of the SVD into 5 regions as depicted in Figure 25b. The amplitudes of the virtual small and virtual medium vectors change based on the variable coefficients ($k_1$, $k_2$, $k_3$). A possible switching sequence with the generated CMV are given in Figure 25c when $\overline{V}_r$ lies in region 1 of the first sector. As it is observed the CMV amplitude do not exceed $V_{dc}/6$.

The effective suppression of the CMV can be ensured by restricting the range of the variable coefficients, as defined below:

$$k_2 \prec \max\left(1.5 \times \left(1 - \frac{t_{v2}}{t_{v3}}\right), 1 + \frac{3-2k_3}{3} \times \frac{t_{v1}}{t_{v3}}\right) \quad (24)$$

where $t_{v1}$, $t_{v2}$, $t_{v3}$ are the dwell times of the virtual vectors.

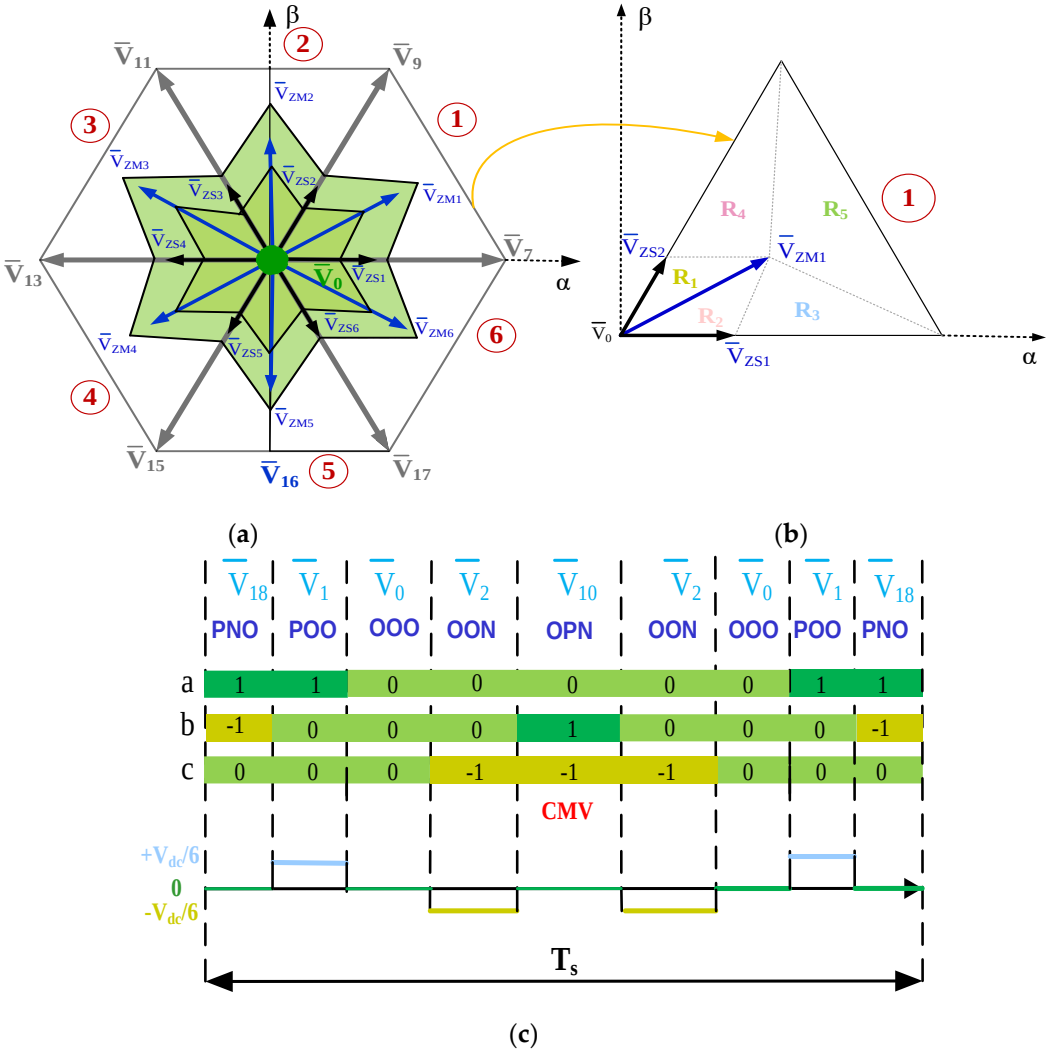



**Figure 25.** (**a**) 3L-SVD using VSVPWM3; (**b**) Sector division; (**c**) Switching sequence distribution for the region $R_1$ of sector 1.

### *4.4. 3L-SVPWM CMVR Methods Based on 2L-SVPWM*

The traditional 3L-SVPWM based on small hexagon method apply the closest three vectors in the 2L-SVD for generating the reference voltage vector. Although the simplicity and the low computation burden of this approach, it does not consider CMV suppression. Based on this approach, a modified 3L-SVPWM is proposed to mitigate the CMV [48]. This alternative is based on the 2L Active Zero State PWM1 (2L-AZSPWM1) [38]. The 2L-AZSPWM1 consists on the application of only the active vectors and avoiding the zero vectors. Two active opposite vectors with equal duration time are used instead of the zero vector, as shown in Figure 26a. According to this principle, the switching sequences of the conventional 3L-SVPWM based on small hexagon have been modified to align with those of the 2L-AZSPWM1. For further clarification, we suppose that the vector $\overline{V}_r$ is located in the subsector 1 within the first small hexagon. In the conventional simplified 3L-SVPWM, the active vectors $\overline{V}_7$ and $\overline{V}_8$ with the vector $\overline{V}_1$ are applied and the CMV oscillates between four levels: $-\mathrm{V_{dc}}/3$, $-\mathrm{V_{dc}}/6$, 0 and $+\mathrm{V_{dc}}/6$. In the 3L-SVPWM based on 2L-AZSPWM1, the vector $\overline{V}_1$, which is applied as a zero vector, is replaced by two opposite active vectors: the small vector $\overline{V}_2$ (OON) and the medium vector $\overline{V}_{18}$ (PNO), as illustrated in Figure 26b. The novel switching sequence including $\overline{V}_2$ and $\overline{V}_{18}$ with the vectors $\overline{V}_7$ and $\overline{V}_8$ as well as the resulting CMV are given in Figure 26c. As can be observed, the produced CMV oscillates between two levels: 0 and $-\mathrm{V_{dc}}/6$. Indeed, the zero level is produced by the medium vectors $\overline{V}_8$ and $\overline{V}_{18}$, while the level $-\mathrm{V_{dc}}/6$ is provided by the large vector

$\overline{V}_7$ and the small vector $\overline{V}_2$. Table 12 hereafter, gives the switching sequences when $\overline{V}_r$ is located within the first small hexagon.

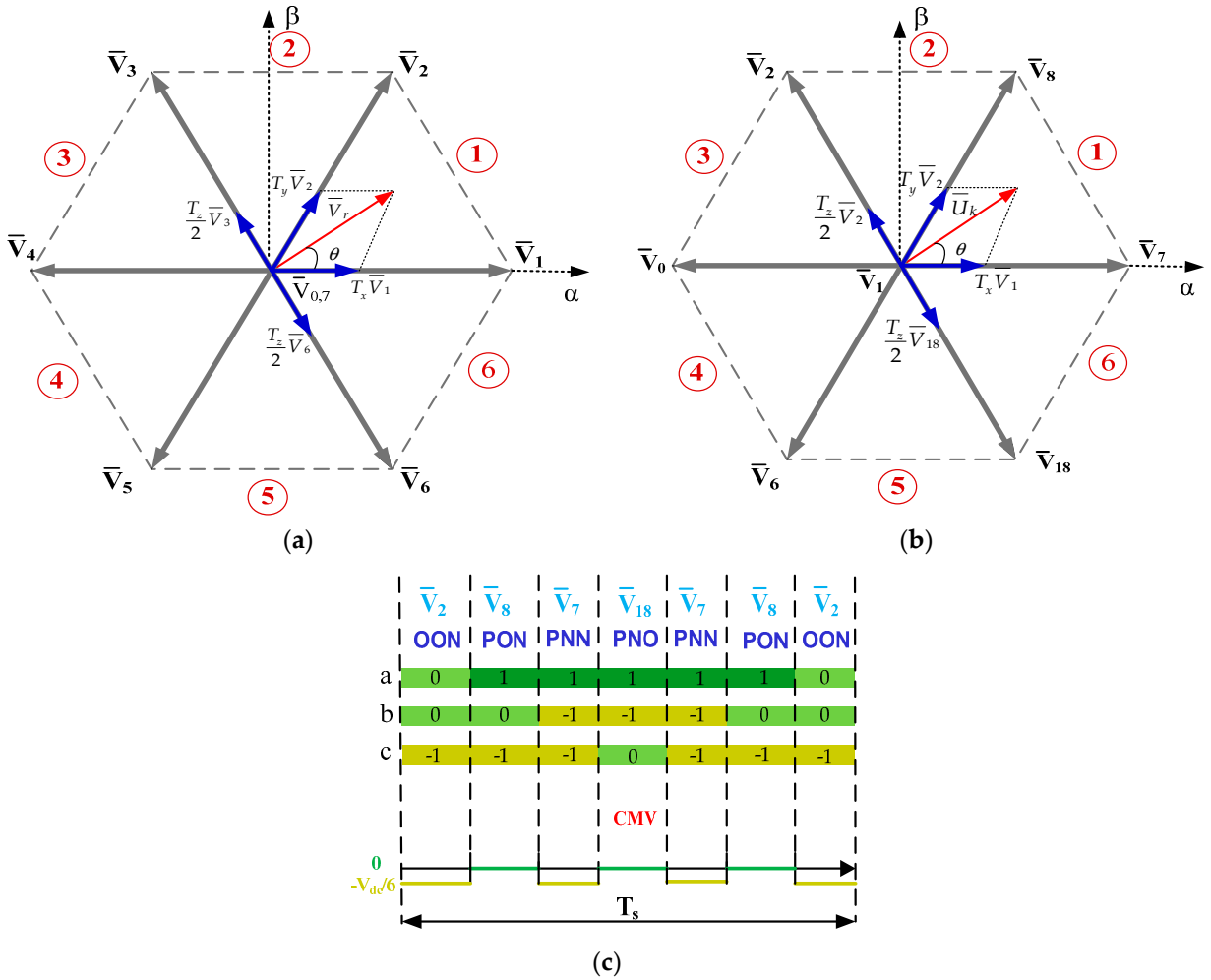



**Figure 26.** (**a**) 2L-SVPWM based on AZSPWM1; (**b**) 3L-SVPWM based on AZSPWM; (**c**) Switching sequence distribution for the 3L-SVPWM based on AZSPWM1.

**Table 12.** Switching sequences distribution for the first small hexagon.

| Subsector | Switching Sequences |
|---|---|
| 1 | OON-PON-PNN-PNO-PNN-PON-OON |
| 2 | OOO-OON-PON-PNN-PON-OON-OOO |
| 3 | ONO-OOO-OON-PON-OON-OOO-ONO |
| 4 | PNO-ONO-OOO-OON-OOO-ONO-PNO |
| 5 | PNN-PNO-ONO-OOO-ONO-PNO-PNN |
| 6 | PON-PNN-PNO-ONO-PNO-PNN-PON |

## 5. Challenges in MLI-RCMV-SVPWM Approaches

To mete out a power conversion system with minimized cost and size, transformerless NPC-MLIs are widely exploited in several applications and above all in renewable power generation and grid-connected inverters. In addition, the removal of the transformer improves the efficiency of the overall power conversion system as well. In the counterparty, the CMV is introduced as the main limitation of this type of inverters. To overcome this issue, the MLI-SVPWM is presented as a promising modulation technique that provides better THD along with higher output voltage. The SVPWM approach is capable to control the switching states which is not possible in the traditional modulation techniques. On the

other hand, it can be easily extended for a high number of level as well as it can be applied in a similar manner for other types of MLI such as CHB-MLI and FC-MLI.

The significant concern raised in MLI-SVPWM pertains to CMV and NPV control. Several research efforts have been devoted to tackling this challenge. However, resolving both issues concurrently through SVPWM techniques proves to be challenging. Specifically, achieving complete CMV elimination while maintaining NPV control is unattainable. This is because the medium vectors with zero CMV contribute to exacerbating the NPV control problem. Resolving the CMV issue in transformer-less MLI can introduce other problems related to the implementation complexity, THD increase, NPV oscillation, limited DC voltage utilization and high switching losses.

The conventional 3L-NTV-SVPWM yields superior output voltage. However, it suffers with poor CMV. Its extension to a high number of level seems to be more difficult. This complexity can be reduced by applying the MLI-SVPWM based on 2L-SVPWM when the MLI-SVD is decomposed into multiple 2L-SVD. The 3L-SVPWM based on small hexagon can be easily implemented but it does not consider the CMV reduction. For a partial reduction of CMV, these two conventional 3L-SVPWM have been modified by avoiding the zero vector (OOO) that produces the highest CMV level. Consequently, the CMV is restricted to $\pm V_{dc}/3$, however, it remains important and it will result in an important leakage current. Contrarily, these conventional techniques allow the self NPV control and provide low switching losses.

The partial elimination of CMV is performed using the applied vector's type such as VCMV, PCMV and NCMV methods, the VSVPWM as well as the small hexagon method. The CMV level is restricted to $\pm V_{dc}/6$ with these approaches. The VCMV, the VSVPWM and small hexagon method lead to greater leakage current when compared with the PCMV and the NCMV methods since the CMV cannot be constant in one switching period. Furthermore, All the VSVPWM techniques and commonly the small hexagon method have the capability of the NPV control. However, the VCMV approach is not capable to ensure the NPV control since it uses the medium vectors. As for switching loss, the PCMV and the NCMV are combined with the ZCMV (2M1Z) to consider this performance criterium by the rearrangement of the switching sequences. In VSVPWM, the medium vectors are discarded since they are responsible for NPV oscillation. The VSVPWM1 approach involves two pairs of small vectors in any given area of the 3L-SVD. One pair needs to be chosen for NPV control. Meanwhile, the second pair is selected to minimize the switching loss and the CMV. Moreover, in VSVPWM2, to reduce the switching loss, the virtual vector that leads to high switching loss is eliminated from the switching sequence. However, the switching loss produced by this VSVPWM technique is higher when compared to the conventional NTV-SVPWM and they are closely equal to the one produced by the VSVPWM1, whereas the VSVPWM3 reduces the switching loss by applying the equal phase duty-ratio method, which optimize the output voltage sequence.

The complete suppress of CMV is also possible by adopting the ZCMV methods such as 2M1Z, 3M and 3M120. The ZCMV methods provide nearly zero leakage current, making them more efficient in terms of this criterium when compared with the partial elimination CMV method. Accordingly, the ZCMV methods are more suitable for transformer-less PV systems which limit the RMS value of the leakage current to 300mA as specified by German standards. However, these approaches do not consider either NPV control or switching loss reduction. The 3M120 is the ZCMV method that produces the most important switching loss and the highest NPV oscillation with limited DC utilization ratio, being an alternative that could be avoided when CMV reduction is required. In general, the ZCMV methods generate significant switching loss compared to the conventional SVPWMs. Table 13 summarizes the performances of the CMR-SVPWM.

**Table 13.** Performances comparison of the studied SVPWMs.

| | | | Max m | CMV Level | CMV Variation | Capability of | | | $THD_i$ | Complexity |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | NPVC | SL-R | IL-S | | |
| Conventional SVPWMs | NTV-SVPWM | | 1.154 | $\pm V_{dc}/2$ | Variable | Yes | Yes | NO | Low | High |
| | SVPWM based small hexagon | | 1.154 | $\pm V_{dc}/2$ | Variable | Yes | Yes | NO | Low | Low |
| CMVR-SVPWM based on vectors type | VCMV | LMZ | 1.154 | $\pm V_{dc}/6$ | Variable | No | No | No | Medium | Low |
| | ZCMV | 2M1Z | 0.866 | 0 | Constant | No | No | Yes | Medium | Low |
| | | 3M | 0.866 | 0 | Constant | No | No | Yes | High | Medium |
| | | 3M120 | 0.577 | 0 | Constant | No | No | Yes | High | Medium |
| | NCMV and PCMV | | 1.154 | $\pm V_{dc}/6$ | Constant | Yes | No | Yes | Medium | High |
| CMVR-SVPWM based on virtual vectors | VSVPWM1 | | 1.154 | $\pm V_{dc}/6$ | Variable | Yes | Yes | No | Medium | High |
| | VSVPWM2 | | 1.154 | $\pm V_{dc}/6$ | Variable | Yes | No | No | Low | High |
| | VSVPWM3 | | 1.154 | $\pm V_{dc}/6$ | Variable | Yes | Yes | No | High | High |
| CMVR-SVPWM based on small hexagon | | | 1.154 | $\pm V_{dc}/6$ | Variable | Yes | Yes | No | Medium | Low |

NPVC: NPV control; SL-R: Switching losses reduction; IL-S: Leakage current suppression.

## 6. Future Trends

In high-power applications, using two-level inverters can result in elevated voltage stress across each switching device, leading to increased switching and conduction losses. Accordingly, MLIs are preferred for high-power applications such as HVDC and FACTS. Reduction of the weight and volume of the MLI in any application is of great importance. Consequently, the removal of transformer in multilevel structure can be beneficial in increasing the power density of this latter. The produced CMV by the transformer-less MLI can be resolved using the RCMV-SVPWM. These techniques can also examine the NPV fluctuation. An efficient and fast NPV control strategy can lead to capacitor size reduction, further enhancing the power density of MLI.

Higher computation times are needed for the implementation of the MLI-SVPWM when compared to the classical 2L inverter. This issue is due to two important factors: the high number of switching states and the requirement of NPV control. To take full advantage of the features offered by MLI structure, fast microprocessors are mandatory. Over the past few decades, the performance of microprocessors has consistently improved. This ongoing trend of enhancement in processing will facilitate the use of MLI equipped with rapid power devices. Alternatively, Artificial Intelligence (AI) could be implemented in this regard to mitigate processing time and memory-related issues.

A distinctive feature of MLI is its fault tolerance capability, which is an important criterium in most applications, namely the traction drive system. This criterium creates an opportunity for the MLI future research. In traditional 2L inverters, fault tolerance is maintained by incorporating a fourth inverter leg that takes over in the event of a failure in one of the principal inverter legs. However, in the case of MLI, fault tolerance can be achieved without the need for an additional leg.

A potential area of research within RCMV-SVPWM could involve achieving equitable power loss distribution between semiconductors. This criterium has a direct impact on the reliability and lifespan of the MLI. It is necessary to enhance RCMV-SVPWM to ensure that the temperature rise of the devices remains consistent across all operating conditions. This improvement will ultimately lead to an increase in the MLI power density.

Another research area is well discussed when the number of levels is high which leads to more complexity. The level of complexity can be diminished by transforming the MLI-SVD to the conventional 2L-SVD or by the use of higher-speed processors to reduce the computation burden. The simplified SVPWM approach can be easily extended to any

level of inverter, making fast implementation of MLI-SVPWM. Otherwise, the adequate level of the MLI must be determined according to the application requirements and under the consideration of reliability, cost, power density and efficiency.

New proposed MLI-SVPWM techniques must consider low $dv/dt$. Otherwise, it is essential to guarantee smooth vector transitions. In the case of motor drive, high $dv/dt$ leads to voltage spikes and sparks, which can cause the failure of the bearing balls or rollers. While the use of shielded cables can help reduce radiated EMI, it is not effective in decreasing conducted emissions. To mitigate the detrimental effects of high-frequency interference, EMI filters and ferrite ring cores can be employed. Nonetheless, the additional passive components increase the cost and the size of the conversion system.

In some applications such as PV energy applications, the DC input voltages are asymmetrical. In addition to CMV reduction, the CMVR-SVPWM must consider the issue of asymmetrical DC source by making a modification in the time duration of the switching vectors. Accordingly, it becomes feasible to operate the NPC-MLI with an asymmetrical DC power source. However, in another side, ensuring equal voltage sharing among capacitors necessitates a significant number of voltage sensors and communication lines, particularly when the number of level is high. This will reduce the reliability and raises the cost of the power conversion system. Therefore, the development of sensor-less approaches appears to be a potential trend for this issue.

Multi-phase inverters have been garnering increased attention in recent research due to their advantages, such as reduced CMV, lower switching losses, and less harmonic content [69,70]. As depicted in Table 14, when the phase number and the level number increase, the CMV is further decreased. For additional CMV reduction and reliability increase, the transformer-less multi-phase NPC MLI is recommended, for example, for renewable energy applications like PV and Wind. The CMV can be minimized by selecting the specific switching vectors.

**Table 14.** Produced CMV levels in multi-phase MLIs.

| | **2L-Inverter** | | **3L-Inverter** | | **5L-Inverter** | |
|---|---|---|---|---|---|---|
| **Level of CMV** | **3-Phase** | **5-Phase** | **3-Phase** | **5-Phase** | **3-Phase** | **5-Phase** |
| 1 | $\pm V_{dc}/6$ | $\pm V_{dc}/10$ | 0 | 0 | 0 | 0 |
| 2 | $\pm 3V_{dc}/6$ | $\pm 3V_{dc}/10$ | $\pm V_{dc}/6$ | $\pm V_{dc}/10$ | $\pm V_{dc}/12$ | $\pm V_{dc}/20$ |
| 3 | - | $\pm 5V_{dc}/10$ | $\pm 2V_{dc}/6$ | $\pm 2V_{dc}/10$ | $\pm 2V_{dc}/12$ | $\pm 2V_{dc}/20$ |
| 4 | - | - | $\pm 3V_{dc}/6$ | $\pm 3V_{dc}/10$ | $\pm 3V_{dc}/12$ | $\pm 3V_{dc}/20$ |
| 5 | - | - | - | $\pm 4V_{dc}/10$ | $\pm 4V_{dc}/12$ | $\pm 4V_{dc}/20$ |
| 6 | - | - | - | $\pm 5V_{dc}/10$ | $\pm 5V_{dc}/12$ | $\pm 5V_{dc}/20$ |
| 7 | - | - | - | - | $\pm 6V_{dc}/12$ | $\pm 6V_{dc}/20$ |
| 8 | - | - | - | - | - | $\pm 7V_{dc}/20$ |
| 9 | - | - | - | - | - | $\pm 8V_{dc}/20$ |
| 10 | - | - | - | - | - | $\pm 9V_{dc}/20$ |
| 11 | - | - | - | - | - | $\pm 10V_{dc}/20$ |

## 7. Conclusions

The use of transformer-less NPC-MLIs is a requirement in various application areas thanks to their several benefits, particularly the removal of bulky and inefficient transformers. They have a wide range of applications, including serving as electric vehicle chargers, motor drives, residential PV inverters, uninterruptible power supplies, grid-tied applications, etc. Considering that industries aim for simplicity and optimal performance in their upcoming power electronic converter technology, the 3L and 5L NPC structures are considered mature and are extensively manufactured by companies for a variety of applications.

In addition to the choice of the most suitable MLI structure, it is also important to make informed decisions about advancement in modulation schemes, especially in the case of transformer-less NPC-MLIs when CMV may occur. Thus, the aim of this article has been to provide an extensive overview of the RCMV-SVPWM developed for NPC-MLIs, encompassing their features in terms of leakage current, THD, NPV control, and switching loss. From this review, it is concluded that conventional SVPWM methods, namely the NTV–SVPWM and SVPWM based small hexagons, provide better-quality outputs; however, they suffer from poor CMV. The partial elimination-based RCMV-SVPWM methods limit the CMV in the range of $\pm V_{dc}/6$, but the leakage current cannot be suppressed due to the high-frequency variation of this voltage. For complete elimination of CMV, ZCMV-SVPWM is highly recommended. The leakage current produced by these techniques is almost nullified. There is always a trade-off between CMV reduction, NPV control, switching loss, and simplicity. Thus, RCMV-SVPWM needs to adapt to the requirements of the specified application. In this article, it is demonstrated that RCMV-SVPWM has significant potential for further development and implementation. Accordingly, in the last section of this paper, future trends and challenges of the RCMV-SVPWM applied to the NPC MLI have been presented. These future perspectives provide valuable insights for researchers and engineers to address these challenges and continue to explore the full potential of the RCMV-SVPWM.

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## Nomenclature

| | | | |
|---|---|---|---|
| PV | Photovoltaic | SVD | Space Vector Diagram |
| MLIs | Multi-Level Inverters | VSVPWM | Virtual Space Vector PWM |
| CMV | Common Mode Voltage | NPV | Neutral Point Voltage |
| CMVR | CMV Reduction | ANPV | Active Neutral Point Voltage |
| NPC | Neutral Point Clamped | AZS-PWM | Active-Zero-State PWM |
| FC | Flying Capacitor | VCMV | Variable CMV |
| CHB | Cascaded H-Bridge | ZCMV | Zero CMV |
| SVPWM | Space Vector Pulse Width Modulation | PCMV | Positive CMV |
| EMI | Electromagnetic Interference | NCMV | Negative CMV |
| NTV | Nearest Three Vectors | THD | Total Harmonic Distortion |

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